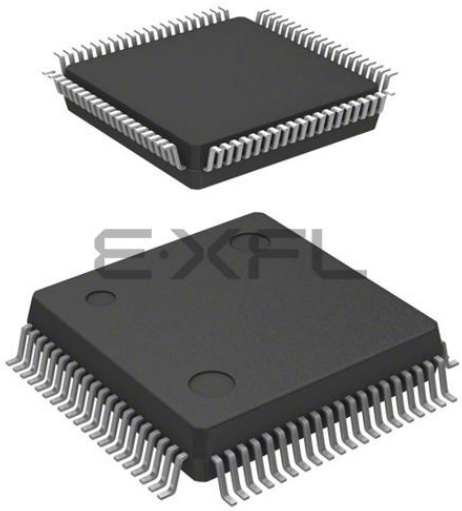
Renesas Electronics America Inc - M30621FCPGP#U5C Datasheet



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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

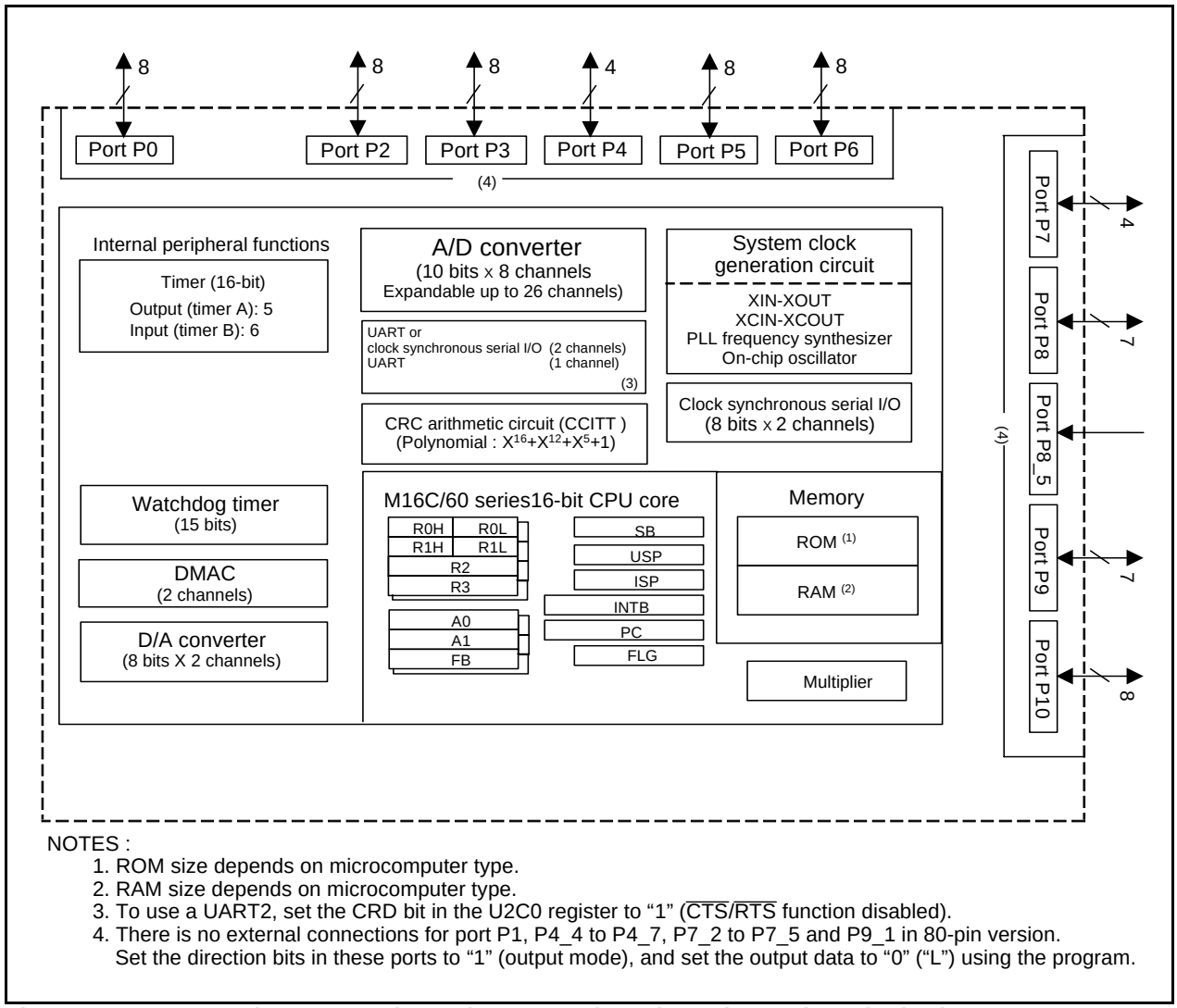
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	M16C/60
Core Size	16-Bit
Speed	24MHz
Connectivity	I²C, IEBus, UART/USART
Peripherals	DMA, WDT
Number of I/O	68
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	10K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 26x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-BQFP
Supplier Device Package	80-QFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/m30621fcpgp-u5c

Table 1.2 Performance Outline of M16C/62P Group (M16C/62P, M16C/62PT)(100-pin version)

	Item	Performance	
		M16C/62P	M16C/62PT(4)
CPU	Number of Basic Instructions	91 instructions	
	Minimum Instruction Execution Time	41.7ns(f(BCLK)=24MHz, VCC1=3.3 to 5.5V) 100ns(f(BCLK)=10MHz, VCC1=2.7 to 5.5V)	41.7ns(f(BCLK)=24MHz, VCC1=4.0 to 5.5V)
	Operating Mode	Single-chip, memory expansion and microprocessor mode	Single-chip
	Address Space	1 Mbyte (Available to 4 Mbytes by memory space expansion function)	1 Mbyte
	Memory Capacity	See **Table 1.4 to 1.7 Product List**	
Peripheral Function	Port	Input/Output : 87 pins, Input : 1 pin	
	Multifunction Timer	Timer A : 16 bits x 5 channels, Timer B : 16 bits x 6 channels, Three phase motor control circuit	
	Serial Interface	3 channels Clock synchronous, UART, I2C bus(1), IEBus(2) 2 channels Clock synchronous	
	A/D Converter	10-bit A/D converter: 1 circuit, 26 channels	
	D/A Converter	8 bits x 2 channels	
	DMAC	2 channels	
	CRC Calculation Circuit	CCITT-CRC	
	Watchdog Timer	15 bits x 1 channel (with prescaler)	
	Interrupt	Internal: 29 sources, External: 8 sources, Software: 4 sources, Priority level: 7 levels	
	Clock Generation Circuit	4 circuits Main clock generation circuit (*), Subclock generation circuit (*), On-chip oscillator, PLL synthesizer (*)Equipped with a built-in feedback resistor.	
	Oscillation Stop Detection Function	Stop detection of main clock oscillation, re-oscillation detection function	
	Voltage Detection Circuit	Available (option (5))	Absent
Electric Characteristics	Supply Voltage	VCC1=3.0 to 5.5 V, VCC2=2.7V to VCC1 (f(BCLK=24MHz) VCC1=2.7 to 5.5 V, VCC2=2.7V to VCC1 (f(BCLK=10MHz)	VCC1=VCC2=4.0 to 5.5V (f(BCLK=24MHz)
	Power Consumption	14 mA (VCC1=VCC2=5V, f(BCLK)=24MHz) 8 mA (VCC1=VCC2=3V, f(BCLK)=10MHz) 1.8µA (VCC1=VCC2=3V, f(XCIN)=32kHz, wait mode) 0.7µA (VCC1=VCC2=3V, stop mode)	14 mA (VCC1=VCC2=5V, f(BCLK)=24MHz) 2.0µA (VCC1=VCC2=5V, f(XCIN)=32kHz, wait mode) 0.8µA (VCC1=VCC2=5V, stop mode)
Flash memory version	Program/Erase Supply Voltage	3.3±0.3 V or 5.0±0.5 V	5.0±0.5 V
	Program and Erase Endurance	100 times (all area) or 1,000 times (user ROM area without block A and block 1) / 10,000 times (block A, block 1) (3)	
Operating Ambient Temperature		-20 to 85°C, -40 to 85°C (3)	T version : -40 to 85°C V version : -40 to 125°C
Package		100-pin plastic mold QFP, LQFP	

NOTES:
1. I2C bus is a registered trademark of Koninklijke Philips Electronics N. V.
2. IEBus is a registered trademark of NEC Electronics Corporation.
3. See **Table 1.8 and 1.9 Product Code** for the program and erase endurance, and operating ambient temperature.
   In addition 1,000 times/10,000 times are under development as of Jul., 2005. Please inquire about a release schedule.
4. Use the M16C/62PT on VCC1=VCC2
5. All options are on request basis.



NOTES :
1. ROM size depends on microcomputer type.
2. RAM size depends on microcomputer type.
3. To use a UART2, set the CRD bit in the U2C0 register to “1” ($\overline{\text{CTS}}$/$\overline{\text{RTS}}$ function disabled).
4. There is no external connections for port P1, P4_4 to P4_7, P7_2 to P7_5 and P9_1 in 80-pin version. Set the direction bits in these ports to “1” (output mode), and set the output data to “0” (“L”) using the program.

Figure 1.2 M16C/62P Group (M16C/62P, M16C/62PT) 80-pin version Block Diagram

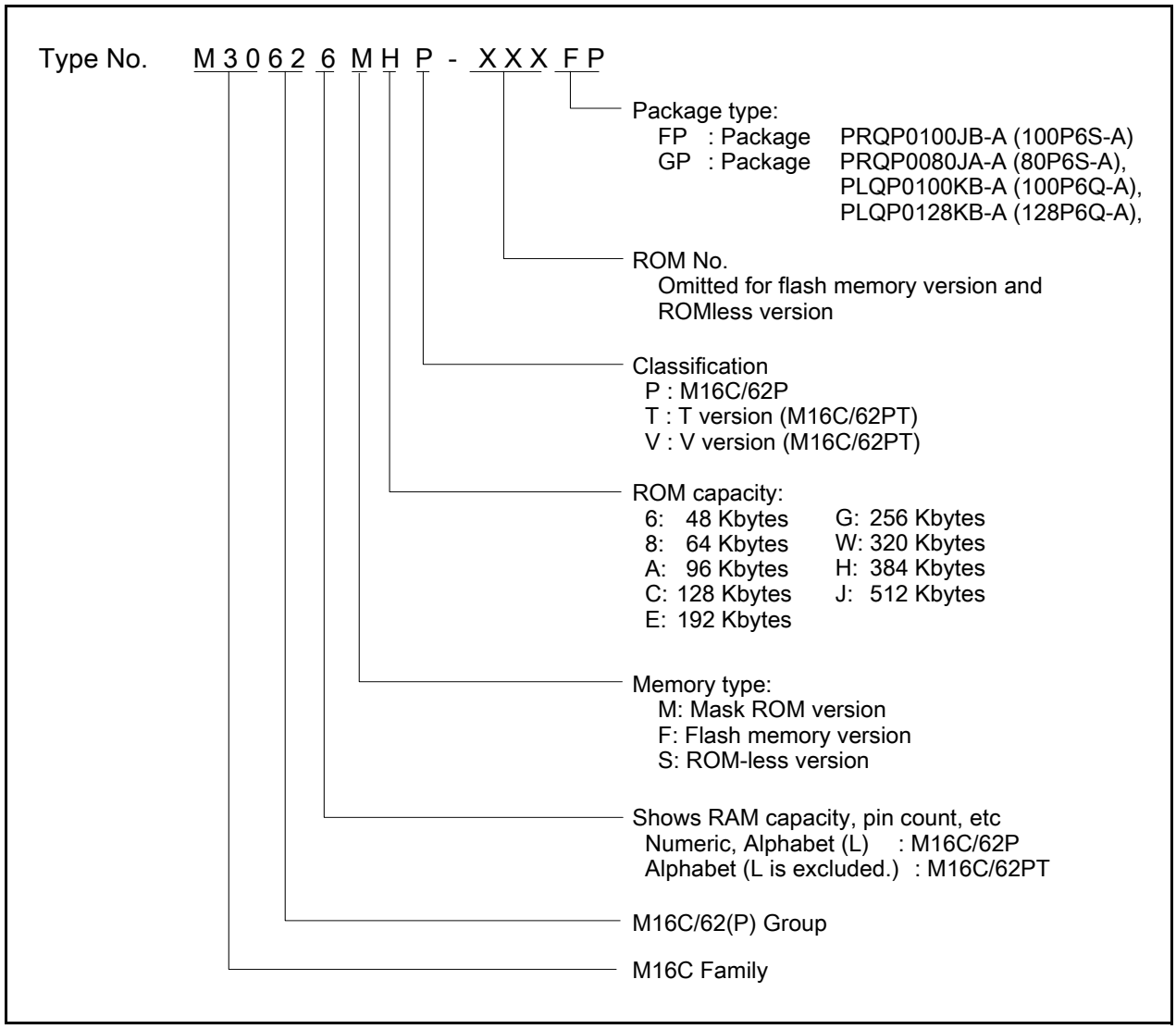


Figure 1.3 Type No., Memory Size, and Package

1.5 Pin Configuration

Figures 1.6 to 1.9 show the Pin Configuration (Top View).

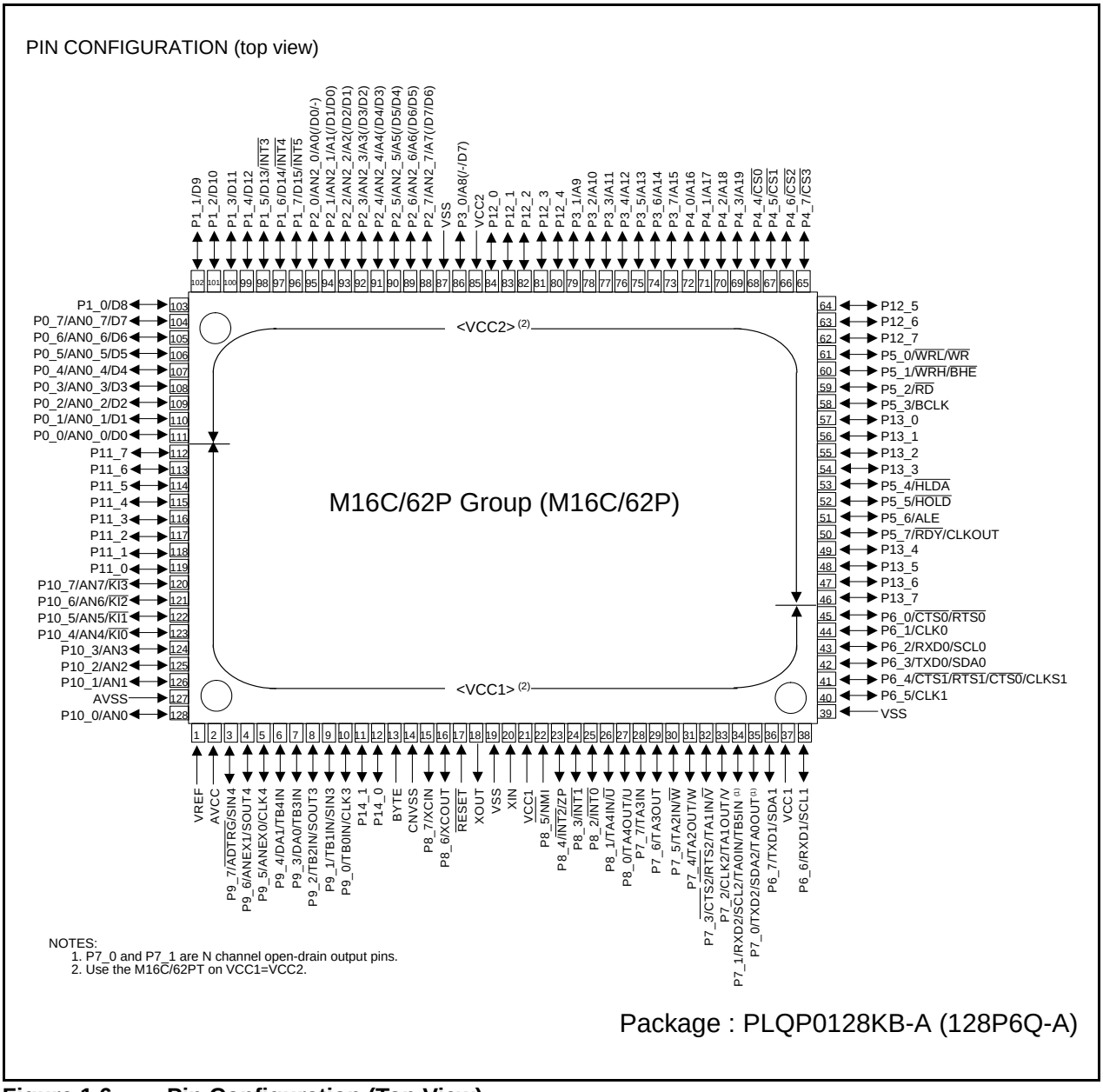


Figure 1.6 Pin Configuration (Top View)

Table 1.13 Pin Characteristics for 100-Pin Package (1)

Pin No.		Control Pin	Port	Interrupt Pin	Timer Pin	UART Pin	Analog Pin	Bus Control Pin
FP	GP							
1	99		P9_6			SOUT4	ANEX1	
2	100		P9_5			CLK4	ANEX0	
3	1		P9_4		TB4IN		DA1	
4	2		P9_3		TB3IN		DA0	
5	3		P9_2		TB2IN	SOUT3		
6	4		P9_1		TB1IN	SIN3		
7	5		P9_0		TB0IN	CLK3		
8	6	BYTE						
9	7	CNVSS						
10	8	XCIN	P8_7					
11	9	XCOUT	P8_6					
12	10	$\overline{\text{RESET}}$						
13	11	XOUT						
14	12	VSS						
15	13	XIN						
16	14	VCC1						
17	15		P8_5	$\overline{\text{NMI}}$				
18	16		P8_4	$\overline{\text{INT2}}$	ZP			
19	17		P8_3	$\overline{\text{INT1}}$				
20	18		P8_2	$\overline{\text{INT0}}$				
21	19		P8_1		TA4IN/$\overline{\text{U}}$			
22	20		P8_0		TA4OUT/U			
23	21		P7_7		TA3IN			
24	22		P7_6		TA3OUT			
25	23		P7_5		TA2IN/$\overline{\text{W}}$			
26	24		P7_4		TA2OUT/W			
27	25		P7_3		TA1IN/$\overline{\text{V}}$	$\overline{\text{CTS2}}$/$\overline{\text{RTS2}}$		
28	26		P7_2		TA1OUT/V	CLK2		
29	27		P7_1		TA0IN/TB5IN	RXD2/SCL2		
30	28		P7_0		TA0OUT	TXD2/SDA2		
31	29		P6_7			TXD1/SDA1		
32	30		P6_6			RXD1/SCL1		
33	31		P6_5			CLK1		
34	32		P6_4			$\overline{\text{CTS1}}$/$\overline{\text{RTS1}}$/$\overline{\text{CTS0}}$/CLKS1		
35	33		P6_3			TXD0/SDA0		
36	34		P6_2			RXD0/SCL0		
37	35		P6_1			CLK0		
38	36		P6_0			$\overline{\text{CTS0}}$/$\overline{\text{RTS0}}$		
39	37		P5_7					$\overline{\text{RDY}}$/CLKOUT
40	38		P5_6					ALE
41	39		P5_5					$\overline{\text{HOLD}}$
42	40		P5_4					$\overline{\text{HLAD}}$
43	41		P5_3					BCLK
44	42		P5_2					$\overline{\text{RD}}$
45	43		P5_1					$\overline{\text{WRH}}$/$\overline{\text{BHE}}$
46	44		P5_0					$\overline{\text{WRL}}$/$\overline{\text{WR}}$
47	45		P4_7					$\overline{\text{CS3}}$
48	46		P4_6					$\overline{\text{CS2}}$
49	47		P4_5					$\overline{\text{CS1}}$
50	48		P4_4					$\overline{\text{CS0}}$

Table 1.15 Pin Characteristics for 80-Pin Package (1)

Pin No.	Control Pin	Port	Interrupt Pin	Timer Pin	UART Pin	Analog Pin	Bus Control Pin
1		P9_5			CLK4	ANEX0	
2		P9_4		TB4IN		DA1	
3		P9_3		TB3IN		DA0	
4		P9_2		TB2IN	SOUT3		
5		P9_0		TB0IN	CLK3		
6	CNVSS (BYTE)						
7	XCIN	P8_7					
8	XCOUT	P8_6					
9	$\overline{\text{RESET}}$						
10	XOUT						
11	VSS						
12	XIN						
13	VCC1						
14		P8_5	$\overline{\text{NMI}}$				
15		P8_4	$\overline{\text{INT2}}$	ZP			
16		P8_3	$\overline{\text{INT1}}$				
17		P8_2	$\overline{\text{INT0}}$				
18		P8_1		TA4IN			
19		P8_0		TA4OUT			
20		P7_7		TA3IN			
21		P7_6		TA3OUT			
22		P7_1		TA0IN/TB5IN	RXD2/SCL2		
23		P7_0		TA0OUT	TXD2/SDA2		
24		P6_7			TXD1/SDA1		
25		P6_6			RXD1/SCL1		
26		P6_5			CLK1		
27		P6_4			$\overline{\text{CTS1}}$/$\overline{\text{RTS1}}$/$\overline{\text{CTS0}}$/CLKS1		
28		P6_3			TXD0/SDA0		
29		P6_2			RXD0/SCL0		
30		P6_1			CLK0		
31		P6_0			$\overline{\text{CTS0}}$/$\overline{\text{RTS0}}$		
32		P5_7					CLKOUT
33		P5_6					
34		P5_5					
35		P5_4					
36		P5_3					
37		P5_2					
38		P5_1					
39		P5_0					
40		P4_3					
41		P4_2					
42		P4_1					
43		P4_0					
44		P3_7					
45		P3_6					
46		P3_5					
47		P3_4					
48		P3_3					
49		P3_2					
50		P3_1					

1.6 Pin Description

Table 1.17 Pin Description (100-pin and 128-pin Version) (1)

Signal Name	Pin Name	I/O Type	Power Supply(3)	Description
Power supply input	VCC1,VCC2 VSS	I	–	Apply 2.7 to 5.5 V to the VCC1 and VCC2 pins and 0 V to the VSS pin. The VCC apply condition is that VCC1 ≥ VCC2. (1, 2)
Analog power supply input	AVCC AVSS	I	VCC1	Applies the power supply for the A/D converter. Connect the AVCC pin to VCC1. Connect the AVSS pin to VSS.
Reset input	$\overline{\text{RESET}}$	I	VCC1	The microcomputer is in a reset state when applying “L” to the this pin.
CNVSS	CNVSS	I	VCC1	Switches processor mode. Connect this pin to VSS to when after a reset to start up in single-chip mode. Connect this pin to VCC1 to start up in microprocessor mode.
External data bus width select input	BYTE	I	VCC1	Switches the data bus in external memory space. The data bus is 16 bits long when the this pin is held "L" and 8 bits long when the this pin is held "H". Set it to either one. Connect this pin to VSS when an single-chip mode.
Bus control pins (4)	D0 to D7	I/O	VCC2	Inputs and outputs data (D0 to D7) when these pins are set as the separate bus.
	D8 to D15	I/O	VCC2	Inputs and outputs data (D8 to D15) when external 16-bit data bus is set as the separate bus.
	A0 to A19	O	VCC2	Output address bits (A0 to A19).
	A0/D0 to A7/D7	I/O	VCC2	Input and output data (D0 to D7) and output address bits (A0 to A7) by timesharing when external 8-bit data bus are set as the multiplexed bus.
	A1/D0 to A8/D7	I/O	VCC2	Input and output data (D0 to D7) and output address bits (A1 to A8) by timesharing when external 16-bit data bus are set as the multiplexed bus.
	$\overline{\text{CS0}}$ to $\overline{\text{CS3}}$	O	VCC2	Output $\overline{\text{CS0}}$ to $\overline{\text{CS3}}$ signals. $\overline{\text{CS0}}$ to $\overline{\text{CS3}}$ are chip-select signals to specify an external space.
	$\overline{\text{WRL}}$/$\overline{\text{WR}}$ $\overline{\text{WRH}}$/$\overline{\text{BHE}}$ $\overline{\text{RD}}$	O	VCC2	Output $\overline{\text{WRL}}$, $\overline{\text{WRH}}$, ($\overline{\text{WR}}$, $\overline{\text{BHE}}$), $\overline{\text{RD}}$ signals. $\overline{\text{WRL}}$ and $\overline{\text{WRH}}$ or $\overline{\text{BHE}}$ and $\overline{\text{WR}}$ can be switched by program. • $\overline{\text{WRL}}$, $\overline{\text{WRH}}$ and $\overline{\text{RD}}$ are selected The $\overline{\text{WRL}}$ signal becomes "L" by writing data to an even address in an external memory space. The $\overline{\text{WRH}}$ signal becomes "L" by writing data to an odd address in an external memory space. The $\overline{\text{RD}}$ pin signal becomes "L" by reading data in an external memory space. • $\overline{\text{WR}}$, $\overline{\text{BHE}}$ and $\overline{\text{RD}}$ are selected The $\overline{\text{WR}}$ signal becomes "L" by writing data in an external memory space. The $\overline{\text{RD}}$ signal becomes "L" by reading data in an external memory space. The $\overline{\text{BHE}}$ signal becomes "L" by accessing an odd address. Select $\overline{\text{WR}}$, $\overline{\text{BHE}}$ and $\overline{\text{RD}}$ for an external 8-bit data bus.
	ALE	O	VCC2	ALE is a signal to latch the address.
	$\overline{\text{HOLD}}$	I	VCC2	While the $\overline{\text{HOLD}}$ pin is held "L", the microcomputer is placed in a hold state.
	$\overline{\text{HLDA}}$	O	VCC2	In a hold state, $\overline{\text{HLDA}}$ outputs a "L" signal.
	$\overline{\text{RDY}}$	I	VCC2	While applying a "L" signal to the $\overline{\text{RDY}}$ pin, the microcomputer is placed in a wait state.

I : Input O : Output I/O : Input and output

Power Supply : Power supplies which relate to the external bus pins are separated as VCC2, thus they can be interfaced using the different voltage as VCC1.

NOTES:

1. In this manual, hereafter, VCC refers to VCC1 unless otherwise noted.
2. In M16C/62PT, apply 4.0 to 5.5 V to the VCC1 and VCC2 pins. Also the apply condition is that VCC1 = VCC2.
3. When use VCC1 > VCC2, contacts due to some points or restrictions to be checked.
4. Bus control pins in M16C/62PT cannot be used.

Table 4.2 SFR Information (2) (1)

Address	Register	Symbol	After Reset
0040h			
0041h			
0042h			
0043h			
0044h	INT3 Interrupt Control Register	INT3IC	XX00X000b
0045h	Timer B5 Interrupt Control Register	TB5IC	XXXXX000b
0046h	Timer B4 Interrupt Control Register, UART1 BUS Collision Detection Interrupt Control Register	TB4IC, U1BCNIC	XXXXX000b
0047h	Timer B3 Interrupt Control Register, UART0 BUS Collision Detection Interrupt Control Register	TB3IC, U0BCNIC	XXXXX000b
0048h	SI/O4 Interrupt Control Register, INT5 Interrupt Control Register	S4IC, INT5IC	XX00X000b
0049h	SI/O3 Interrupt Control Register, INT4 Interrupt Control Register	S3IC, INT4IC	XX00X000b
004Ah	UART2 Bus Collision Detection Interrupt Control Register	BCNIC	XXXXX000b
004Bh	DMA0 Interrupt Control Register	DM0IC	XXXXX000b
004Ch	DMA1 Interrupt Control Register	DM1IC	XXXXX000b
004Dh	Key Input Interrupt Control Register	KUPIC	XXXXX000b
004Eh	A/D Conversion Interrupt Control Register	ADIC	XXXXX000b
004Fh	UART2 Transmit Interrupt Control Register	S2TIC	XXXXX000b
0050h	UART2 Receive Interrupt Control Register	S2RIC	XXXXX000b
0051h	UART0 Transmit Interrupt Control Register	S0TIC	XXXXX000b
0052h	UART0 Receive Interrupt Control Register	S0RIC	XXXXX000b
0053h	UART1 Transmit Interrupt Control Register	S1TIC	XXXXX000b
0054h	UART1 Receive Interrupt Control Register	S1RIC	XXXXX000b
0055h	Timer A0 Interrupt Control Register	TA0IC	XXXXX000b
0056h	Timer A1 Interrupt Control Register	TA1IC	XXXXX000b
0057h	Timer A2 Interrupt Control Register	TA2IC	XXXXX000b
0058h	Timer A3 Interrupt Control Register	TA3IC	XXXXX000b
0059h	Timer A4 Interrupt Control Register	TA4IC	XXXXX000b
005Ah	Timer B0 Interrupt Control Register	TB0IC	XXXXX000b
005Bh	Timer B1 Interrupt Control Register	TB1IC	XXXXX000b
005Ch	Timer B2 Interrupt Control Register	TB2IC	XXXXX000b
005Dh	INT0 Interrupt Control Register	INT0IC	XX00X000b
005Eh	INT1 Interrupt Control Register	INT1IC	XX00X000b
005Fh	INT2 Interrupt Control Register	INT2IC	XX00X000b
0060h			
0061h			
0062h			
0063h			
0064h			
0065h			
0066h			
0067h			
0068h			
0069h			
006Ah			
006Bh			
006Ch			
006Dh			
006Eh			
006Fh			
0070h			
0071h			
0072h			
0073h			
0074h			
0075h			
0076h			
0077h			
0078h			
0079h			
007Ah			
007Bh			
007Ch			
007Dh			
007Eh			
007Fh			

NOTES:
1. The blank areas are reserved and cannot be accessed by users.

X : Nothing is mapped to this bit

Table 4.4 SFR Information (4) (1)

Address	Register	Symbol	After Reset
0340h	Timer B3, 4, 5 Count Start Flag	TBSR	000XXXXXb
0341h			
0342h	Timer A1-1 Register	TA11	XXh
0343h			XXh
0344h	Timer A2-1 Register	TA21	XXh
0345h			XXh
0346h	Timer A4-1 Register	TA41	XXh
0347h			XXh
0348h	Three-Phase PWM Control Register 0	INVC0	00h
0349h	Three-Phase PWM Control Register 1	INVC1	00h
034Ah	Three-Phase Output Buffer Register 0	IDB0	00h
034Bh	Three-Phase Output Buffer Register 1	IDB1	00h
034Ch	Dead Time Timer	DTT	XXh
034Dh	Timer B2 Interrupt Occurrence Frequency Set Counter	ICTB2	XXh
034Eh			
034Fh			
0350h	Timer B3 Register	TB3	XXh
0351h			XXh
0352h	Timer B4 Register	TB4	XXh
0353h			XXh
0354h	Timer B5 Register	TB5	XXh
0355h			XXh
0356h			
0357h			
0358h			
0359h			
035Ah			
035Bh	Timer B3 Mode Register	TB3MR	00XX0000b
035Ch	Timer B4 Mode Register	TB4MR	00XX0000b
035Dh	Timer B5 Mode Register	TB5MR	00XX0000b
035Eh	Interrupt Factor Select Register 2	IFSR2A	00XXXXXXb
035Fh	Interrupt Factor Select Register	IFSR	00h
0360h	SI/O3 Transmit/Receive Register	S3TRR	XXh
0361h			
0362h	SI/O3 Control Register	S3C	01000000b
0363h	SI/O3 Bit Rate Generator	S3BRG	XXh
0364h	SI/O4 Transmit/Receive Register	S4TRR	XXh
0365h			
0366h	SI/O4 Control Register	S4C	01000000b
0367h	SI/O4 Bit Rate Generator	S4BRG	XXh
0368h			
0369h			
036Ah			
036Bh			
036Ch	UART0 Special Mode Register 4	U0SMR4	00h
036Dh	UART0 Special Mode Register 3	U0SMR3	000X0X0Xb
036Eh	UART0 Special Mode Register 2	U0SMR2	X0000000b
036Fh	UART0 Special Mode Register	U0SMR	X0000000b
0370h	UART1 Special Mode Register 4	U1SMR4	00h
0371h	UART1 Special Mode Register 3	U1SMR3	000X0X0Xb
0372h	UART1 Special Mode Register 2	U1SMR2	X0000000b
0373h	UART1 Special Mode Register	U1SMR	X0000000b
0374h	UART2 Special Mode Register 4	U2SMR4	00h
0375h	UART2 Special Mode Register 3	U2SMR3	000X0X0Xb
0376h	UART2 Special Mode Register 2	U2SMR2	X0000000b
0377h	UART2 Special Mode Register	U2SMR	X0000000b
0378h	UART2 Transmit/Receive Mode Register	U2MR	00h
0379h	UART2 Bit Rate Generator	U2BRG	XXh
037Ah	UART2 Transmit Buffer Register	U2TB	XXh
037Bh			XXh
037Ch	UART2 Transmit/Receive Control Register 0	U2C0	00001000b
037Dh	UART2 Transmit/Receive Control Register 1	U2C1	00000010b
037Eh	UART2 Receive Buffer Register	U2RB	XXh
037Fh			XXh

NOTES:
1. The blank areas are reserved and cannot be accessed by users.

X : Nothing is mapped to this bit

5. Electrical Characteristics

5.1 Electrical Characteristics (M16C/62P)

Table 5.1 Absolute Maximum Ratings

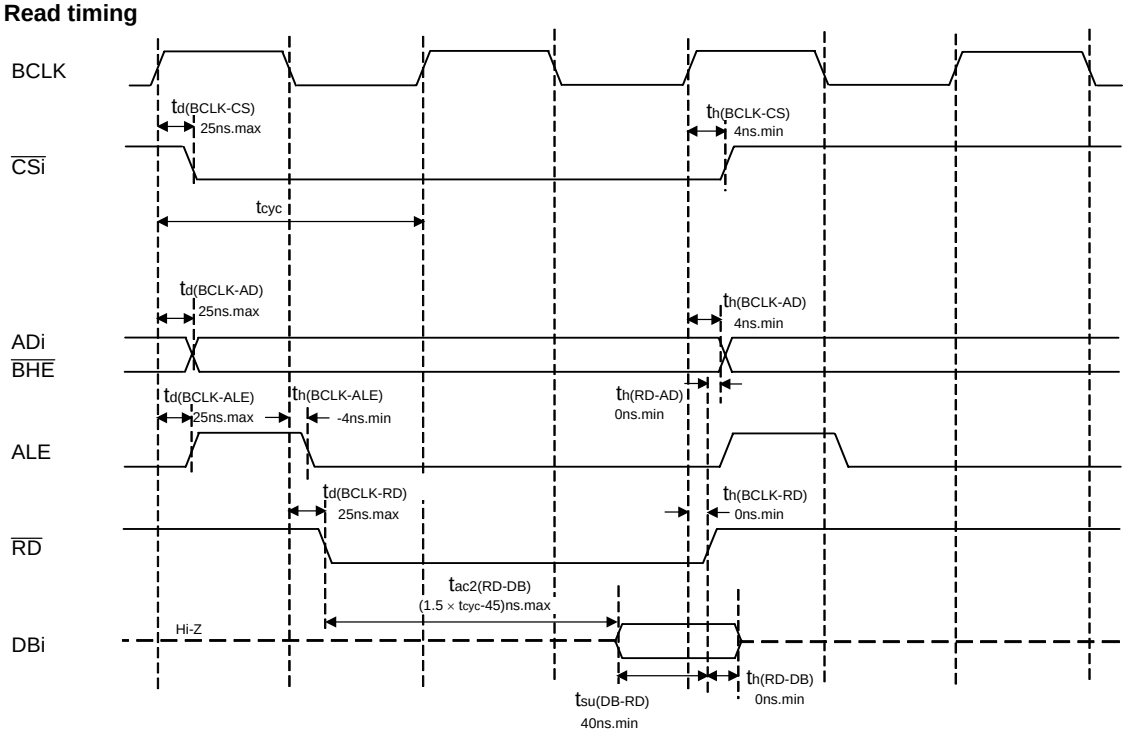
Symbol	Parameter		Condition	Rated Value	Unit
V_{CC1}, V_{CC2}	Supply Voltage		V_{CC1}=AVcc	–0.3 to 6.5	V
V_{CC2}	Supply Voltage		V_{CC2}	–0.3 to V_{CC1}+0.1	V
AVcc	Analog Supply Voltage		V_{CC1}=AVcc	–0.3 to 6.5	V
V_I	Input Voltage	$\overline{\text{RESET}}$, CNVSS, BYTE, P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P14_0, P14_1, VREF, XIN		–0.3 to V_{CC1}+0.3 (1)	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P12_0 to P12_7, P13_0 to P13_7		–0.3 to V_{CC2}+0.3 (1)	V
		P7_0, P7_1		–0.3 to 6.5	V
V_O	Output Voltage	P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P14_0, P14_1, XOUT		–0.3 to V_{CC1}+0.3 (1)	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P12_0 to P12_7, P13_0 to P13_7		–0.3 to V_{CC2}+0.3 (1)	V
		P7_0, P7_1		–0.3 to 6.5	V
P_d	Power Dissipation		–40°C<T_{opr}≤85°C	300	mW
T_{opr}	Operating Ambient Temperature	When the Microcomputer is Operating		–20 to 85 / –40 to 85	°C
		Flash Program Erase		0 to 60	
T_{stg}	Storage Temperature			–65 to 150	°C

NOTES:
1. There is no external connections for port P1_0 to P1_7, P4_4 to P4_7, P7_2 to P7_5 and P9_1 in 80-pin version.

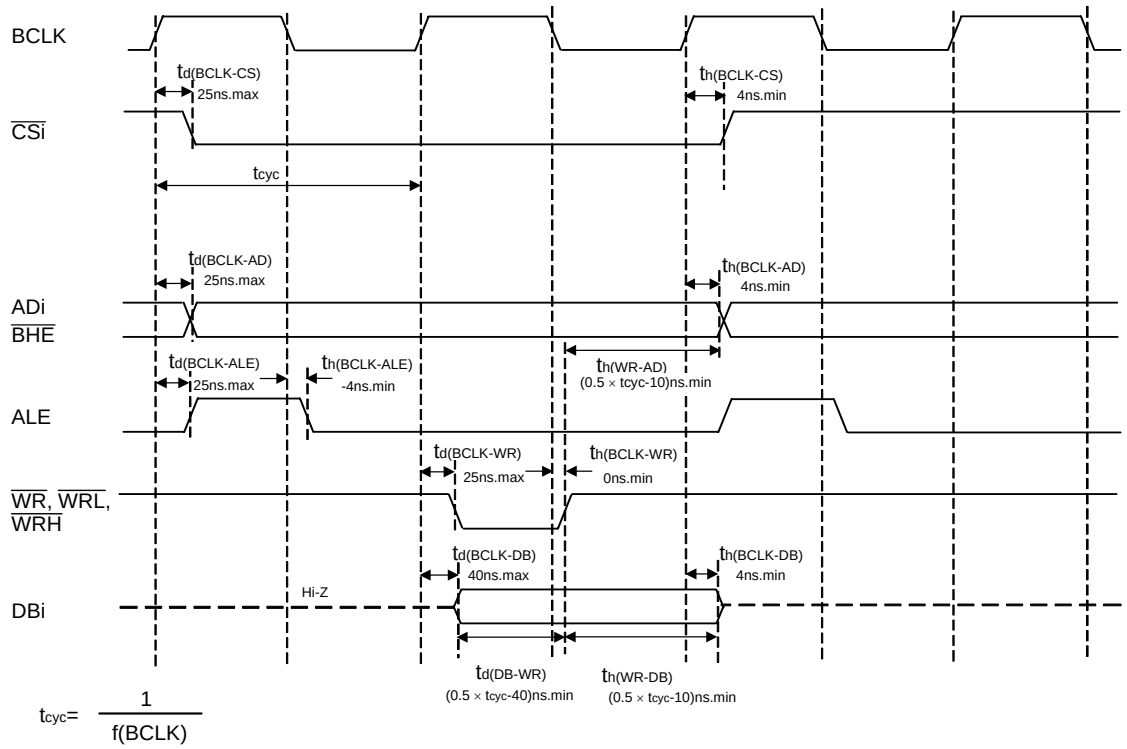
$V_{CC1}=V_{CC2}=5V$

Memory Expansion Mode, Microprocessor Mode
(for 1-wait setting and external area access**)**

Read timing



Write timing



$$t_{cyc}=\frac{1}{f(BCLK)}$$

Measuring conditions
· $V_{CC1}=V_{CC2}=5V$
· Input timing voltage : $V_{IL}=0.8V$, $V_{IH}=2.0V$
· Output timing voltage : $V_{OL}=0.4V$, $V_{OH}=2.4V$

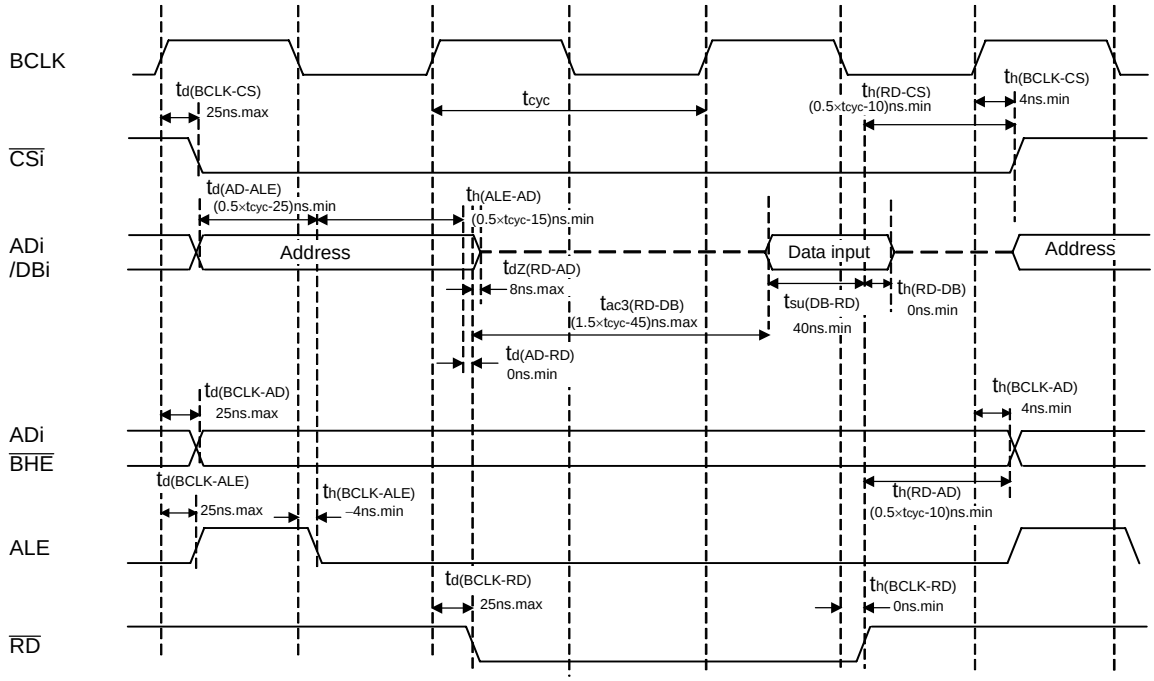
Figure 5.7 Timing Diagram (5)

$V_{CC1}=V_{CC2}=5V$

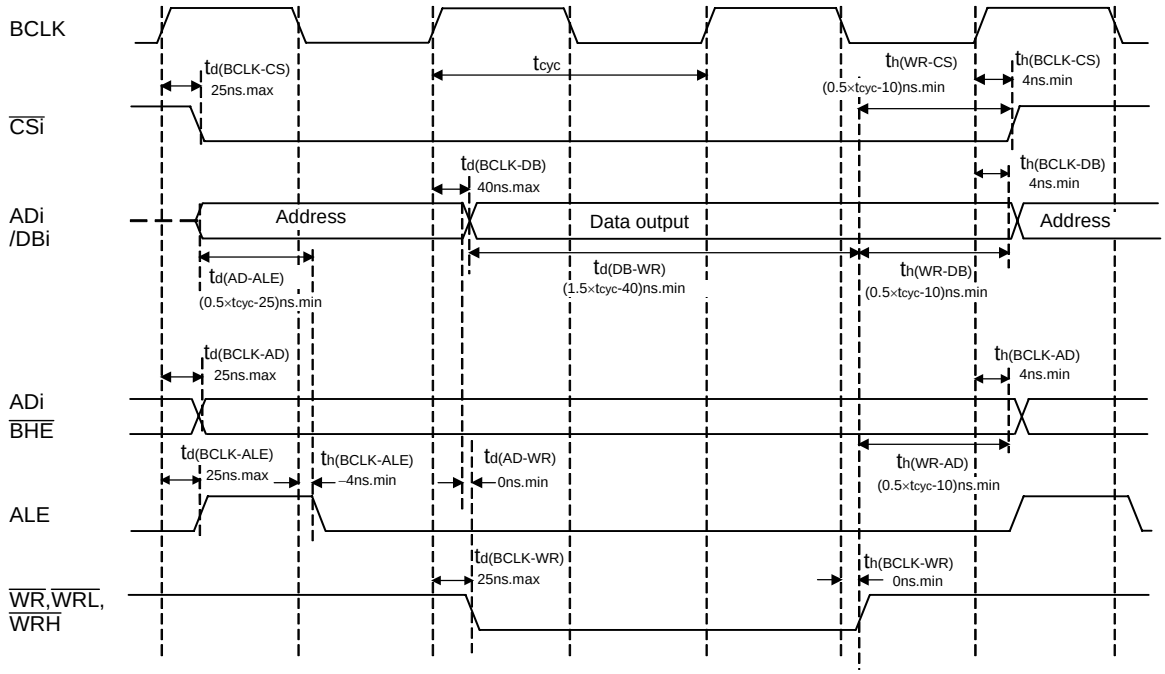
Memory Expansion Mode, Microprocessor Mode

(For 1- or 2-wait setting, external area access and multiplex bus selection**)**

Read timing



Write timing



Measuring conditions
· $V_{CC1}=V_{CC2}=5V$
· Input timing voltage : $V_{IL}=0.8V$, $V_{IH}=2.0V$
· Output timing voltage : $V_{OL}=0.4V$, $V_{OH}=2.4V$

Figure 5.10 Timing Diagram (8)

$V_{CC1}=V_{CC2}=3V$

Table 5.30 Electrical Characteristics (1) (1)

Symbol	Parameter		Measuring Condition	Standard			Unit
				Min.	Typ.	Max.	
V_{OH}	HIGH Output Voltage (3)	P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P14_0, P14_1	I_{OH}=–1mA	V_{CC1}–0.5		V_{CC1}	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P12_0 to P12_7, P13_0 to P13_7	I_{OH}=–1mA (2)	V_{CC2}–0.5		V_{CC2}	
V_{OH}	HIGH Output Voltage XOUT	HIGHPOWER	I_{OH}=–0.1mA	V_{CC1}–0.5		V_{CC1}	V
		LOWPOWER	I_{OH}=–50µA	V_{CC1}–0.5		V_{CC1}	
	HIGH Output Voltage XCOUT	HIGHPOWER	With no load applied		2.5		V
		LOWPOWER	With no load applied		1.6		
V_{OL}	LOW Output Voltage (3)	P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P14_0, P14_1	I_{OL}=1mA			0.5	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P12_0 to P12_7, P13_0 to P13_7	I_{OL}=1mA (2)			0.5	
V_{OL}	LOW Output Voltage XOUT	HIGHPOWER	I_{OL}=0.1mA			0.5	V
		LOWPOWER	I_{OL}=50µA			0.5	
	LOW Output Voltage XCOUT	HIGHPOWER	With no load applied		0		V
		LOWPOWER	With no load applied		0		
V_{T+}-V_{T-}	Hysteresis	$\overline{HOLD}$, $\overline{RDY}$, TA0IN to TA4IN, $\overline{TB0IN}$ to $\overline{TB5IN}$, $\overline{INT0}$ to $\overline{INT5}$, $\overline{NMI}$, $\overline{ADTRG}$, $\overline{CTS0}$ to $\overline{CTS2}$, CLK0 to CLK4, TA0OUT to TA4OUT, $\overline{KI0}$ to $\overline{KI3}$, RXD0 to RXD2, SCL0 to SCL2, SDA0 to SDA2, SIN3, SIN4		0.2		0.8	V
V_{T+}-V_{T-}	Hysteresis	$\overline{RESET}$		0.2	(0.7)	1.8	V
I_{IH}	HIGH Input Current (3)	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1, XIN, $\overline{RESET}$, CNVSS, BYTE	V_I=3V			4.0	µA
I_{IL}	LOW Input Current (3)	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1, XIN, $\overline{RESET}$, CNVSS, BYTE	V_I=0V			–4.0	µA
R_{PULLUP}	Pull-Up Resistance (3)	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7,P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1	V_I=0V	50	100	500	kΩ
R_{fXIN}	Feedback Resistance XIN				3.0		MΩ
R_{fXCIN}	Feedback Resistance XCIN				25		MΩ
V_{RAM}	RAM Retention Voltage		At stop mode	2.0			V

NOTES:
1. Referenced to V_{CC1} = V_{CC2} = 2.7 to 3.3V, V_{SS} = 0V at Topr = –20 to 85°C / –40 to 85°C, f(XIN)=10MHz no wait unless otherwise specified.
2. V_{CC1} for the port P6 to P11 and P14, and V_{CC2} for the port P0 to P5 and P12 to P13
3. There is no external connections for port P1_0 to P1_7, P4_4 to P4_7, P7_2 to P7_5 and P9_1 in 80-pin version.

$V_{CC1}=V_{CC2}=3V$

Switching Characteristics

(V_{CC1} = V_{CC2} = 3V, V_{SS} = 0V, at T_{opr} = –20 to 85°C / –40 to 85°C unless otherwise specified)

Table 5.46 Memory Expansion and Microprocessor Modes (for setting with no wait)

Symbol	Parameter		Standard		Unit
			Min.	Max.	
td(BCLK-AD)	Address Output Delay Time	See **Figure 5.12**		30	ns
th(BCLK-AD)	Address Output Hold Time (in relation to BCLK)		4		ns
th(RD-AD)	Address Output Hold Time (in relation to RD)		0		ns
th(WR-AD)	Address Output Hold Time (in relation to WR)		(NOTE 2)		ns
td(BCLK-CS)	Chip Select Output Delay Time			30	ns
th(BCLK-CS)	Chip Select Output Hold Time (in relation to BCLK)		4		ns
td(BCLK-ALE)	ALE Signal Output Delay Time			25	ns
th(BCLK-ALE)	ALE Signal Output Hold Time		–4		ns
td(BCLK-RD)	RD Signal Output Delay Time			30	ns
th(BCLK-RD)	RD Signal Output Hold Time		0		ns
td(BCLK-WR)	WR Signal Output Delay Time			30	ns
th(BCLK-WR)	WR Signal Output Hold Time		0		ns
td(BCLK-DB)	Data Output Delay Time (in relation to BCLK)			40	ns
th(BCLK-DB)	Data Output Hold Time (in relation to BCLK) (3)		4		ns
td(DB-WR)	Data Output Delay Time (in relation to WR)		(NOTE 1)		ns
th(WR-DB)	Data Output Hold Time (in relation to WR) (3)		(NOTE 2)		ns
td(BCLK-HLDA)	HLDA Output Delay Time			40	ns

NOTES:

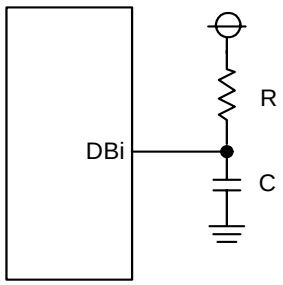
1. Calculated according to the BCLK frequency as follows:

$$\frac{0.5\times10^{9}}{f(BCLK)} - 40[ns]$$ f(BCLK) is 12.5MHz or less.

2. Calculated according to the BCLK frequency as follows:

$$\frac{0.5\times10^{9}}{f(BCLK)} - 10[ns]$$

3. This standard value shows the timing when the output is off, and does not show hold time of data bus.
   Hold time of data bus varies with capacitor volume and pull-up (pull-down) resistance value.
   Hold time of data bus is expressed in
   $t = -CR \times \ln(1 - V_{OL} / V_{CC2})$
   by a circuit of the right figure.
   For example, when $V_{OL} = 0.2V_{CC2}$, C = 30pF, R = 1kΩ, hold time of output "L" level is
   $t = -30pF \times 1k\Omega \times \ln(1 - 0.2V_{CC2} / V_{CC2})$
   = 6.7ns.



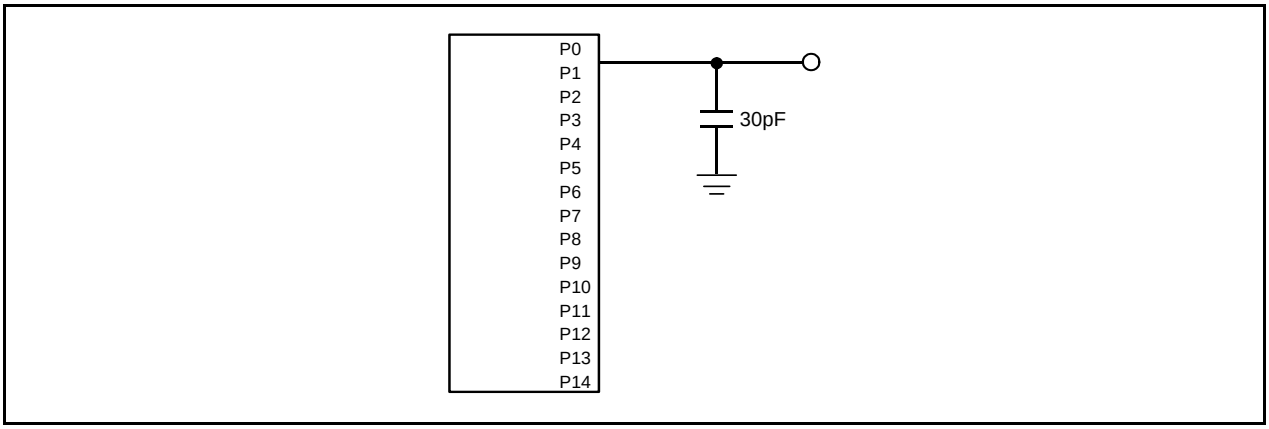


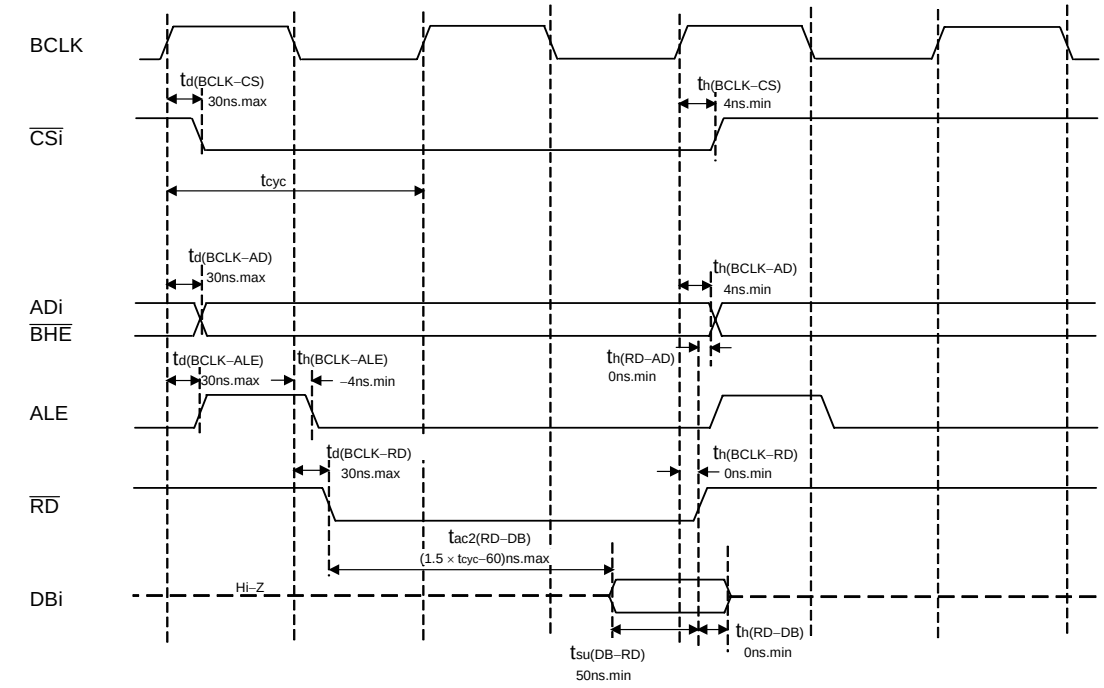
Figure 5.12 Ports P0 to P14 Measurement Circuit

Memory Expansion Mode, Microprocessor Mode

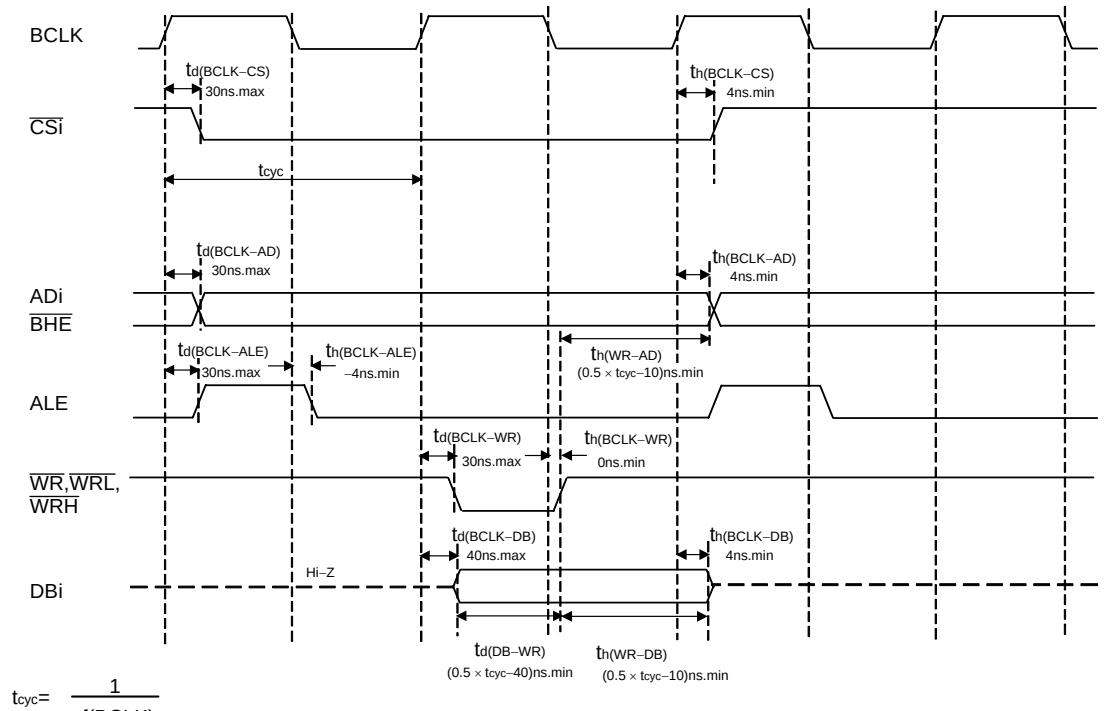
(for 1-wait setting and external area access**)**

$V_{CC1}=V_{CC2}=3V$

Read timing



Write timing



$$t_{cyc}=\frac{1}{f(BCLK)}$$

Measuring conditions

· $V_{CC1}=V_{CC2}=3V$

· Input timing voltage : $V_{IL}=0.6V$, $V_{IH}=2.4V$

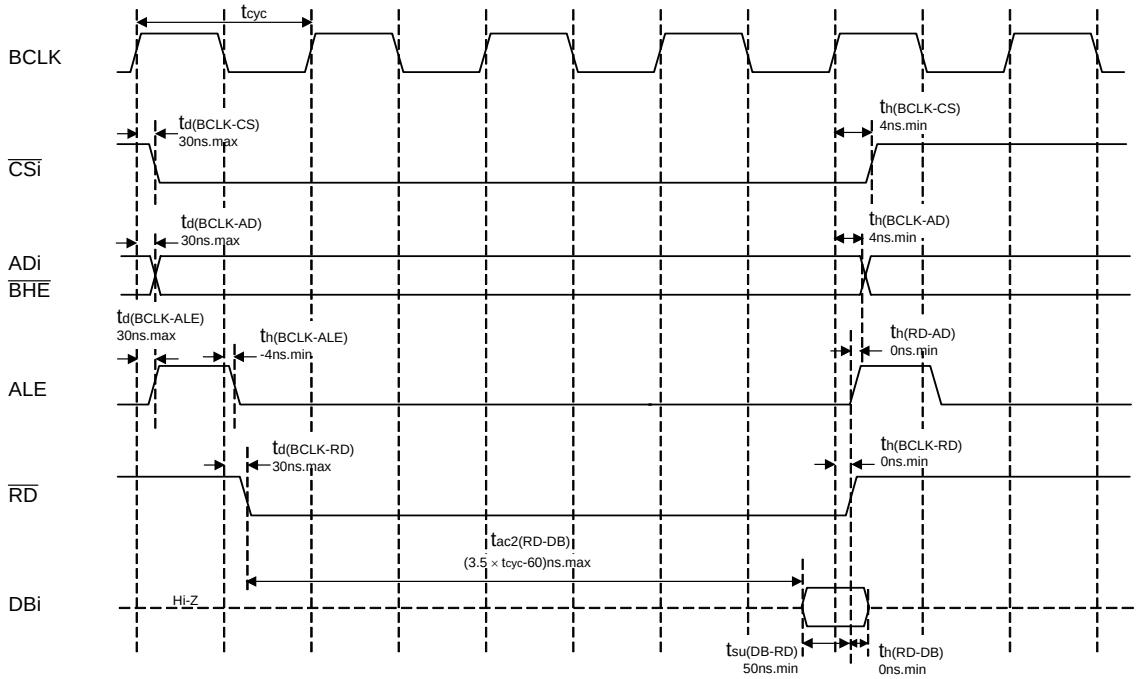
· Output timing voltage : $V_{OL}=1.5V$, $V_{OH}=1.5V$

Figure 5.17 Timing Diagram (5)

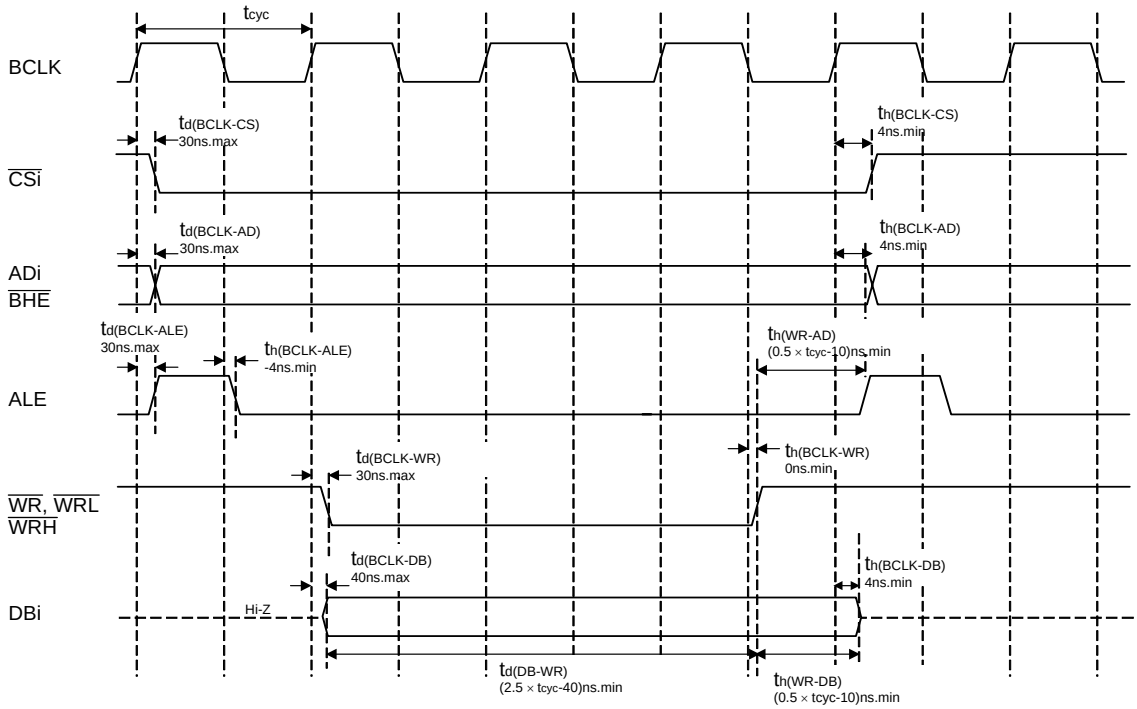
$V_{CC1} = V_{CC2} = 3V$

Memory Expansion Mode, Microprocessor Mode
(for 3-wait setting and external area access**)**

Read timing



Write timing



$$t_{cyc} = \frac{1}{f(BCLK)}$$

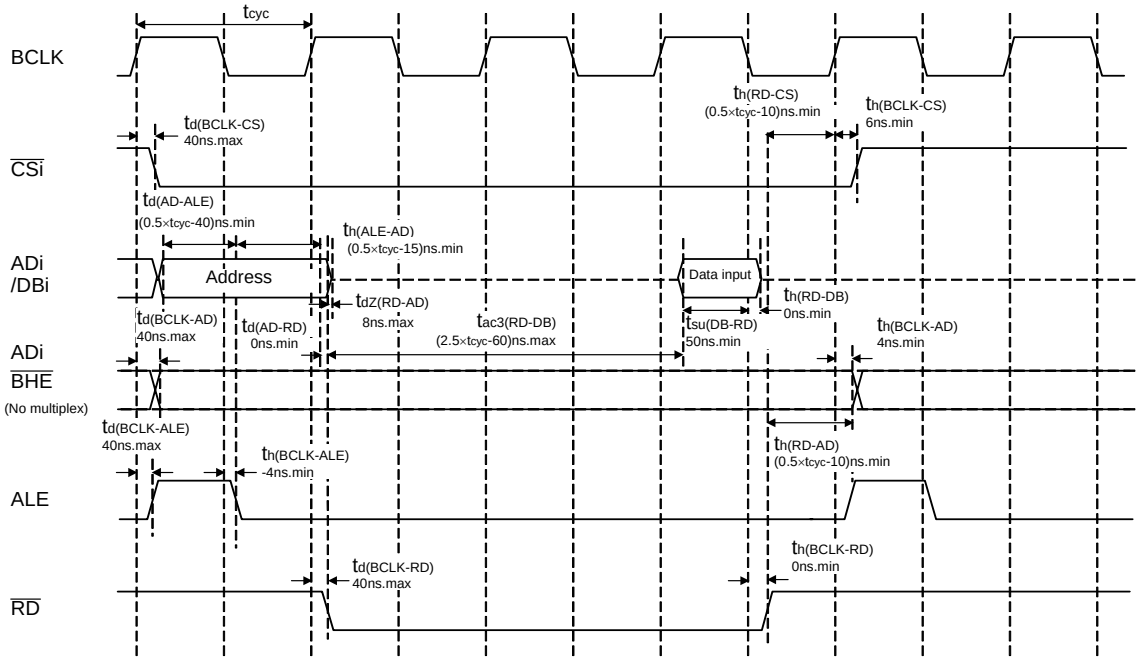
Measuring conditions
· V_{CC1}=V_{CC2}=3V
· Input timing voltage : V_{IL}=0.6V, V_{IH}=2.4V
· Output timing voltage : V_{OL}=1.5V, V_{OH}=1.5V

Figure 5.19 Timing Diagram (7)

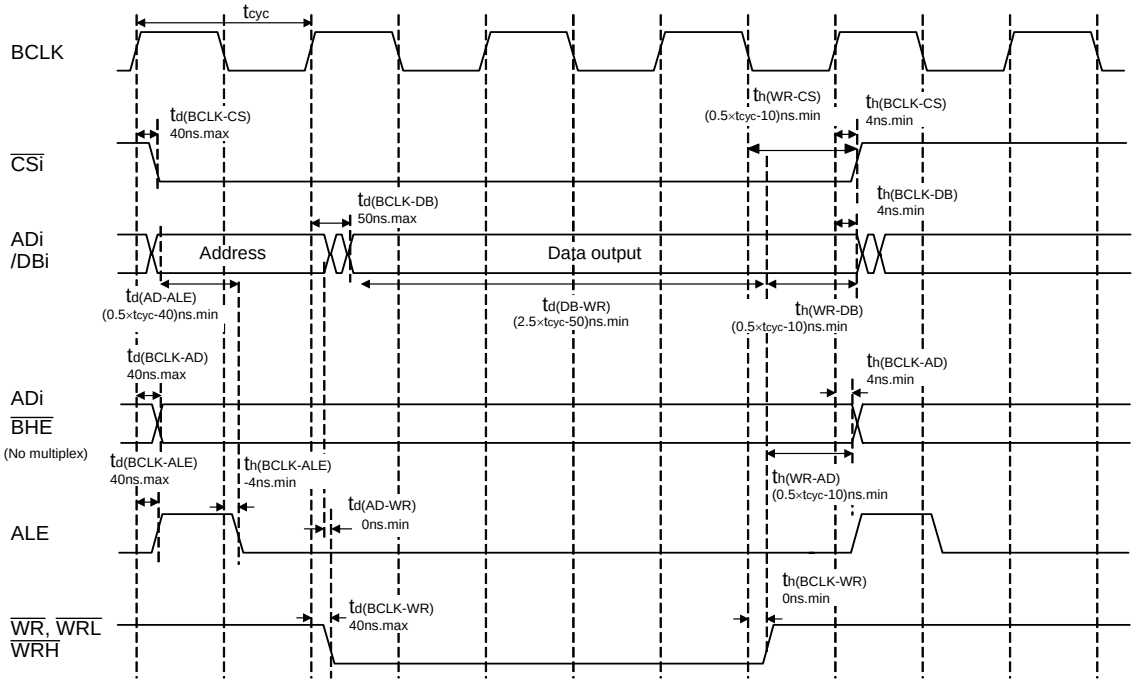
$V_{CC1}=V_{CC2}=3V$

Memory Expansion Mode, Microprocessor Mode
(For 3-wait setting, external area access and multiplex bus selection)

Read timing



Write timing



$$t_{cyc}=\frac{1}{f(BCLK)}$$

Measuring conditions
- $V_{CC1}=V_{CC2}=3V$
- Input timing voltage : $V_{IL}=0.6V$, $V_{IH}=2.4V$
- Output timing voltage : $V_{OL}=1.5V$, $V_{OH}=1.5V$

Figure 5.21 Timing Diagram (9)

Table 5.53 Flash Memory Version Electrical Characteristics (1) for 100 cycle products (B, U)

Symbol	Parameter		Standard			Unit
			Min.	Typ.	Max.	
–	Program and Erase Endurance (3)		100			cycle
–	Word Program Time (V_{CC1}=5.0V)			25	200	µs
–	Lock Bit Program Time			25	200	µs
–	Block Erase Time (V_{CC1}=5.0V)	4-Kbyte block	4	0.3	4	s
–		8-Kbyte block		0.3	4	s
–		32-Kbyte block		0.5	4	s
–		64-Kbyte block		0.8	4	s
–	Erase All Unlocked Blocks Time (2)				4×n	s
t_{PS}	Flash Memory Circuit Stabilization Wait Time				15	µs
–	Data Hold Time (5)		20			year

Table 5.54 Flash Memory Version Electrical Characteristics (6) for 10,000 cycle products (B7, U7) (Block A and Block 1 (7))

Symbol	Parameter		Standard			Unit
			Min.	Typ.	Max.	
–	Program and Erase Endurance (3, 8, 9)		10,000 (4)			cycle
–	Word Program Time (V_{CC}1=5.0V)			25		µs
–	Lock Bit Program Time			25		µs
–	Block Erase Time (V_{CC1}=5.0V)	4-Kbyte block	4	0.3		s
t_{PS}	Flash Memory Circuit Stabilization Wait Time				15	µs
–	Data Hold Time (5)		20			year

NOTES:
1. Referenced to V_{CC1}=4.5 to 5.5V at T_{opr} = 0 to 60 °C unless otherwise specified.
2. n denotes the number of block erases.
3. Program and Erase Endurance refers to the number of times a block erase can be performed.
   If the program and erase endurance is n (n=100, 1,000, or 10,000), each block can be erased n times.
   For example, if a 4 Kbytes block A is erased after writing 1 word data 2,048 times, each to a different address, this counts as one program and erase endurance. Data cannot be written to the same address more than once without erasing the block. (Rewrite prohibited)
4. Maximum number of E/W cycles for which operation is guaranteed.
5. Ta (ambient temperature)=55 °C. As to the data hold time except Ta=55 °C, please contact Renesas Technology Corp. or an authorized Renesas Technology Corp. product distributor.
6. Referenced to V_{CC1} = 4.5 to 5.5V at T_{opr} = –40 to 85 °C (B7, U7 (T version)) / –40 to 125 °C (B7, U7 (V version)) unless otherwise specified.
7. Table 5.54 applies for block A or block 1 program and erase endurance > 1,000. Otherwise, use Table 5.53.
8. To reduce the number of program and erase endurance when working with systems requiring numerous rewrites, write to unused word addresses within the block instead of rewrite. Erase block only after all possible addresses are used. For example, an 8-word program can be written 256 times maximum before erase becomes necessary.
   Maintaining an equal number of erasure between block A and block 1 will also improve efficiency. It is important to track the total number of times erasure is used.
9. Should erase error occur during block erase, attempt to execute clear status register command, then block erase command at least three times until erase error disappears.
10. Set the PM17 bit in the PM1 register to “1” (wait state) when executing more than 100 times rewrites (B7 and U7).
11. Customers desiring E/W failure rate information should contact their Renesas technical support representative.

Table 5.55 Flash Memory Version Program/Erase Voltage and Read Operation Voltage Characteristics (at T_{opr} = 0 to 60 °C(B, U), T_{opr} = –40 to 85 °C (B7, U7 (T version)) / –40 to 125 °C (B7, U7 (V version))

Flash Program, Erase Voltage	Flash Read Operation Voltage
V_{CC1} = 5.0 V ± 0.5 V	V_{CC1}=4.0 to 5.5 V

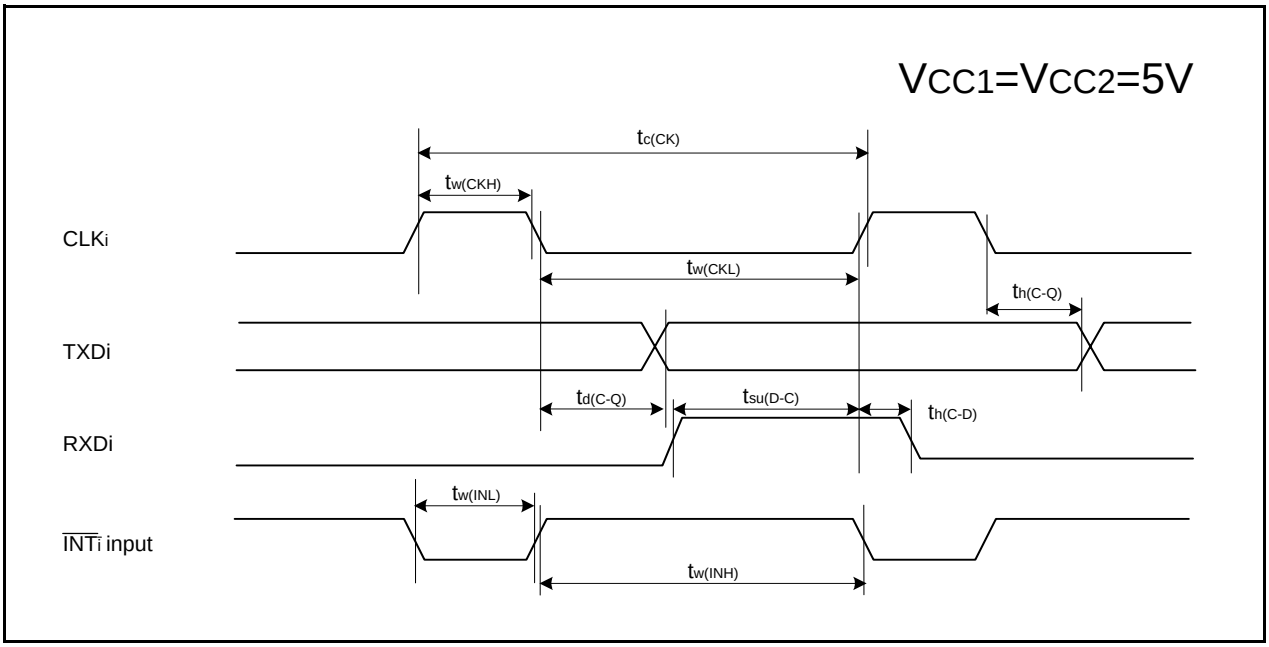


Figure 5.25 Timing Diagram (2)

Rev.	Date	Description	
		Page	Summary
		33	Table 5.4 A-D Conversion Characteristics is revised.
			Table 5.5 D-A Conversion Characteristics revised.
		34,74	Table 5.6 to 5.7 and table 5.54 to 5.55 are revised.
		36	Table 5.11 is revised.
		38,55	Table 5.14 and 5.33 HLDA output deley time is deleted.
		41	Figure 5.1 is partly revised.
		41-43, 58-60	Table 5.27 to 5.29 and table 5.46 to 48 HLDA output deley time is added.
		44	Figure 5.2 Timing Diagram (1) XIN input is added.
		47-48	Figure 5.5 to 5.6 Read timing DB → DBi
		49-50	Figure 5.7 to 5.8 Write timing DB → DBi
		52	Figure 5.10 DB → DBi
		53	Table 5.30 is revised.
		58	Figure 5.11 is partly revised.
		61	Figure 5.12 Timing Diagram (1) XIN input is added.
		64-65	Figure 5.15 to 5.16 Read timing DB → DBi
		66-67	Figure 5.17 to 5.18 Write timing DB → DBi
		69	Figure 5.20 DB → DBi
		70-85	Electrical Characteristics (M16C/62PT) is added.
2.10	Nov 07, 2003	8-9	Table 1.5 to 1.7 Product List is partly revised. Note 1 is deleted.
		23	Table 3.1 is revised.
		71	Table 5.50 is revised.
		72	Table 5.51 is deleted.
2.11	Jan 06, 2004	16	Table 1.9 NOTE 3 VCC1 VCC2 → VCC1 > VCC2
		17-18	Table 1.10 to 1.11 NOTE 1 VCC1 VCC2 → VCC1 > VCC2
		31	Table 5.2 Power Supply Ripple Allowable Frequency Unit MHz → kHz
2.30	Sep 01, 2004	12	Table 1.9 and Figure 1.5 are added.
		18, 20	Table 1.11 to 1.13 are revised.
		19,21	Table 1.12 to 1.14 are revised.
		24	Figure 3.1 is partly revised.
			Note 3 is added.
		25	Note 6 is added.
		33	Table 5.3 is revised.
			Note 2 in Table 5.4 is added.
		34	Table 5.5 to 5.6 is partly revised.
		35	Table 5.8 is revised.
			Table 5.9 is revised.
		37	Table 5.11 is revised.