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Details

Product Status	Obsolete
Core Processor	M16C/60
Core Size	16-Bit
Speed	24MHz
Connectivity	I ² C, IEBus, UART/USART
Peripherals	DMA, WDT
Number of I/O	85
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 26x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-BQFP
Supplier Device Package	100-QFP (14x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/m30622f8pfp-u7c

Table 1.5 Product List (2) (M16C/62P)

As of Dec. 2005

Type No.	ROM Capacity	RAM Capacity	Package Type ⁽¹⁾	Remarks
M30622MHP-XXXFP	384 Kbytes	16 Kbytes	PRQP0100JB-A	Mask ROM version
M30622MHP-XXXGP			PLQP0100KB-A	
M30623MHP-XXXGP			PLQP0128KB-A	
M30624MHP-XXXFP		24 Kbytes	PRQP0100JB-A	
M30624MHP-XXXGP			PLQP0100KB-A	
M30625MHP-XXXGP			PLQP0128KB-A	
M30626MHP-XXXFP		31 Kbytes	PRQP0100JB-A	
M30626MHP-XXXGP			PLQP0100KB-A	
M30627MHP-XXXGP			PLQP0128KB-A	
M30626MJP-XXXFP (D)	512 Kbytes	31 Kbytes	PRQP0100JB-A	Flash memory version ⁽²⁾
M30626MJP-XXXGP (D)			PLQP0100KB-A	
M30627MJP-XXXGP (D)			PLQP0128KB-A	
M30622F8PFP	64K+4 Kbytes	4 Kbytes	PRQP0100JB-A	
M30622F8PGP			PLQP0100KB-A	
M30623F8PGP			PRQP0080JA-A	
M30620FCPFP	128K+4 Kbytes	10 Kbytes	PRQP0100JB-A	
M30620FCPGP			PLQP0100KB-A	
M30621FCPGP			PRQP0080JA-A	
M3062LFGPFP ⁽³⁾ (D)	256K+4 Kbytes	20 Kbytes	PRQP0100JB-A	
M3062LFGPGP ⁽³⁾ (D)			PLQP0100KB-A	
M30625FGPGP			PLQP0128KB-A	
M30626FHPFP	384K+4 Kbytes	31 Kbytes	PRQP0100JB-A	ROM-less version
M30626FHPPGP			PLQP0100KB-A	
M30627FHPPGP			PLQP0128KB-A	
M30626FJPFP	512K+4 Kbytes	31 Kbytes	PRQP0100JB-A	
M30626FJPPGP			PLQP0100KB-A	
M30627FJPPGP			PLQP0128KB-A	
M30622SPFP	–	4 Kbytes	PRQP0100JB-A	
M30622SPGP			PLQP0100KB-A	
M30620SPFP		10 Kbytes	PRQP0100JB-A	
M30620SPGP			PLQP0100KB-A	
M30624SPFP (D)	–	20 Kbytes	PRQP0100JB-A	
M30624SPGP (D)			PLQP0100KB-A	
M30626SPFP (D)		31 Kbytes	PRQP0100JB-A	
M30626SPGP (D)			PLQP0100KB-A	

(D): Under development

NOTES:

- The old package type numbers of each package type are as follows.
 PLQP0128KB-A : 128P6Q-A,
 PRQP0100JB-A : 100P6S-A,
 PLQP0100KB-A : 100P6Q-A,
 PRQP0080JA-A : 80P6S-A
- In the flash memory version, there is 4K bytes area (block A).
- Please use M3062LFGPFP and M3062LFGPGP for your new system instead of M30624FGPFP and M30624FGPGP. The M16C/62P Group (M16C/62P, M16C/62PT) hardware manual is still good for M30624FGPFP and M30624FGPGP.

M30624FGPFP	256K+4 Kbytes	20 Kbytes	PRQP0100JB-A	Flash memory version
M30624FGPGP			PLQP0100KB-A	

Table 1.7 Product List (4) (V version (M16C/62PT))

As of Dec. 2005

Type No.	ROM Capacity	RAM Capacity	Package Type ⁽¹⁾	Remarks	
M3062CM6V-XXXFP (P)	48 Kbytes	4 Kbytes	PRQP0100JB-A	Mask ROM version	V Version (High reliability 125°C version)
M3062CM6V-XXXGP (P)			PLQP0100KB-A		
M3062EM6V-XXXGP (P)			PRQP0080JA-A		
M3062CM8V-XXXFP (P)	64 Kbytes	4 Kbytes	PRQP0100JB-A		
M3062CM8V-XXXGP (P)			PLQP0100KB-A		
M3062EM8V-XXXGP (P)			PRQP0080JA-A		
M3062CMAV-XXXFP (P)	96 Kbytes	5 Kbytes	PRQP0100JB-A		
M3062CMAV-XXXGP (P)			PLQP0100KB-A		
M3062EMAV-XXXGP (P)			PRQP0080JA-A		
M3062AMCV-XXXFP (D)	128 Kbytes	10 Kbytes	PRQP0100JB-A		
M3062AMCV-XXXGP (D)			PLQP0100KB-A		
M3062BMCV-XXXGP (P)			PRQP0080JA-A		
M3062AFCVFP (D)	128K+4 Kbytes	10 Kbytes	PRQP0100JB-A	Flash memory version ⁽²⁾	
M3062AFCVGP (D)			PLQP0100KB-A		
M3062BFCVGP (P)			PRQP0080JA-A		
M3062JFHVFP (P)	384K+4 Kbytes	31 Kbytes	PRQP0100JB-A		
M3062JFHVGP (P)			PLQP0100KB-A		

(D): Under development

(P): Under planning

NOTES:

- The old package type numbers of each package type are as follows.
 PLQP0128KB-A : 128P6Q-A,
 PRQP0100JB-A : 100P6S-A,
 PLQP0100KB-A : 100P6Q-A,
 PRQP0080JA-A : 80P6S-A
- In the flash memory version, there is 4K bytes area (block A).

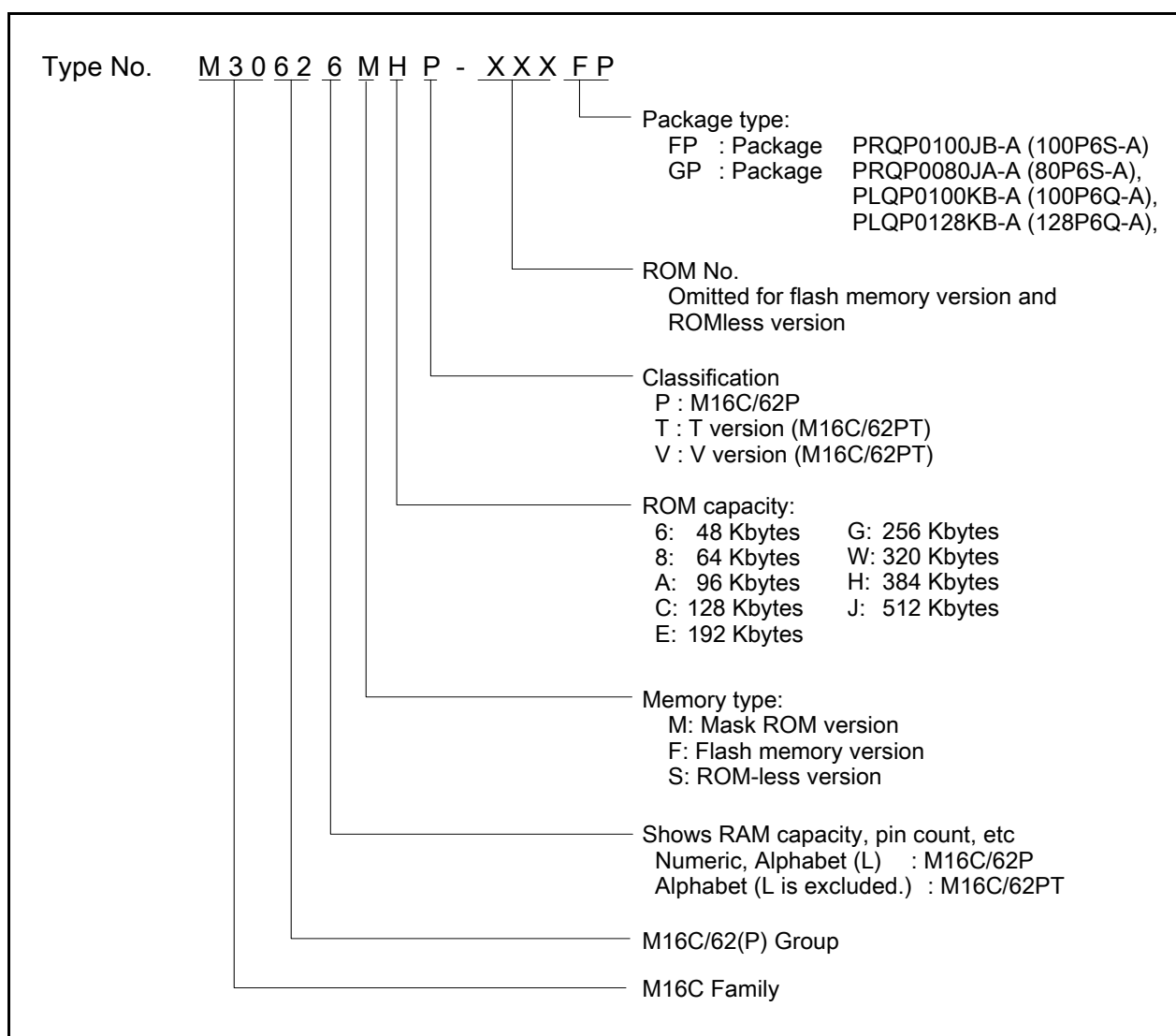


Figure 1.3 Type No., Memory Size, and Package

Table 1.20 Pin Description (80-pin Version) (1) (1)

Signal Name	Pin Name	I/O Type	Power Supply	Description
Power supply input	VCC1, VSS	I	–	Apply 2.7 to 5.5 V to the VCC1 pin and 0 V to the VSS pin. (1, 2)
Analog power supply input	AVCC AVSS	I	VCC1	Applies the power supply for the A/D converter. Connect the AVCC pin to VCC1. Connect the AVSS pin to VSS.
Reset input	RESET	I	VCC1	The microcomputer is in a reset state when applying “L” to the this pin.
CNVSS	CNVSS (BYTE)	I	VCC1	Switches processor mode. Connect this pin to VSS to when after a reset to start up in single-chip mode. Connect this pin to VCC1 to start up in microprocessor mode. As for the BYTE pin of the 80-pin versions, pull-up processing is performed within the microcomputer.
Main clock input	XIN	I	VCC1	I/O pins for the main clock generation circuit. Connect a ceramic resonator or crystal oscillator between XIN and XOUT (3). To use the external clock, input the clock from XIN and leave XOUT open.
Main clock output	XOUT	O	VCC1	
Sub clock input	XCIN	I	VCC1	I/O pins for a sub clock oscillation circuit. Connect a crystal oscillator between XCIN and XCOUT (3). To use the external clock, input the clock from XCIN and leave XCOUT open.
Sub clock output	XCOUT	O	VCC1	
Clock output	CLKOUT	O	VCC2	The clock of the same cycle as fC, f8, or f32 is outputted.
INT interrupt input	INT0 to INT2	I	VCC1	Input pins for the INT interrupt.
NMI interrupt input	NMI	I	VCC1	Input pin for the NMI interrupt.
Key input interrupt input	KI0 to KI3	I	VCC1	Input pins for the key input interrupt.
Timer A	TA0OUT, TA3OUT, TA4OUT	I/O	VCC1	These are Timer A0, Timer A3 and Timer A4 I/O pins. (however, output of TA0OUT for the N-channel open drain output.)
	TA0IN, TA3IN, TA4IN	I	VCC1	These are Timer A0, Timer A3 and Timer A4 input pins.
	ZP	I	VCC1	Input pin for the Z-phase.
Timer B	TB0IN, TB2IN to TB5IN	I	VCC1	These are Timer B0, Timer B2 to Timer B5 input pins.
Serial interface	CTS0 to CTS1	I	VCC1	These are send control input pins.
	RTS0 to RTS1	O	VCC1	These are receive control output pins.
	CLK0, CLK1, CLK3, CLK4	I/O	VCC1	These are transfer clock I/O pins.
	RXD0 to RXD2	I	VCC1	These are serial data input pins.
	SIN4	I	VCC1	This is serial data input pin.
	TXD0 to TXD2	O	VCC1	These are serial data output pins. (however, output of TXD2 for the N-channel open drain output.)
	SOUT3, SOUT4	O	VCC1	These are serial data output pins.
	CLKS1	O	VCC1	This is output pin for transfer clock output from multiple pins function.
I ² C mode	SDA0 to SDA2	I/O	VCC1	These are serial data I/O pins. (however, output of SDA2 for the N-channel open drain output.)
	SCL0 to SCL2	I/O	VCC1	These are transfer clock I/O pins. (however, output of SCL2 for the N-channel open drain output.)

I : Input O : Output I/O : Input and output

NOTES:

1. In this manual, hereafter, VCC refers to VCC1 unless otherwise noted.
2. In M16C/62PT, apply 4.0 to 5.5 V to the VCC1 pin.
3. Ask the oscillator maker the oscillation characteristic.

2.2 Address Registers (A0 and A1)

The register A0 consists of 16 bits, and is used for address register indirect addressing and address register relative addressing. They also are used for transfers and logic/logic operations. A1 is the same as A0.

In some instructions, registers A1 and A0 can be combined for use as a 32-bit address register (A1A0).

2.3 Frame Base Register (FB)

FB is configured with 16 bits, and is used for FB relative addressing.

2.4 Interrupt Table Register (INTB)

INTB is configured with 20 bits, indicating the start address of an interrupt vector table.

2.5 Program Counter (PC)

PC is configured with 20 bits, indicating the address of an instruction to be executed.

2.6 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

Stack pointer (SP) comes in two types: USP and ISP, each configured with 16 bits.

Your desired type of stack pointer (USP or ISP) can be selected by the U flag of FLG.

2.7 Static Base Register (SB)

SB is configured with 16 bits, and is used for SB relative addressing.

2.8 Flag Register (FLG)

FLG consists of 11 bits, indicating the CPU status.

2.8.1 Carry Flag (C Flag)

This flag retains a carry, borrow, or shift-out bit that has occurred in the arithmetic/logic unit.

2.8.2 Debug Flag (D Flag)

The D flag is used exclusively for debugging purpose. During normal use, it must be set to "0".

2.8.3 Zero Flag (Z Flag)

This flag is set to "1" when an arithmetic operation resulted in 0; otherwise, it is "0".

2.8.4 Sign Flag (S Flag)

This flag is set to "1" when an arithmetic operation resulted in a negative value; otherwise, it is "0".

2.8.5 Register Bank Select Flag (B Flag)

Register bank 0 is selected when this flag is "0"; register bank 1 is selected when this flag is "1".

2.8.6 Overflow Flag (O Flag)

This flag is set to "1" when the operation resulted in an overflow; otherwise, it is "0".

2.8.7 Interrupt Enable Flag (I Flag)

This flag enables a maskable interrupt.

Maskable interrupts are disabled when the I flag is "0", and are enabled when the I flag is "1". The I flag is cleared to "0" when the interrupt request is accepted.

Table 4.3 SFR Information (3) ⁽¹⁾

Address	Register	Symbol	After Reset
0080h			
0081h			
0082h			
0083h			
0084h			
0085h			
0086h			
0087h to 01AFh			
01B0h			
01B1h			
01B2h			
01B3h			
01B4h	Flash Identification Register ⁽²⁾	FIDR	XXXXXX00b
01B5h	Flash Memory Control Register 1 ⁽²⁾	FMR1	0X00XX0Xb
01B6h			
01B7h	Flash Memory Control Register 0 ⁽²⁾	FMR0	00000001b
01B8h	Address Match Interrupt Register 2	RMAD2	00h
01B9h			00h
01BAh			XXh
01BBh			XXXXXX00b
01BCh	Address Match Interrupt Register 3	RMAD3	00h
01BDh			00h
01BEh			XXh
01C0h to 024Fh			
0250h			
0251h			
0252h			
0253h			
0254h			
0255h			
0256h			
0257h			
0258h			
0259h			
025Ah			
025Bh			
025Ch			
025Dh			
025Eh	Peripheral Clock Select Register	PCLKR	00000011b
025Fh			
0260h to 032Fh			
0330h			
0331h			
0332h			
0333h			
0334h			
0335h			
0336h			
0337h			
0338h			
0339h			
033Ah			
033Bh			
033Ch			
033Dh			
033Eh			
033Fh			

NOTES:

1. The blank areas are reserved and cannot be accessed by users.
2. This register is included in the flash memory version.

X : Nothing is mapped to this bit

Table 5.4 A/D Conversion Characteristics (1)

Symbol	Parameter		Measuring Condition		Standard			Unit
					Min.	Typ.	Max.	
–	Resolution		VREF=VCC1				10	Bits
INL	Integral Non-Linearity Error	10bit	VREF=VCC1=5V	AN0 to AN7 input, AN0_0 to AN0_7 input, AN2_0 to AN2_7 input, ANEX0, ANEX1 input			±3	LSB
				External operation amp connection mode			±7	LSB
			VREF=VCC1=3.3V	AN0 to AN7 input, AN0_0 to AN0_7 input, AN2_0 to AN2_7 input, ANEX0, ANEX1 input			±5	LSB
				External operation amp connection mode			±7	LSB
		8bit	VREF=VCC1=5V, 3.3V				±2	LSB
		–	Absolute Accuracy	10bit	VREF=VCC1=5V	AN0 to AN7 input, AN0_0 to AN0_7 input, AN2_0 to AN2_7 input, ANEX0, ANEX1 input		
External operation amp connection mode						±7	LSB	
VREF=VCC1=3.3V	AN0 to AN7 input, AN0_0 to AN0_7 input, AN2_0 to AN2_7 input, ANEX0, ANEX1 input					±5	LSB	
	External operation amp connection mode					±7	LSB	
8bit	VREF=VCC1=5V, 3.3V					±2	LSB	
–	Tolerance Level Impedance						3	
DNL	Differential Non-Linearity Error						±1	LSB
–	Offset Error						±3	LSB
–	Gain Error						±3	LSB
RLADDER	Ladder Resistance		VREF=VCC1		10		40	kΩ
tCONV	10-bit Conversion Time, Sample & Hold Available		VREF=VCC1=5V, φAD=12MHz		2.75			μs
tCONV	8-bit Conversion Time, Sample & Hold Available		VREF=VCC1=5V, φAD=12MHz		2.33			μs
tsAMP	Sampling Time				0.25			μs
VREF	Reference Voltage				2.0		VCC1	V
VIA	Analog Input Voltage				0		VREF	V

NOTES:

1. Referenced to VCC1=AVCC=VREF=3.3 to 5.5V, VSS=AVSS=0V at T_{opr} = –20 to 85°C / –40 to 85°C unless otherwise specified.
2. If VCC1 > VCC2, do not use AN0_0 to AN0_7 and AN2_0 to AN2_7 as analog input pins.
3. φAD frequency must be 12 MHz or less. And divide the fAD if VCC1 is less than 4.0V, and φAD frequency into 10 MHz or less.
4. When sample & hold is disabled, φAD frequency must be 250 kHz or more, in addition to the limitation in Note 3.
When sample & hold is enabled, φAD frequency must be 1MHz or more, in addition to the limitation in Note 3.

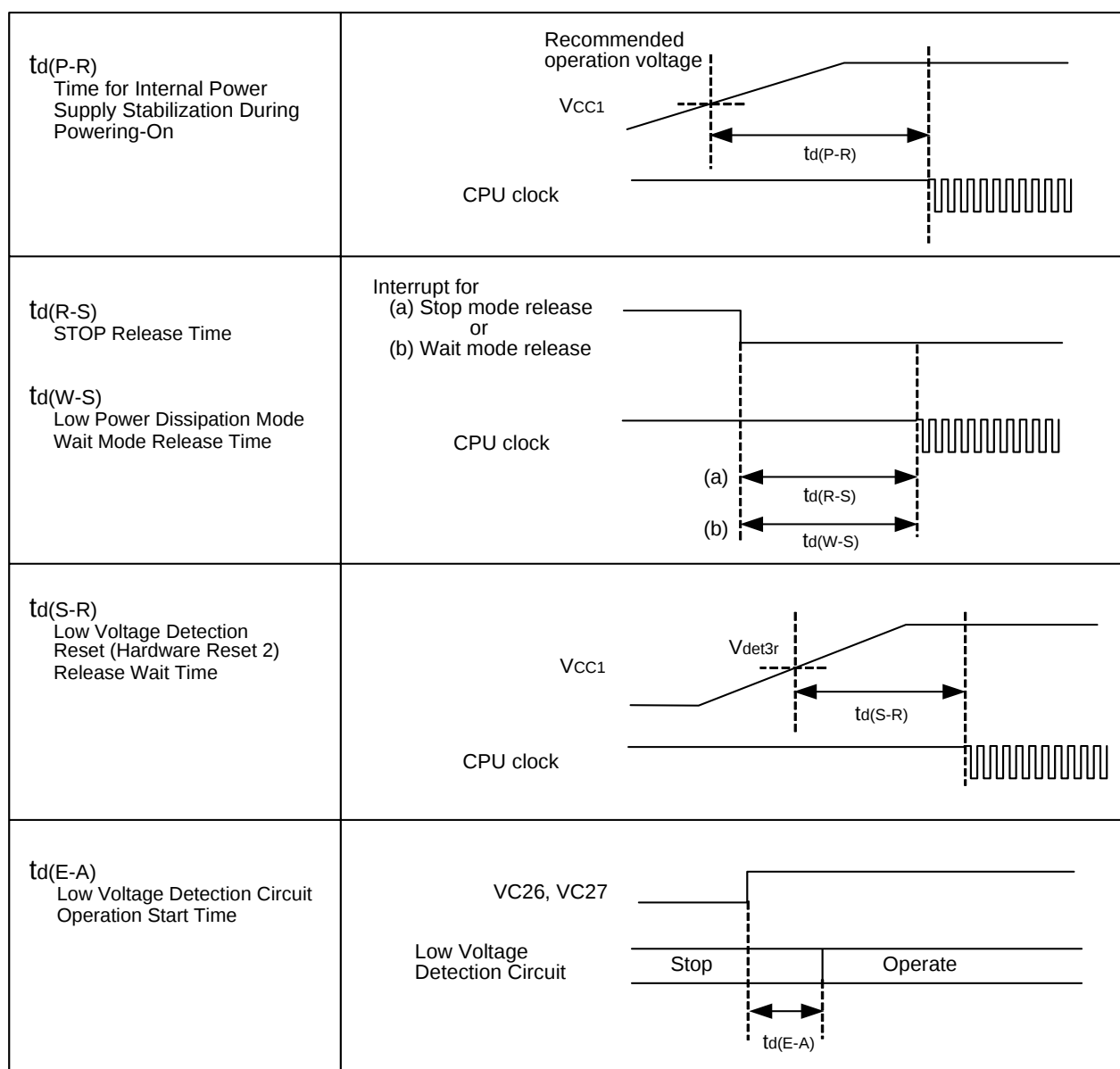


Figure 5.1 Power Supply Circuit Timing Diagram

$$V_{CC1}=V_{CC2}=5V$$

Timing Requirements

($V_{CC1} = V_{CC2} = 5V$, $V_{SS} = 0V$, at $T_{opr} = -20$ to $85^{\circ}C$ / -40 to $85^{\circ}C$ unless otherwise specified)

Table 5.13 External Clock Input (XIN input) ⁽¹⁾

Symbol	Parameter	Standard		Unit
		Min.	Max.	
t_c	External Clock Input Cycle Time	62.5		ns
$t_{w(H)}$	External Clock Input HIGH Pulse Width	25		ns
$t_{w(L)}$	External Clock Input LOW Pulse Width	25		ns
t_r	External Clock Rise Time		15	ns
t_f	External Clock Fall Time		15	ns

NOTES:

1. The condition is $V_{CC1}=V_{CC2}=3.0$ to $5.0V$.

Table 5.14 Memory Expansion Mode and Microprocessor Mode

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{ac1(RD-DB)}$	Data Input Access Time (for setting with no wait)		(NOTE 1)	ns
$t_{ac2(RD-DB)}$	Data Input Access Time (for setting with wait)		(NOTE 2)	ns
$t_{ac3(RD-DB)}$	Data Input Access Time (when accessing multiplex bus area)		(NOTE 3)	ns
$t_{su(DB-RD)}$	Data Input Setup Time	40		ns
$t_{su(RDY-BCLK)}$	RDY Input Setup Time	30		ns
$t_{su(HOLD-BCLK)}$	HOLD Input Setup Time	40		ns
$t_h(RD-DB)$	Data Input Hold Time	0		ns
$t_h(BCLK-RDY)$	RDY Input Hold Time	0		ns
$t_h(BCLK-HOLD)$	HOLD Input Hold Time	0		ns

NOTES:

1. Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f(BCLK)} - 45 [ns]$$

2. Calculated according to the BCLK frequency as follows:

$$\frac{(n-0.5) \times 10^9}{f(BCLK)} - 45 [ns] \quad n \text{ is "2" for 1-wait setting, "3" for 2-wait setting and "4" for 3-wait setting.}$$

3. Calculated according to the BCLK frequency as follows:

$$\frac{(n-0.5) \times 10^9}{f(BCLK)} - 45 [ns] \quad n \text{ is "2" for 2-wait setting, "3" for 3-wait setting.}$$

$$V_{CC1}=V_{CC2}=5V$$

Switching Characteristics

($V_{CC1} = V_{CC2} = 5V$, $V_{SS} = 0V$, at $T_{opr} = -20$ to $85^{\circ}C$ / -40 to $85^{\circ}C$ unless otherwise specified)

Table 5.28 Memory Expansion and Microprocessor Modes (for 1- to 3-wait setting and external area access)

Symbol	Parameter		Standard		Unit
			Min.	Max.	
$t_d(BCLK-AD)$	Address Output Delay Time	See Figure 5.2		25	ns
$t_h(BCLK-AD)$	Address Output Hold Time (in relation to BCLK)		4		ns
$t_h(RD-AD)$	Address Output Hold Time (in relation to RD)		0		ns
$t_h(WR-AD)$	Address Output Hold Time (in relation to WR)		(NOTE 2)		ns
$t_d(BCLK-CS)$	Chip Select Output Delay Time			25	ns
$t_h(BCLK-CS)$	Chip Select Output Hold Time (in relation to BCLK)		4		ns
$t_d(BCLK-ALE)$	ALE Signal Output Delay Time			15	ns
$t_h(BCLK-ALE)$	ALE Signal Output Hold Time		-4		ns
$t_d(BCLK-RD)$	RD Signal Output Delay Time			25	ns
$t_h(BCLK-RD)$	RD Signal Output Hold Time		0		ns
$t_d(BCLK-WR)$	WR Signal Output Delay Time			25	ns
$t_h(BCLK-WR)$	WR Signal Output Hold Time		0		ns
$t_d(BCLK-DB)$	Data Output Delay Time (in relation to BCLK)			40	ns
$t_h(BCLK-DB)$	Data Output Hold Time (in relation to BCLK) ⁽³⁾		4		ns
$t_d(DB-WR)$	Data Output Delay Time (in relation to WR)		(NOTE 1)		ns
$t_h(WR-DB)$	Data Output Hold Time (in relation to WR) ⁽³⁾		(NOTE 2)		ns
$t_d(BCLK-HLDA)$	HLDA Output Delay Time			40	ns

NOTES:

1. Calculated according to the BCLK frequency as follows:

$$\frac{(n-0.5) \times 10^9}{f(BCLK)} - 40[ns]$$

n is "1" for 1-wait setting, "2" for 2-wait setting and "3" for 3-wait setting.
(BCLK) is 12.5MHz or less.

2. Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f(BCLK)} - 10[ns]$$

3. This standard value shows the timing when the output is off, and does not show hold time of data bus.
Hold time of data bus varies with capacitor volume and pull-up (pull-down) resistance value.

Hold time of data bus is expressed in

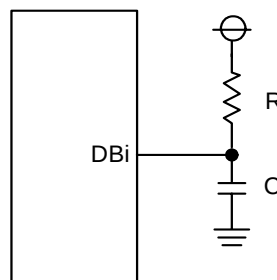
$$t = -CR \times \ln(1 - V_{OL} / V_{CC2})$$

by a circuit of the right figure.

For example, when $V_{OL} = 0.2V_{CC2}$, $C = 30pF$, $R = 1k\Omega$, hold time of output "L" level is

$$t = -30pF \times 1k\Omega \times \ln(1 - 0.2V_{CC2} / V_{CC2})$$

$$= 6.7ns.$$



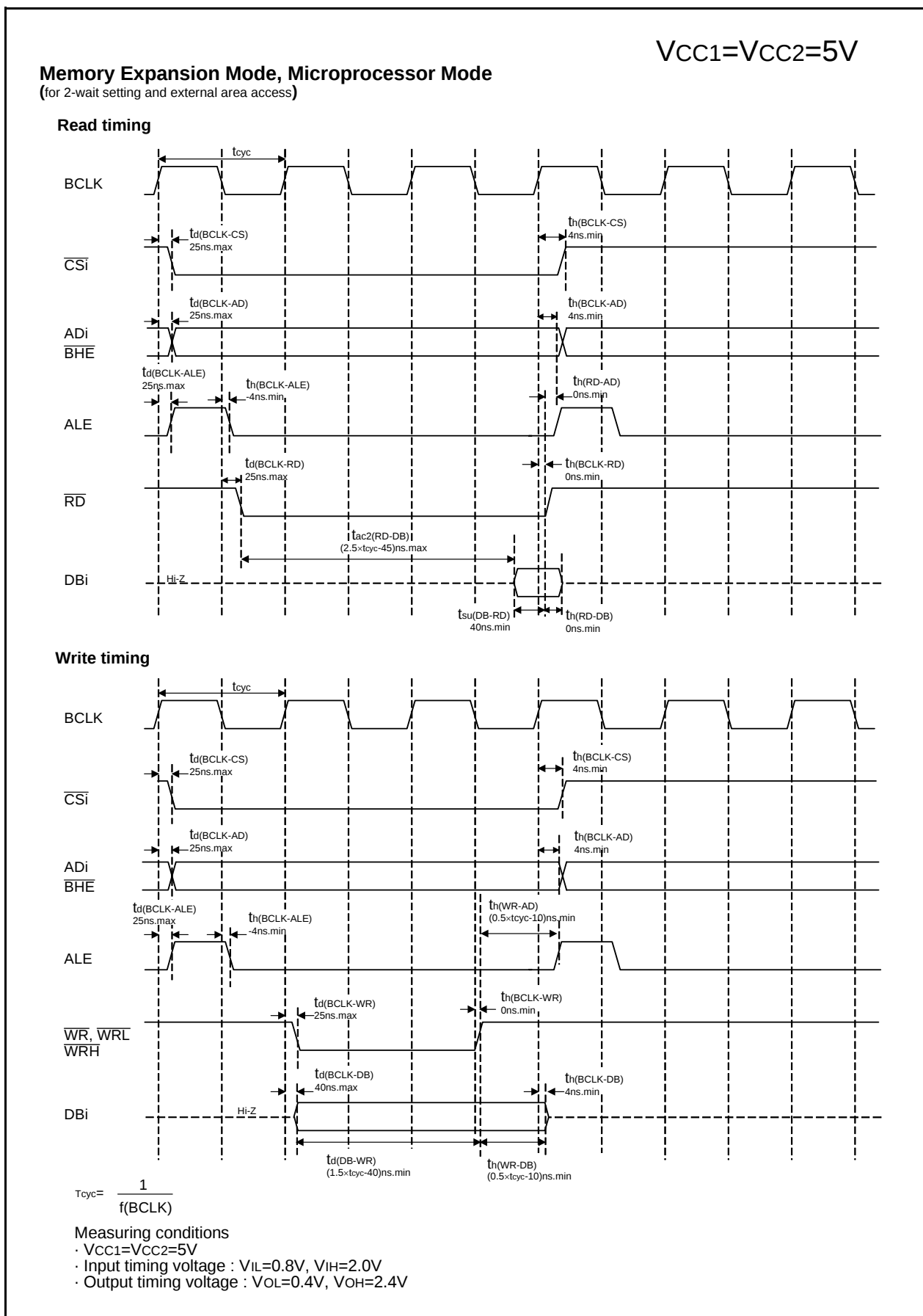


Figure 5.8 Timing Diagram (6)

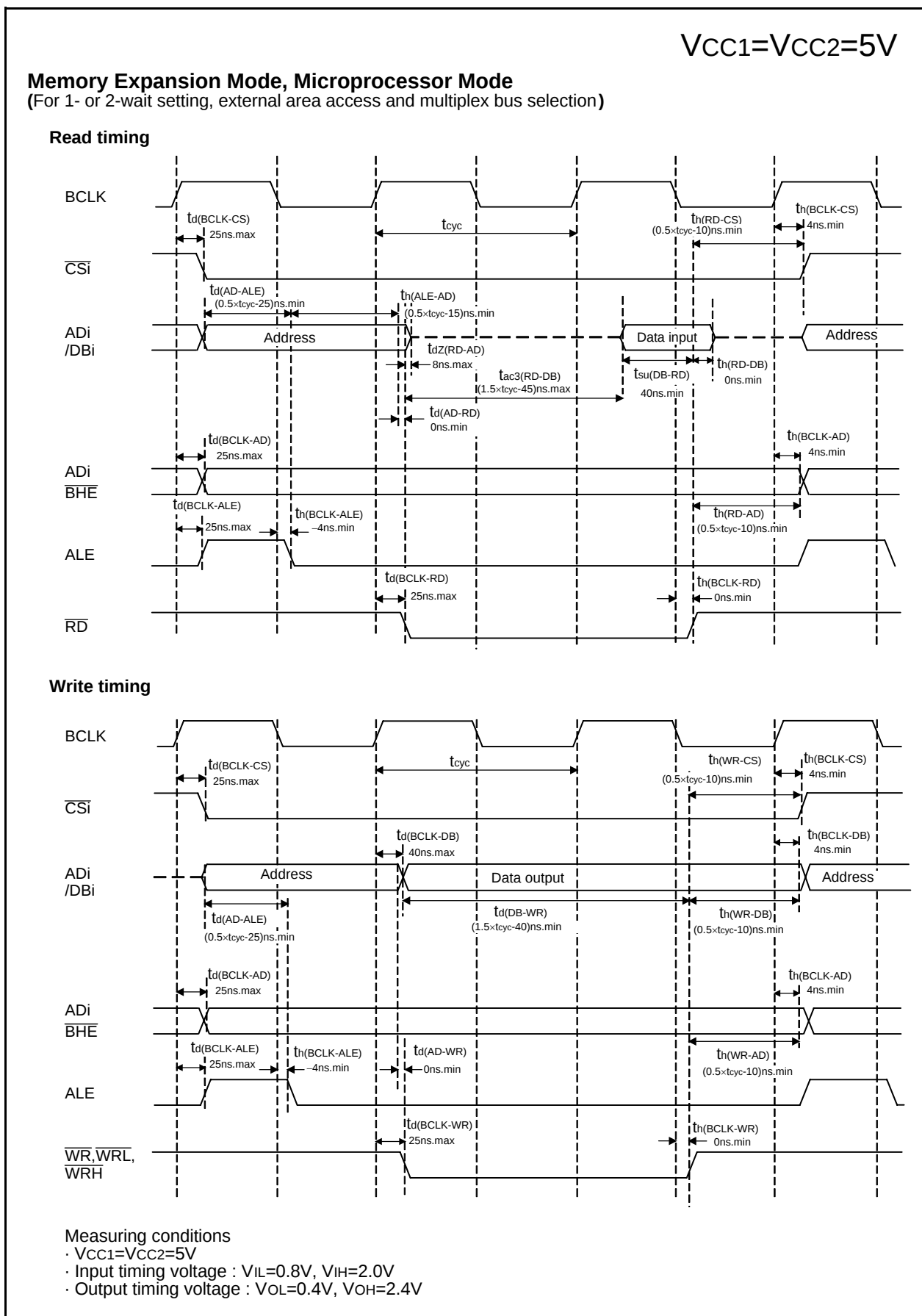


Figure 5.10 Timing Diagram (8)

Table 5.31 Electrical Characteristics (2) ⁽¹⁾

Symbol	Parameter		Measuring Condition		Standard			Unit
					Min.	Typ.	Max.	
I _{cc}	Power Supply Current (V _{cc1} =V _{cc2} =2.7V to 3.6V)	In single-chip mode, the output pins are open and other pins are V _{ss}	Mask ROM	f(BCLK)=10MHz No division		8	11	mA
				No division, On-chip oscillation		1		mA
			Flash Memory	f(BCLK)=10MHz, No division		8	13	mA
				No division, On-chip oscillation		1.8		mA
			Flash Memory Program	f(BCLK)=10MHz, VCC1=3.0V		12		mA
			Flash Memory Erase	f(BCLK)=10MHz, VCC1=3.0V		22		mA
			Mask ROM	f(XCIN)=32kHz Low power dissipation mode, ROM ⁽³⁾		25		μA
			Flash Memory	f(BCLK)=32kHz Low power dissipation mode, RAM ⁽³⁾		25		μA
				f(BCLK)=32kHz Low power dissipation mode, Flash Memory ⁽³⁾		420		μA
				On-chip oscillation, Wait mode		45		μA
				Mask ROM Flash Memory	f(BCLK)=32kHz Wait mode ⁽²⁾ , Oscillation capability High		6.0	
			f(BCLK)=32kHz Wait mode ⁽²⁾ , Oscillation capability Low			1.8		μA
			Stop mode T _{opr} =25°C			0.7	3.0	μA
I _{det4}	Low Voltage Detection Dissipation Current ⁽⁴⁾					0.6	4	μA
I _{det3}	Reset Area Detection Dissipation Current ⁽⁴⁾					0.4	2	μA

NOTES:

1. Referenced to V_{CC1}=V_{CC2}=2.7 to 3.3V, V_{SS} = 0V at T_{opr} = -20 to 85°C / -40 to 85°C, f(BCLK)=10MHz unless otherwise specified.
2. With one timer operated using fC32.
3. This indicates the memory in which the program to be executed exists.
4. I_{det} is dissipation current when the following bit is set to "1" (detection circuit enabled).
I_{det4}: VC27 bit in the VCR2 register
I_{det3}: VC26 bit in the VCR2 register

5.2 Electrical Characteristics (M16C/62PT)

Table 5.49 Absolute Maximum Ratings

Symbol	Parameter		Condition	Rated Value	Unit
V _{CC1} , V _{CC2}	Supply Voltage		V _{CC1} =V _{CC2} =AV _{CC}	−0.3 to 6.5	V
AV _{CC}	Analog Supply Voltage		V _{CC1} =V _{CC2} =AV _{CC}	−0.3 to 6.5	V
V _I	Input Voltage	RESET, CNVSS, BYTE, P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P14_0, P14_1, VREF, XIN		−0.3 to V _{CC1} +0.3 ⁽¹⁾	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P12_0 to P12_7, P13_0 to P13_7		−0.3 to V _{CC2} +0.3 ⁽¹⁾	V
		P7_0, P7_1		−0.3 to 6.5	V
V _O	Output Voltage	P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P14_0, P14_1, XOUT		−0.3 to V _{CC1} +0.3 ⁽¹⁾	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P12_0 to P12_7, P13_0 to P13_7		−0.3 to V _{CC2} +0.3 ⁽¹⁾	V
		P7_0, P7_1		−0.3 to 6.5	V
P _d	Power Dissipation		−40°C<T _{opr} ≤85°C	300	mW
			85°C<T _{opr} ≤125°C	200	
T _{opr}	Operating Ambient Temperature	When the Microcomputer is Operating		−40 to 85 / −40 to 125 ⁽²⁾	°C
		Flash Program Erase		0 to 60	
T _{stg}	Storage Temperature			−65 to 150	°C

NOTES:

1. There is no external connections for port P1_0 to P1_7, P4_4 to P4_7, P7_2 to P7_5 and P9_1 in 80-pin version.
2. T version = −40 to 85 °C, V version= −40 to 125 °C.

Table 5.51 A/D Conversion Characteristics (1)

Symbol	Parameter		Measuring Condition	Standard			Unit
				Min.	Typ.	Max.	
–	Resolution		$V_{REF}=V_{CC1}$			10	Bits
INL	Integral Non-Linearity Error	10bit	$V_{REF}=V_{CC1}=5V$ AN0 to AN7 input, AN0_0 to AN0_7 input, AN2_0 to AN2_7 input, ANEX0, ANEX1 input			± 3	LSB
			External operation amp connection mode			± 7	LSB
		8bit	$V_{REF}=V_{CC1}=5V$			± 2	LSB
–	Absolute Accuracy	10bit	$V_{REF}=V_{CC1}=5V$ AN0 to AN7 input, AN0_0 to AN0_7 input, AN2_0 to AN2_7 input, ANEX0, ANEX1 input			± 3	LSB
			External operation amp connection mode			± 7	LSB
		8bit	$V_{REF}=V_{CC1}=5V$			± 2	LSB
–	Tolerance Level Impedance				3		$k\Omega$
DNL	Differential Non-Linearity Error					± 1	LSB
–	Offset Error					± 3	LSB
–	Gain Error					± 3	LSB
RLADDER	Ladder Resistance		$V_{REF}=V_{CC1}$	10		40	$k\Omega$
tCONV	10-bit Conversion Time, Sample & Hold Function Available		$V_{REF}=V_{CC1}=5V$, $\phi AD=12MHz$	2.75			μs
tCONV	8-bit Conversion Time, Sample & Hold Function Available		$V_{REF}=V_{CC1}=5V$, $\phi AD=12MHz$	2.33			μs
tsAMP	Sampling Time			0.25			μs
VREF	Reference Voltage			2.0		V_{CC1}	V
Via	Analog Input Voltage			0		V_{REF}	V

NOTES:

1. Referenced to $V_{CC1}=AV_{CC}=V_{REF}=4.0$ to $5.5V$, $V_{SS}=AV_{SS}=0V$ at $T_{opr} = -40$ to $85^{\circ}C$ / -40 to $125^{\circ}C$ unless otherwise specified.
T version = -40 to $85^{\circ}C$, V version = -40 to $125^{\circ}C$
2. ϕAD frequency must be 12 MHz or less.
3. When sample & hold is disabled, ϕAD frequency must be 250 kHz or more, in addition to the limitation in Note 2.
When sample & hold is enabled, ϕAD frequency must be 1MHz or more, in addition to the limitation in Note 2.

Table 5.52 D/A Conversion Characteristics (1)

Symbol	Parameter	Measuring Condition	Standard			Unit
			Min.	Typ.	Max.	
–	Resolution				8	Bits
–	Absolute Accuracy				1.0	%
tsu	Setup Time				3	μs
Ro	Output Resistance		4	10	20	$k\Omega$
IvREF	Reference Power Supply Input Current	(NOTE 2)			1.5	mA

NOTES:

1. Referenced to $V_{CC1}=V_{REF}=4.0$ to $5.5V$, $V_{SS}=AV_{SS}=0V$ at $T_{opr} = -40$ to $85^{\circ}C$ / -40 to $125^{\circ}C$ unless otherwise specified. T version = -40 to $85^{\circ}C$, V version = -40 to $125^{\circ}C$
2. This applies when using one D/A converter, with the D/A register for the unused D/A converter set to "00h". The resistor ladder of the A/D converter is not included. Also, when D/A register contents are not "00h", the IvREF will flow even if Vref is disconnected by the A/D control register.

Table 5.53 Flash Memory Version Electrical Characteristics ⁽¹⁾ for 100 cycle products (B, U)

Symbol	Parameter		Standard			Unit
			Min.	Typ.	Max.	
–	Program and Erase Endurance ⁽³⁾		100			cycle
–	Word Program Time (V _{CC1} =5.0V)			25	200	μs
–	Lock Bit Program Time			25	200	μs
–	Block Erase Time (V _{CC1} =5.0V)	4-Kbyte block	4	0.3	4	s
–		8-Kbyte block		0.3	4	s
–		32-Kbyte block		0.5	4	s
–		64-Kbyte block		0.8	4	s
–	Erase All Unlocked Blocks Time ⁽²⁾				4×n	s
tps	Flash Memory Circuit Stabilization Wait Time				15	μs
–	Data Hold Time ⁽⁵⁾		20			year

Table 5.54 Flash Memory Version Electrical Characteristics ⁽⁶⁾ for 10,000 cycle products (B7, U7) (Block A and Block 1 ⁽⁷⁾)

Symbol	Parameter		Standard			Unit
			Min.	Typ.	Max.	
–	Program and Erase Endurance ^(3, 8, 9)		10,000 ⁽⁴⁾			cycle
–	Word Program Time (V _{CC1} =5.0V)			25		μs
–	Lock Bit Program Time			25		μs
–	Block Erase Time (V _{CC1} =5.0V)	4-Kbyte block	4	0.3		s
tps	Flash Memory Circuit Stabilization Wait Time				15	μs
–	Data Hold Time ⁽⁵⁾		20			year

NOTES:

1. Referenced to V_{CC1}=4.5 to 5.5V at T_{opr} = 0 to 60 °C unless otherwise specified.
2. n denotes the number of block erases.
3. Program and Erase Endurance refers to the number of times a block erase can be performed.
If the program and erase endurance is n (n=100, 1,000, or 10,000), each block can be erased n times.
For example, if a 4 Kbytes block A is erased after writing 1 word data 2,048 times, each to a different address, this counts as one program and erase endurance. Data cannot be written to the same address more than once without erasing the block.
(Rewrite prohibited)
4. Maximum number of E/W cycles for which operation is guaranteed.
5. Ta (ambient temperature)=55 °C. As to the data hold time except Ta=55 °C, please contact Renesas Technology Corp. or an authorized Renesas Technology Corp. product distributor.
6. Referenced to V_{CC1} = 4.5 to 5.5V at T_{opr} = –40 to 85 °C (B7, U7 (T version)) / –40 to 125 °C (B7, U7 (V version)) unless otherwise specified.
7. Table 5.54 applies for block A or block 1 program and erase endurance > 1,000. Otherwise, use Table 5.53.
8. To reduce the number of program and erase endurance when working with systems requiring numerous rewrites, write to unused word addresses within the block instead of rewrite. Erase block only after all possible addresses are used. For example, an 8-word program can be written 256 times maximum before erase becomes necessary.
Maintaining an equal number of erasure between block A and block 1 will also improve efficiency. It is important to track the total number of times erasure is used.
9. Should erase error occur during block erase, attempt to execute clear status register command, then block erase command at least three times until erase error disappears.
10. Set the PM17 bit in the PM1 register to “1” (wait state) when executing more than 100 times rewrites (B7 and U7).
11. Customers desiring E/W failure rate information should contact their Renesas technical support representative.

Table 5.55 Flash Memory Version Program/Erase Voltage and Read Operation Voltage Characteristics (at T_{opr} = 0 to 60 °C (B, U), T_{opr} = –40 to 85 °C (B7, U7 (T version)) / –40 to 125 °C (B7, U7 (V version))

Flash Program, Erase Voltage	Flash Read Operation Voltage
V _{CC1} = 5.0 V ± 0.5 V	V _{CC1} =4.0 to 5.5 V

$$V_{CC1}=V_{CC2}=5V$$

Timing Requirements

($V_{CC1} = V_{CC2} = 5V$, $V_{SS} = 0V$, at $T_{opr} = -40$ to $85^{\circ}C$ (T version) / -40 to $125^{\circ}C$ (V version) unless otherwise specified)

Table 5.59 External Clock Input (XIN input)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
t_c	External Clock Input Cycle Time	62.5		ns
$t_{w(H)}$	External Clock Input HIGH Pulse Width	25		ns
$t_{w(L)}$	External Clock Input LOW Pulse Width	25		ns
t_r	External Clock Rise Time		15	ns
t_f	External Clock Fall Time		15	ns

$$V_{CC1}=V_{CC2}=5V$$

Timing Requirements

($V_{CC1} = V_{CC2} = 5V$, $V_{SS} = 0V$, at $T_{opr} = -40$ to $85^{\circ}C$ (T version) / -40 to $125^{\circ}C$ (V version) unless otherwise specified)

Table 5.66 Timer B Input (Counter Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN Input Cycle Time (counted on one edge)	100		ns
$t_{w(TBH)}$	TBiIN Input HIGH Pulse Width (counted on one edge)	40		ns
$t_{w(TBL)}$	TBiIN Input LOW Pulse Width (counted on one edge)	40		ns
$t_{c(TB)}$	TBiIN Input Cycle Time (counted on both edges)	200		ns
$t_{w(TBH)}$	TBiIN Input HIGH Pulse Width (counted on both edges)	80		ns
$t_{w(TBL)}$	TBiIN Input LOW Pulse Width (counted on both edges)	80		ns

Table 5.67 Timer B Input (Pulse Period Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN Input Cycle Time	400		ns
$t_{w(TBH)}$	TBiIN Input HIGH Pulse Width	200		ns
$t_{w(TBL)}$	TBiIN Input LOW Pulse Width	200		ns

Table 5.68 Timer B Input (Pulse Width Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN Input Cycle Time	400		ns
$t_{w(TBH)}$	TBiIN Input HIGH Pulse Width	200		ns
$t_{w(TBL)}$	TBiIN Input LOW Pulse Width	200		ns

Table 5.69 A/D Trigger Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(AD)}$	$\overline{ADTRG}$ Input Cycle Time	1000		ns
$t_{w(ADL)}$	$\overline{ADTRG}$ input LOW Pulse Width	125		ns

Table 5.70 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi Input Cycle Time	200		ns
$t_{w(CKH)}$	CLKi Input HIGH Pulse Width	100		ns
$t_{w(CKL)}$	CLKi Input LOW Pulse Width	100		ns
$t_{d(C-Q)}$	TXDi Output Delay Time		80	ns
$t_{h(C-Q)}$	TXDi Hold Time	0		ns
$t_{su(D-C)}$	RXDi Input Setup Time	70		ns
$t_{h(C-D)}$	RXDi Input Hold Time	90		ns

Table 5.71 External Interrupt $\overline{INTi}$ Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(INH)}$	$\overline{INTi}$ Input HIGH Pulse Width	250		ns
$t_{w(INL)}$	$\overline{INTi}$ Input LOW Pulse Width	250		ns

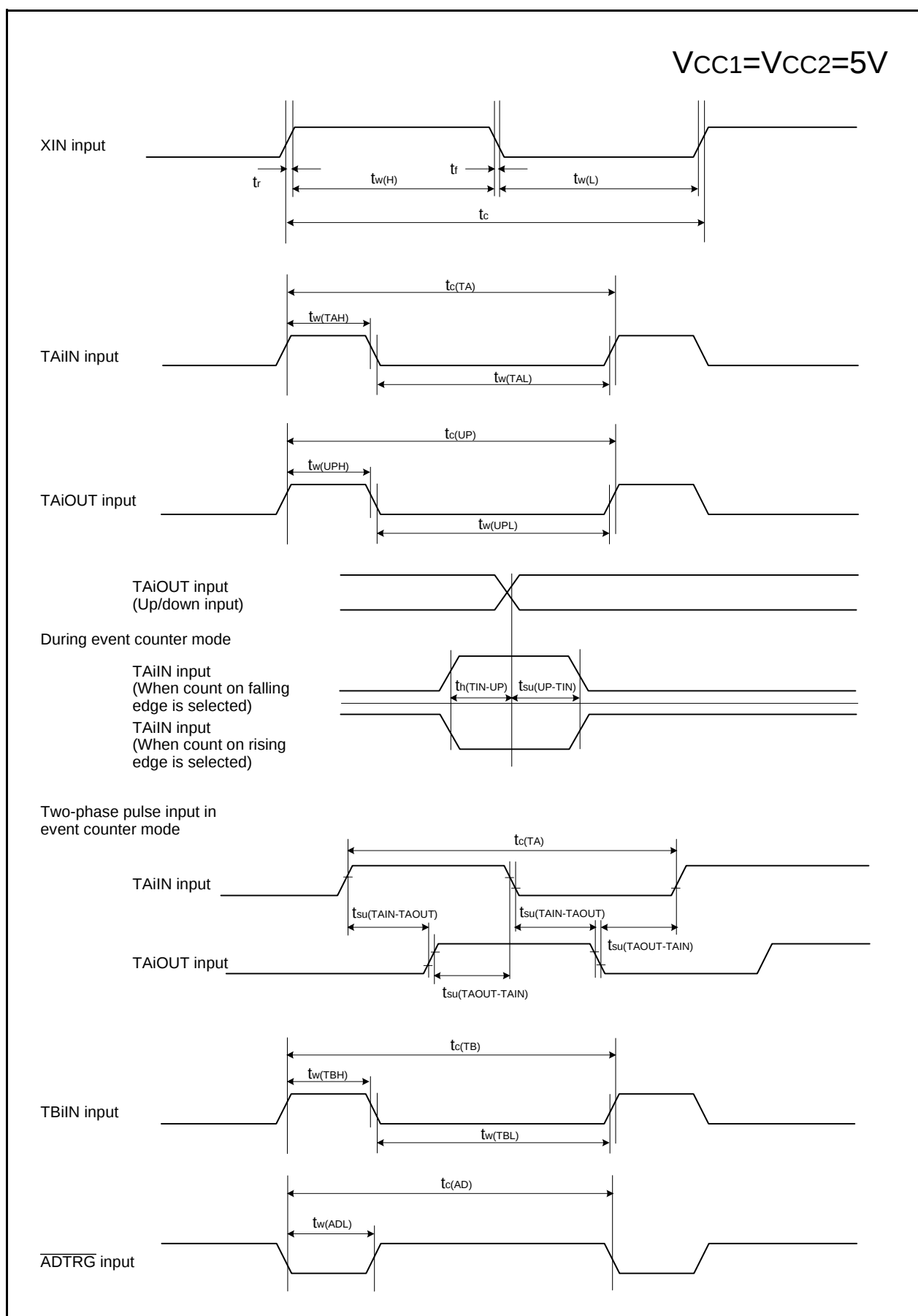


Figure 5.24 Timing Diagram (1)

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP100-14x14-0.50	PLQP0100KB-A	100P6Q-A / FP-100U / FP-100UV	0.6g

NOTE)

- DIMENSIONS *1* AND *2* DO NOT INCLUDE MOLD FLASH.
- DIMENSION *3* DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	13.9	14.0	14.1
E	13.9	14.0	14.1
A ₂	—	1.4	—
H _D	15.8	16.0	16.2
H _E	15.8	16.0	16.2
A	—	—	1.7
A ₁	0.05	0.1	0.15
b _D	0.15	0.20	0.25
b ₁	—	0.18	—
c	0.09	0.145	0.20
c ₁	—	0.125	—
θ	0°	—	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
Z _D	—	1.0	—
Z _E	—	1.0	—
L	0.35	0.5	0.65
L ₁	—	1.0	—

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-QFP80-14x14-0.65	PROQ0080JA-A	80P6S-A	1.1g

NOTE)

- DIMENSIONS *1* AND *2* DO NOT INCLUDE MOLD FLASH.
- DIMENSION *3* DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	13.8	14.0	14.2
E	13.8	14.0	14.2
A ₂	—	2.8	—
H _D	16.5	16.8	17.1
H _E	16.5	16.8	17.1
A	—	—	3.05
A ₁	0	0.1	0.2
b _D	0.25	0.3	0.4
c	0.13	0.15	0.2
θ	0°	—	10°
e	—	0.5	0.65
y	—	—	0.10
Z _D	—	0.825	—
Z _E	—	0.825	—
L	0.4	0.6	0.8