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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	M16C/60
Core Size	16-Bit
Speed	24MHz
Connectivity	I ² C, IEBus, UART/USART
Peripherals	DMA, WDT
Number of I/O	85
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 26x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-BQFP
Supplier Device Package	100-QFP (14x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/m30622f8pfp-u9c

1. Overview

The M16C/62P Group (M16C/62P, M16C/62PT) of single-chip microcomputers are built using the high performance silicon gate CMOS process using a M16C/60 Series CPU core and are packaged in a 80-pin, 100-pin and 128-pin plastic molded QFP. These single-chip microcomputers operate using sophisticated instructions featuring a high level of instruction efficiency. With 1M bytes of address space, they are capable of executing instructions at high speed. In addition, this microcomputer contains a multiplier and DMAC which combined with fast instruction processing capability, makes it suitable for control of various OA, communication, and industrial equipment which requires high-speed arithmetic/logic operations.

1.1 Applications

Audio, cameras, television, home appliance, office/communications/portable/industrial equipment, automobile, etc.

Specifications written in this manual are believed to be accurate, but are not guaranteed to be entirely free of error. Specifications in this manual may be changed for functional or performance improvements. Please make sure your manual is the latest edition.

Table 1.5 Product List (2) (M16C/62P)

As of Dec. 2005

Type No.	ROM Capacity	RAM Capacity	Package Type ⁽¹⁾	Remarks
M30622MHP-XXXFP	384 Kbytes	16 Kbytes	PRQP0100JB-A	Mask ROM version
M30622MHP-XXXGP			PLQP0100KB-A	
M30623MHP-XXXGP			PLQP0128KB-A	
M30624MHP-XXXFP		24 Kbytes	PRQP0100JB-A	
M30624MHP-XXXGP			PLQP0100KB-A	
M30625MHP-XXXGP			PLQP0128KB-A	
M30626MHP-XXXFP		31 Kbytes	PRQP0100JB-A	
M30626MHP-XXXGP			PLQP0100KB-A	
M30627MHP-XXXGP			PLQP0128KB-A	
M30626MJP-XXXFP (D)	512 Kbytes	31 Kbytes	PRQP0100JB-A	Flash memory version ⁽²⁾
M30626MJP-XXXGP (D)			PLQP0100KB-A	
M30627MJP-XXXGP (D)			PLQP0128KB-A	
M30622F8PFP	64K+4 Kbytes	4 Kbytes	PRQP0100JB-A	
M30622F8PGP			PLQP0100KB-A	
M30623F8PGP			PRQP0080JA-A	
M30620FCPFP	128K+4 Kbytes	10 Kbytes	PRQP0100JB-A	
M30620FCPGP			PLQP0100KB-A	
M30621FCPGP			PRQP0080JA-A	
M3062LFGPFP ⁽³⁾ (D)	256K+4 Kbytes	20 Kbytes	PRQP0100JB-A	
M3062LFGPGP ⁽³⁾ (D)			PLQP0100KB-A	
M30625FGPGP			PLQP0128KB-A	
M30626FHPFP	384K+4 Kbytes	31 Kbytes	PRQP0100JB-A	ROM-less version
M30626FHPGP			PLQP0100KB-A	
M30627FHPGP			PLQP0128KB-A	
M30626FJPFP	512K+4 Kbytes	31 Kbytes	PRQP0100JB-A	
M30626FJPGP			PLQP0100KB-A	
M30627FJPGP			PLQP0128KB-A	
M30622SPFP	–	4 Kbytes	PRQP0100JB-A	
M30622SPGP			PLQP0100KB-A	
M30620SPFP		10 Kbytes	PRQP0100JB-A	
M30620SPGP			PLQP0100KB-A	
M30624SPFP (D)	–	20 Kbytes	PRQP0100JB-A	
M30624SPGP (D)			PLQP0100KB-A	
M30626SPFP (D)		31 Kbytes	PRQP0100JB-A	
M30626SPGP (D)			PLQP0100KB-A	

(D): Under development

NOTES:

1. The old package type numbers of each package type are as follows.

PLQP0128KB-A : 128P6Q-A,

PRQP0100JB-A : 100P6S-A,

PLQP0100KB-A : 100P6Q-A,

PRQP0080JA-A : 80P6S-A

2. In the flash memory version, there is 4K bytes area (block A).

3. Please use M3062LFGPFP and M3062LFGPGP for your new system instead of M30624FGPFP and M30624FGPGP. The M16C/62P Group (M16C/62P, M16C/62PT) hardware manual is still good for M30624FGPFP and M30624FGPGP.

M30624FGPFP	256K+4 Kbytes	20 Kbytes	PRQP0100JB-A	Flash memory version
M30624FGPGP			PLQP0100KB-A	

Table 1.9 Product Code of Flash Memory version for M16C/62PT

		Product Code	Package	Internal ROM (User ROM Area Without Block A, Block 1)		Internal ROM (Block A, Block 1)		Operating Ambient Temperature
				Program and Erase Endurance	Temperature Range	Program and Erase Endurance	Temperature Range	
Flash memory Version	T Version	B	Lead- included	100	0°C to 60°C	100	0°C to 60°C	-40°C to 85°C
	V Version							-40°C to 125°C
	T Version	B7		1,000		10,000	-40°C to 85°C	-40°C to 85°C
	V Version						-40°C to 125°C	-40°C to 125°C
	T Version	U	Lead-free	100		100	0°C to 60°C	-40°C to 85°C
	V Version							-40°C to 125°C
	T Version	U7		1,000		10,000	-40°C to 85°C	-40°C to 85°C
	V Version						-40°C to 125°C	-40°C to 125°C

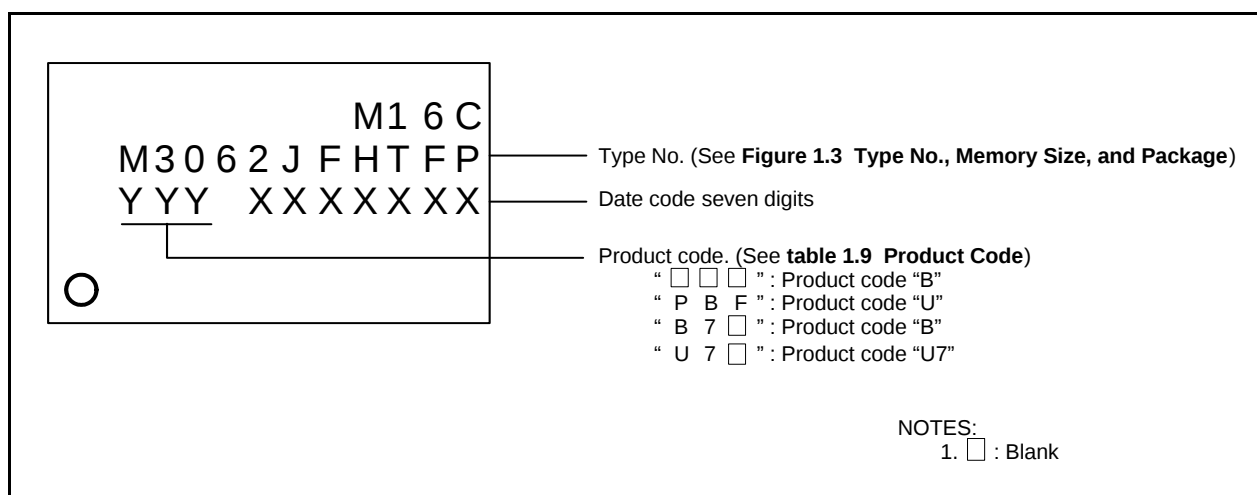
**Figure 1.5 Marking Diagram of Flash Memory version for M16C/62PT (Top View)**

Table 1.11 Pin Characteristics for 128-Pin Package (2)

Pin No.	Control Pin	Port	Interrupt Pin	Timer Pin	UART Pin	Analog Pin	Bus Control Pin
51		P5_6					ALE
52		P5_5					$\overline{\text{HOLD}}$
53		P5_4					$\overline{\text{HLDA}}$
54		P13_3					
55		P13_2					
56		P13_1					
57		P13_0					
58		P5_3					BCLK
59		P5_2					$\overline{\text{RD}}$
60		P5_1					$\overline{\text{WRH/BHE}}$
61		P5_0					$\overline{\text{WRL/WR}}$
62		P12_7					
63		P12_6					
64		P12_5					
65		P4_7					$\overline{\text{CS3}}$
66		P4_6					$\overline{\text{CS2}}$
67		P4_5					$\overline{\text{CS1}}$
68		P4_4					$\overline{\text{CS0}}$
69		P4_3					A19
70		P4_2					A18
71		P4_1					A17
72		P4_0					A16
73		P3_7					A15
74		P3_6					A14
75		P3_5					A13
76		P3_4					A12
77		P3_3					A11
78		P3_2					A10
79		P3_1					A9
80		P12_4					
81		P12_3					
82		P12_2					
83		P12_1					
84		P12_0					
85	VCC2						
86		P3_0					A8(/D7)
87	VSS						
88		P2_7				AN2_7	A7(/D7/D6)
89		P2_6				AN2_6	A6(/D6/D5)
90		P2_5				AN2_5	A5(/D5/D4)
91		P2_4				AN2_4	A4(/D4/D3)
92		P2_3				AN2_3	A3(/D3/D2)
93		P2_2				AN2_2	A2(/D2/D1)
94		P2_1				AN2_1	A1(/D1/D0)
95		P2_0				AN2_0	A0(/D0/-)
96		P1_7	$\overline{\text{INT5}}$				D15
97		P1_6	$\overline{\text{INT4}}$				D14
98		P1_5	$\overline{\text{INT3}}$				D13
99		P1_4					D12
100		P1_3					D11

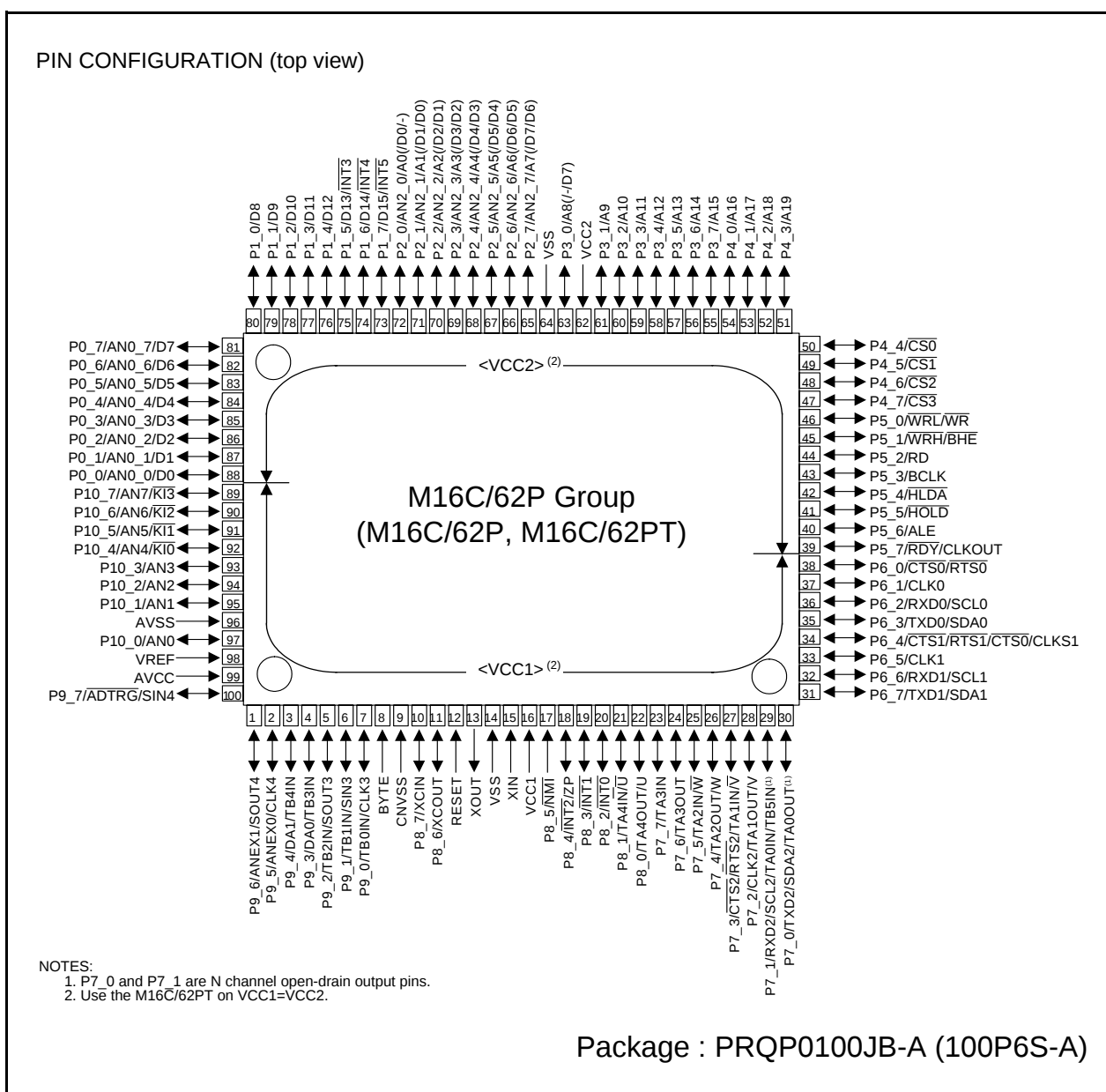


Figure 1.7 Pin Configuration (Top View)

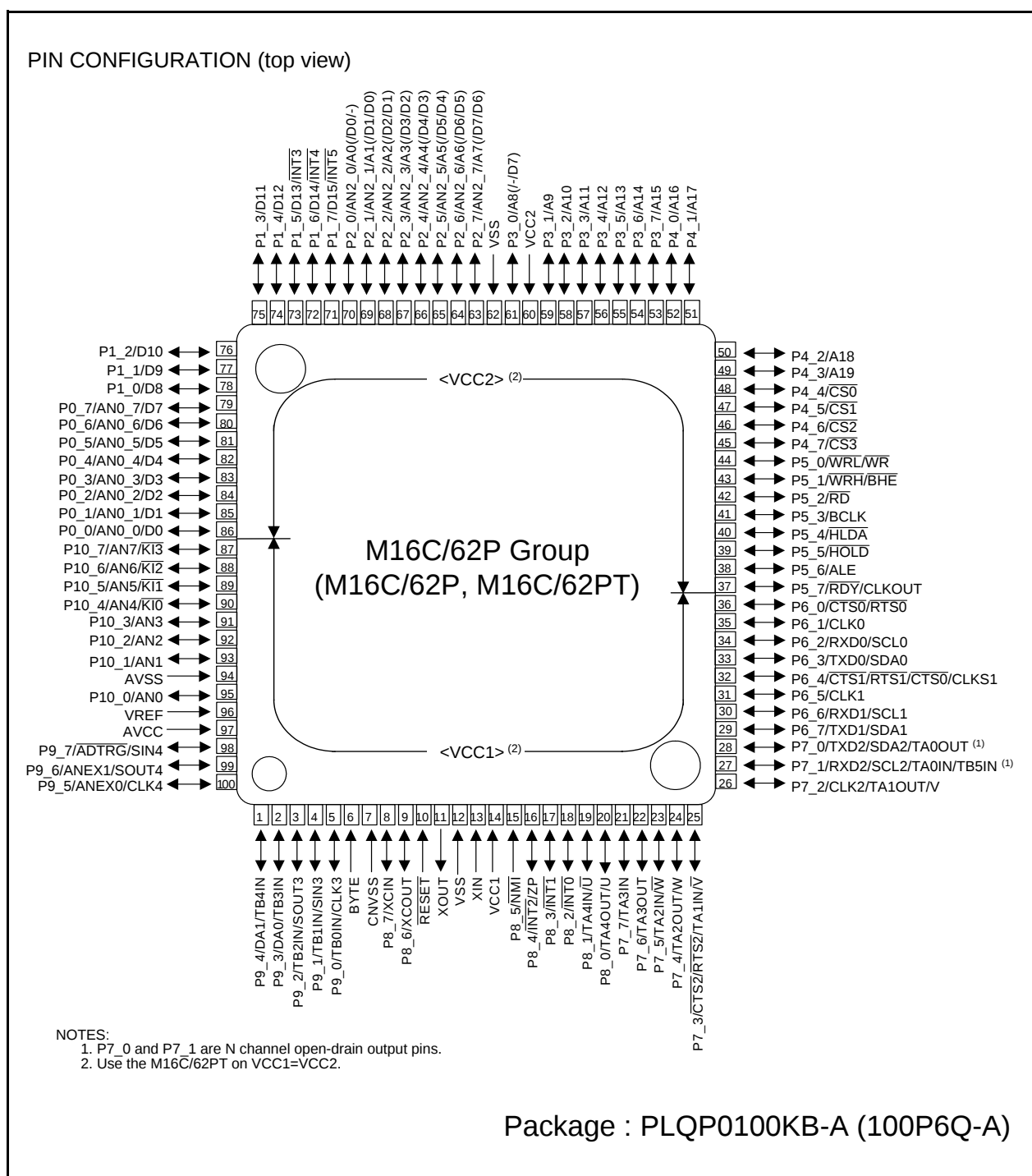


Figure 1.8 Pin Configuration (Top View)

Table 4.4 SFR Information (4) ⁽¹⁾

Address	Register	Symbol	After Reset
0340h	Timer B3, 4, 5 Count Start Flag	TBSR	000XXXXb
0341h			
0342h	Timer A1-1 Register	TA11	XXh
0343h			XXh
0344h	Timer A2-1 Register	TA21	XXh
0345h			XXh
0346h	Timer A4-1 Register	TA41	XXh
0347h			XXh
0348h	Three-Phase PWM Control Register 0	INVC0	00h
0349h	Three-Phase PWM Control Register 1	INVC1	00h
034Ah	Three-Phase Output Buffer Register 0	IDB0	00h
034Bh	Three-Phase Output Buffer Register 1	IDB1	00h
034Ch	Dead Time Timer	DTT	XXh
034Dh	Timer B2 Interrupt Occurrence Frequency Set Counter	ICTB2	XXh
034Eh			
034Fh			
0350h	Timer B3 Register	TB3	XXh
0351h			XXh
0352h	Timer B4 Register	TB4	XXh
0353h			XXh
0354h	Timer B5 Register	TB5	XXh
0355h			XXh
0356h			
0357h			
0358h			
0359h			
035Ah			
035Bh	Timer B3 Mode Register	TB3MR	00XX0000b
035Ch	Timer B4 Mode Register	TB4MR	00XX0000b
035Dh	Timer B5 Mode Register	TB5MR	00XX0000b
035Eh	Interrupt Factor Select Register 2	IFSR2A	00XXXXXXb
035Fh	Interrupt Factor Select Register	IFSR	00h
0360h	SI/O3 Transmit/Receive Register	S3TRR	XXh
0361h			
0362h	SI/O3 Control Register	S3C	01000000b
0363h	SI/O3 Bit Rate Generator	S3BRG	XXh
0364h	SI/O4 Transmit/Receive Register	S4TRR	XXh
0365h			
0366h	SI/O4 Control Register	S4C	01000000b
0367h	SI/O4 Bit Rate Generator	S4BRG	XXh
0368h			
0369h			
036Ah			
036Bh			
036Ch	UART0 Special Mode Register 4	U0SMR4	00h
036Dh	UART0 Special Mode Register 3	U0SMR3	000X0X0Xb
036Eh	UART0 Special Mode Register 2	U0SMR2	X0000000b
036Fh	UART0 Special Mode Register	U0SMR	X0000000b
0370h	UART1 Special Mode Register 4	U1SMR4	00h
0371h	UART1 Special Mode Register 3	U1SMR3	000X0X0Xb
0372h	UART1 Special Mode Register 2	U1SMR2	X0000000b
0373h	UART1 Special Mode Register	U1SMR	X0000000b
0374h	UART2 Special Mode Register 4	U2SMR4	00h
0375h	UART2 Special Mode Register 3	U2SMR3	000X0X0Xb
0376h	UART2 Special Mode Register 2	U2SMR2	X0000000b
0377h	UART2 Special Mode Register	U2SMR	X0000000b
0378h	UART2 Transmit/Receive Mode Register	U2MR	00h
0379h	UART2 Bit Rate Generator	U2BRG	XXh
037Ah	UART2 Transmit Buffer Register	U2TB	XXh
037Bh			XXh
037Ch	UART2 Transmit/Receive Control Register 0	U2C0	00001000b
037Dh	UART2 Transmit/Receive Control Register 1	U2C1	00000010b
037Eh	UART2 Receive Buffer Register	U2RB	XXh
037Fh			XXh

NOTES:

- The blank areas are reserved and cannot be accessed by users.

X : Nothing is mapped to this bit

Table 4.5 SFR Information (5) ⁽¹⁾

Address	Register	Symbol	After Reset
0380h	Count Start Flag	TABSR	00h
0381h	Clock Prescaler Reset Flag	CPSRF	0XXXXXXb
0382h	One-Shot Start Flag	ONSF	00h
0383h	Trigger Select Register	TRGSR	00h
0384h	Up-Down Flag	UDF	00h ⁽²⁾
0385h			
0386h	Timer A0 Register	TA0	XXh
0387h			XXh
0388h	Timer A1 Register	TA1	XXh
0389h			XXh
038Ah	Timer A2 Register	TA2	XXh
038Bh			XXh
038Ch	Timer A3 Register	TA3	XXh
038Dh			XXh
038Eh	Timer A4 Register	TA4	XXh
038Fh			XXh
0390h	Timer B0 Register	TB0	XXh
0391h			XXh
0392h	Timer B1 Register	TB1	XXh
0393h			XXh
0394h	Timer B2 Register	TB2	XXh
0395h			XXh
0396h	Timer A0 Mode Register	TA0MR	00h
0397h	Timer A1 Mode Register	TA1MR	00h
0398h	Timer A2 Mode Register	TA2MR	00h
0399h	Timer A3 Mode Register	TA3MR	00h
039Ah	Timer A4 Mode Register	TA4MR	00h
039Bh	Timer B0 Mode Register	TB0MR	00XX0000b
039Ch	Timer B1 Mode Register	TB1MR	00XX0000b
039Dh	Timer B2 Mode Register	TB2MR	00XX0000b
039Eh	Timer B2 Special Mode Register	TB2SC	XXXXXX00b
039Fh			
03A0h	UART0 Transmit/Receive Mode Register	U0MR	00h
03A1h	UART0 Bit Rate Generator	U0BRG	XXh
03A2h	UART0 Transmit Buffer Register	U0TB	XXh
03A3h			XXh
03A4h	UART0 Transmit/Receive Control Register 0	U0C0	00001000b
03A5h	UART0 Transmit/Receive Control Register 1	U0C1	00XX0010b
03A6h	UART0 Receive Buffer Register	U0RB	XXh
03A7h			XXh
03A8h	UART1 Transmit/Receive Mode Register	U1MR	00h
03A9h	UART1 Bit Rate Generator	U1BRG	XXh
03AAh	UART1 Transmit Buffer Register	U1TB	XXh
03ABh			XXh
03ACh	UART1 Transmit/Receive Control Register 0	U1C0	00001000b
03ADh	UART1 Transmit/Receive Control Register 1	U1C1	00XX0010b
03AEh	UART1 Receive Buffer Register	U1RB	XXh
03AFh			XXh
03B0h	UART Transmit/Receive Control Register 2	U0CON	X0000000b
03B1h			
03B2h			
03B3h			
03B4h			
03B5h			
03B6h			
03B7h			
03B8h	DMA0 Request Factor Select Register	DM0SL	00h
03B9h			
03BAh	DMA1 Request Factor Select Register	DM1SL	00h
03BBh			
03BCh	CRC Data Register	CRCD	XXh
03BDh			XXh
03BEh	CRC Input Register	CRCIN	XXh
03BFh			

NOTES:

1. The blank areas are reserved and cannot be accessed by users.
2. Bit 5 in the Up-down flag is "0" by reset. However, The values in these bits when read are indeterminate.

X : Nothing is mapped to this bit

Table 5.6 Flash Memory Version Electrical Characteristics ⁽¹⁾ for 100 cycle products (D3, D5, U3, U5)

Symbol	Parameter		Standard			Unit
			Min.	Typ.	Max.	
–	Program and Erase Endurance ⁽³⁾		100			cycle
–	Word Program Time (Vcc1=5.0V)			25	200	μs
–	Lock Bit Program Time			25	200	μs
–	Block Erase Time (Vcc1=5.0V)	4-Kbyte block		0.3	4	s
–		8-Kbyte block		0.3	4	s
–		32-Kbyte block		0.5	4	s
–		64-Kbyte block		0.8	4	s
–	Erase All Unlocked Blocks Time ⁽²⁾				4×n	s
tps	Flash Memory Circuit Stabilization Wait Time				15	μs
–	Data Hold Time ⁽⁵⁾		10			year

Table 5.7 Flash Memory Version Electrical Characteristics ⁽⁶⁾ for 10,000 cycle products (D7, D9, U7, U9) (Block A and Block 1 ⁽⁷⁾)

Symbol	Parameter	Standard			Unit
		Min.	Typ.	Max.	
—	Program and Erase Endurance ^(3, 8, 9)	10,000 ⁽⁴⁾			cycle
—	Word Program Time (V _{CC1} =5.0V)		25		μs
—	Lock Bit Program Time		25		μs
—	Block Erase Time (V _{CC1} =5.0V)	4-Kbyte block		0.3	s
t _{PS}	Flash Memory Circuit Stabilization Wait Time			15	μs
—	Data Hold Time ⁽⁵⁾	10			year

NOTES:

1. Referenced to V_{CC1}=4.5 to 5.5V, 3.0 to 3.6V at T_{opr} = 0 to 60 °C (D3, D5, U3, U5) unless otherwise specified.
2. n denotes the number of block erases.
3. Program and Erase Endurance refers to the number of times a block erase can be performed.
If the program and erase endurance is n (n=100, 1,000, or 10,000), each block can be erased n times.
For example, if a 4 Kbytes block A is erased after writing 1 word data 2,048 times, each to a different address, this counts as one program and erase endurance. Data cannot be written to the same address more than once without erasing the block.
(Rewrite prohibited)
4. Maximum number of E/W cycles for which operation is guaranteed.
5. T_{opr} = -40 to 85 °C (D3, D7, U3, U7) / -20 to 85 °C (D5, D9, U5, U9).
6. Referenced to V_{CC1} = 4.5 to 5.5V, 3.0 to 3.6V at T_{opr} = -40 to 85 °C (D7, U7) / -20 to 85 °C (D9, U9) unless otherwise specified.
7. Table 5.7 applies for block A or block 1 program and erase endurance > 1,000. Otherwise, use Table 5.6.
8. To reduce the number of program and erase endurance when working with systems requiring numerous rewrites, write to unused word addresses within the block instead of rewrite. Erase block only after all possible addresses are used. For example, an 8-word program can be written 256 times maximum before erase becomes necessary.
Maintaining an equal number of erasure between block A and block 1 will also improve efficiency. It is important to track the total number of times erasure is used.
9. Should erase error occur during block erase, attempt to execute clear status register command, then block erase command at least three times until erase error disappears.
10. Set the PM17 bit in the PM1 register to "1" (wait state) when executing more than 100 times rewrites (D7, D9, U7 and U9).
11. Customers desiring E/W failure rate information should contact their Renesas technical support representative.

Table 5.8 Flash Memory Version Program / Erase Voltage and Read Operation Voltage Characteristics (at T_{opr} = 0 to 60 °C(D3, D5, U3, U5), T_{opr} = -40 to 85 °C(D7, U7) / T_{opr} = -20 to 85 °C(D9, U9))

Flash Program, Erase Voltage	Flash Read Operation Voltage
V _{CC1} = 3.3 V ± 0.3 V or 5.0 V ± 0.5 V	V _{CC1} =2.7 to 5.5 V

$$V_{CC1}=V_{CC2}=5V$$

Table 5.11 Electrical Characteristics (1) (1)

Symbol	Parameter		Measuring Condition	Standard			Unit
				Min.	Typ.	Max.	
VOH	HIGH Output Voltage (3)	P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P14_0, P14_1	IOH=-5mA	VCC1-2.0		VCC1	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P12_0 to P12_7, P13_0 to P13_7	IOH=-5mA (2)	VCC2-2.0		VCC2	
VOH	HIGH Output Voltage (3)	P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P14_0, P14_1	OH=-200μA	VCC1-0.3		VCC1	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P12_0 to P12_7, P13_0 to P13_7	IOH=-200μA (2)	VCC2-0.3		VCC2	
VOH	HIGH Output Voltage XOUT	HIGHPOWER	IOH=-1mA	VCC1-2.0		VCC1	V
		LOWPOWER	IOH=-0.5mA	VCC1-2.0		VCC1	
	HIGH Output Voltage XCOUT	HIGHPOWER	With no load applied		2.5		V
		LOWPOWER	With no load applied		1.6		
VOL	LOW Output Voltage (3)	P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P14_0, P14_1	IOL=5mA			2.0	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P12_0 to P12_7, P13_0 to P13_7	IOL=5mA (2)			2.0	
VOL	LOW Output Voltage (3)	P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P14_0, P14_1	IOL=200μA			0.45	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P12_0 to P12_7, P13_0 to P13_7	IOL=200μA (2)			0.45	
VOL	LOW Output Voltage XOUT	HIGHPOWER	IOL=1mA			2.0	V
		LOWPOWER	IOL=0.5mA			2.0	
	LOW Output Voltage XCOUT	HIGHPOWER	With no load applied		0		V
		LOWPOWER	With no load applied		0		
VT+-VT-	Hysteresis	HOLD, RDY, TA0IN to TA4IN, TB0IN to TB5IN, INT0 to INT5, NMI, ADTRG, CTS0 to CTS2, CLK0 to CLK4, TA0OUT to TA4OUT, KI0 to KI3, RXD0 to RXD2, SCL0 to SCL2, SDA0 to SDA2, SIN3, SIN4		0.2		1.0	V
VT+-VT-	Hysteresis	RESET		0.2		2.5	V
IiH	HIGH Input Current (3)	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1, XIN, RESET, CNVSS, BYTE	Vi=5V			5.0	μA
IiL	LOW Input Current (3)	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1, XIN, RESET, CNVSS, BYTE	Vi=0V			-5.0	μA
RPULLUP	Pull-Up Resistance (3)	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1	Vi=0V	30	50	170	kΩ
RtXIN	Feedback Resistance XIN				1.5		MΩ
RtXCIN	Feedback Resistance XCIN				15		MΩ
VRAM	RAM Retention Voltage		At stop mode	2.0			V

NOTES:

1. Referenced to VCC1=VCC2=4.2 to 5.5V, VSS = 0V at Topr = -20 to 85°C / -40 to 85°C, f(BCLK)=24MHz unless otherwise specified.
2. Where the product is used at VCC1 = 5 V and VCC2 = 3 V, refer to the 3 V version value for the pin specified value on VCC2 port side.
3. There is no external connections for port P1_0 to P1_7, P4_4 to P4_7, P7_2 to P7_5 and P9_1 in 80-pin version.

$$V_{CC1}=V_{CC2}=5V$$

Timing Requirements

($V_{CC1} = V_{CC2} = 5V$, $V_{SS} = 0V$, at $T_{opr} = -20$ to $85^{\circ}C$ / -40 to $85^{\circ}C$ unless otherwise specified)

Table 5.13 External Clock Input (XIN input) ⁽¹⁾

Symbol	Parameter	Standard		Unit
		Min.	Max.	
t_c	External Clock Input Cycle Time	62.5		ns
$t_{w(H)}$	External Clock Input HIGH Pulse Width	25		ns
$t_{w(L)}$	External Clock Input LOW Pulse Width	25		ns
t_r	External Clock Rise Time		15	ns
t_f	External Clock Fall Time		15	ns

NOTES:

1. The condition is $V_{CC1}=V_{CC2}=3.0$ to $5.0V$.

Table 5.14 Memory Expansion Mode and Microprocessor Mode

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{ac1(RD-DB)}$	Data Input Access Time (for setting with no wait)		(NOTE 1)	ns
$t_{ac2(RD-DB)}$	Data Input Access Time (for setting with wait)		(NOTE 2)	ns
$t_{ac3(RD-DB)}$	Data Input Access Time (when accessing multiplex bus area)		(NOTE 3)	ns
$t_{su(DB-RD)}$	Data Input Setup Time	40		ns
$t_{su(RDY-BCLK)}$	RDY Input Setup Time	30		ns
$t_{su(HOLD-BCLK)}$	HOLD Input Setup Time	40		ns
$t_h(RD-DB)$	Data Input Hold Time	0		ns
$t_h(BCLK-RDY)$	RDY Input Hold Time	0		ns
$t_h(BCLK-HOLD)$	HOLD Input Hold Time	0		ns

NOTES:

1. Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f(BCLK)} - 45[ns]$$

2. Calculated according to the BCLK frequency as follows:

$$\frac{(n-0.5) \times 10^9}{f(BCLK)} - 45[ns] \quad n \text{ is "2" for 1-wait setting, "3" for 2-wait setting and "4" for 3-wait setting.}$$

3. Calculated according to the BCLK frequency as follows:

$$\frac{(n-0.5) \times 10^9}{f(BCLK)} - 45[ns] \quad n \text{ is "2" for 2-wait setting, "3" for 3-wait setting.}$$

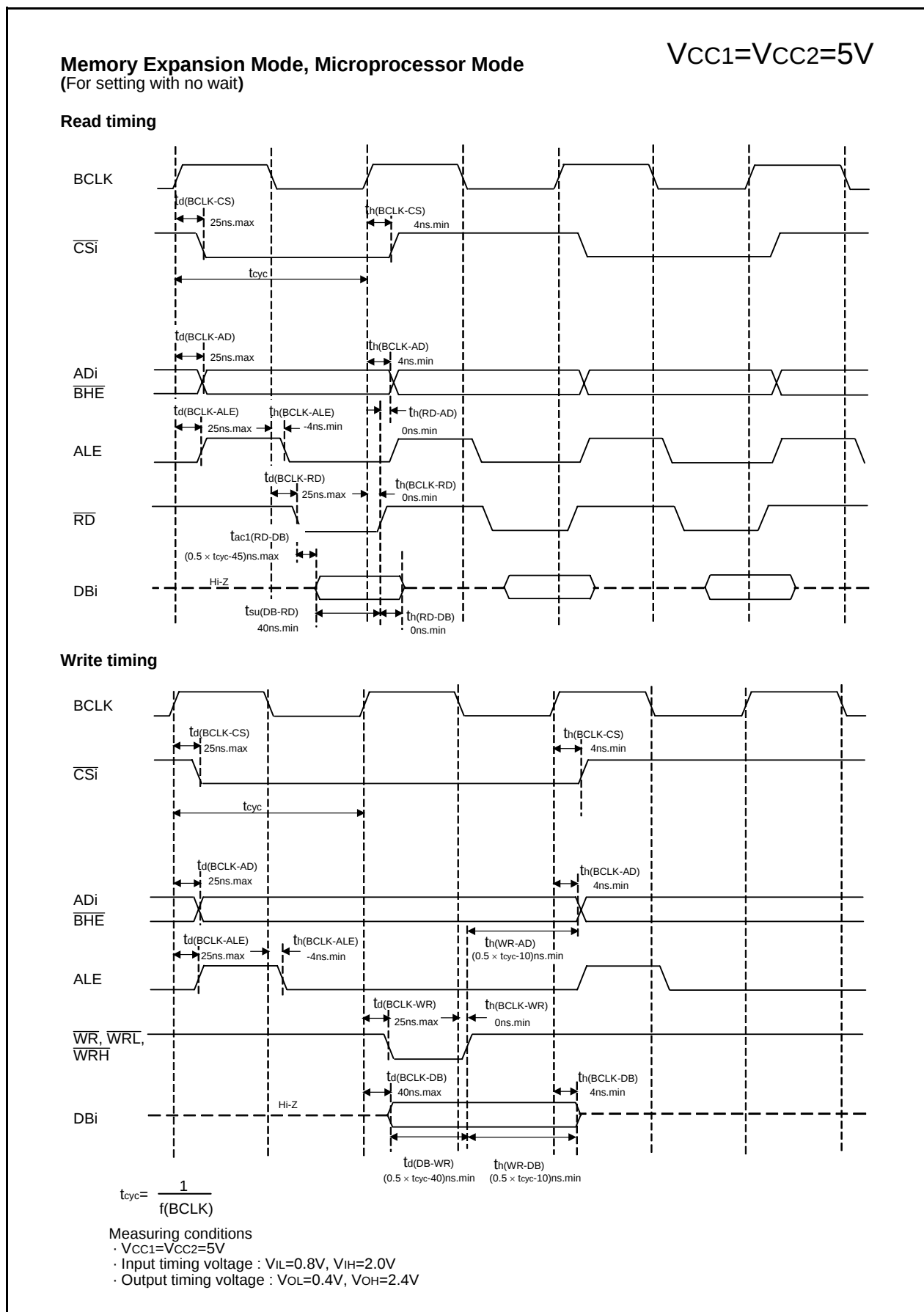


Figure 5.6 Timing Diagram (4)

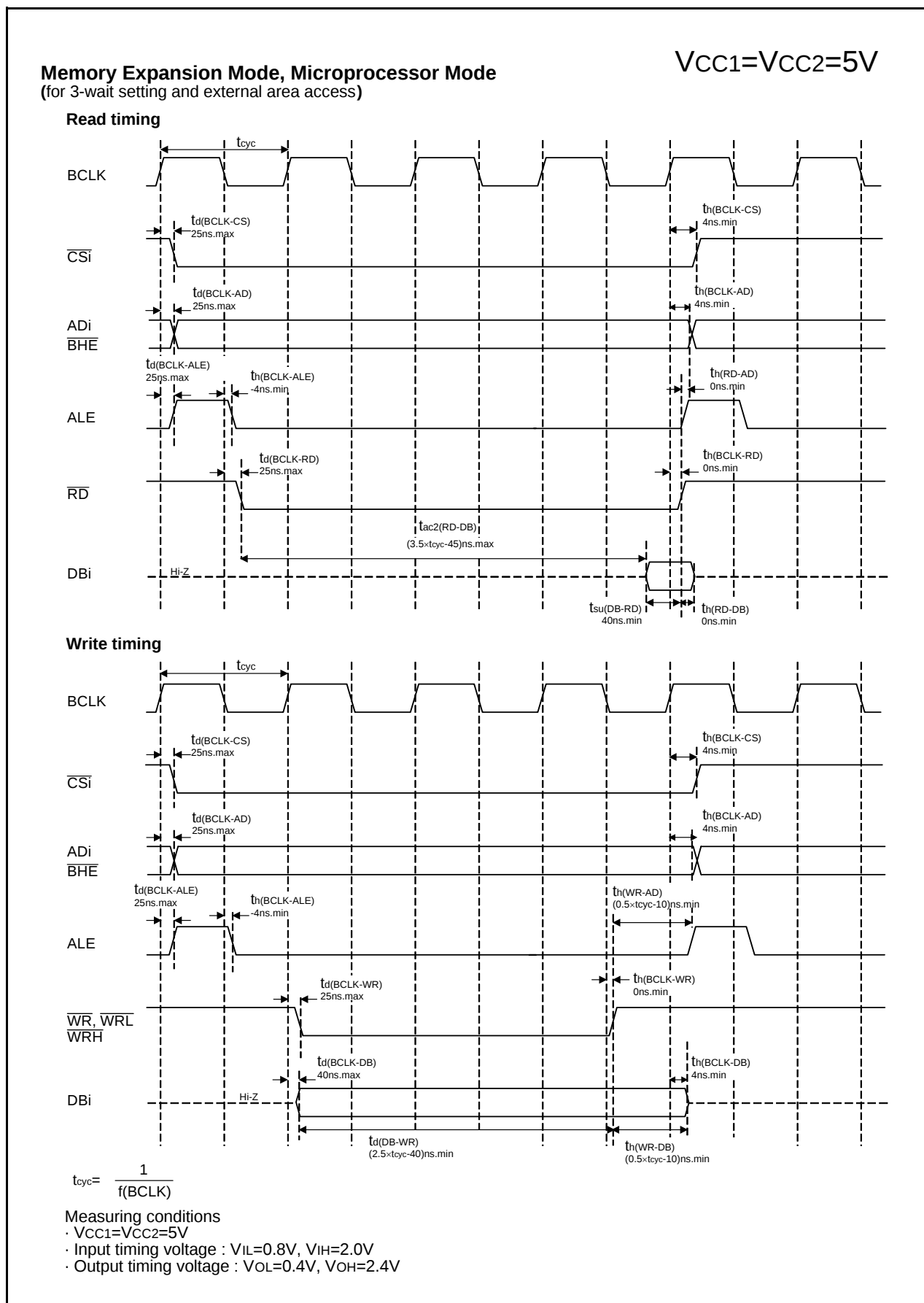


Figure 5.9 Timing Diagram (7)

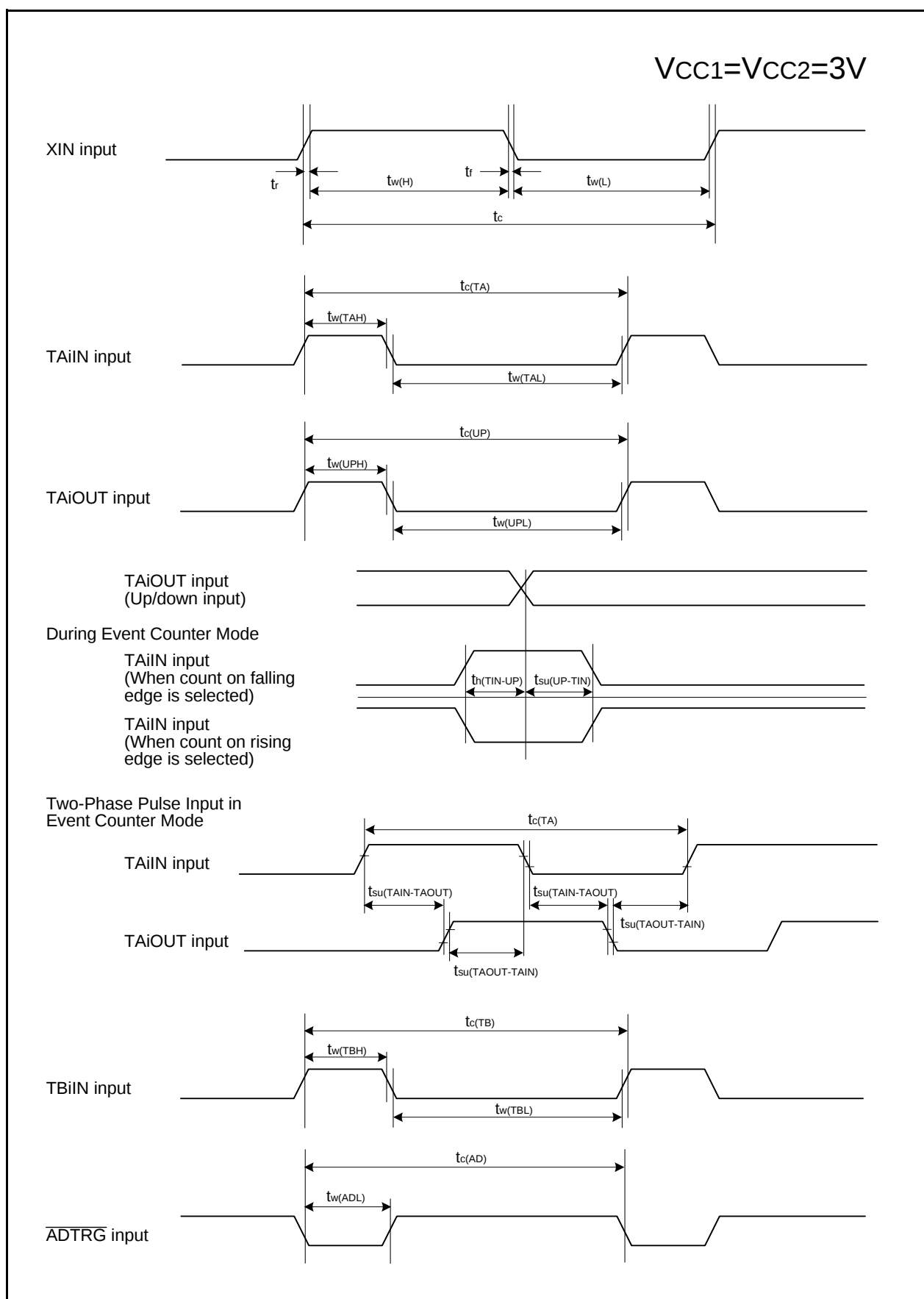
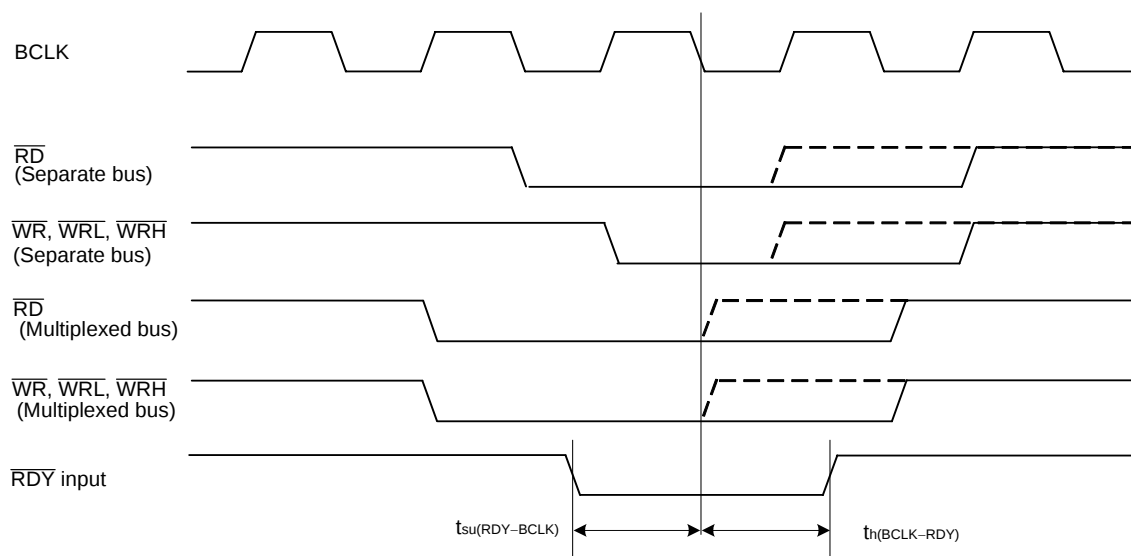


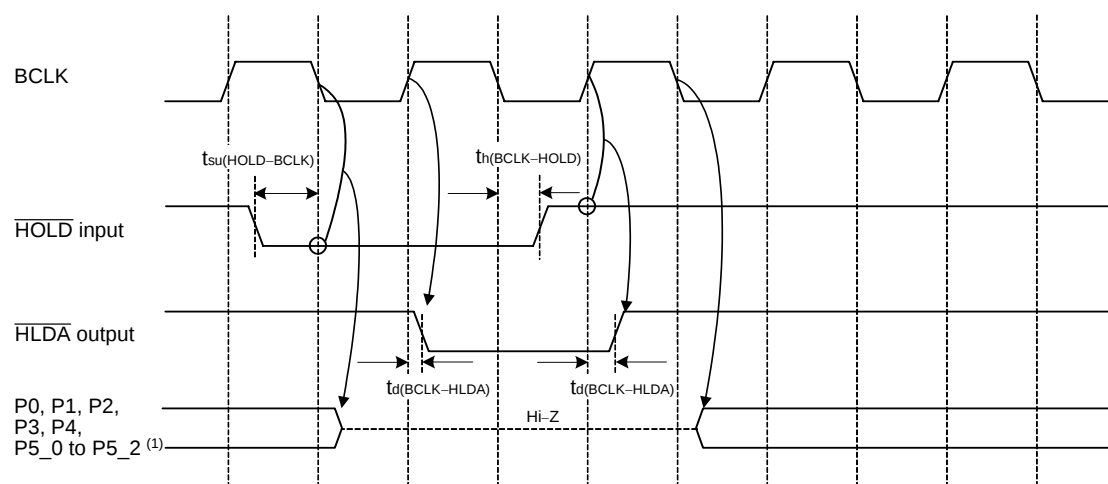
Figure 5.13 Timing Diagram (1)

Memory Expansion Mode, Microprocessor Mode

(Effective for setting with wait)

 $V_{CC1}=V_{CC2}=3V$ 

(Common to setting with wait and setting without wait)

**NOTES:**

- These pins are set to high-impedance regardless of the input level of the BYTE pin, PM06 bit in PM0 register and PM11 bit in PM1 register.

Measuring conditions :

- $V_{CC1}=V_{CC2}=3V$
- Input timing voltage : Determined with $V_{IL}=0.6V$, $V_{IH}=2.4V$
- Output timing voltage : Determined with $V_{OL}=1.5V$, $V_{OH}=1.5V$

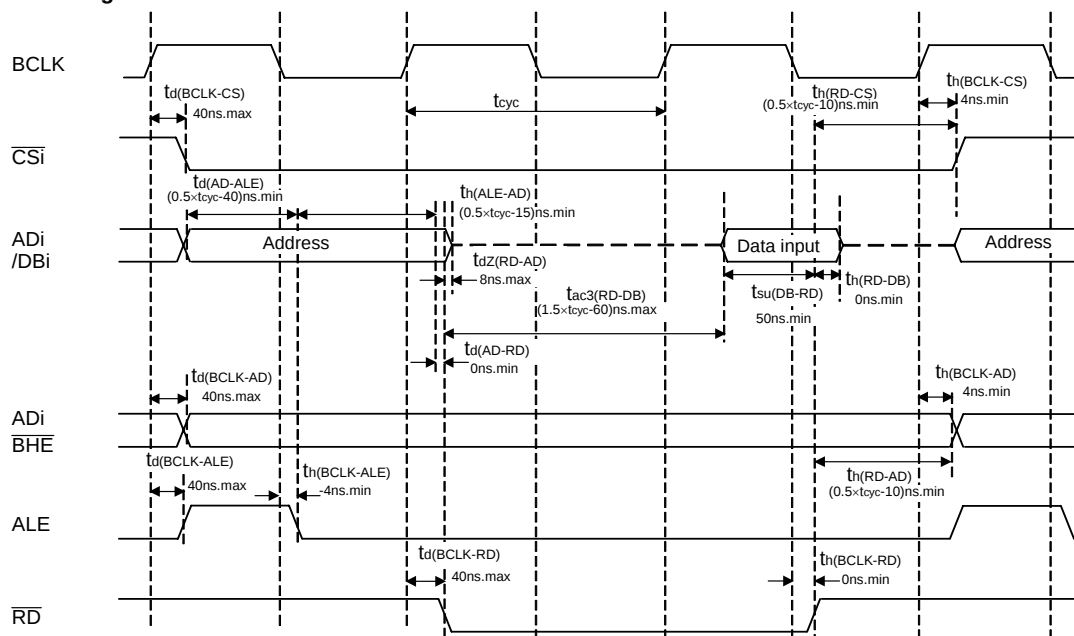
Figure 5.15 Timing Diagram (3)

Memory Expansion Mode, Microprocessor Mode

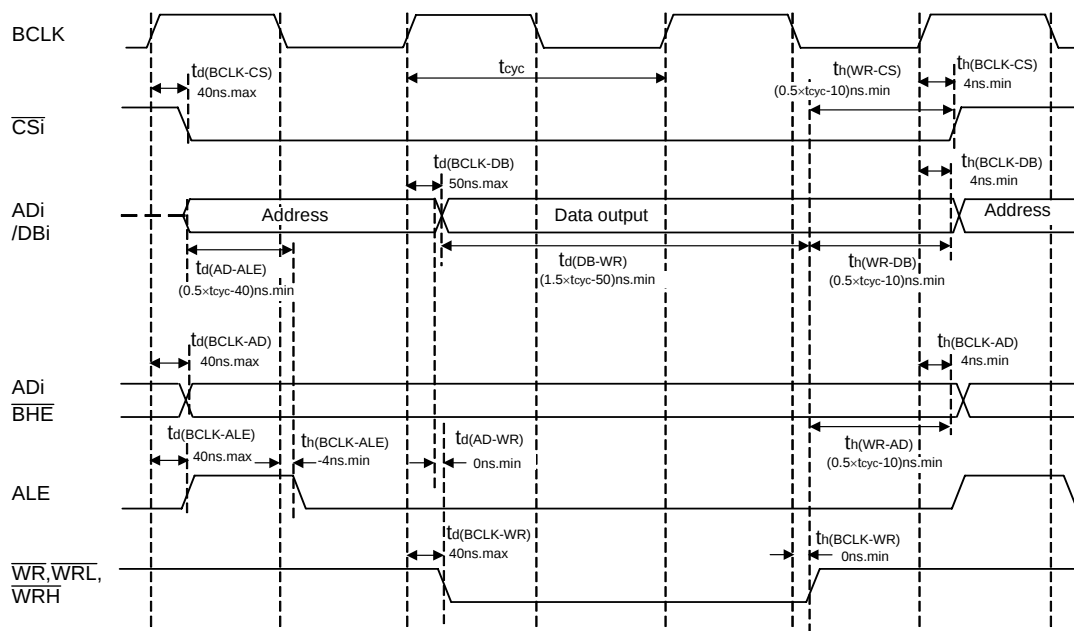
(For 2-wait setting, external area access and multiplex bus selection)

 $V_{CC1}=V_{CC2}=3V$

Read timing



Write timing



$$t_{\text{cyc}} = \frac{1}{f(\text{BCLK})}$$

Measuring conditions

- $V_{CC1}=V_{CC2}=3V$
- Input timing voltage : $V_{IL}=0.6V$, $V_{IH}=2.4V$
- Output timing voltage : $V_{OL}=1.5V$, $V_{OH}=1.5V$

Figure 5.20 Timing Diagram (8)

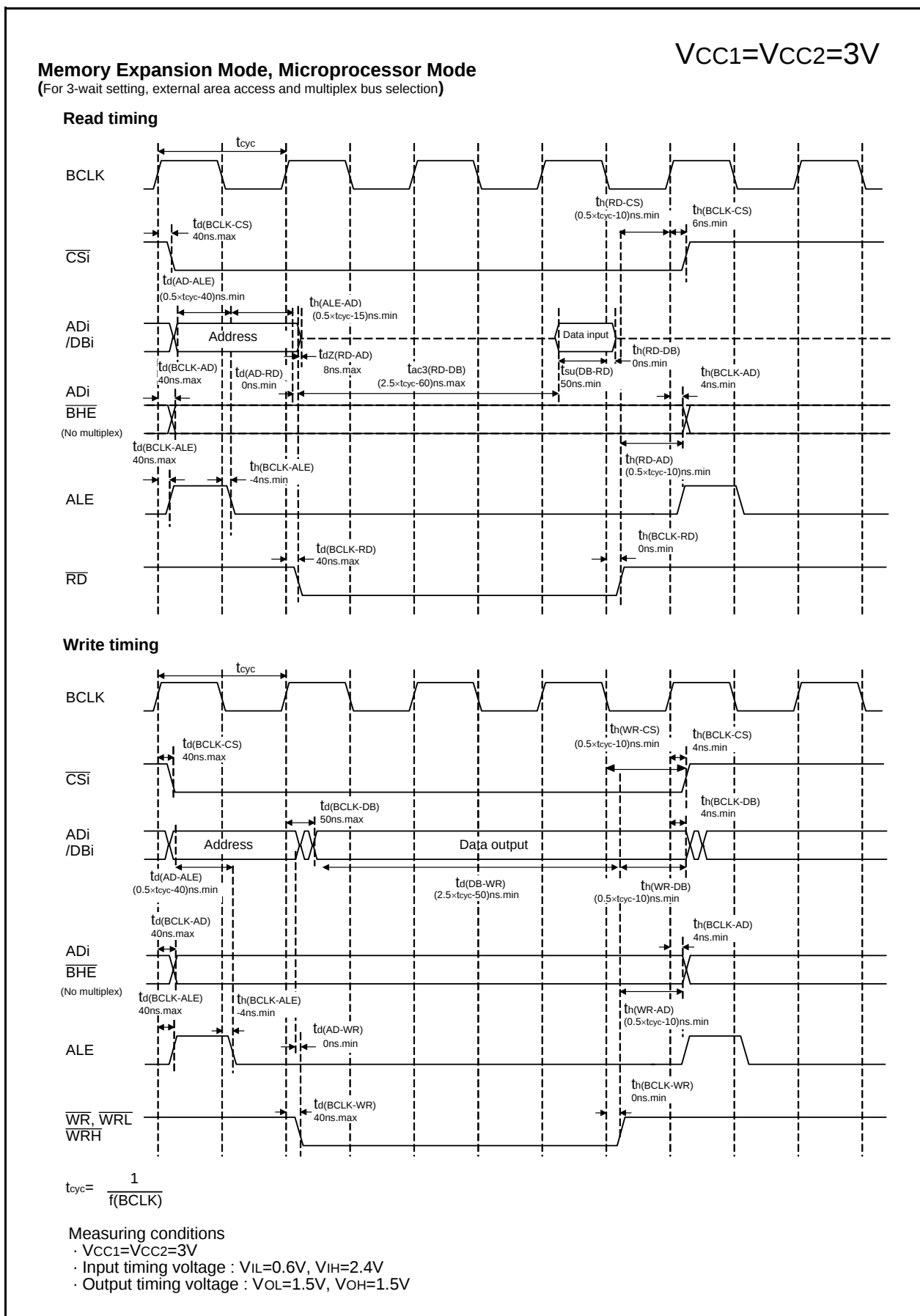


Figure 5.21 Timing Diagram (9)

5.2 Electrical Characteristics (M16C/62PT)

Table 5.49 Absolute Maximum Ratings

Symbol	Parameter		Condition	Rated Value	Unit
V _{CC1} , V _{CC2}	Supply Voltage		V _{CC1} =V _{CC2} =AV _{CC}	−0.3 to 6.5	V
AV _{CC}	Analog Supply Voltage		V _{CC1} =V _{CC2} =AV _{CC}	−0.3 to 6.5	V
V _I	Input Voltage	RESET, CNVSS, BYTE, P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P14_0, P14_1, VREF, XIN		−0.3 to V _{CC1} +0.3 ⁽¹⁾	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P12_0 to P12_7, P13_0 to P13_7		−0.3 to V _{CC2} +0.3 ⁽¹⁾	V
		P7_0, P7_1		−0.3 to 6.5	V
V _O	Output Voltage	P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P14_0, P14_1, XOUT		−0.3 to V _{CC1} +0.3 ⁽¹⁾	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P12_0 to P12_7, P13_0 to P13_7		−0.3 to V _{CC2} +0.3 ⁽¹⁾	V
		P7_0, P7_1		−0.3 to 6.5	V
P _d	Power Dissipation		−40°C<T _{opr} ≤85°C	300	mW
			85°C<T _{opr} ≤125°C	200	
T _{opr}	Operating Ambient Temperature	When the Microcomputer is Operating		−40 to 85 / −40 to 125 ⁽²⁾	°C
		Flash Program Erase		0 to 60	
T _{stg}	Storage Temperature			−65 to 150	°C

NOTES:

1. There is no external connections for port P1_0 to P1_7, P4_4 to P4_7, P7_2 to P7_5 and P9_1 in 80-pin version.
2. T version = −40 to 85 °C, V version= −40 to 125 °C.

$$V_{CC1}=V_{CC2}=5V$$

Table 5.57 Electrical Characteristics (1) ⁽¹⁾

Symbol	Parameter		Measuring Condition	Standard			Unit
				Min.	Typ.	Max.	
VOH	HIGH Output Voltage ⁽²⁾	P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P14_0, P14_1	IOH=−5mA	VCC1−2.0		VCC1	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P12_0 to P12_7, P13_0 to P13_7	IOH=−5mA	VCC2−2.0		VCC2	
VOH	HIGH Output Voltage ⁽²⁾	P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P14_0, P14_1	OH=−200μA	VCC1−0.3		VCC1	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P12_0 to P12_7, P13_0 to P13_7	IOH=−200μA	VCC2−0.3		VCC2	
VOH	HIGH Output Voltage XOUT	HIGHPOWER	IOH=−1mA	VCC1−2.0		VCC1	V
		LOWPOWER	IOH=−0.5mA	VCC1−2.0		VCC1	
	HIGH Output Voltage XCOUT	HIGHPOWER	With no load applied		2.5		V
		LOWPOWER	With no load applied		1.6		
VOL	LOW Output Voltage ⁽²⁾	P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P14_0, P14_1	IOL=5mA			2.0	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P12_0 to P12_7, P13_0 to P13_7	IOL=5mA			2.0	
VOL	LOW Output Voltage ⁽²⁾	P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P14_0, P14_1	IOL=200μA			0.45	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P12_0 to P12_7, P13_0 to P13_7	IOL=200μA			0.45	
VOL	LOW Output Voltage XOUT	HIGHPOWER	IOL=1mA			2.0	V
		LOWPOWER	IOL=0.5mA			2.0	
	LOW Output Voltage XCOUT	HIGHPOWER	With no load applied		0		V
		LOWPOWER	With no load applied		0		
VT+−VT−	Hysteresis	HOLD, RDY, TA0IN to TA4IN, TB0IN to TB5IN, INT0 to INT5, NMI, ADTRG, CTS0 to CTS2, CLK0 to CLK4, TA0OUT to TA4OUT, KI0 to KI3, RXD0 to RXD2, SCL0 to SCL2, SDA0 to SDA2, SIN3, SIN4		0.2		1.0	V
VT+−VT−	Hysteresis	RESET		0.2		2.5	V
I _{IH}	HIGH Input Current ⁽²⁾	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1, XIN, RESET, CNVSS, BYTE	Vi=5V			5.0	μA
I _{IL}	LOW Input Current ⁽²⁾	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1, XIN, RESET, CNVSS, BYTE	Vi=0V			−5.0	μA
R _{PULLUP}	Pull-Up Resistance ⁽²⁾	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1	Vi=0V	30	50	170	kΩ
R _{IXIN}	Feedback Resistance XIN				1.5		MΩ
R _{IXCIN}	Feedback Resistance XCIN				15		MΩ
V _{RAM}	RAM Retention Voltage		At stop mode	2.0			V

NOTES:

1. Referenced to VCC1=VCC2=4.0 to 5.5V, VSS = 0V at T_{opr} = −40 to 85°C / −40 to 125°C, f(BCLK)=24MHz unless otherwise specified. T version = −40 to 85°C, V version = −40 to 125°C.
2. There is no external connections for port P1_0 to P1_7, P4_4 to P4_7, P7_2 to P7_5 and P9_1 in 80-pin version.

REVISION HISTORY		M16C/62P Group (M16C/62P, M16C/62PT) Hardware Manual	
Rev.	Date	Description	
		Page	Summary
		40	Table 5.24 is partly revised.
		57	Table 5.43 is partly revised.
		70	Table 5.48 is partly revised.
		72	Table 5.50 is partly revised.
		73	Table 5.53 is partly revised.
		74	Table 5.55 is revised.
		76	Table 5.57 is partly revised.
		79	Table 5.69 is partly revised.
2.41	Jan 01, 2006	-	voltage down detection reset -> brown-out detection Reset
		2-4	Tables 1.1 to 1.3 Performance outline of M16C/62P group are partly revised.
		7	Table 1.4 Product List (1) is partly revised. Note 1 is added.
		8	Table 1.5 Product List (2) is partly revised. Note 1, 2 and 3 are added.
		9	Table 1.6 Product List (3) is partly revised. Note 1 and 2 are added.
		10	Table 1.7 Product List (4) is partly revised. Note 1 and 2 are added.
		11	Figure 1.3 Type No., Memory Size, Shows RAM capacity, and Package is partly revised
		12	Table 1.8 Product Code of Flash Memory version and ROMless version for M16C/62P is partly revised.
		13	Table 1.9 Product Code of Flash Memory version for M16C/62P is partly revised.
		14	Figure 1.6 Pin Configuration (Top View) is partly revised.
		15-17	Tables 1.10 to 1.12 Pin Characteristics for 128-Pin Package are added.
		18-19	Figure 1.7 and 1.8 Pin Configuration (Top View) are partly revised.
		20-21	Tables 1.13 to 1.14 Pin Characteristics for 100-Pin Package are added.
		22	Figure 1.9 Pin Configuration (Top View) is partly revised.
		23-24	Tables 1.15 to 1.16 Pin Characteristics for 80-Pin Package are added.
		25-29	Tables 1.17 to 1.21 are partly revised.
		34	Note 4 of Table 4.1 SFR Information is partly revised.
		43	Table 5.4 A/D Conversion Characteristics is partly revised.
		45	Table 5.6 Flash Memory Version Electrical Characteristics for 100 cycle products is partly revised. Table 5.7 Flash Memory Version Electrical Characteristics for 10,000 cycle products is partly revised. Table 5.8 Flash Memory Version Program / Erase Voltage and Read Operation Voltage Characteristics is partly revised.
		46	Table 5.9 Low Voltage Detection Circuit Electrical Characteristics is partly revised.