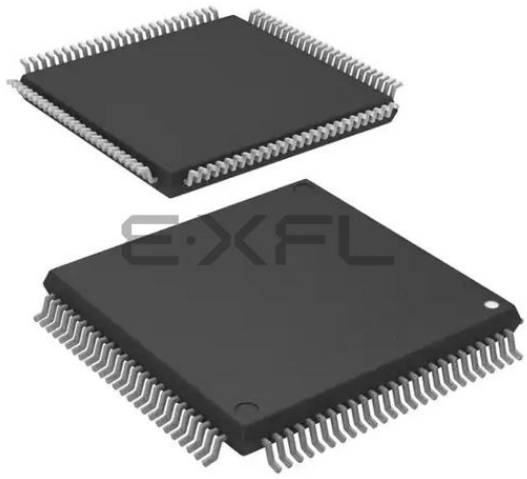
Renesas Electronics America Inc - M30622F8PGP#U3C Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	M16C/60
Core Size	16-Bit
Speed	24MHz
Connectivity	I²C, IEBus, UART/USART
Peripherals	DMA, WDT
Number of I/O	85
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 26x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LFQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/m30622f8pgp-u3c

Table 1.5 Product List (2) (M16C/62P) As of Dec. 2005

Type No.	ROM Capacity	RAM Capacity	Package Type (1)	Remarks
M30622MHP-XXXFP	384 Kbytes	16 Kbytes	PRQP0100JB-A	Mask ROM version
M30622MHP-XXXGP			PLQP0100KB-A	
M30623MHP-XXXGP			PLQP0128KB-A	
M30624MHP-XXXFP		24 Kbytes	PRQP0100JB-A	
M30624MHP-XXXGP			PLQP0100KB-A	
M30625MHP-XXXGP			PLQP0128KB-A	
M30626MHP-XXXFP		31 Kbytes	PRQP0100JB-A	
M30626MHP-XXXGP			PLQP0100KB-A	
M30627MHP-XXXGP			PLQP0128KB-A	
M30626MJP-XXXFP (D)	512 Kbytes	31 Kbytes	PRQP0100JB-A	
M30626MJP-XXXGP (D)			PLQP0100KB-A	
M30627MJP-XXXGP (D)			PLQP0128KB-A	
M30622F8PFP	64K+4 Kbytes	4 Kbytes	PRQP0100JB-A	Flash memory version (2)
M30622F8PGP			PLQP0100KB-A	
M30623F8PGP			PRQP0080JA-A	
M30620FCPFP	128K+4 Kbytes	10 Kbytes	PRQP0100JB-A	
M30620FCPGP			PLQP0100KB-A	
M30621FCPGP			PRQP0080JA-A	
M3062LFGPFP(3) (D)	256K+4 Kbytes	20 Kbytes	PRQP0100JB-A	
M3062LFGPGP(3) (D)			PLQP0100KB-A	
M30625FGPGP			PLQP0128KB-A	
M30626FHPFP	384K+4 Kbytes	31 Kbytes	PRQP0100JB-A	
M30626FHPGP			PLQP0100KB-A	
M30627FHPGP			PLQP0128KB-A	
M30626FJPFP	512K+4 Kbytes	31 Kbytes	PRQP0100JB-A	
M30626FJPGP			PLQP0100KB-A	
M30627FJPGP			PLQP0128KB-A	
M30622SPFP	–	4 Kbytes	PRQP0100JB-A	ROM-less version
M30622SPGP			PLQP0100KB-A	
M30620SPFP		10 Kbytes	PRQP0100JB-A	
M30620SPGP			PLQP0100KB-A	
M30624SPFP (D)	–	20 Kbytes	PRQP0100JB-A	
M30624SPGP (D)			PLQP0100KB-A	
M30626SPFP (D)		31 Kbytes	PRQP0100JB-A	
M30626SPGP (D)			PLQP0100KB-A	

(D): Under development

NOTES:

1. The old package type numbers of each package type are as follows.
   PLQP0128KB-A : 128P6Q-A,
   PRQP0100JB-A : 100P6S-A,
   PLQP0100KB-A : 100P6Q-A,
   PRQP0080JA-A : 80P6S-A
2. In the flash memory version, there is 4K bytes area (block A).
3. Please use M3062LFGPFP and M3062LFGPGP for your new system instead of M30624FGPFP and M30624FGPGP. The M16C/62P Group (M16C/62P, M16C/62PT) hardware manual is still good for M30624FGPFP and M30624FGPGP.

M30624FGPFP	256K+4 Kbytes	20 Kbytes	PRQP0100JB-A	Flash memory version
M30624FGPGP			PLQP0100KB-A	

1.5 Pin Configuration

Figures 1.6 to 1.9 show the Pin Configuration (Top View).

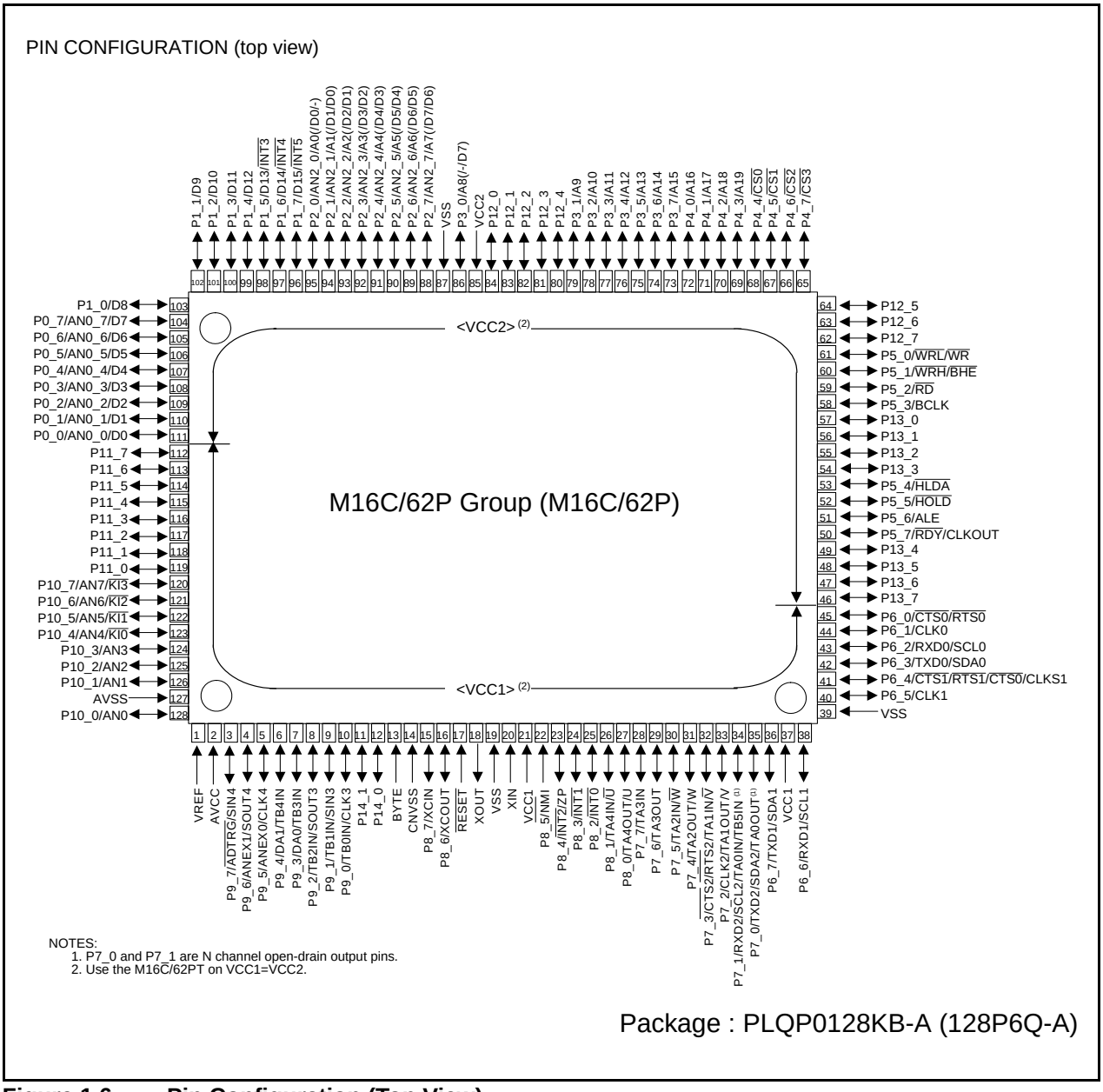


Figure 1.6 Pin Configuration (Top View)

Table 1.14 Pin Characteristics for 100-Pin Package (2)

Pin No.		Control Pin	Port	Interrupt Pin	Timer Pin	UART Pin	Analog Pin	Bus Control Pin
FP	GP							
51	49		P4_3					A19
52	50		P4_2					A18
53	51		P4_1					A17
54	52		P4_0					A16
55	53		P3_7					A15
56	54		P3_6					A14
57	55		P3_5					A13
58	56		P3_4					A12
59	57		P3_3					A11
60	58		P3_2					A10
61	59		P3_1					A9
62	60	VCC2						
63	61		P3_0					A8(/-/D7)
64	62	VSS						
65	63		P2_7				AN2_7	A7(/D7/D6)
66	64		P2_6				AN2_6	A6(/D6/D5)
67	65		P2_5				AN2_5	A5(/D5/D4)
68	66		P2_4				AN2_4	A4(/D4/D3)
69	67		P2_3				AN2_3	A3(/D3/D2)
70	68		P2_2				AN2_2	A2(/D2/D1)
71	69		P2_1				AN2_1	A1(/D1/D0)
72	70		P2_0				AN2_0	A0(/D0/-)
73	71		P1_7	$\overline{\text{INT5}}$				D15
74	72		P1_6	$\overline{\text{INT4}}$				D14
75	73		P1_5	$\overline{\text{INT3}}$				D13
76	74		P1_4					D12
77	75		P1_3					D11
78	76		P1_2					D10
79	77		P1_1					D9
80	78		P1_0					D8
81	79		P0_7				AN0_7	D7
82	80		P0_6				AN0_6	D6
83	81		P0_5				AN0_5	D5
84	82		P0_4				AN0_4	D4
85	83		P0_3				AN0_3	D3
86	84		P0_2				AN0_2	D2
87	85		P0_1				AN0_1	D1
88	86		P0_0				AN0_0	D0
89	87		P10_7	$\overline{\text{KI3}}$			AN7	
90	88		P10_6	$\overline{\text{KI2}}$			AN6	
91	89		P10_5	$\overline{\text{KI1}}$			AN5	
92	90		P10_4	$\overline{\text{KI0}}$			AN4	
93	91		P10_3				AN3	
94	92		P10_2				AN2	
95	93		P10_1				AN1	
96	94	AVSS						
97	95		P10_0				AN0	
98	96	VREF						
99	97	AVCC						
100	98		P9_7			SIN4	$\overline{\text{ADTRG}}$	

4. Special Function Register (SFR)

SFR(Special Function Register) is the control register of peripheral functions. Tables 4.1 to 4.6 list the SFR information.

Table 4.1 SFR Information (1) (1)

Address	Register	Symbol	After Reset
0000h			
0001h			
0002h			
0003h			
0004h	Processor Mode Register 0 (2)	PM0	00000000b(CNVSS pin is "L") 00000011b(CNVSS pin is "H")
0005h	Processor Mode Register 1	PM1	00001000b
0006h	System Clock Control Register 0	CM0	01001000b
0007h	System Clock Control Register 1	CM1	00100000b
0008h	Chip Select Control Register (6)	CSR	00000001b
0009h	Address Match Interrupt Enable Register	AIER	XXXXXX00b
000Ah	Protect Register	PRCR	XX000000b
000Bh	Data Bank Register (6)	DBR	00h
000Ch	Oscillation Stop Detection Register (3)	CM2	0X000000b
000Dh			
000Eh	Watchdog Timer Start Register	WDTS	XXh
000Fh	Watchdog Timer Control Register	WDC	00XXXXXXb (4)
0010h 0011h 0012h	Address Match Interrupt Register 0	RMAD0	00h 00h X0h
0013h			
0014h 0015h 0016h	Address Match Interrupt Register 1	RMAD1	00h 00h X0h
0017h			
0018h			
0019h	Voltage Detection Register 1 (5, 6)	VCR1	00001000b
001Ah	Voltage Detection Register 2 (5, 6)	VCR2	00h
001Bh	Chip Select Expansion Control Register (6)	CSE	00h
001Ch	PLL Control Register 0	PLC0	0001X010b
001Dh			
001Eh	Processor Mode Register 2	PM2	XXX00000b
001Fh	Low Voltage Detection Interrupt Register (6)	D4INT	00h
0020h 0021h 0022h	DMA0 Source Pointer	SAR0	XXh XXh XXh
0023h			
0024h 0025h 0026h	DMA0 Destination Pointer	DAR0	XXh XXh XXh
0027h			
0028h 0029h	DMA0 Transfer Counter	TCR0	XXh XXh
002Ah			
002Bh			
002Ch	DMA0 Control Register	DM0CON	00000X00b
002Dh			
002Eh			
002Fh			
0030h 0031h 0032h	DMA1 Source Pointer	SAR1	XXh XXh XXh
0033h			
0034h 0035h 0036h	DMA1 Destination Pointer	DAR1	XXh XXh XXh
0037h			
0038h 0039h	DMA1 Transfer Counter	TCR1	XXh XXh
003Ah			
003Bh			
003Ch	DMA1 Control Register	DM1CON	00000X00b
003Dh			
003Eh			
003Fh			

NOTES:
1. The blank areas are reserved and cannot be accessed by users.
2. The PM00 and PM01 bits do not change at software reset, watchdog timer reset and oscillation stop detection reset.
3. The CM20, CM21, and CM27 bits do not change at oscillation stop detection reset.
4. The WDC5 bit is "0" (cold start) immediately after power-on. I t can only be set to "1" in a program.
5. This register does not change at software reset, watchdog timer reset and oscillation stop detection reset.
6. This register in M16C/62PT cannot be used.

X : Nothing is mapped to this bit

Table 4.2 SFR Information (2) (1)

Address	Register	Symbol	After Reset
0040h			
0041h			
0042h			
0043h			
0044h	INT3 Interrupt Control Register	INT3IC	XX00X000b
0045h	Timer B5 Interrupt Control Register	TB5IC	XXXXX000b
0046h	Timer B4 Interrupt Control Register, UART1 BUS Collision Detection Interrupt Control Register	TB4IC, U1BCNIC	XXXXX000b
0047h	Timer B3 Interrupt Control Register, UART0 BUS Collision Detection Interrupt Control Register	TB3IC, U0BCNIC	XXXXX000b
0048h	SI/O4 Interrupt Control Register, INT5 Interrupt Control Register	S4IC, INT5IC	XX00X000b
0049h	SI/O3 Interrupt Control Register, INT4 Interrupt Control Register	S3IC, INT4IC	XX00X000b
004Ah	UART2 Bus Collision Detection Interrupt Control Register	BCNIC	XXXXX000b
004Bh	DMA0 Interrupt Control Register	DM0IC	XXXXX000b
004Ch	DMA1 Interrupt Control Register	DM1IC	XXXXX000b
004Dh	Key Input Interrupt Control Register	KUPIC	XXXXX000b
004Eh	A/D Conversion Interrupt Control Register	ADIC	XXXXX000b
004Fh	UART2 Transmit Interrupt Control Register	S2TIC	XXXXX000b
0050h	UART2 Receive Interrupt Control Register	S2RIC	XXXXX000b
0051h	UART0 Transmit Interrupt Control Register	S0TIC	XXXXX000b
0052h	UART0 Receive Interrupt Control Register	S0RIC	XXXXX000b
0053h	UART1 Transmit Interrupt Control Register	S1TIC	XXXXX000b
0054h	UART1 Receive Interrupt Control Register	S1RIC	XXXXX000b
0055h	Timer A0 Interrupt Control Register	TA0IC	XXXXX000b
0056h	Timer A1 Interrupt Control Register	TA1IC	XXXXX000b
0057h	Timer A2 Interrupt Control Register	TA2IC	XXXXX000b
0058h	Timer A3 Interrupt Control Register	TA3IC	XXXXX000b
0059h	Timer A4 Interrupt Control Register	TA4IC	XXXXX000b
005Ah	Timer B0 Interrupt Control Register	TB0IC	XXXXX000b
005Bh	Timer B1 Interrupt Control Register	TB1IC	XXXXX000b
005Ch	Timer B2 Interrupt Control Register	TB2IC	XXXXX000b
005Dh	INT0 Interrupt Control Register	INT0IC	XX00X000b
005Eh	INT1 Interrupt Control Register	INT1IC	XX00X000b
005Fh	INT2 Interrupt Control Register	INT2IC	XX00X000b
0060h			
0061h			
0062h			
0063h			
0064h			
0065h			
0066h			
0067h			
0068h			
0069h			
006Ah			
006Bh			
006Ch			
006Dh			
006Eh			
006Fh			
0070h			
0071h			
0072h			
0073h			
0074h			
0075h			
0076h			
0077h			
0078h			
0079h			
007Ah			
007Bh			
007Ch			
007Dh			
007Eh			
007Fh			

NOTES:
1. The blank areas are reserved and cannot be accessed by users.

X : Nothing is mapped to this bit

Table 4.3 SFR Information (3) (1)

Address	Register	Symbol	After Reset
0080h			
0081h			
0082h			
0083h			
0084h			
0085h			
0086h			
0087h to 01AFh			
01B0h			
01B1h			
01B2h			
01B3h			
01B4h	Flash Identification Register (2)	FIDR	XXXXXX00b
01B5h	Flash Memory Control Register 1 (2)	FMR1	0X00XX0Xb
01B6h			
01B7h	Flash Memory Control Register 0 (2)	FMR0	00000001b
01B8h	Address Match Interrupt Register 2	RMAD2	00h
01B9h			00h
01BAh			XXh
01BBh	Address Match Interrupt Enable Register 2	AIER2	XXXXXX00b
01BCh	Address Match Interrupt Register 3	RMAD3	00h
01BDh			00h
01BEh			XXh
01C0h to 024Fh			
0250h			
0251h			
0252h			
0253h			
0254h			
0255h			
0256h			
0257h			
0258h			
0259h			
025Ah			
025Bh			
025Ch			
025Dh			
025Eh	Peripheral Clock Select Register	PCLKR	00000011b
025Fh			
0260h to 032Fh			
0330h			
0331h			
0332h			
0333h			
0334h			
0335h			
0336h			
0337h			
0338h			
0339h			
033Ah			
033Bh			
033Ch			
033Dh			
033Eh			
033Fh			

NOTES:
1. The blank areas are reserved and cannot be accessed by users.
2. This register is included in the flash memory version.

X : Nothing is mapped to this bit

Table 4.4 SFR Information (4) (1)

Address	Register	Symbol	After Reset
0340h	Timer B3, 4, 5 Count Start Flag	TBSR	000XXXXXb
0341h			
0342h	Timer A1-1 Register	TA11	XXh
0343h			XXh
0344h	Timer A2-1 Register	TA21	XXh
0345h			XXh
0346h	Timer A4-1 Register	TA41	XXh
0347h			XXh
0348h	Three-Phase PWM Control Register 0	INVC0	00h
0349h	Three-Phase PWM Control Register 1	INVC1	00h
034Ah	Three-Phase Output Buffer Register 0	IDB0	00h
034Bh	Three-Phase Output Buffer Register 1	IDB1	00h
034Ch	Dead Time Timer	DTT	XXh
034Dh	Timer B2 Interrupt Occurrence Frequency Set Counter	ICTB2	XXh
034Eh			
034Fh			
0350h	Timer B3 Register	TB3	XXh
0351h			XXh
0352h	Timer B4 Register	TB4	XXh
0353h			XXh
0354h	Timer B5 Register	TB5	XXh
0355h			XXh
0356h			
0357h			
0358h			
0359h			
035Ah			
035Bh	Timer B3 Mode Register	TB3MR	00XX0000b
035Ch	Timer B4 Mode Register	TB4MR	00XX0000b
035Dh	Timer B5 Mode Register	TB5MR	00XX0000b
035Eh	Interrupt Factor Select Register 2	IFSR2A	00XXXXXXb
035Fh	Interrupt Factor Select Register	IFSR	00h
0360h	SI/O3 Transmit/Receive Register	S3TRR	XXh
0361h			
0362h	SI/O3 Control Register	S3C	01000000b
0363h	SI/O3 Bit Rate Generator	S3BRG	XXh
0364h	SI/O4 Transmit/Receive Register	S4TRR	XXh
0365h			
0366h	SI/O4 Control Register	S4C	01000000b
0367h	SI/O4 Bit Rate Generator	S4BRG	XXh
0368h			
0369h			
036Ah			
036Bh			
036Ch	UART0 Special Mode Register 4	U0SMR4	00h
036Dh	UART0 Special Mode Register 3	U0SMR3	000X0X0Xb
036Eh	UART0 Special Mode Register 2	U0SMR2	X0000000b
036Fh	UART0 Special Mode Register	U0SMR	X0000000b
0370h	UART1 Special Mode Register 4	U1SMR4	00h
0371h	UART1 Special Mode Register 3	U1SMR3	000X0X0Xb
0372h	UART1 Special Mode Register 2	U1SMR2	X0000000b
0373h	UART1 Special Mode Register	U1SMR	X0000000b
0374h	UART2 Special Mode Register 4	U2SMR4	00h
0375h	UART2 Special Mode Register 3	U2SMR3	000X0X0Xb
0376h	UART2 Special Mode Register 2	U2SMR2	X0000000b
0377h	UART2 Special Mode Register	U2SMR	X0000000b
0378h	UART2 Transmit/Receive Mode Register	U2MR	00h
0379h	UART2 Bit Rate Generator	U2BRG	XXh
037Ah	UART2 Transmit Buffer Register	U2TB	XXh
037Bh			XXh
037Ch	UART2 Transmit/Receive Control Register 0	U2C0	00001000b
037Dh	UART2 Transmit/Receive Control Register 1	U2C1	00000010b
037Eh	UART2 Receive Buffer Register	U2RB	XXh
037Fh			XXh

NOTES:
1. The blank areas are reserved and cannot be accessed by users.

X : Nothing is mapped to this bit

Table 4.6 SFR Information (6) (1)

Address	Register	Symbol	After Reset
03C0h 03C1h	A/D Register 0	AD0	XXh XXh
03C2h 03C3h	A/D Register 1	AD1	XXh XXh
03C4h 03C5h	A/D Register 2	AD2	XXh XXh
03C6h 03C7h	A/D Register 3	AD3	XXh XXh
03C8h 03C9h	A/D Register 4	AD4	XXh XXh
03CAh 03CBh	A/D Register 5	AD5	XXh XXh
03CCh 03CDh	A/D Register 6	AD6	XXh XXh
03CEh 03CFh	A/D Register 7	AD7	XXh XXh
03D0h			
03D1h			
03D2h			
03D3h			
03D4h	A/D Control Register 2	ADCON2	00h
03D5h			
03D6h	A/D Control Register 0	ADCON0	00000XXXb
03D7h	A/D Control Register 1	ADCON1	00h
03D8h	D/A Register 0	DA0	00h
03D9h			
03DAh	D/A Register 1	DA1	00h
03DBh			
03DCh	D/A Control Register	DACON	00h
03DDh			
03DEh	Port P14 Control Register (3)	PC14	XX00XXXXb
03DFh	Pull-Up Control Register 3 (3)	PUR3	00h
03E0h	Port P0 Register	P0	XXh
03E1h	Port P1 Register	P1	XXh
03E2h	Port P0 Direction Register	PD0	00h
03E3h	Port P1 Direction Register	PD1	00h
03E4h	Port P2 Register	P2	XXh
03E5h	Port P3 Register	P3	XXh
03E6h	Port P2 Direction Register	PD2	00h
03E7h	Port P3 Direction Register	PD3	00h
03E8h	Port P4 Register	P4	XXh
03E9h	Port P5 Register	P5	XXh
03EAh	Port P4 Direction Register	PD4	00h
03EBh	Port P5 Direction Register	PD5	00h
03ECh	Port P6 Register	P6	XXh
03EDh	Port P7 Register	P7	XXh
03EEh	Port P6 Direction Register	PD6	00h
03EFh	Port P7 Direction Register	PD7	00h
03F0h	Port P8 Register	P8	XXh
03F1h	Port P9 Register	P9	XXh
03F2h	Port P8 Direction Register	PD8	00X00000b
03F3h	Port P9 Direction Register	PD9	00h
03F4h	Port P10 Register	P10	XXh
03F5h	Port P11 Register (3)	P11	XXh
03F6h	Port P10 Direction Register	PD10	00h
03F7h	Port P11 Direction Register (3)	PD11	00h
03F8h	Port P12 Register (3)	P12	XXh
03F9h	Port P13 Register (3)	P13	XXh
03FAh	Port P12 Direction Register (3)	PD12	00h
03FBh	Port P13 Direction Register (3)	PD13	00h
03FCh	Pull-Up Control Register 0	PUR0	00h
03FDh	Pull-Up Control Register 1	PUR1	00000000b (2) 00000010b (2)
03FEh	Pull-Up Control Register 2	PUR2	00h
03FFh	Port Control Register	PCR	00h

NOTES:
1. The blank areas are reserved and cannot be accessed by users.
2. At hardware reset 1 or hardware reset 2, the register is as follows:
   - "00000000b" where "L" is inputted to the CNVSS pin
   - "00000010b" where "H" is inputted to the CNVSS pin

   At software reset, watchdog timer reset and oscillation stop detection reset, the register is as follows:
   - "00000000b" where the PM01 to PM00 bits in the PM0 register are "00b" (single-chip mode).
   - "00000010b" where the PM01 to PM00 bits in the PM0 register are "01b" (memory expansion mode) or "11b" (microprocessor mode).
3. These registers do not exist in M16C/62P (80-pin version), and M16C/62PT (80-pin version).

X : Nothing is mapped to this bit

Table 5.4 A/D Conversion Characteristics (1)

Symbol	Parameter		Measuring Condition		Standard			Unit
					Min.	Typ.	Max.	
–	Resolution		$V_{REF}=V_{CC1}$				10	Bits
INL	Integral Non-Linearity Error	10bit	$V_{REF}=V_{CC1}=5V$	AN0 to AN7 input, AN0_0 to AN0_7 input, AN2_0 to AN2_7 input, ANEX0, ANEX1 input			±3	LSB
				External operation amp connection mode			±7	LSB
			$V_{REF}=V_{CC1}=3.3V$	AN0 to AN7 input, AN0_0 to AN0_7 input, AN2_0 to AN2_7 input, ANEX0, ANEX1 input			±5	LSB
				External operation amp connection mode			±7	LSB
		8bit	$V_{REF}=V_{CC1}$=5V, 3.3V				±2	LSB
–	Absolute Accuracy	10bit	$V_{REF}=V_{CC1}=5V$	AN0 to AN7 input, AN0_0 to AN0_7 input, AN2_0 to AN2_7 input, ANEX0, ANEX1 input			±3	LSB
				External operation amp connection mode			±7	LSB
			$V_{REF}=V_{CC1}=3.3V$	AN0 to AN7 input, AN0_0 to AN0_7 input, AN2_0 to AN2_7 input, ANEX0, ANEX1 input			±5	LSB
				External operation amp connection mode			±7	LSB
		8bit	$V_{REF}=V_{CC1}$=5V, 3.3V				±2	LSB
–	Tolerance Level Impedance					3		kΩ
DNL	Differential Non-Linearity Error						±1	LSB
–	Offset Error						±3	LSB
–	Gain Error						±3	LSB
R_{LADDER}	Ladder Resistance		$V_{REF}=V_{CC1}$		10		40	kΩ
t_{CONV}	10-bit Conversion Time, Sample & Hold Available		$V_{REF}=V_{CC1}$=5V, ϕAD=12MHz		2.75			µs
t_{CONV}	8-bit Conversion Time, Sample & Hold Available		$V_{REF}=V_{CC1}$=5V, ϕAD=12MHz		2.33			µs
t_{SAMP}	Sampling Time				0.25			µs
V_{REF}	Reference Voltage				2.0		V_{CC1}	V
V_{IA}	Analog Input Voltage				0		V_{REF}	V

NOTES:
1. Referenced to $V_{CC1}=AV_{CC}=V_{REF}$=3.3 to 5.5V, $V_{SS}=AV_{SS}$=0V at T_{opr} = −20 to 85°C / −40 to 85°C unless otherwise specified.
2. If $V_{CC1} > V_{CC2}$, do not use AN0_0 to AN0_7 and AN2_0 to AN2_7 as analog input pins.
3. ϕAD frequency must be 12 MHz or less. And divide the fAD if V_{CC1} is less than 4.0V, and ϕAD frequency into 10 MHz or less.
4. When sample & hold is disabled, ϕAD frequency must be 250 kHz or more, in addition to the limitation in Note 3.
   When sample & hold is enabled, ϕAD frequency must be 1MHz or more, in addition to the limitation in Note 3.

Table 5.9 Low Voltage Detection Circuit Electrical Characteristics

Symbol	Parameter	Measuring Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{det4}	Low Voltage Detection Voltage (1)	V_{CC1}=0.8V to 5.5V	3.3	3.8	4.4	V
V_{det3}	Reset Level Detection Voltage (1, 2)		2.2	2.8	3.6	V
V_{det4}-V_{det3}	Electric potential difference of Low Voltage Detection and Reset Level Detection		0.3			V
V_{det3s}	Low Voltage Reset Retention Voltage				0.8	V
V_{det3r}	Low Voltage Reset Release Voltage (3)		2.2	2.9	4.0	V

NOTES:
1. $V_{det4} > V_{det3}$.
2. Where reset level detection voltage is less than 2.7 V, if the supply power voltage is greater than the reset level detection voltage, the microcomputer operates with f(BCLK) ≤ 10MHz.
3. $V_{det3r} > V_{det3}$ is not guaranteed.
4. The voltage detection circuit is designed to use when VCC1 is set to 5V.

Table 5.10 Power Supply Circuit Timing Characteristics

Symbol	Parameter	Measuring Condition	Standard			Unit
			Min.	Typ.	Max.	
$t_{d(P-R)}$	Time for Internal Power Supply Stabilization During Powering-On	V_{CC1}=2.7V to 5.5V			2	ms
$t_{d(R-S)}$	STOP Release Time				150	µs
$t_{d(W-S)}$	Low Power Dissipation Mode Wait Mode Release Time				150	µs
$t_{d(S-R)}$	Brown-out Detection Reset (Hardware Reset 2) Release Wait Time	V_{CC1}=V_{det3r} to 5.5V		6 (1)	20	ms
$t_{d(E-A)}$	Low Voltage Detection Circuit Operation Start Time	V_{CC1}=2.7V to 5.5V			20	µs

NOTES:
1. When V_{CC1} = 5V.

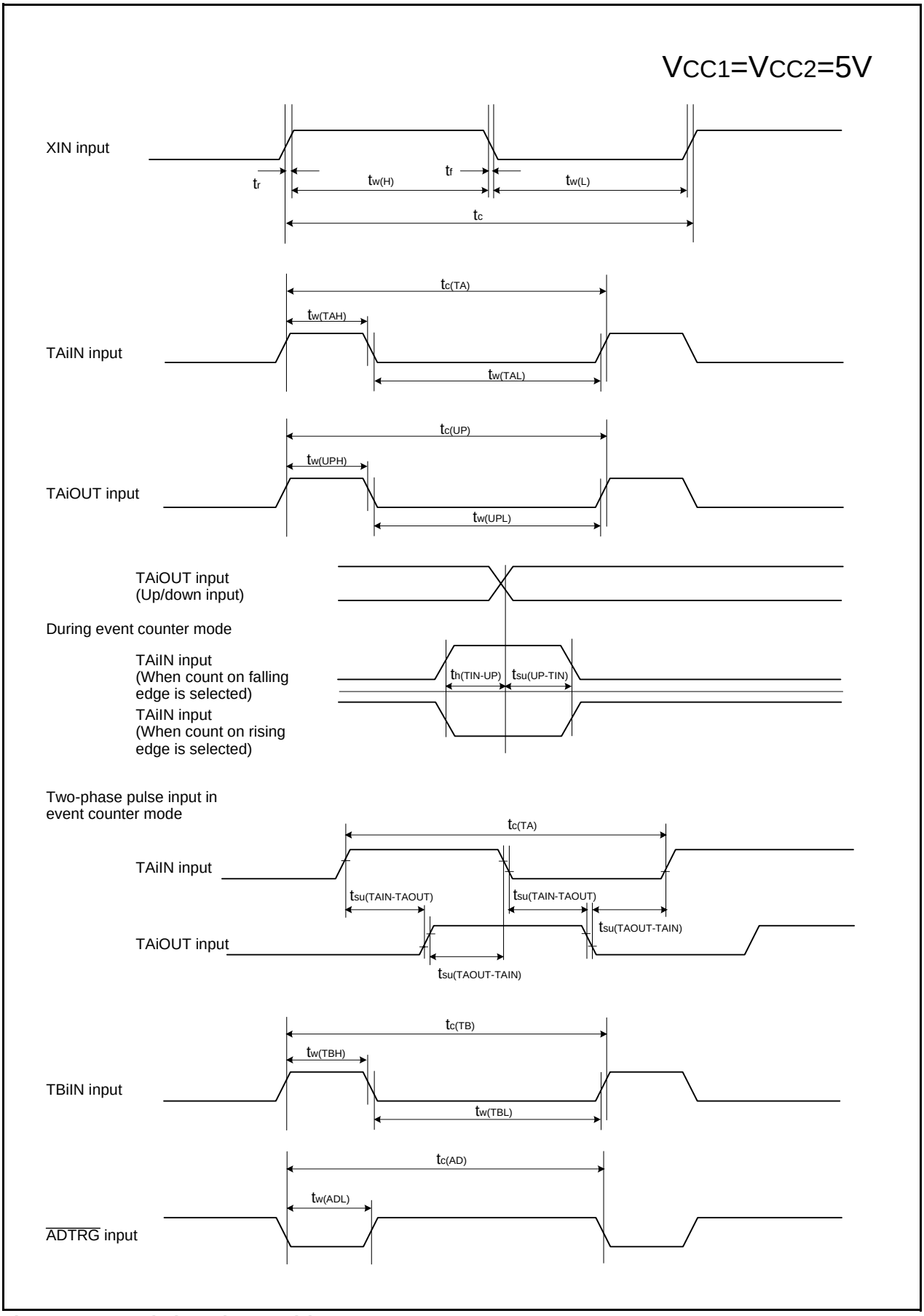
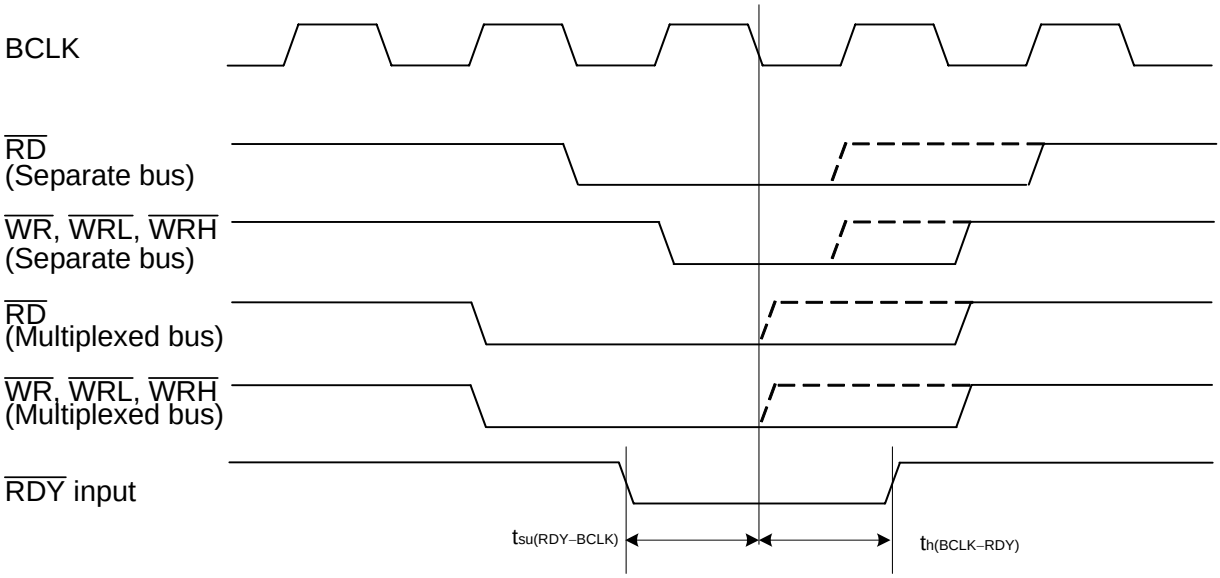


Figure 5.3 Timing Diagram (1)

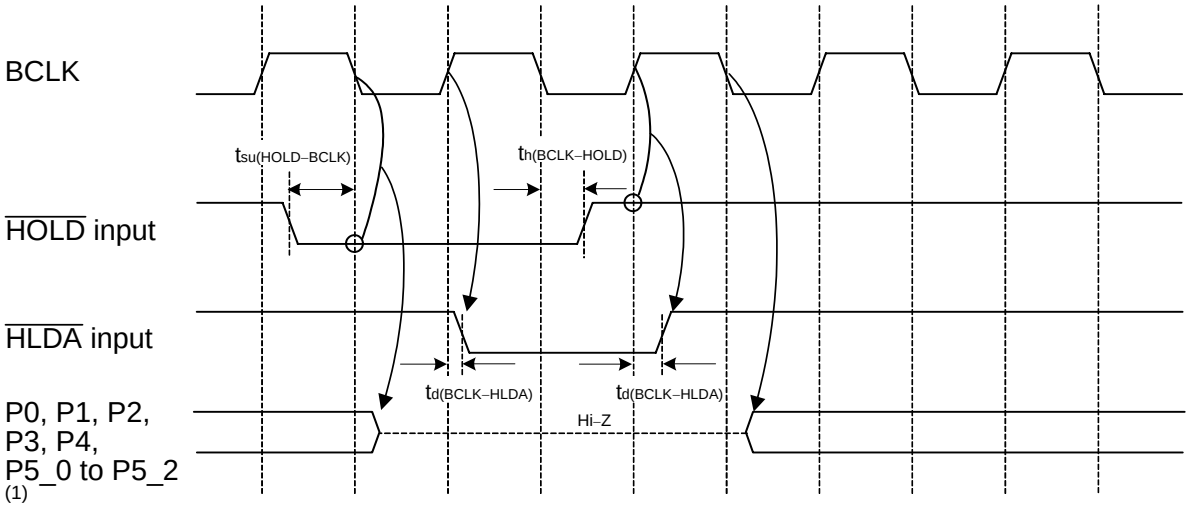
$V_{CC1}=V_{CC2}=5V$

Memory Expansion Mode, Microprocessor Mode

(Effective for setting with wait**)**



(Common to setting with wait and setting without wait**)**



NOTES:

1. These pins are set to high-impedance regardless of the input level of the BYTE pin, PM06 bit in PM0 register and PM11 bit in PM1 register.

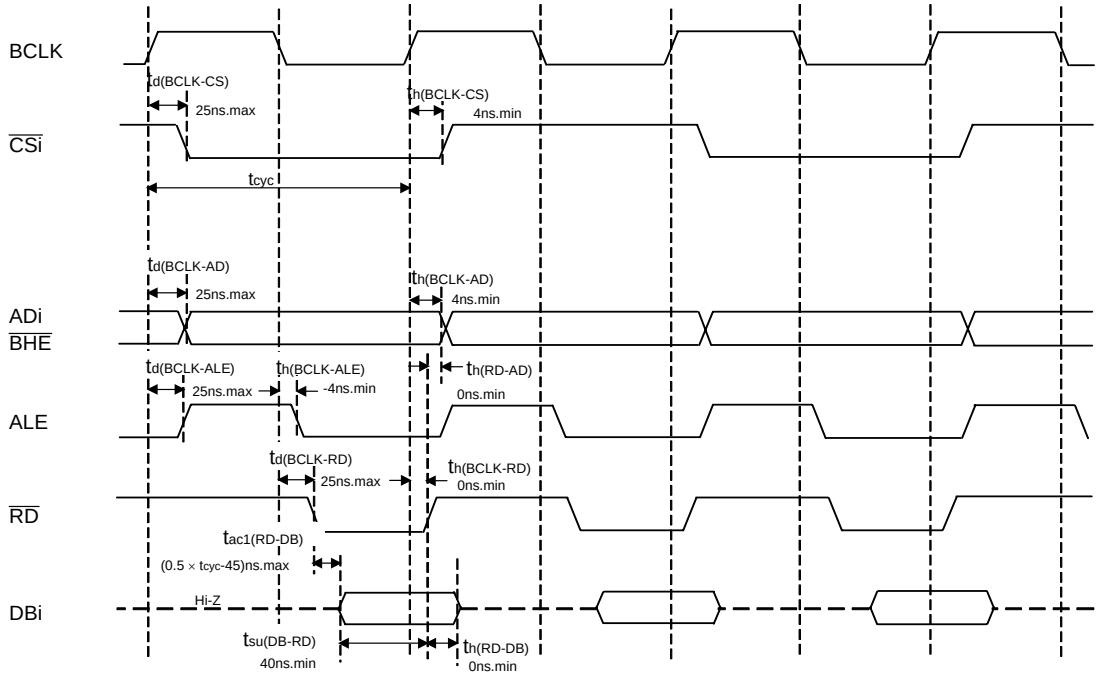
· Measuring conditions :
· $V_{CC1}=V_{CC2}=5V$
· Input timing voltage : Determined with $V_{IL}=1.0V$, $V_{IH}=4.0V$
· Output timing voltage : Determined with $V_{OL}=2.5V$, $V_{OH}=2.5V$

Figure 5.5 Timing Diagram (3)

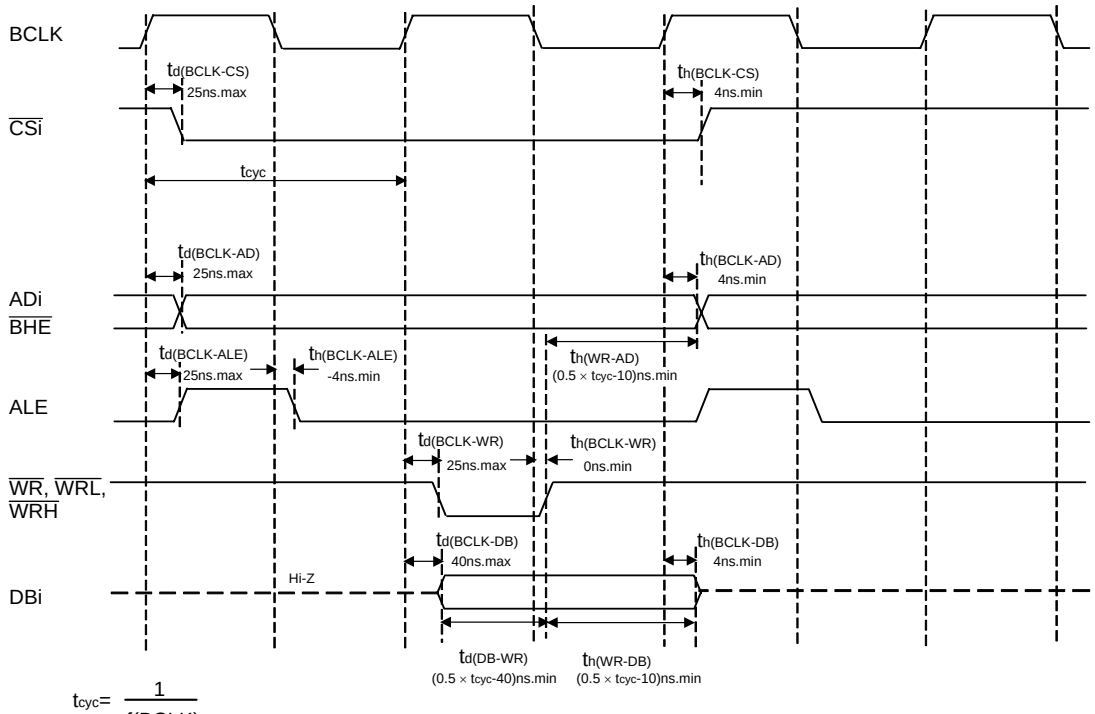
Memory Expansion Mode, Microprocessor Mode
(For setting with no wait**)**

$V_{CC1}=V_{CC2}=5V$

Read timing



Write timing



$$t_{cyc}=\frac{1}{f(BCLK)}$$

Measuring conditions
· $V_{CC1}=V_{CC2}=5V$
· Input timing voltage : $V_{IL}=0.8V$, $V_{IH}=2.0V$
· Output timing voltage : $V_{OL}=0.4V$, $V_{OH}=2.4V$

Figure 5.6 Timing Diagram (4)

$V_{CC1}=V_{CC2}=3V$

Timing Requirements
(V_{CC1} = V_{CC2} = 3V, V_{SS} = 0V, at T_{opr} = –20 to 85°C / –40 to 85°C unless otherwise specified)

Table 5.40 Timer B Input (Counter Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN Input Cycle Time (counted on one edge)	150		ns
$t_{w(TBH)}$	TBiIN Input HIGH Pulse Width (counted on one edge)	60		ns
$t_{w(TBL)}$	TBiIN Input LOW Pulse Width (counted on one edge)	60		ns
$t_{c(TB)}$	TBiIN Input Cycle Time (counted on both edges)	300		ns
$t_{w(TBH)}$	TBiIN Input HIGH Pulse Width (counted on both edges)	120		ns
$t_{w(TBL)}$	TBiIN Input LOW Pulse Width (counted on both edges)	120		ns

Table 5.41 Timer B Input (Pulse Period Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN Input Cycle Time	600		ns
$t_{w(TBH)}$	TBiIN Input HIGH Pulse Width	300		ns
$t_{w(TBL)}$	TBiIN Input LOW Pulse Width	300		ns

Table 5.42 Timer B Input (Pulse Width Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN Input Cycle Time	600		ns
$t_{w(TBH)}$	TBiIN Input HIGH Pulse Width	300		ns
$t_{w(TBL)}$	TBiIN Input LOW Pulse Width	300		ns

Table 5.43 A/D Trigger Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(AD)}$	$\overline{\text{ADTRG}}$ Input Cycle Time	1500		ns
$t_{w(ADL)}$	$\overline{\text{ADTRG}}$ Input LOW Pulse Width	200		ns

Table 5.44 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi Input Cycle Time	300		ns
$t_{w(CKH)}$	CLKi Input HIGH Pulse Width	150		ns
$t_{w(CKL)}$	CLKi Input LOW Pulse Width	150		ns
$t_{d(C-Q)}$	TXDi Output Delay Time		160	ns
$t_{h(C-Q)}$	TXDi Hold Time	0		ns
$t_{su(D-C)}$	RXDi Input Setup Time	100		ns
$t_{h(C-D)}$	RXDi Input Hold Time	90		ns

Table 5.45 External Interrupt $\overline{\text{INTi}}$ Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(INH)}$	$\overline{\text{INTi}}$ Input HIGH Pulse Width	380		ns
$t_{w(INL)}$	$\overline{\text{INTi}}$ Input LOW Pulse Width	380		ns

$V_{CC1}=V_{CC2}=3V$

Switching Characteristics
(V_{CC1} = V_{CC2} = 5V, V_{SS} = 0V, at T_{opr} = –20 to 85°C / –40 to 85°C unless otherwise specified)

Table 5.48 Memory Expansion and Microprocessor Modes (for 2- to 3-wait setting, external area access and multiplex bus selection)

Symbol	Parameter		Standard		Unit
			Min.	Max.	
$t_{d(BCLK-AD)}$	Address Output Delay Time	See **Figure 5.12**		50	ns
$t_{h(BCLK-AD)}$	Address Output Hold Time (in relation to BCLK)		4		ns
$t_{h(RD-AD)}$	Address Output Hold Time (in relation to RD)		(NOTE 1)		ns
$t_{h(WR-AD)}$	Address Output Hold Time (in relation to WR)		(NOTE 1)		ns
$t_{d(BCLK-CS)}$	Chip Select Output Delay Time			50	ns
$t_{h(BCLK-CS)}$	Chip Select Output Hold Time (in relation to BCLK)		4		ns
$t_{h(RD-CS)}$	Chip Select Output Hold Time (in relation to RD)		(NOTE 1)		ns
$t_{h(WR-CS)}$	Chip Select Output Hold Time (in relation to WR)		(NOTE 1)		ns
$t_{d(BCLK-RD)}$	RD Signal Output Delay Time			40	ns
$t_{h(BCLK-RD)}$	RD Signal Output Hold Time		0		ns
$t_{d(BCLK-WR)}$	WR Signal Output Delay Time			40	ns
$t_{h(BCLK-WR)}$	WR Signal Output Hold Time		0		ns
$t_{d(BCLK-DB)}$	Data Output Delay Time (in relation to BCLK)			50	ns
$t_{h(BCLK-DB)}$	Data Output Hold Time (in relation to BCLK)		4		ns
$t_{d(DB-WR)}$	Data Output Delay Time (in relation to WR)		(NOTE 2)		ns
$t_{h(WR-DB)}$	Data Output Hold Time (in relation to WR)		(NOTE 1)		ns
$t_{d(BCLK-HLDA)}$	HLDA Output Delay Time			40	ns
$t_{d(BCLK-ALE)}$	ALE Signal Output Delay Time (in relation to BCLK)			25	ns
$t_{h(BCLK-ALE)}$	ALE Signal Output Hold Time (in relation to BCLK)		–4		ns
$t_{d(AD-ALE)}$	ALE Signal Output Delay Time (in relation to Address)		(NOTE 3)		ns
$t_{h(AD-ALE)}$	ALE Signal Output Hold Time (in relation to Address)		(NOTE 4)		ns
$t_{d(AD-RD)}$	RD Signal Output Delay From the End of Address		0		ns
$t_{d(AD-WR)}$	WR Signal Output Delay From the End of Address		0		ns
$t_{dz(RD-AD)}$	Address Output Floating Start Time			8	ns

NOTES:
1. Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f(BCLK)} - 10[ns]$$

2. Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f(BCLK)} - 50[ns]$$ n is “2” for 2-wait setting, “3” for 3-wait setting.

3. Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f(BCLK)} - 40[ns]$$

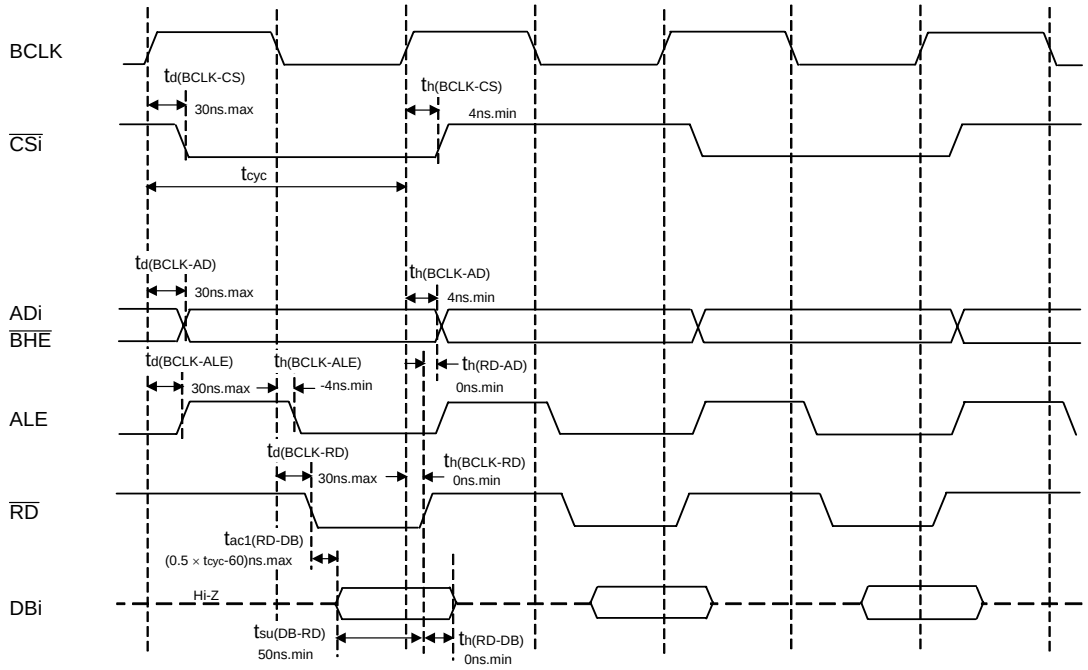
4. Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f(BCLK)} - 15[ns]$$

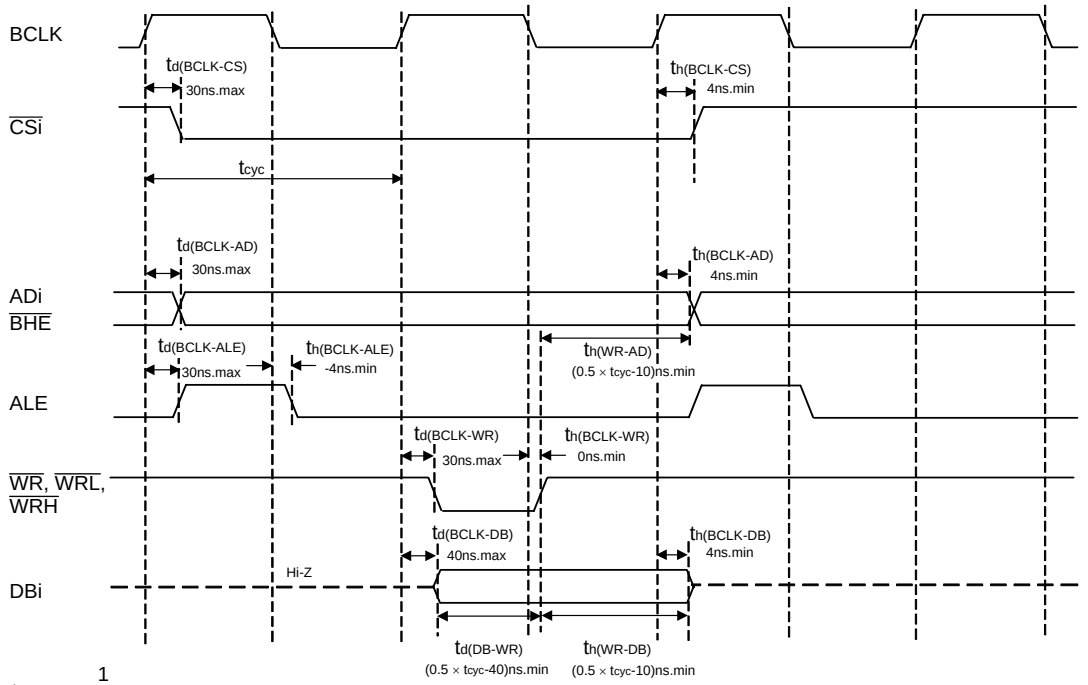
Memory Expansion Mode, Microprocessor Mode
(for setting with no wait**)**

$V_{CC1}=V_{CC2}=3V$

Read timing



Write timing



$$t_{cyc}=\frac{1}{f(BCLK)}$$

Measuring conditions
· $V_{CC1}=V_{CC2}=3V$
· Input timing voltage : $V_{IL}=0.6V$, $V_{IH}=2.4V$
· Output timing voltage : $V_{OL}=1.5V$, $V_{OH}=1.5V$

Figure 5.16 Timing Diagram (4)

Table 5.53 Flash Memory Version Electrical Characteristics (1) for 100 cycle products (B, U)

Symbol	Parameter		Standard			Unit
			Min.	Typ.	Max.	
–	Program and Erase Endurance (3)		100			cycle
–	Word Program Time (V_{CC1}=5.0V)			25	200	µs
–	Lock Bit Program Time			25	200	µs
–	Block Erase Time (V_{CC1}=5.0V)	4-Kbyte block	4	0.3	4	s
–		8-Kbyte block		0.3	4	s
–		32-Kbyte block		0.5	4	s
–		64-Kbyte block		0.8	4	s
–	Erase All Unlocked Blocks Time (2)				4×n	s
t_{PS}	Flash Memory Circuit Stabilization Wait Time				15	µs
–	Data Hold Time (5)		20			year

Table 5.54 Flash Memory Version Electrical Characteristics (6) for 10,000 cycle products (B7, U7) (Block A and Block 1 (7))

Symbol	Parameter		Standard			Unit
			Min.	Typ.	Max.	
–	Program and Erase Endurance (3, 8, 9)		10,000 (4)			cycle
–	Word Program Time (V_{CC}1=5.0V)			25		µs
–	Lock Bit Program Time			25		µs
–	Block Erase Time (V_{CC1}=5.0V)	4-Kbyte block	4	0.3		s
t_{PS}	Flash Memory Circuit Stabilization Wait Time				15	µs
–	Data Hold Time (5)		20			year

NOTES:
1. Referenced to V_{CC1}=4.5 to 5.5V at T_{opr} = 0 to 60 °C unless otherwise specified.
2. n denotes the number of block erases.
3. Program and Erase Endurance refers to the number of times a block erase can be performed.
   If the program and erase endurance is n (n=100, 1,000, or 10,000), each block can be erased n times.
   For example, if a 4 Kbytes block A is erased after writing 1 word data 2,048 times, each to a different address, this counts as one program and erase endurance. Data cannot be written to the same address more than once without erasing the block. (Rewrite prohibited)
4. Maximum number of E/W cycles for which operation is guaranteed.
5. Ta (ambient temperature)=55 °C. As to the data hold time except Ta=55 °C, please contact Renesas Technology Corp. or an authorized Renesas Technology Corp. product distributor.
6. Referenced to V_{CC1} = 4.5 to 5.5V at T_{opr} = –40 to 85 °C (B7, U7 (T version)) / –40 to 125 °C (B7, U7 (V version)) unless otherwise specified.
7. Table 5.54 applies for block A or block 1 program and erase endurance > 1,000. Otherwise, use Table 5.53.
8. To reduce the number of program and erase endurance when working with systems requiring numerous rewrites, write to unused word addresses within the block instead of rewrite. Erase block only after all possible addresses are used. For example, an 8-word program can be written 256 times maximum before erase becomes necessary.
   Maintaining an equal number of erasure between block A and block 1 will also improve efficiency. It is important to track the total number of times erasure is used.
9. Should erase error occur during block erase, attempt to execute clear status register command, then block erase command at least three times until erase error disappears.
10. Set the PM17 bit in the PM1 register to “1” (wait state) when executing more than 100 times rewrites (B7 and U7).
11. Customers desiring E/W failure rate information should contact their Renesas technical support representative.

Table 5.55 Flash Memory Version Program/Erase Voltage and Read Operation Voltage Characteristics (at T_{opr} = 0 to 60 °C(B, U), T_{opr} = –40 to 85 °C (B7, U7 (T version)) / –40 to 125 °C (B7, U7 (V version))

Flash Program, Erase Voltage	Flash Read Operation Voltage
V_{CC1} = 5.0 V ± 0.5 V	V_{CC1}=4.0 to 5.5 V

$V_{CC1}=V_{CC2}=5V$

Timing Requirements
(V_{CC1} = V_{CC2} = 5V, V_{SS} = 0V, at T_{opr} = –40 to 85°C (T version) / –40 to 125°C (V version) unless otherwise specified)

Table 5.59 External Clock Input (XIN input)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
t_c	External Clock Input Cycle Time	62.5		ns
$t_{w(H)}$	External Clock Input HIGH Pulse Width	25		ns
$t_{w(L)}$	External Clock Input LOW Pulse Width	25		ns
t_r	External Clock Rise Time		15	ns
t_f	External Clock Fall Time		15	ns

V_{CC1}=V_{CC2}=5V

Timing Requirements
(V_{CC1} = V_{CC2} = 5V, V_{SS} = 0V, at T_{opr} = –40 to 85°C (T version) / –40 to 125°C (V version) unless otherwise specified)

Table 5.66 Timer B Input (Counter Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN Input Cycle Time (counted on one edge)	100		ns
$t_{w(TBH)}$	TBiIN Input HIGH Pulse Width (counted on one edge)	40		ns
$t_{w(TBL)}$	TBiIN Input LOW Pulse Width (counted on one edge)	40		ns
$t_{c(TB)}$	TBiIN Input Cycle Time (counted on both edges)	200		ns
$t_{w(TBH)}$	TBiIN Input HIGH Pulse Width (counted on both edges)	80		ns
$t_{w(TBL)}$	TBiIN Input LOW Pulse Width (counted on both edges)	80		ns

Table 5.67 Timer B Input (Pulse Period Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN Input Cycle Time	400		ns
$t_{w(TBH)}$	TBiIN Input HIGH Pulse Width	200		ns
$t_{w(TBL)}$	TBiIN Input LOW Pulse Width	200		ns

Table 5.68 Timer B Input (Pulse Width Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN Input Cycle Time	400		ns
$t_{w(TBH)}$	TBiIN Input HIGH Pulse Width	200		ns
$t_{w(TBL)}$	TBiIN Input LOW Pulse Width	200		ns

Table 5.69 A/D Trigger Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(AD)}$	$\overline{\text{ADTRG}}$ Input Cycle Time	1000		ns
$t_{w(ADL)}$	$\overline{\text{ADTRG}}$ input LOW Pulse Width	125		ns

Table 5.70 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi Input Cycle Time	200		ns
$t_{w(CKH)}$	CLKi Input HIGH Pulse Width	100		ns
$t_{w(CKL)}$	CLKi Input LOW Pulse Width	100		ns
$t_{d(C-Q)}$	TXDi Output Delay Time		80	ns
$t_{h(C-Q)}$	TXDi Hold Time	0		ns
$t_{su(D-C)}$	RXDi Input Setup Time	70		ns
$t_{h(C-D)}$	RXDi Input Hold Time	90		ns

Table 5.71 External Interrupt $\overline{\text{INTi}}$ Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(INH)}$	$\overline{\text{INTi}}$ Input HIGH Pulse Width	250		ns
$t_{w(INL)}$	$\overline{\text{INTi}}$ Input LOW Pulse Width	250		ns

$V_{CC1}=V_{CC2}=5V$

Switching Characteristics
(V_{CC1} = V_{CC2} = 5V, V_{SS} = 0V, at T_{opr} = –40 to 85°C (T version) / –40 to 125°C (V version) unless otherwise specified)

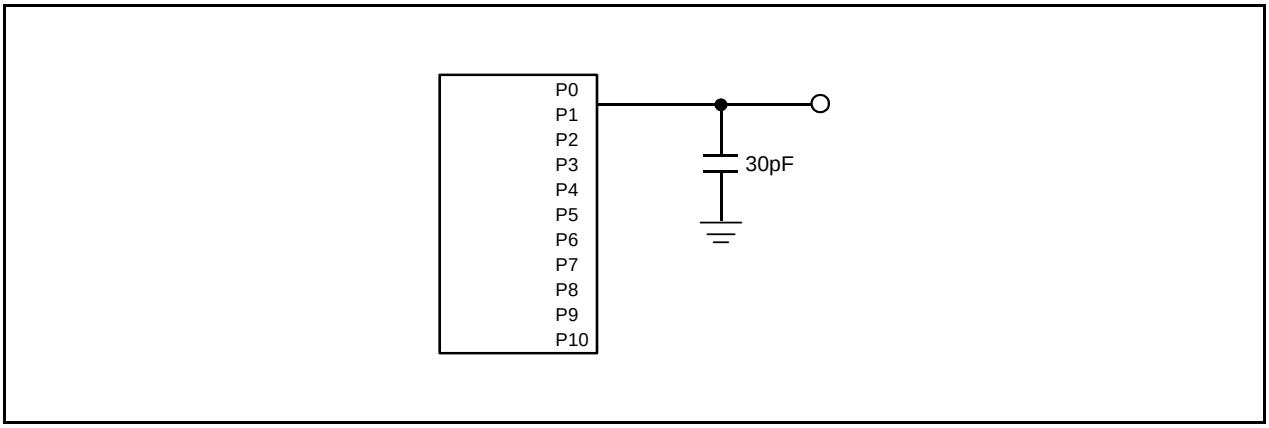


Figure 5.23 Ports P0 to P10 Measurement Circuit