Renesas Electronics America Inc - M30622SPFP#U5C Datasheet

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	M16C/60
Core Size	16-Bit
Speed	24MHz
Connectivity	I²C, IEBus, UART/USART
Peripherals	DMA, WDT
Number of I/O	50
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 26x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-BQFP
Supplier Device Package	100-QFP (14x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/m30622spfp-u5c

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1. Overview

The M16C/62P Group (M16C/62P, M16C/62PT) of single-chip microcomputers are built using the high performance silicon gate CMOS process using a M16C/60 Series CPU core and are packaged in a 80-pin, 100-pin and 128-pin plastic molded QFP. These single-chip microcomputers operate using sophisticated instructions featuring a high level of instruction efficiency. With 1M bytes of address space, they are capable of executing instructions at high speed. In addition, this microcomputer contains a multiplier and DMAC which combined with fast instruction processing capability, makes it suitable for control of various OA, communication, and industrial equipment which requires high-speed arithmetic/logic operations.

1.1 Applications

Audio, cameras, television, home appliance, office/communications/portable/industrial equipment, automobile, etc.

Specifications written in this manual are believed to be accurate, but are not guaranteed to be entirely free of error. Specifications in this manual may be changed for functional or performance improvements. Please make sure your manual is the latest edition.

Table 1.2 Performance Outline of M16C/62P Group (M16C/62P, M16C/62PT)(100-pin version)

	Item	Performance	
		M16C/62P	M16C/62PT(4)
CPU	Number of Basic Instructions	91 instructions	
	Minimum Instruction Execution Time	41.7ns(f(BCLK)=24MHz, VCC1=3.3 to 5.5V) 100ns(f(BCLK)=10MHz, VCC1=2.7 to 5.5V)	41.7ns(f(BCLK)=24MHz, VCC1=4.0 to 5.5V)
	Operating Mode	Single-chip, memory expansion and microprocessor mode	Single-chip
	Address Space	1 Mbyte (Available to 4 Mbytes by memory space expansion function)	1 Mbyte
	Memory Capacity	See **Table 1.4 to 1.7 Product List**	
Peripheral Function	Port	Input/Output : 87 pins, Input : 1 pin	
	Multifunction Timer	Timer A : 16 bits x 5 channels, Timer B : 16 bits x 6 channels, Three phase motor control circuit	
	Serial Interface	3 channels Clock synchronous, UART, I2C bus(1), IEBus(2) 2 channels Clock synchronous	
	A/D Converter	10-bit A/D converter: 1 circuit, 26 channels	
	D/A Converter	8 bits x 2 channels	
	DMAC	2 channels	
	CRC Calculation Circuit	CCITT-CRC	
	Watchdog Timer	15 bits x 1 channel (with prescaler)	
	Interrupt	Internal: 29 sources, External: 8 sources, Software: 4 sources, Priority level: 7 levels	
	Clock Generation Circuit	4 circuits Main clock generation circuit (*), Subclock generation circuit (*), On-chip oscillator, PLL synthesizer (*)Equipped with a built-in feedback resistor.	
	Oscillation Stop Detection Function	Stop detection of main clock oscillation, re-oscillation detection function	
	Voltage Detection Circuit	Available (option (5))	Absent
Electric Characteristics	Supply Voltage	VCC1=3.0 to 5.5 V, VCC2=2.7V to VCC1 (f(BCLK=24MHz) VCC1=2.7 to 5.5 V, VCC2=2.7V to VCC1 (f(BCLK=10MHz)	VCC1=VCC2=4.0 to 5.5V (f(BCLK=24MHz)
	Power Consumption	14 mA (VCC1=VCC2=5V, f(BCLK)=24MHz) 8 mA (VCC1=VCC2=3V, f(BCLK)=10MHz) 1.8µA (VCC1=VCC2=3V, f(XCIN)=32kHz, wait mode) 0.7µA (VCC1=VCC2=3V, stop mode)	14 mA (VCC1=VCC2=5V, f(BCLK)=24MHz) 2.0µA (VCC1=VCC2=5V, f(XCIN)=32kHz, wait mode) 0.8µA (VCC1=VCC2=5V, stop mode)
Flash memory version	Program/Erase Supply Voltage	3.3±0.3 V or 5.0±0.5 V	5.0±0.5 V
	Program and Erase Endurance	100 times (all area) or 1,000 times (user ROM area without block A and block 1) / 10,000 times (block A, block 1) (3)	
Operating Ambient Temperature		-20 to 85°C, -40 to 85°C (3)	T version : -40 to 85°C V version : -40 to 125°C
Package		100-pin plastic mold QFP, LQFP	

NOTES:
1. I2C bus is a registered trademark of Koninklijke Philips Electronics N. V.
2. IEBus is a registered trademark of NEC Electronics Corporation.
3. See **Table 1.8 and 1.9 Product Code** for the program and erase endurance, and operating ambient temperature.
   In addition 1,000 times/10,000 times are under development as of Jul., 2005. Please inquire about a release schedule.
4. Use the M16C/62PT on VCC1=VCC2
5. All options are on request basis.

Table 1.11 Pin Characteristics for 128-Pin Package (2)

Pin No.	Control Pin	Port	Interrupt Pin	Timer Pin	UART Pin	Analog Pin	Bus Control Pin
51		P5_6					ALE
52		P5_5					$\overline{\text{HOLD}}$
53		P5_4					$\overline{\text{HLDA}}$
54		P13_3					
55		P13_2					
56		P13_1					
57		P13_0					
58		P5_3					BCLK
59		P5_2					$\overline{\text{RD}}$
60		P5_1					$\overline{\text{WRH}}$/$\overline{\text{BHE}}$
61		P5_0					$\overline{\text{WRL}}$/$\overline{\text{WR}}$
62		P12_7					
63		P12_6					
64		P12_5					
65		P4_7					$\overline{\text{CS3}}$
66		P4_6					$\overline{\text{CS2}}$
67		P4_5					$\overline{\text{CS1}}$
68		P4_4					$\overline{\text{CS0}}$
69		P4_3					A19
70		P4_2					A18
71		P4_1					A17
72		P4_0					A16
73		P3_7					A15
74		P3_6					A14
75		P3_5					A13
76		P3_4					A12
77		P3_3					A11
78		P3_2					A10
79		P3_1					A9
80		P12_4					
81		P12_3					
82		P12_2					
83		P12_1					
84		P12_0					
85	VCC2						
86		P3_0					A8(/-/D7)
87	VSS						
88		P2_7				AN2_7	A7(/D7/D6)
89		P2_6				AN2_6	A6(/D6/D5)
90		P2_5				AN2_5	A5(/D5/D4)
91		P2_4				AN2_4	A4(/D4/D3)
92		P2_3				AN2_3	A3(/D3/D2)
93		P2_2				AN2_2	A2(/D2/D1)
94		P2_1				AN2_1	A1(/D1/D0)
95		P2_0				AN2_0	A0(/D0/-)
96		P1_7	$\overline{\text{INT5}}$				D15
97		P1_6	$\overline{\text{INT4}}$				D14
98		P1_5	$\overline{\text{INT3}}$				D13
99		P1_4					D12
100		P1_3					D11

Table 1.12 Pin Characteristics for 128-Pin Package (3)

Pin No.	Control Pin	Port	Interrupt Pin	Timer Pin	UART Pin	Analog Pin	Bus Control Pin
101		P1_2					D10
102		P1_1					D9
103		P1_0					D8
104		P0_7				AN0_7	D7
105		P0_6				AN0_6	D6
106		P0_5				AN0_5	D5
107		P0_4				AN0_4	D4
108		P0_3				AN0_3	D3
109		P0_2				AN0_2	D2
110		P0_1				AN0_1	D1
111		P0_0				AN0_0	D0
112		P11_7					
113		P11_6					
114		P11_5					
115		P11_4					
116		P11_3					
117		P11_2					
118		P11_1					
119		P11_0					
120		P10_7	$\overline{KI3}$			AN7	
121		P10_6	$\overline{KI2}$			AN6	
122		P10_5	$\overline{KI1}$			AN5	
123		P10_4	$\overline{KI0}$			AN4	
124		P10_3				AN3	
125		P10_2				AN2	
126		P10_1				AN1	
127	AVSS						
128		P10_0				AN0	

2.2 Address Registers (A0 and A1)

The register A0 consists of 16 bits, and is used for address register indirect addressing and address register relative addressing. They also are used for transfers and logic/logic operations. A1 is the same as A0.
In some instructions, registers A1 and A0 can be combined for use as a 32-bit address register (A1A0).

2.3 Frame Base Register (FB)

FB is configured with 16 bits, and is used for FB relative addressing.

2.4 Interrupt Table Register (INTB)

INTB is configured with 20 bits, indicating the start address of an interrupt vector table.

2.5 Program Counter (PC)

PC is configured with 20 bits, indicating the address of an instruction to be executed.

2.6 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

Stack pointer (SP) comes in two types: USP and ISP, each configured with 16 bits.
Your desired type of stack pointer (USP or ISP) can be selected by the U flag of FLG.

2.7 Static Base Register (SB)

SB is configured with 16 bits, and is used for SB relative addressing.

2.8 Flag Register (FLG)

FLG consists of 11 bits, indicating the CPU status.

2.8.1 Carry Flag (C Flag)

This flag retains a carry, borrow, or shift-out bit that has occurred in the arithmetic/logic unit.

2.8.2 Debug Flag (D Flag)

The D flag is used exclusively for debugging purpose. During normal use, it must be set to “0”.

2.8.3 Zero Flag (Z Flag)

This flag is set to “1” when an arithmetic operation resulted in 0; otherwise, it is “0”.

2.8.4 Sign Flag (S Flag)

This flag is set to “1” when an arithmetic operation resulted in a negative value; otherwise, it is “0”.

2.8.5 Register Bank Select Flag (B Flag)

Register bank 0 is selected when this flag is “0” ; register bank 1 is selected when this flag is “1”.

2.8.6 Overflow Flag (O Flag)

This flag is set to “1” when the operation resulted in an overflow; otherwise, it is “0”.

2.8.7 Interrupt Enable Flag (I Flag)

This flag enables a maskable interrupt.
Maskable interrupts are disabled when the I flag is “0”, and are enabled when the I flag is “1”. The I flag is cleared to “0” when the interrupt request is accepted.

2.8.8 Stack Pointer Select Flag (U Flag)

ISP is selected when the U flag is “0”; USP is selected when the U flag is “1”.
The U flag is cleared to “0” when a hardware interrupt request is accepted or an INT instruction for software interrupt Nos. 0 to 31 is executed.

2.8.9 Processor Interrupt Priority Level (IPL)

IPL is configured with three bits, for specification of up to eight processor interrupt priority levels from level 0 to level 7.
If a requested interrupt has priority greater than IPL, the interrupt is enabled.

2.8.10 Reserved Area

When write to this bit, write “0”. When read, its content is indeterminate.

5. Electrical Characteristics

5.1 Electrical Characteristics (M16C/62P)

Table 5.1 Absolute Maximum Ratings

Symbol	Parameter		Condition	Rated Value	Unit
V_{CC1}, V_{CC2}	Supply Voltage		V_{CC1}=AVcc	–0.3 to 6.5	V
V_{CC2}	Supply Voltage		V_{CC2}	–0.3 to V_{CC1}+0.1	V
AVcc	Analog Supply Voltage		V_{CC1}=AVcc	–0.3 to 6.5	V
V_I	Input Voltage	$\overline{\text{RESET}}$, CNVSS, BYTE, P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P14_0, P14_1, VREF, XIN		–0.3 to V_{CC1}+0.3 (1)	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P12_0 to P12_7, P13_0 to P13_7		–0.3 to V_{CC2}+0.3 (1)	V
		P7_0, P7_1		–0.3 to 6.5	V
V_O	Output Voltage	P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P14_0, P14_1, XOUT		–0.3 to V_{CC1}+0.3 (1)	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P12_0 to P12_7, P13_0 to P13_7		–0.3 to V_{CC2}+0.3 (1)	V
		P7_0, P7_1		–0.3 to 6.5	V
P_d	Power Dissipation		–40°C<T_{opr}≤85°C	300	mW
T_{opr}	Operating Ambient Temperature	When the Microcomputer is Operating		–20 to 85 / –40 to 85	°C
		Flash Program Erase		0 to 60	
T_{stg}	Storage Temperature			–65 to 150	°C

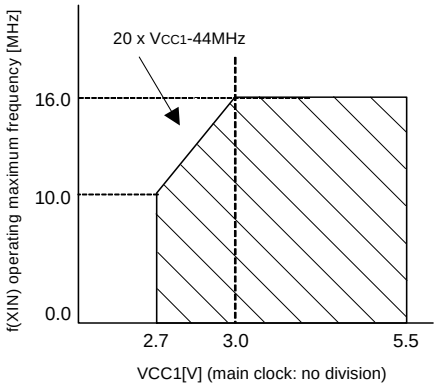
NOTES:
1. There is no external connections for port P1_0 to P1_7, P4_4 to P4_7, P7_2 to P7_5 and P9_1 in 80-pin version.

Table 5.3 Recommended Operating Conditions (2) (1)

Symbol	Parameter		Standard			Unit
			Min.	Typ.	Max.	
f(XIN)	Main Clock Input Oscillation Frequency (2)	V_{CC1}=3.0V to 5.5V	0		16	MHz
		V_{CC1}=2.7V to 3.0V	0		$20\times V_{CC1}-44$	MHz
f(XCIN)	Sub-Clock Oscillation Frequency			32.768	50	kHz
f(Ring)	On-chip Oscillation Frequency		0.5	1	2	MHz
f(PLL)	PLL Clock Oscillation Frequency (2)	V_{CC1}=3.0V to 5.5V	10		24	MHz
		V_{CC1}=2.7V to 3.0V	10		$46.67\times V_{CC1}-116$	MHz
f(BCLK)	CPU Operation Clock		0		24	MHz
t_{SU}(PLL)	PLL Frequency Synthesizer Stabilization Wait Time	V_{CC1}=5.5V			20	ms
		V_{CC1}=3.0V			50	ms

NOTES:
1. Referenced to V_{CC1} = V_{CC2} = 2.7 to 5.5V at T_{opr} = –20 to 85°C / –40 to 85°C unless otherwise specified.
2. Relationship between main clock oscillation frequency, and supply voltage.

Main clock input oscillation frequency



PLL clock oscillation frequency

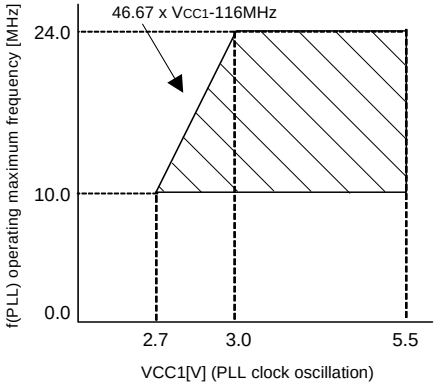


Table 5.5 D/A Conversion Characteristics (1)

Symbol	Parameter	Measuring Condition	Standard			Unit
			Min.	Typ.	Max.	
–	Resolution				8	Bits
–	Absolute Accuracy				1.0	%
t_{SU}	Setup Time				3	µs
R_O	Output Resistance		4	10	20	kΩ
I_{VREF}	Reference Power Supply Input Current	(NOTE 2)			1.5	mA

NOTES:

1. Referenced to V_{CC1}=V_{REF}=3.3 to 5.5V, V_{SS}=AV_{SS}=0V at T_{opr} = –20 to 85°C / –40 to 85°C unless otherwise specified.
2. This applies when using one D/A converter, with the D/A register for the unused D/A converter set to “00h”. The resistor ladder of the A/D converter is not included. Also, when D/A register contents are not “00h”, the I_{VREF} will flow even if Vref id disconnected by the A/D control register.

$V_{CC1}=V_{CC2}=5V$

Table 5.11 Electrical Characteristics (1) (1)

Symbol	Parameter			Measuring Condition	Standard			Unit
					Min.	Typ.	Max.	
V_{OH}	HIGH Output Voltage (3)	P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P14_0, P14_1		I_{OH}=−5mA	V_{CC1}−2.0		V_{CC1}	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P12_0 to P12_7, P13_0 to P13_7		I_{OH}=−5mA (2)	V_{CC2}−2.0		V_{CC2}	
V_{OH}	HIGH Output Voltage (3)	P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P14_0, P14_1		I_{OH}=−200μA	V_{CC1}−0.3		V_{CC1}	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P12_0 to P12_7, P13_0 to P13_7		I_{OH}=−200μA (2)	V_{CC2}−0.3		V_{CC2}	
V_{OH}	HIGH Output Voltage XOUT		HIGHPOWER	I_{OH}=−1mA	V_{CC1}−2.0		V_{CC1}	V
			LOWPOWER	I_{OH}=−0.5mA	V_{CC1}−2.0		V_{CC1}	
	HIGH Output Voltage XCOUT		HIGHPOWER	With no load applied		2.5		V
			LOWPOWER	With no load applied		1.6		
V_{OL}	LOW Output Voltage (3)	P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P14_0, P14_1		I_{OL}=5mA			2.0	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P12_0 to P12_7, P13_0 to P13_7		I_{OL}=5mA (2)			2.0	
V_{OL}	LOW Output Voltage (3)	P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P14_0, P14_1		I_{OL}=200μA			0.45	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P12_0 to P12_7, P13_0 to P13_7		I_{OL}=200μA (2)			0.45	
V_{OL}	LOW Output Voltage XOUT		HIGHPOWER	I_{OL}=1mA			2.0	V
			LOWPOWER	I_{OL}=0.5mA			2.0	
	LOW Output Voltage XCOUT		HIGHPOWER	With no load applied		0		V
			LOWPOWER	With no load applied		0		
V_{T+}-V_{T-}	Hysteresis	$\overline{HOLD}$, $\overline{RDY}$, TA0IN to TA4IN, TB0IN to TB5IN, $\overline{INT0}$ to $\overline{INT5}$, $\overline{NMI}$, $\overline{ADTRG}$, $\overline{CTS0}$ to $\overline{CTS2}$, CLK0 to CLK4, TA0OUT to TA4OUT, $\overline{KI0}$ to $\overline{KI3}$, RXD0 to RXD2, SCL0 to SCL2, SDA0 to SDA2, SIN3, SIN4			0.2		1.0	V
V_{T+}-V_{T-}	Hysteresis	$\overline{RESET}$			0.2		2.5	V
I_{IH}	HIGH Input Current (3)	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1, XIN, $\overline{RESET}$, CNVSS, BYTE		V_I=5V			5.0	μA
I_{IL}	LOW Input Current (3)	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7,P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1, XIN, $\overline{RESET}$, CNVSS, BYTE		V_I=0V			−5.0	μA
R_{PULLUP}	Pull-Up Resistance (3)	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7,P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1		V_I=0V	30	50	170	kΩ
R_{fXIN}	Feedback Resistance XIN					1.5		MΩ
R_{fXCIN}	Feedback Resistance XCIN					15		MΩ
V_{RAM}	RAM Retention Voltage			At stop mode	2.0			V

NOTES:
1. Referenced to V_{CC1}=V_{CC2}=4.2 to 5.5V, V_{SS} = 0V at T_{opr} = −20 to 85°C / −40 to 85°C, f(BCLK)=24MHz unless otherwise specified.
2. Where the product is used at V_{CC1} = 5 V and V_{CC2} = 3 V, refer to the 3 V version value for the pin specified value on V_{CC2} port side.
3. There is no external connections for port P1_0 to P1_7, P4_4 to P4_7, P7_2 to P7_5 and P9_1 in 80-pin version.

Table 5.12 Electrical Characteristics (2) (1)

Symbol	Parameter		Measuring Condition		Standard			Unit
					Min.	Typ.	Max.	
I_{CC}	Power Supply Current (V_{CC1}=V_{CC2}=4.0V to 5.5V)	In single-chip mode, the output pins are open and other pins are V_{SS}	Mask ROM	f(BCLK)=24MHz No division, PLL operation		14	20	mA
				No division, On-chip oscillation		1		mA
			Flash Memory	f(BCLK)=24MHz, No division, PLL operation		18	27	mA
				No division, On-chip oscillation		1.8		mA
			Flash Memory Program	f(BCLK)=10MHz, VCC1=5.0V		15		mA
			Flash Memory Erase	f(BCLK)=10MHz, VCC1=5.0V		25		mA
			Mask ROM	f(XCIN)=32kHz Low power dissipation mode, ROM (3)		25		µA
			Flash Memory	f(BCLK)=32kHz Low power dissipation mode, RAM (3)		25		µA
				f(BCLK)=32kHz Low power dissipation mode, Flash Memory (3)		420		µA
				On-chip oscillation, Wait mode		50		µA
			Mask ROM Flash Memory	f(BCLK)=32kHz Wait mode (2), Oscillation capability High		7.5		µA
				f(BCLK)=32kHz Wait mode (2), Oscillation capability Low		2.0		µA
				Stop mode Topr =25°C		0.8	3.0	µA
I_{det4}	Low Voltage Detection Dissipation Current (4)					0.7	4	µA
I_{det3}	Reset Area Detection Dissipation Current (4)					1.2	8	µA

NOTES:
1. Referenced to V_{CC1}=V_{CC2}=4.2 to 5.5V, V_{SS} = 0V at T_{opr} = –20 to 85°C / –40 to 85°C, f(BCLK)=24MHz unless otherwise specified.
2. With one timer operated using fC32.
3. This indicates the memory in which the program to be executed exists.
4. I_{det} is dissipation current when the following bit is set to “1” (detection circuit enabled).

   I_{det4}: VC27 bit in the VCR2 register

   I_{det3}: VC26 bit in the VCR2 register

$V_{CC1}=V_{CC2}=5V$

Switching Characteristics

(V_{CC1} = V_{CC2} = 5V, V_{SS} = 0V, at T_{opr} = –20 to 85°C / –40 to 85°C unless otherwise specified)

Table 5.28 Memory Expansion and Microprocessor Modes (for 1- to 3-wait setting and external area access)

Symbol	Parameter		Standard		Unit
			Min.	Max.	
$t_{d(BCLK-AD)}$	Address Output Delay Time	See **Figure 5.2**		25	ns
$t_{h(BCLK-AD)}$	Address Output Hold Time (in relation to BCLK)		4		ns
$t_{h(RD-AD)}$	Address Output Hold Time (in relation to RD)		0		ns
$t_{h(WR-AD)}$	Address Output Hold Time (in relation to WR)		(NOTE 2)		ns
$t_{d(BCLK-CS)}$	Chip Select Output Delay Time			25	ns
$t_{h(BCLK-CS)}$	Chip Select Output Hold Time (in relation to BCLK)		4		ns
$t_{d(BCLK-ALE)}$	ALE Signal Output Delay Time			15	ns
$t_{h(BCLK-ALE)}$	ALE Signal Output Hold Time		-4		ns
$t_{d(BCLK-RD)}$	RD Signal Output Delay Time			25	ns
$t_{h(BCLK-RD)}$	RD Signal Output Hold Time		0		ns
$t_{d(BCLK-WR)}$	WR Signal Output Delay Time			25	ns
$t_{h(BCLK-WR)}$	WR Signal Output Hold Time		0		ns
$t_{d(BCLK-DB)}$	Data Output Delay Time (in relation to BCLK)			40	ns
$t_{h(BCLK-DB)}$	Data Output Hold Time (in relation to BCLK) (3)		4		ns
$t_{d(DB-WR)}$	Data Output Delay Time (in relation to WR)		(NOTE 1)		ns
th(WR-DB)	Data Output Hold Time (in relation to WR)(3)		(NOTE 2)		ns
$t_{d(BCLK-HLDA)}$	HLDA Output Delay Time			40	ns

NOTES:

1. Calculated according to the BCLK frequency as follows:

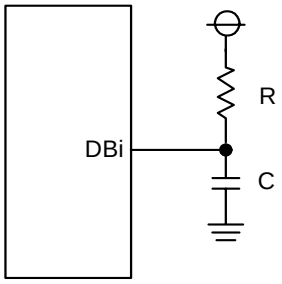
$$\frac{(n-0.5)\times 10^9}{f(BCLK)} - 40[ns]$$

n is “1” for 1-wait setting, “2” for 2-wait setting and “3” for 3-wait setting.
(BCLK) is 12.5MHz or less.

2. Calculated according to the BCLK frequency as follows:

$$\frac{0.5\times 10^9}{f(BCLK)} - 10[ns]$$

3. This standard value shows the timing when the output is off, and does not show hold time of data bus.
Hold time of data bus varies with capacitor volume and pull-up (pull-down) resistance value.
Hold time of data bus is expressed in
$t = -CR \times \ln(1 - V_{OL} / V_{CC2})$
by a circuit of the right figure.
For example, when V_{OL} = 0.2V_{CC2}, C = 30pF, R = 1kΩ, hold time of output ”L” level is
$t = -30pF \times 1k\Omega \times \ln(1 - 0.2V_{CC2} / V_{CC2})$
= 6.7ns.



$V_{CC1}=V_{CC2}=5V$

Switching Characteristics

(V_{CC1} = V_{CC2} = 5V, V_{SS} = 0V, at T_{opr} = –20 to 85°C / –40 to 85°C unless otherwise specified)

Table 5.29 Memory Expansion and Microprocessor Modes (for 2- to 3-wait setting, external area access and multiplex bus selection)

Symbol	Parameter		Standard		Unit
			Min.	Max.	
td(BCLK-AD)	Address Output Delay Time	See **Figure 5.2**		25	ns
th(BCLK-AD)	Address Output Hold Time (in relation to BCLK)		4		ns
th(RD-AD)	Address Output Hold Time (in relation to RD)		(NOTE 1)		ns
th(WR-AD)	Address Output Hold Time (in relation to WR)		(NOTE 1)		ns
td(BCLK-CS)	Chip Select Output Delay Time			25	ns
th(BCLK-CS)	Chip Select Output Hold Time (in relation to BCLK)		4		ns
th(RD-CS)	Chip Select Output Hold Time (in relation to RD)		(NOTE 1)		ns
th(WR-CS)	Chip Select Output Hold Time (in relation to WR)		(NOTE 1)		ns
td(BCLK-RD)	RD Signal Output Delay Time			25	ns
th(BCLK-RD)	RD Signal Output Hold Time		0		ns
td(BCLK-WR)	WR Signal Output Delay Time			25	ns
th(BCLK-WR)	WR Signal Output Hold Time		0		ns
td(BCLK-DB)	Data Output Delay Time (in relation to BCLK)			40	ns
th(BCLK-DB)	Data Output Hold Time (in relation to BCLK)		4		ns
td(DB-WR)	Data Output Delay Time (in relation to WR)		(NOTE 2)		ns
th(WR-DB)	Data Output Hold Time (in relation to WR)		(NOTE 1)		ns
td(BCLK-HLDA)	HLDA Output Delay Time			40	ns
td(BCLK-ALE)	ALE Signal Output Delay Time (in relation to BCLK)			15	ns
th(BCLK-ALE)	ALE Signal Output Hold Time (in relation to BCLK)		–4		ns
td(AD-ALE)	ALE Signal Output Delay Time (in relation to Address)		(NOTE 3)		ns
th(AD-ALE)	ALE Signal Output Hold Time (in relation to Address)		(NOTE 4)		ns
td(AD-RD)	RD Signal Output Delay From the End of Address		0		ns
td(AD-WR)	WR Signal Output Delay From the End of Address		0		ns
tdz(RD-AD)	Address Output Floating Start Time			8	ns

NOTES:

1. Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f(BCLK)} - 10[ns]$$

2. Calculated according to the BCLK frequency as follows:

$$\frac{(n-0.5) \times 10^9}{f(BCLK)} - 40[ns]$$

n is “2” for 2-wait setting, “3” for 3-wait setting.

3. Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f(BCLK)} - 25[ns]$$

4. Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f(BCLK)} - 15[ns]$$

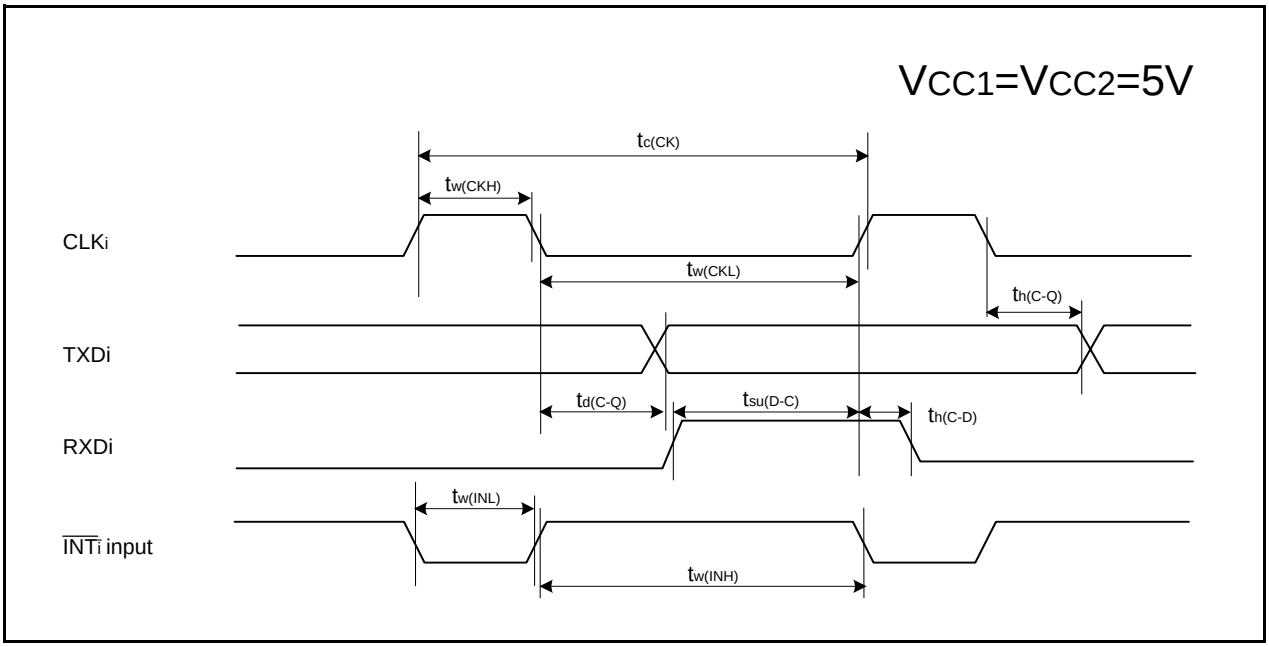


Figure 5.4 Timing Diagram (2)

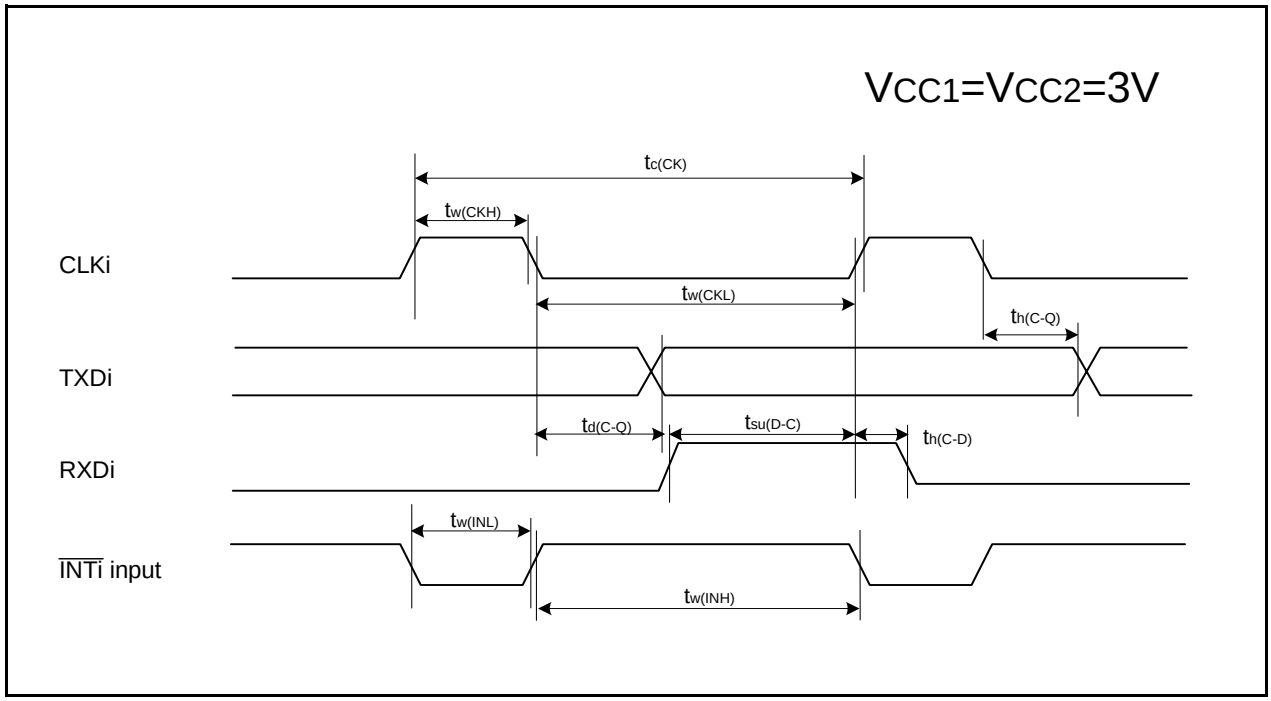
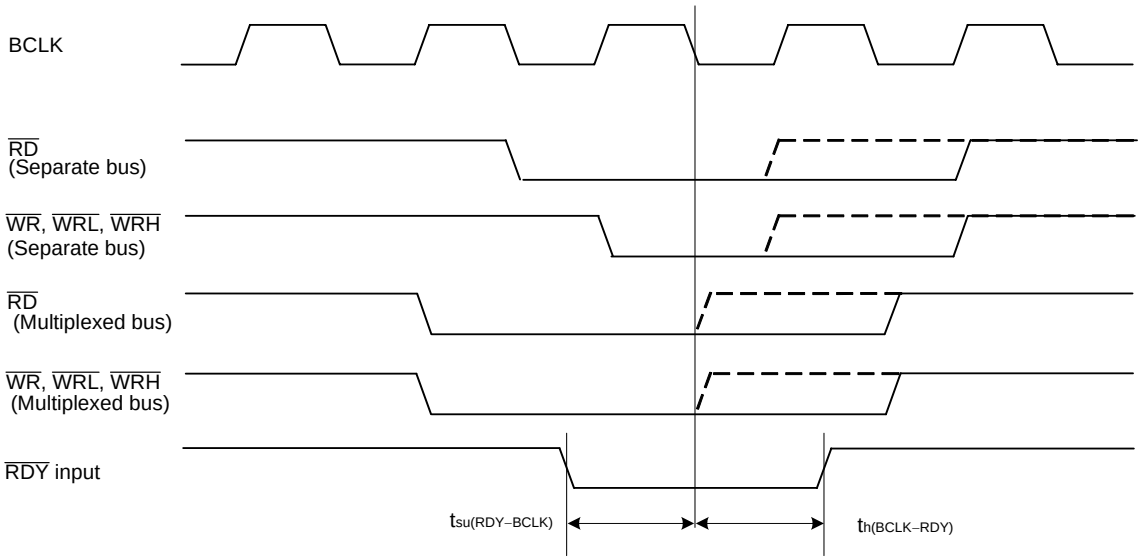


Figure 5.14 Timing Diagram (2)

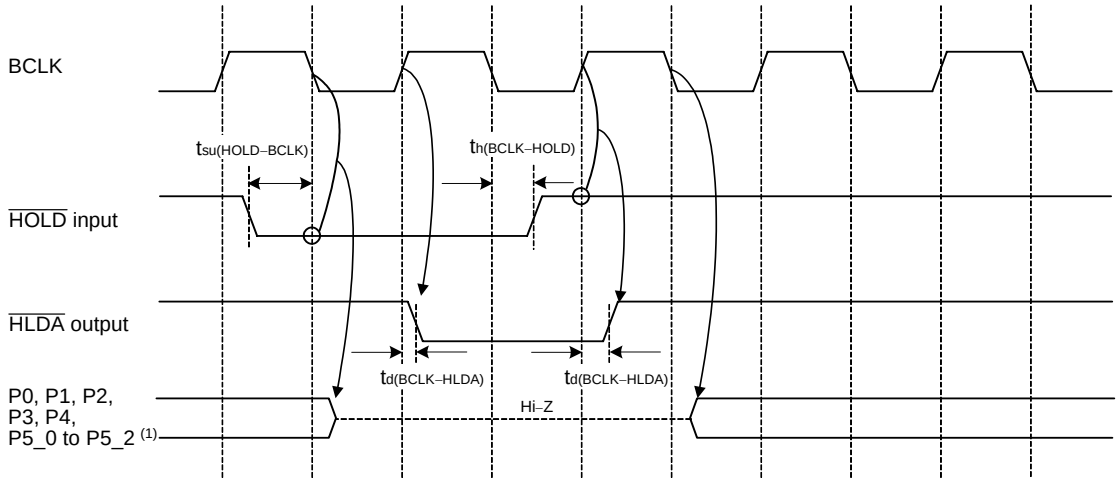
Memory Expansion Mode, Microprocessor Mode

$V_{CC1}=V_{CC2}=3V$

(Effective for setting with wait)



(Common to setting with wait and setting without wait)



NOTES:
1. These pins are set to high-impedance regardless of the input level of the BYTE pin, PM06 bit in PM0 register and PM11 bit in PM1 register.

Measuring conditions :
· $V_{CC1}=V_{CC2}=3V$
· Input timing voltage : Determined with $V_{IL}=0.6V$, $V_{IH}=2.4V$
· Output timing voltage : Determined with $V_{OL}=1.5V$, $V_{OH}=1.5V$

Figure 5.15 Timing Diagram (3)

Table 5.50 Recommended Operating Conditions (1) (1)

Symbol	Parameter		Standard			Unit
			Min.	Typ.	Max.	
V_{CC1}, V_{CC2}	Supply Voltage (V_{CC1} = V_{CC2})		4.0	5.0	5.5	V
AVcc	Analog Supply Voltage			V_{CC1}		V
Vss	Supply Voltage			0		V
AVss	Analog Supply Voltage			0		V
V_{IH}	HIGH Input Voltage (4)	P3_1 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P12_0 to P12_7, P13_0 to P13_7	0.8V_{CC2}		V_{CC2}	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 (during single-chip mode)	0.8V_{CC2}		V_{CC2}	V
		P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P14_0, P14_1, XIN, RESET, CNVSS, BYTE	0.8V_{CC1}		V_{CC1}	V
		P7_0, P7_1	0.8V_{CC1}		6.5	V
V_{IL}	LOW Input Voltage (4)	P3_1 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P12_0 to P12_7, P13_0 to P13_7	0		0.2V_{CC2}	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 (during single-chip mode)	0		0.2V_{CC2}	V
		P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P14_0, P14_1, XIN, RESET, CNVSS, BYTE	0		0.2Vcc	V
$I_{OH(peak)}$	HIGH Peak Output Current (4)	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1			–10.0	mA
$I_{OH(avg)}$	HIGH Average Output Current (4)	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1			–5.0	mA
$I_{OL(peak)}$	LOW Peak Output Current (4)	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1			10.0	mA
$I_{OL(avg)}$	LOW Average Output Current (4)	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1			5.0	mA
f(XIN)	Main Clock Input Oscillation Frequency	V_{CC1}=4.0V to 5.5V	0		16	MHz
f(XCIN)	Sub-Clock Oscillation Frequency			32.768	50	kHz
f(Ring)	On-chip Oscillation Frequency		0.5	1	2	MHz
f(PLL)	PLL Clock Oscillation Frequency	V_{CC1}=4.0V to 5.5V	10		24	MHz
f(BCLK)	CPU Operation Clock		0		24	MHz
t_{SU}(PLL)	PLL Frequency Synthesizer Stabilization Wait Time	V_{CC1}=5.5V			20	ms

NOTES:

1. Referenced to V_{CC1} = V_{CC2} = 4.7 to 5.5V at T_{opr} = –40 to 85°C / –40 to 125°C unless otherwise specified.
   T version = –40 to 85 °C, V version= –40 to 125 °C.
2. The Average Output Current is the mean value within 100ms.
3. The total $I_{OL(peak)}$ for ports P0, P1, P2, P8_6, P8_7, P9, P10 P1, P14_0 and P14_1 must be 80mA max. The total $I_{OL(peak)}$ for ports P3, P4, P5, P6, P7, P8_0 to P8_4, P12, and P13 must be 80mA max. The total $I_{OH(peak)}$ for ports P0, P1, and P2 must be –40mA max. The total $I_{OH(peak)}$ for ports P3, P4, P5, P12, and P13 must be –40mA max. The total $I_{OH(peak)}$ for ports P6, P7, and P8_0 to P8_4 must be –40mA max. The total $I_{OH(peak)}$ for ports P8_6, P8_7, P9 , P10, P11, P14_0, and P14_1 must be –40mA max.
   As for 80-pin version, the total $I_{OL(peak)}$ for all ports and $I_{OH(peak)}$ must be 80mA. max. due to one V_{CC} and one V_{SS}.
4. There is no external connections for port P1_0 to P1_7, P4_4 to P4_7, P7_2 to P7_5 and P9_1 in 80-pin version.

$V_{CC1}=V_{CC2}=5V$

Switching Characteristics
(V_{CC1} = V_{CC2} = 5V, V_{SS} = 0V, at T_{opr} = –40 to 85°C (T version) / –40 to 125°C (V version) unless otherwise specified)

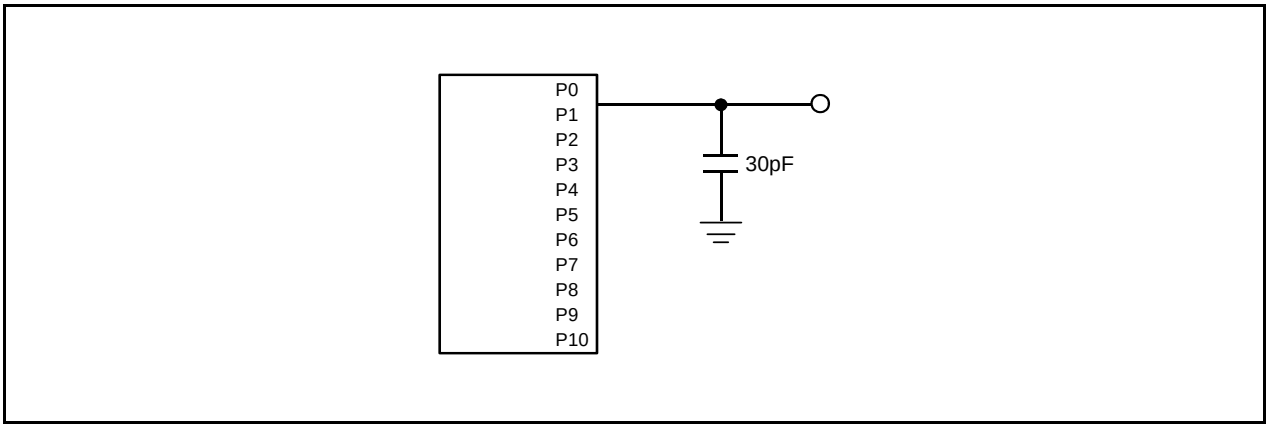


Figure 5.23 Ports P0 to P10 Measurement Circuit

REVISION HISTORY	M16C/62P Group (M16C/62P, M16C/62PT) Hardware Manual

Rev.	Date	Description	
		Page	Summary
1.10	May 28, 2003	1	Applications are partly revised.
		2	Table 1.1.1 is partly revised.
		4-5	Table 1.1.2 and 1.1.3 is partly revised. "Note 1" is partly revised.
		22	Table 1.5.3 is partly revised.
		23	Table 1.5.5 is partly revised. Table 1.5.6 is added.
		24	Table 1.5.9 is partly revised.
		30	Notes 1 and 2 in Table 1.5.26 is partly revised.
		31	Notes 1 in Table 1.5.27 is partly revised.
		30-31	Note 3 is added to "Data output hold time (refers to BCLK)" in Table 1.5.26 and 1.5.27.
		32	Note 4 is added to "th(ALE-AD)" in Table 1.5.28.
		30-32	Switching Characteristics is partly revised.
		36-39	th(WR-AD) and th(WR-DB) in Figure 1.5.5 to 1.5.8 is partly revised.
		40-41	th(ALE-AD), th(WR-CS), th(WR-DB) and th(WR-AD) in Figure 1.5.9 to 1.5.10 is partly revised.
		42	Note 2 is added to Table 1.5.29.
		47	Notes 1 and 2 in Table 1.5.45 is partly revised.
		48	Notes 1 in Table 1.5.46 is partly revised.
		47-48	Note 3 is added to "Data output hold time (refers to BCLK)" in Table 1.5.45 and 1.5.46.
		49	Note 4 is added to "th(ALE-AD)" in Table 1.5.47.
		47-48	Switching Characteristics is partly revised.
		53-56	th(WR-AD) and th(WR-DB) in Figure 1.5.15 to 1.5.18 is partly revised.
		57-58	th(ALE-AD), th(WR-CS), th(WR-DB) and th(WR-AD) in Figure 1.5.19 to 1.5.20 is partly revised.
2.00	Oct 29, 2003	-	Since high reliability version is added, a group name is revised. M16C/62 Group (M16C/62P) → M16C/62 Group (M16C/62P, M16C/62PT)
		2-4	Table 1.1 to 1.3 are revised. Note 3 is partly revised.
		2-4	Table 1.1 to 1.3 are revised. Note 3 is partly revised.
		6	Figure 1.2 Note5 is deleted.
		7-9	Table 1.4 to 1.7 Product List is partly revised.
		11	Table 1.8 and Figure 1.4 are added.
		12-15	Figure 1.5 to 1.9 ZP is added.
		17,19	Table 1.10 and 1.12 ZP is added to timer A.
		18,20	Table 1.11 and 1.13 VCC1 is added to VREF.
		30	Table 5.1 is revised.
		31-32	Table 5.2 and 5.3 are revised.