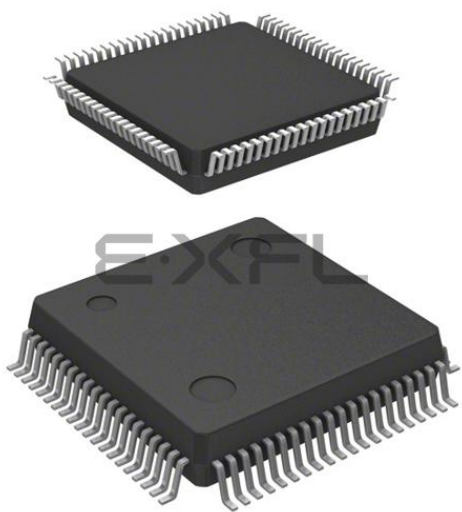




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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	M16C/60
Core Size	16-Bit
Speed	24MHz
Connectivity	I ² C, IEBus, UART/USART
Peripherals	DMA, WDT
Number of I/O	68
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 26x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-BQFP
Supplier Device Package	80-QFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/m30623f8pgp-u5c

1. Overview

The M16C/62P Group (M16C/62P, M16C/62PT) of single-chip microcomputers are built using the high performance silicon gate CMOS process using a M16C/60 Series CPU core and are packaged in a 80-pin, 100-pin and 128-pin plastic molded QFP. These single-chip microcomputers operate using sophisticated instructions featuring a high level of instruction efficiency. With 1M bytes of address space, they are capable of executing instructions at high speed. In addition, this microcomputer contains a multiplier and DMAC which combined with fast instruction processing capability, makes it suitable for control of various OA, communication, and industrial equipment which requires high-speed arithmetic/logic operations.

1.1 Applications

Audio, cameras, television, home appliance, office/communications/portable/industrial equipment, automobile, etc.

Specifications written in this manual are believed to be accurate, but are not guaranteed to be entirely free of error. Specifications in this manual may be changed for functional or performance improvements. Please make sure your manual is the latest edition.

1.3 Block Diagram

Figure 1.1 is a M16C/62P Group (M16C/62P, M16C/62PT) 128-pin and 100-pin version Block Diagram,
Figure 1.2 is a M16C/62P Group (M16C/62P, M16C/62PT) 80-pin version Block Diagram.

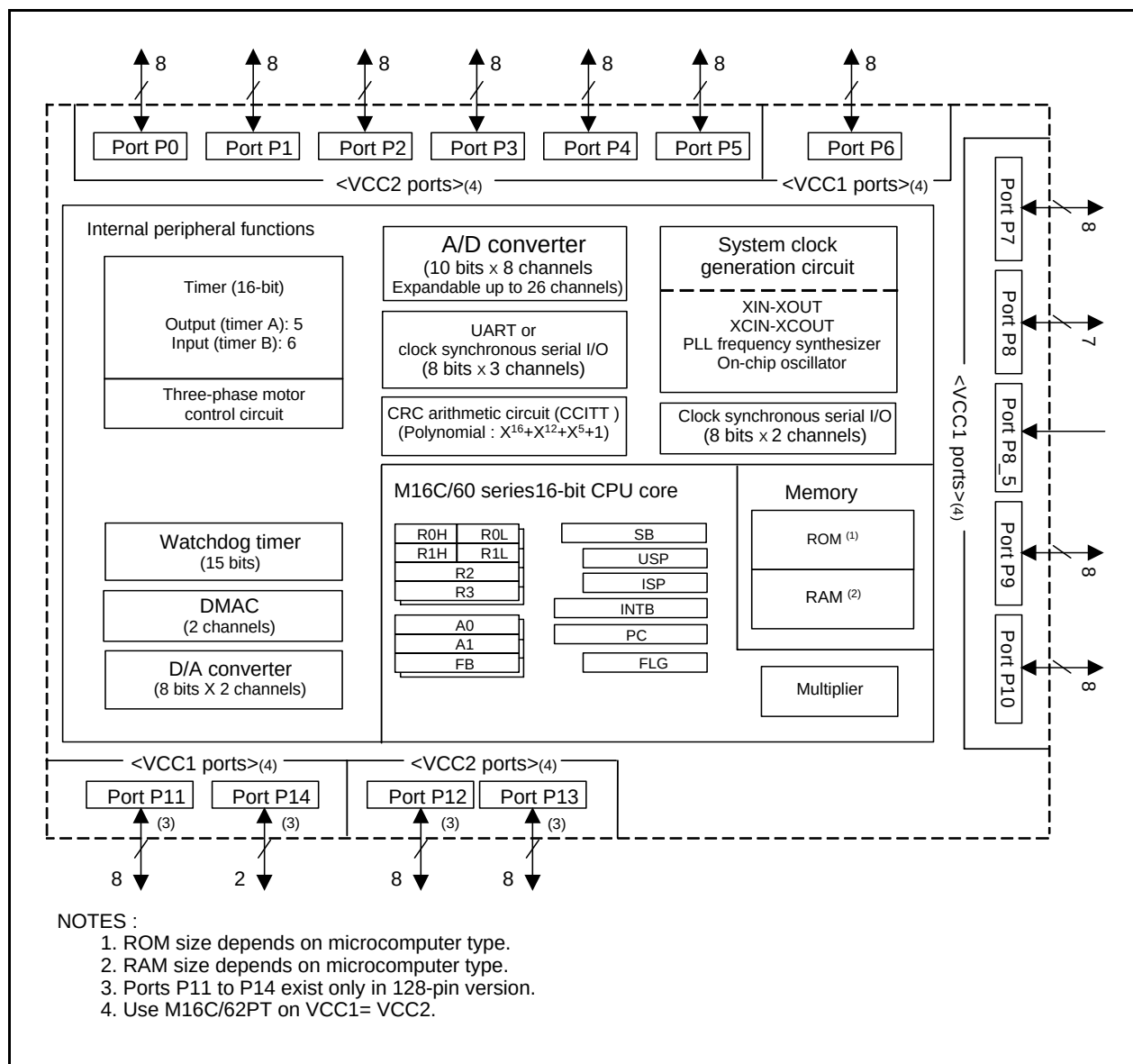


Figure 1.1 M16C/62P Group (M16C/62P, M16C/62PT) 128-pin and 100-pin version Block Diagram

Table 1.5 Product List (2) (M16C/62P)

As of Dec. 2005

Type No.	ROM Capacity	RAM Capacity	Package Type ⁽¹⁾	Remarks
M30622MHP-XXXFP	384 Kbytes	16 Kbytes	PRQP0100JB-A	Mask ROM version
M30622MHP-XXXGP			PLQP0100KB-A	
M30623MHP-XXXGP			PLQP0128KB-A	
M30624MHP-XXXFP		24 Kbytes	PRQP0100JB-A	
M30624MHP-XXXGP			PLQP0100KB-A	
M30625MHP-XXXGP			PLQP0128KB-A	
M30626MHP-XXXFP		31 Kbytes	PRQP0100JB-A	
M30626MHP-XXXGP			PLQP0100KB-A	
M30627MHP-XXXGP			PLQP0128KB-A	
M30626MJP-XXXFP (D)	512 Kbytes	31 Kbytes	PRQP0100JB-A	Flash memory version ⁽²⁾
M30626MJP-XXXGP (D)			PLQP0100KB-A	
M30627MJP-XXXGP (D)			PLQP0128KB-A	
M30622F8PFP	64K+4 Kbytes	4 Kbytes	PRQP0100JB-A	
M30622F8PGP			PLQP0100KB-A	
M30623F8PGP			PRQP0080JA-A	
M30620FCPFP	128K+4 Kbytes	10 Kbytes	PRQP0100JB-A	
M30620FCPGP			PLQP0100KB-A	
M30621FCPGP			PRQP0080JA-A	
M3062LFGPFP ⁽³⁾ (D)	256K+4 Kbytes	20 Kbytes	PRQP0100JB-A	
M3062LFGPGP ⁽³⁾ (D)			PLQP0100KB-A	
M30625FGPGP			PLQP0128KB-A	
M30626FHPFP	384K+4 Kbytes	31 Kbytes	PRQP0100JB-A	ROM-less version
M30626FHPPGP			PLQP0100KB-A	
M30627FHPPGP			PLQP0128KB-A	
M30626FJPFP	512K+4 Kbytes	31 Kbytes	PRQP0100JB-A	
M30626FJPPGP			PLQP0100KB-A	
M30627FJPPGP			PLQP0128KB-A	
M30622SPFP	–	4 Kbytes	PRQP0100JB-A	
M30622SPGP			PLQP0100KB-A	
M30620SPFP		10 Kbytes	PRQP0100JB-A	
M30620SPGP			PLQP0100KB-A	
M30624SPFP (D)	–	20 Kbytes	PRQP0100JB-A	
M30624SPGP (D)			PLQP0100KB-A	
M30626SPFP (D)		31 Kbytes	PRQP0100JB-A	
M30626SPGP (D)			PLQP0100KB-A	

(D): Under development

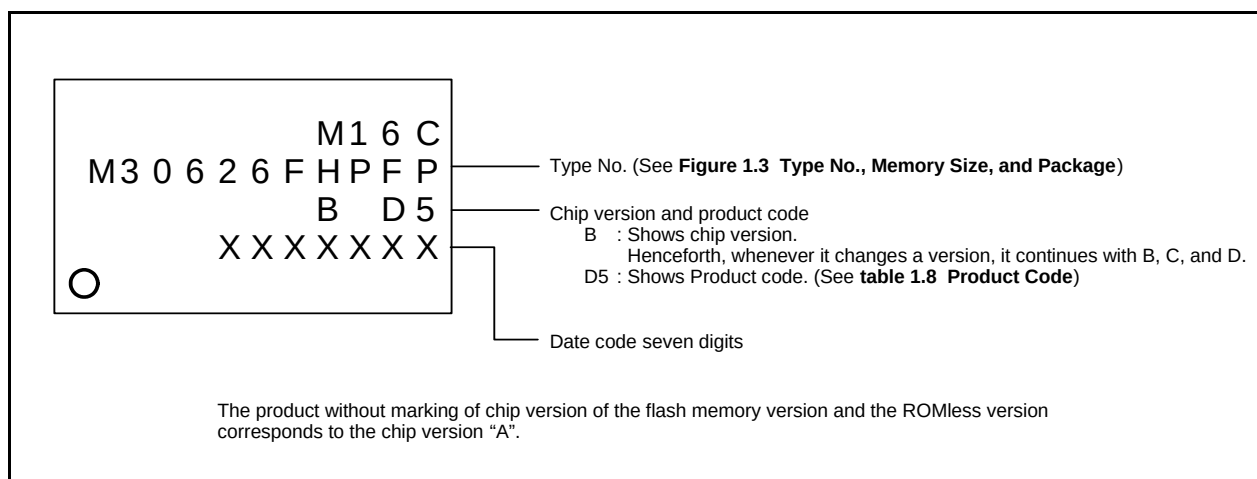
NOTES:

- The old package type numbers of each package type are as follows.
 PLQP0128KB-A : 128P6Q-A,
 PRQP0100JB-A : 100P6S-A,
 PLQP0100KB-A : 100P6Q-A,
 PRQP0080JA-A : 80P6S-A
- In the flash memory version, there is 4K bytes area (block A).
- Please use M3062LFGPFP and M3062LFGPGP for your new system instead of M30624FGPFP and M30624FGPGP. The M16C/62P Group (M16C/62P, M16C/62PT) hardware manual is still good for M30624FGPFP and M30624FGPGP.

M30624FGPFP	256K+4 Kbytes	20 Kbytes	PRQP0100JB-A	Flash memory version
M30624FGPGP			PLQP0100KB-A	

Table 1.8 Product Code of Flash Memory version and ROMless version for M16C/62P

	Product Code	Package	Internal ROM (User ROM Area Without Block A, Block 1)		Internal ROM (Block A, Block 1)		Operating Ambient Temperature
			Program and Erase Endurance	Temperature Range	Program and Erase Endurance	Temperature Range	
Flash memory Version	D3	Lead-included	100	0°C to 60°C	100	0°C to 60°C	-40°C to 85°C
	D5						-20°C to 85°C
	D7		1,000		10,000	-40°C to 85°C	-40°C to 85°C
	D9					-20°C to 85°C	-20°C to 85°C
	U3	Lead-free	100		100	0°C to 60°C	-40°C to 85°C
	U5					-20°C to 85°C	
	U7		1,000		10,000	-40°C to 85°C	-40°C to 85°C
	U9					-20°C to 85°C	-20°C to 85°C
ROM-less version	D3	Lead-included	—	—	—	—	-40°C to 85°C
	D5						-20°C to 85°C
	U3	Lead-free	—	—	—	—	-40°C to 85°C
	U5						-20°C to 85°C

**Figure 1.4 Marking Diagram of Flash Memory version and ROM-less version for M16C/62P (Top View)**

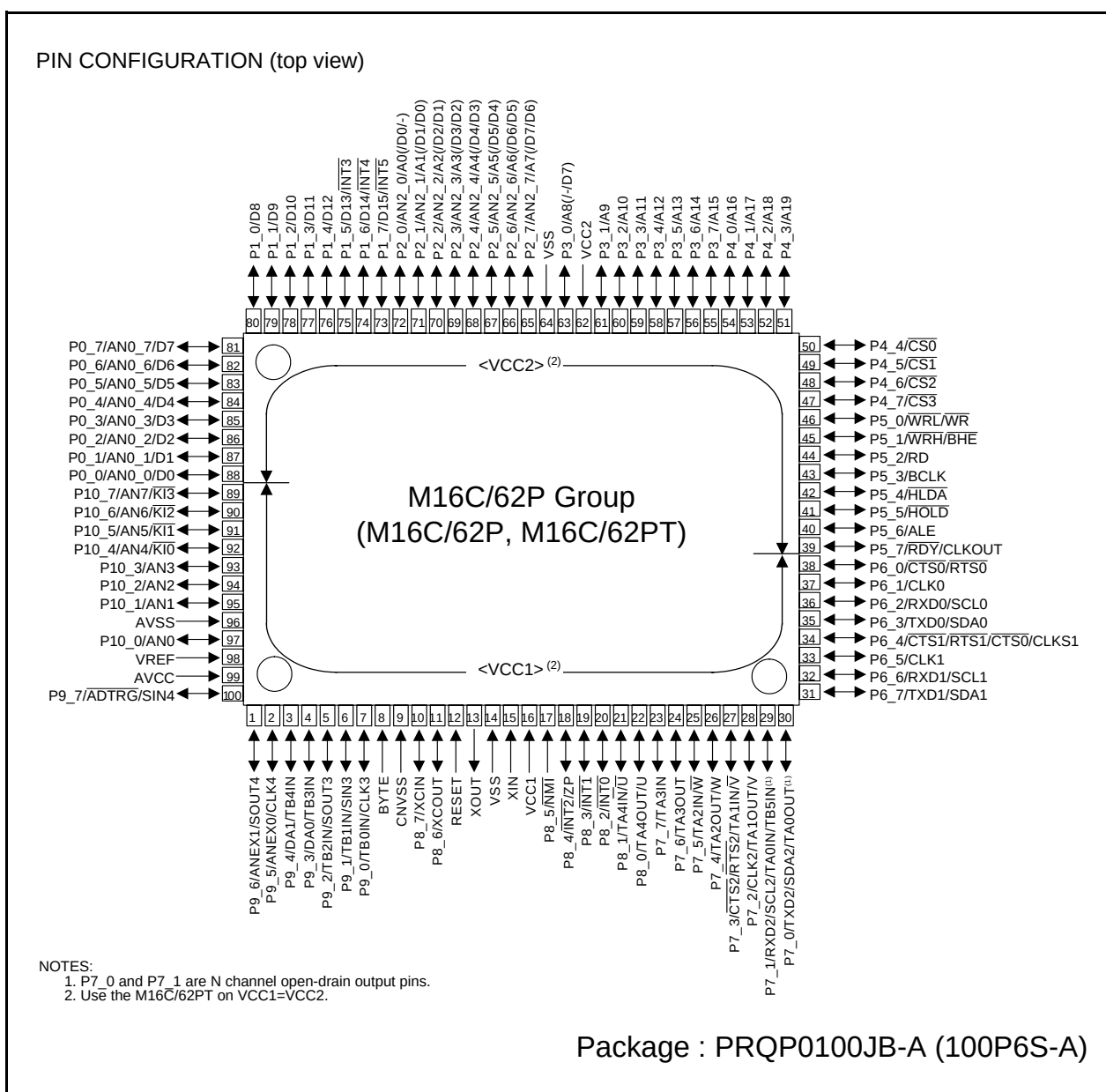


Figure 1.7 Pin Configuration (Top View)

Table 1.14 Pin Characteristics for 100-Pin Package (2)

Pin No.		Control Pin	Port	Interrupt Pin	Timer Pin	UART Pin	Analog Pin	Bus Control Pin
FP	GP							
51	49		P4_3					A19
52	50		P4_2					A18
53	51		P4_1					A17
54	52		P4_0					A16
55	53		P3_7					A15
56	54		P3_6					A14
57	55		P3_5					A13
58	56		P3_4					A12
59	57		P3_3					A11
60	58		P3_2					A10
61	59		P3_1					A9
62	60	VCC2						
63	61		P3_0					A8(/-D7)
64	62	VSS						
65	63		P2_7				AN2_7	A7(/D7/D6)
66	64		P2_6				AN2_6	A6(/D6/D5)
67	65		P2_5				AN2_5	A5(/D5/D4)
68	66		P2_4				AN2_4	A4(/D4/D3)
69	67		P2_3				AN2_3	A3(/D3/D2)
70	68		P2_2				AN2_2	A2(/D2/D1)
71	69		P2_1				AN2_1	A1(/D1/D0)
72	70		P2_0				AN2_0	A0(/D0/-)
73	71		P1_7	INT5				D15
74	72		P1_6	INT4				D14
75	73		P1_5	INT3				D13
76	74		P1_4					D12
77	75		P1_3					D11
78	76		P1_2					D10
79	77		P1_1					D9
80	78		P1_0					D8
81	79		P0_7				AN0_7	D7
82	80		P0_6				AN0_6	D6
83	81		P0_5				AN0_5	D5
84	82		P0_4				AN0_4	D4
85	83		P0_3				AN0_3	D3
86	84		P0_2				AN0_2	D2
87	85		P0_1				AN0_1	D1
88	86		P0_0				AN0_0	D0
89	87		P10_7	KI3			AN7	
90	88		P10_6	KI2			AN6	
91	89		P10_5	KI1			AN5	
92	90		P10_4	KI0			AN4	
93	91		P10_3				AN3	
94	92		P10_2				AN2	
95	93		P10_1				AN1	
96	94	AVSS						
97	95		P10_0				AN0	
98	96	VREF						
99	97	AVCC						
100	98		P9_7			SIN4	ADTRG	

4. Special Function Register (SFR)

SFR(Special Function Register) is the control register of peripheral functions. Tables 4.1 to 4.6 list the SFR information.

Table 4.1 SFR Information (1) (1)

Address	Register	Symbol	After Reset
0000h			
0001h			
0002h			
0003h			
0004h	Processor Mode Register 0 ⁽²⁾	PM0	0000000b(CNVSS pin is "L") 0000011b(CNVSS pin is "H")
0005h	Processor Mode Register 1	PM1	00001000b
0006h	System Clock Control Register 0	CM0	01001000b
0007h	System Clock Control Register 1	CM1	00100000b
0008h	Chip Select Control Register ⁽⁶⁾	CSR	00000001b
0009h	Address Match Interrupt Enable Register	AIER	XXXXXX00b
000Ah	Protect Register	PRCR	XX000000b
000Bh	Data Bank Register ⁽⁶⁾	DBR	00h
000Ch	Oscillation Stop Detection Register ⁽³⁾	CM2	0X000000b
000Dh			
000Eh	Watchdog Timer Start Register	WDTs	XXh
000Fh	Watchdog Timer Control Register	WDC	00XXXXXXb ⁽⁴⁾
0010h	Address Match Interrupt Register 0	RMAD0	00h
0011h			00h
0012h			X0h
0013h			
0014h	Address Match Interrupt Register 1	RMAD1	00h
0015h			00h
0016h			X0h
0017h			
0018h			
0019h	Voltage Detection Register 1 ^(5, 6)	VCR1	00001000b
001Ah	Voltage Detection Register 2 ^(5, 6)	VCR2	00h
001Bh	Chip Select Expansion Control Register ⁽⁶⁾	CSE	00h
001Ch	PLL Control Register 0	PLC0	0001X010b
001Dh			
001Eh	Processor Mode Register 2	PM2	XXX00000b
001Fh	Low Voltage Detection Interrupt Register ⁽⁶⁾	D4INT	00h
0020h	DMA0 Source Pointer	SAR0	XXh
0021h			XXh
0022h			XXh
0023h			
0024h	DMA0 Destination Pointer	DAR0	XXh
0025h			XXh
0026h			XXh
0027h			
0028h	DMA0 Transfer Counter	TCR0	XXh
0029h			XXh
002Ah			
002Bh			
002Ch	DMA0 Control Register	DM0CON	00000X00b
002Dh			
002Eh			
002Fh			
0030h	DMA1 Source Pointer	SAR1	XXh
0031h			XXh
0032h			XXh
0033h			
0034h	DMA1 Destination Pointer	DAR1	XXh
0035h			XXh
0036h			XXh
0037h			
0038h	DMA1 Transfer Counter	TCR1	XXh
0039h			XXh
003Ah			
003Bh			
003Ch	DMA1 Control Register	DM1CON	00000X00b
003Dh			
003Eh			
003Fh			

NOTES:

1. The blank areas are reserved and cannot be accessed by users.
2. The PM00 and PM01 bits do not change at software reset, watchdog timer reset and oscillation stop detection reset.
3. The CM20, CM21, and CM27 bits do not change at oscillation stop detection reset.
4. The WDC5 bit is "0" (cold start) immediately after power-on. It can only be set to "1" in a program.
5. This register does not change at software reset, watchdog timer reset and oscillation stop detection reset.
6. This register in M16C/62PT cannot be used.

X : Nothing is mapped to this bit

Table 4.4 SFR Information (4) ⁽¹⁾

Address	Register	Symbol	After Reset
0340h	Timer B3, 4, 5 Count Start Flag	TBSR	000XXXXb
0341h			
0342h	Timer A1-1 Register	TA11	XXh
0343h			XXh
0344h	Timer A2-1 Register	TA21	XXh
0345h			XXh
0346h	Timer A4-1 Register	TA41	XXh
0347h			XXh
0348h	Three-Phase PWM Control Register 0	INVC0	00h
0349h	Three-Phase PWM Control Register 1	INVC1	00h
034Ah	Three-Phase Output Buffer Register 0	IDB0	00h
034Bh	Three-Phase Output Buffer Register 1	IDB1	00h
034Ch	Dead Time Timer	DTT	XXh
034Dh	Timer B2 Interrupt Occurrence Frequency Set Counter	ICTB2	XXh
034Eh			
034Fh			
0350h	Timer B3 Register	TB3	XXh
0351h			XXh
0352h	Timer B4 Register	TB4	XXh
0353h			XXh
0354h	Timer B5 Register	TB5	XXh
0355h			XXh
0356h			
0357h			
0358h			
0359h			
035Ah			
035Bh	Timer B3 Mode Register	TB3MR	00XX0000b
035Ch	Timer B4 Mode Register	TB4MR	00XX0000b
035Dh	Timer B5 Mode Register	TB5MR	00XX0000b
035Eh	Interrupt Factor Select Register 2	IFSR2A	00XXXXXXb
035Fh	Interrupt Factor Select Register	IFSR	00h
0360h	SI/O3 Transmit/Receive Register	S3TRR	XXh
0361h			
0362h	SI/O3 Control Register	S3C	01000000b
0363h	SI/O3 Bit Rate Generator	S3BRG	XXh
0364h	SI/O4 Transmit/Receive Register	S4TRR	XXh
0365h			
0366h	SI/O4 Control Register	S4C	01000000b
0367h	SI/O4 Bit Rate Generator	S4BRG	XXh
0368h			
0369h			
036Ah			
036Bh			
036Ch	UART0 Special Mode Register 4	U0SMR4	00h
036Dh	UART0 Special Mode Register 3	U0SMR3	000X0X0Xb
036Eh	UART0 Special Mode Register 2	U0SMR2	X0000000b
036Fh	UART0 Special Mode Register	U0SMR	X0000000b
0370h	UART1 Special Mode Register 4	U1SMR4	00h
0371h	UART1 Special Mode Register 3	U1SMR3	000X0X0Xb
0372h	UART1 Special Mode Register 2	U1SMR2	X0000000b
0373h	UART1 Special Mode Register	U1SMR	X0000000b
0374h	UART2 Special Mode Register 4	U2SMR4	00h
0375h	UART2 Special Mode Register 3	U2SMR3	000X0X0Xb
0376h	UART2 Special Mode Register 2	U2SMR2	X0000000b
0377h	UART2 Special Mode Register	U2SMR	X0000000b
0378h	UART2 Transmit/Receive Mode Register	U2MR	00h
0379h	UART2 Bit Rate Generator	U2BRG	XXh
037Ah	UART2 Transmit Buffer Register	U2TB	XXh
037Bh			XXh
037Ch	UART2 Transmit/Receive Control Register 0	U2C0	00001000b
037Dh	UART2 Transmit/Receive Control Register 1	U2C1	00000010b
037Eh	UART2 Receive Buffer Register	U2RB	XXh
037Fh			XXh

NOTES:

- The blank areas are reserved and cannot be accessed by users.

X : Nothing is mapped to this bit

Table 5.2 Recommended Operating Conditions (1) (1)

Symbol	Parameter		Standard			Unit
			Min.	Typ.	Max.	
V _{CC1} , V _{CC2}	Supply Voltage (V _{CC1} ≥ V _{CC2})		2.7	5.0	5.5	V
AV _{CC}	Analog Supply Voltage			V _{CC1}		V
V _{SS}	Supply Voltage			0		V
AV _{SS}	Analog Supply Voltage			0		V
V _{IH}	HIGH Input Voltage	P3_1 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P12_0 to P12_7, P13_0 to P13_7	0.8V _{CC2}		V _{CC2}	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 (during single-chip mode)	0.8V _{CC2}		V _{CC2}	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 (data input during memory expansion and microprocessor mode)	0.5V _{CC2}		V _{CC2}	V
		P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P14_0, P14_1, XIN, RESET, CNVSS, BYTE	0.8V _{CC1}		V _{CC1}	V
		P7_0, P7_1	0.8V _{CC1}		6.5	V
V _{IL}	LOW Input Voltage	P3_1 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P12_0 to P12_7, P13_0 to P13_7	0		0.2V _{CC2}	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 (during single-chip mode)	0		0.2V _{CC2}	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 (data input during memory expansion and microprocessor mode)	0		0.16V _{CC2}	V
		P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P14_0, P14_1, XIN, RESET, CNVSS, BYTE	0		0.2V _{CC}	V
I _{OH(peak)}	HIGH Peak Output Current	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1			−10.0	mA
I _{OH(avg)}	HIGH Average Output Current	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1			−5.0	mA
I _{OL(peak)}	LOW Peak Output Current	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1			10.0	mA
I _{OL(avg)}	LOW Average Output Current	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1			5.0	mA

NOTES:

1. Referenced to V_{CC1} = V_{CC2} = 2.7 to 5.5V at T_{opr} = −20 to 85°C / −40 to 85°C unless otherwise specified.
2. The Average Output Current is the mean value within 100ms.
3. The total I_{OL(peak)} for ports P0, P1, P2, P8_6, P8_7, P9, P10, P11, P14_0, and P14_1 must be 80mA max. The total I_{OH(peak)} for ports P3, P4, P5, P6, P7, P8_0 to P8_4, P12, and P13 must be 80mA max. The total I_{OH(peak)} for ports P0, P1, and P2 must be −40mA max. The total I_{OH(peak)} for ports P3, P4, P5, P12, and P13 must be −40mA max. The total I_{OH(peak)} for ports P6, P7, and P8_0 to P8_4 must be −40mA max. The total I_{OH(peak)} for ports P8_6, P8_7, P9, P10, P14_0, and P14_1 must be −40mA max. Set Average Output Current to 1/2 of peak. The total I_{OH(peak)} for ports P8_6, P8_7, P9, P10, P11, P14_0, and P14_1 must be −40mA max.
As for 80-pin version, the total I_{OL(peak)} for all ports and I_{OH(peak)} must be 80mA. max. due to one V_{CC} and one V_{SS}.
4. There is no external connections for port P1_0 to P1_7, P4_4 to P4_7, P7_2 to P7_5 and P9_1 in 80-pin version.

Table 5.12 Electrical Characteristics (2) ⁽¹⁾

Symbol	Parameter		Measuring Condition		Standard			Unit
					Min.	Typ.	Max.	
Icc	Power Supply Current (Vcc1=Vcc2=4.0V to 5.5V)	In single-chip mode, the output pins are open and other pins are Vss	Mask ROM	f(BCLK)=24MHz No division, PLL operation		14	20	mA
				No division, On-chip oscillation		1		mA
			Flash Memory	f(BCLK)=24MHz, No division, PLL operation		18	27	mA
				No division, On-chip oscillation		1.8		mA
			Flash Memory Program	f(BCLK)=10MHz, VCC1=5.0V		15		mA
			Flash Memory Erase	f(BCLK)=10MHz, VCC1=5.0V		25		mA
			Mask ROM	f(XCIN)=32kHz Low power dissipation mode, ROM ⁽³⁾		25		μA
			Flash Memory	f(BCLK)=32kHz Low power dissipation mode, RAM ⁽³⁾		25		μA
				f(BCLK)=32kHz Low power dissipation mode, Flash Memory ⁽³⁾		420		μA
				On-chip oscillation, Wait mode		50		μA
				Mask ROM Flash Memory	f(BCLK)=32kHz Wait mode ⁽²⁾ , Oscillation capability High		7.5	
			f(BCLK)=32kHz Wait mode ⁽²⁾ , Oscillation capability Low			2.0		μA
			Stop mode Topr =25°C			0.8	3.0	μA
Idet4	Low Voltage Detection Dissipation Current ⁽⁴⁾					0.7	4	μA
Idet3	Reset Area Detection Dissipation Current ⁽⁴⁾					1.2	8	μA

NOTES:

1. Referenced to V_{CC1}=V_{CC2}=4.2 to 5.5V, V_{SS} = 0V at T_{opr} = -20 to 85°C / -40 to 85°C, f(BCLK)=24MHz unless otherwise specified.
2. With one timer operated using fC32.
3. This indicates the memory in which the program to be executed exists.
4. I_{det} is dissipation current when the following bit is set to "1" (detection circuit enabled).
I_{det4}: VC27 bit in the VCR2 register
I_{det3}: VC26 bit in the VCR2 register

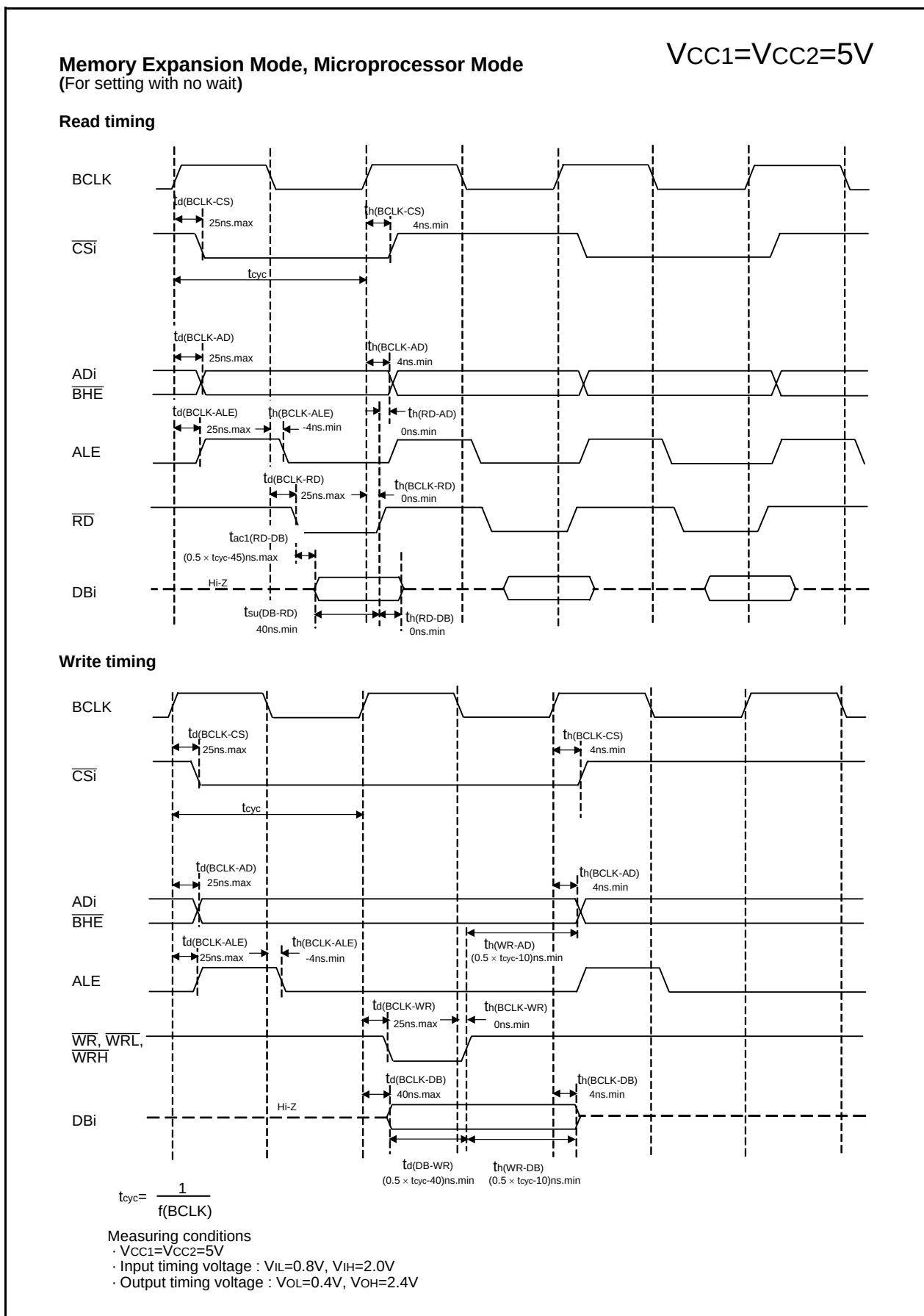


Figure 5.6 Timing Diagram (4)

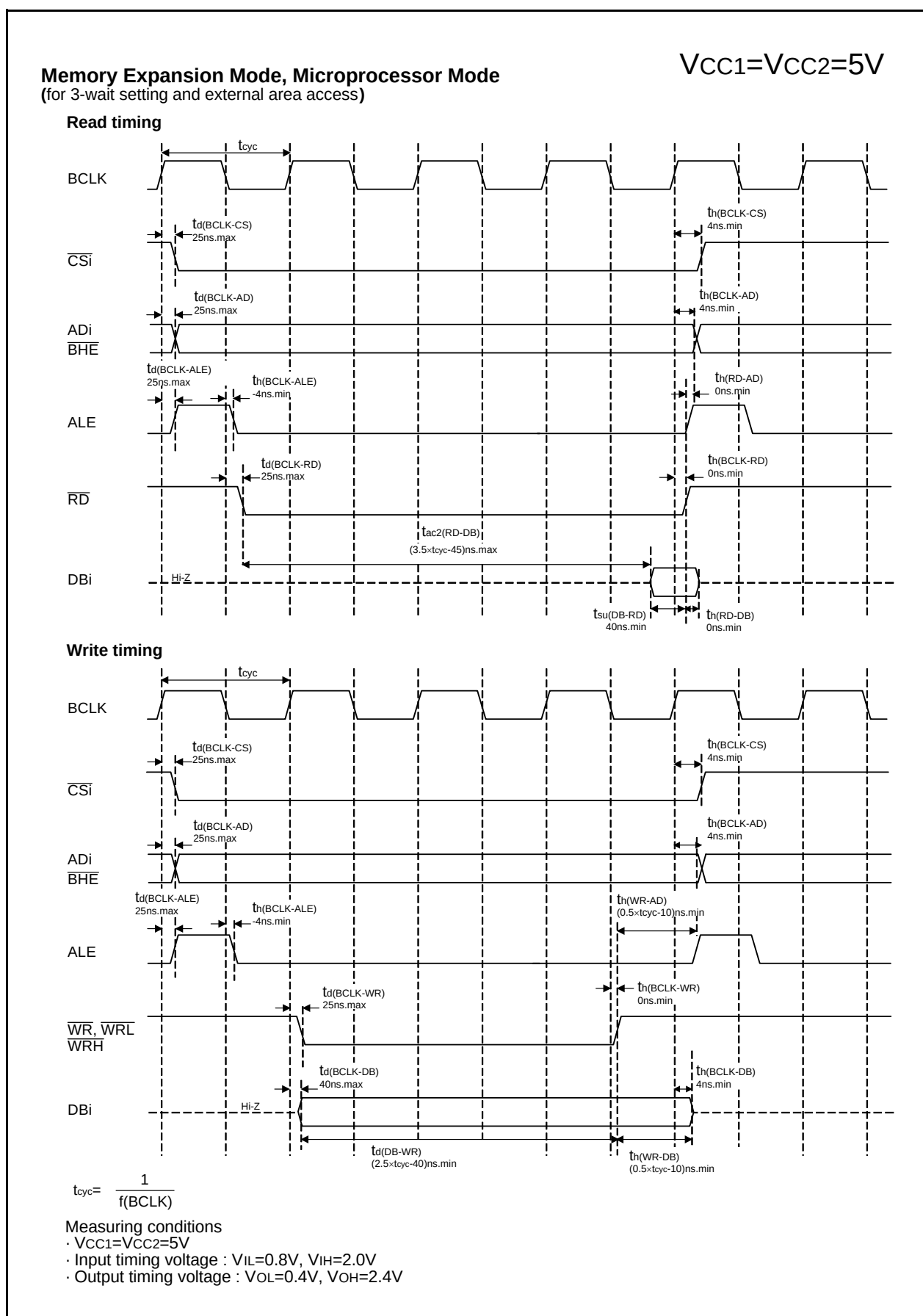
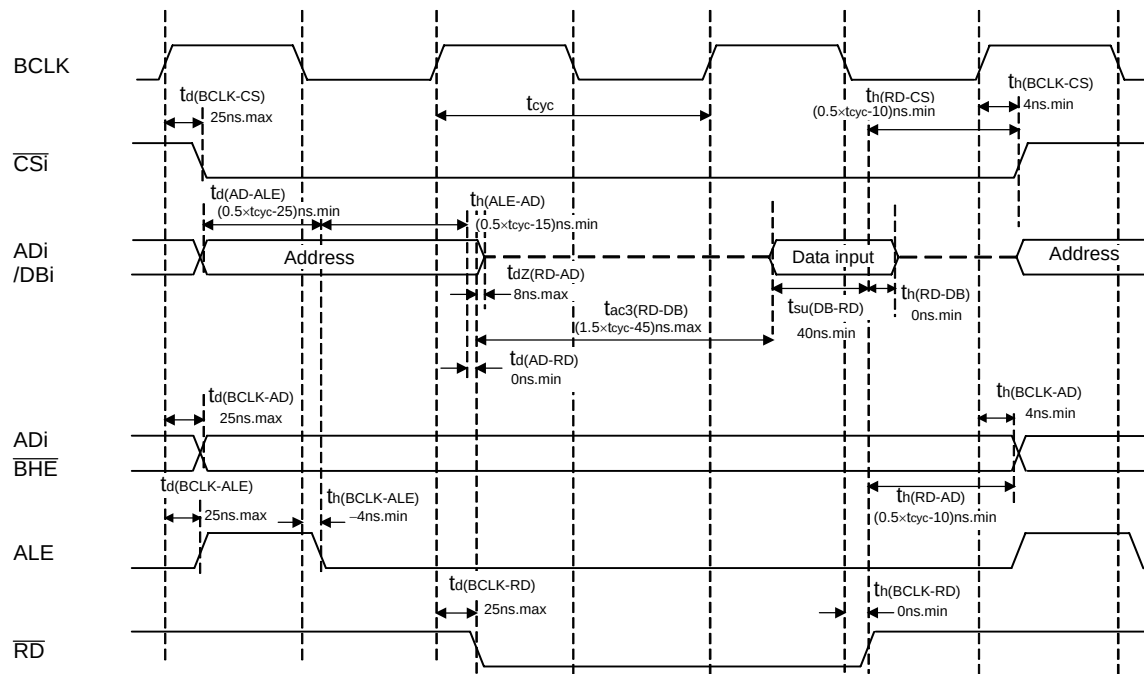
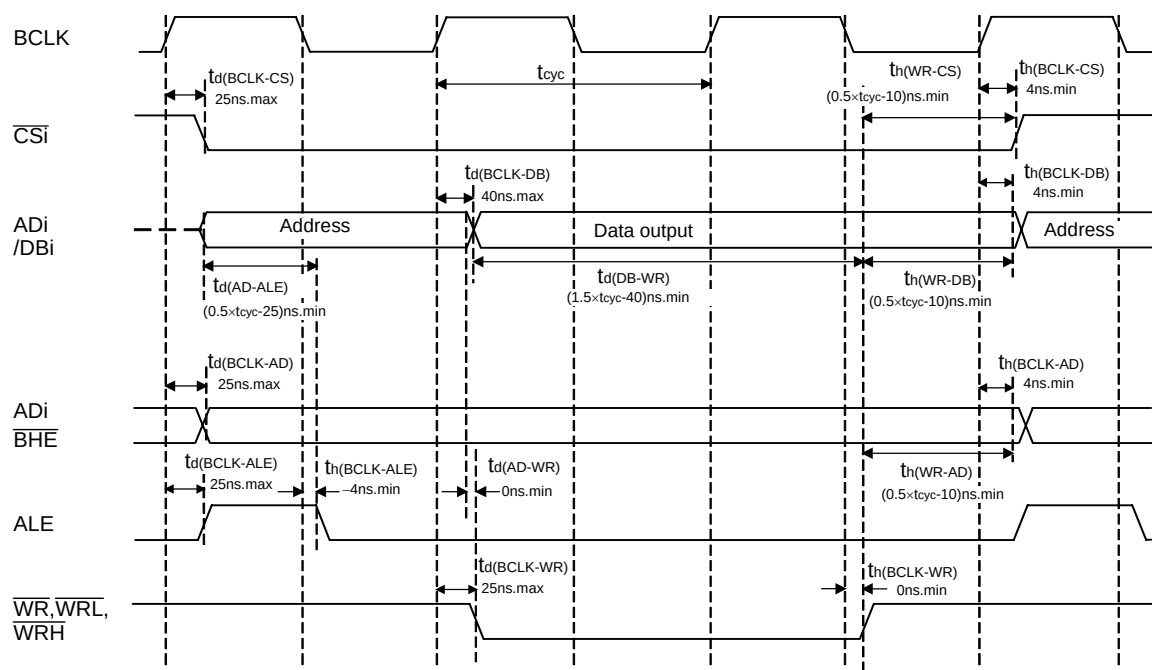


Figure 5.9 Timing Diagram (7)

VCC1=VCC2=5V

Memory Expansion Mode, Microprocessor Mode

(For 1- or 2-wait setting, external area access and multiplex bus selection)

Read timing**Write timing****Measuring conditions**

- VCC1=VCC2=5V
- Input timing voltage : $V_{IL}=0.8\text{V}$, $V_{IH}=2.0\text{V}$
- Output timing voltage : $V_{OL}=0.4\text{V}$, $V_{OH}=2.4\text{V}$

Figure 5.10 Timing Diagram (8)

$$V_{CC1}=V_{CC2}=3V$$

Switching Characteristics(V_{CC1} = V_{CC2} = 5V, V_{SS} = 0V, at T_{opr} = –20 to 85°C / –40 to 85°C unless otherwise specified)**Table 5.48 Memory Expansion and Microprocessor Modes (for 2- to 3-wait setting, external area access and multiplex bus selection)**

Symbol	Parameter		Standard		Unit
			Min.	Max.	
t _d (BCLK-AD)	Address Output Delay Time	See Figure 5.12		50	ns
t _h (BCLK-AD)	Address Output Hold Time (in relation to BCLK)		4		ns
t _h (RD-AD)	Address Output Hold Time (in relation to RD)		(NOTE 1)		ns
t _h (WR-AD)	Address Output Hold Time (in relation to WR)		(NOTE 1)		ns
t _d (BCLK-CS)	Chip Select Output Delay Time			50	ns
t _h (BCLK-CS)	Chip Select Output Hold Time (in relation to BCLK)		4		ns
t _h (RD-CS)	Chip Select Output Hold Time (in relation to RD)		(NOTE 1)		ns
t _h (WR-CS)	Chip Select Output Hold Time (in relation to WR)		(NOTE 1)		ns
t _d (BCLK-RD)	RD Signal Output Delay Time			40	ns
t _h (BCLK-RD)	RD Signal Output Hold Time		0		ns
t _d (BCLK-WR)	WR Signal Output Delay Time			40	ns
t _h (BCLK-WR)	WR Signal Output Hold Time		0		ns
t _d (BCLK-DB)	Data Output Delay Time (in relation to BCLK)			50	ns
t _h (BCLK-DB)	Data Output Hold Time (in relation to BCLK)		4		ns
t _d (DB-WR)	Data Output Delay Time (in relation to WR)		(NOTE 2)		ns
t _h (WR-DB)	Data Output Hold Time (in relation to WR)		(NOTE 1)		ns
t _d (BCLK-HLDA)	HLDA Output Delay Time			40	ns
t _d (BCLK-ALE)	ALE Signal Output Delay Time (in relation to BCLK)			25	ns
t _h (BCLK-ALE)	ALE Signal Output Hold Time (in relation to BCLK)		–4		ns
t _d (AD-ALE)	ALE Signal Output Delay Time (in relation to Address)		(NOTE 3)		ns
t _h (AD-ALE)	ALE Signal Output Hold Time (in relation to Address)		(NOTE 4)		ns
t _d (AD-RD)	RD Signal Output Delay From the End of Address		0		ns
t _d (AD-WR)	WR Signal Output Delay From the End of Address		0		ns
t _{dz} (RD-AD)	Address Output Floating Start Time			8	ns

NOTES:

1. Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f(\text{BCLK})} - 10 [\text{ns}]$$

2. Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f(\text{BCLK})} - 50 [\text{ns}] \quad n \text{ is "2" for 2-wait setting, "3" for 3-wait setting.}$$

3. Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f(\text{BCLK})} - 40 [\text{ns}]$$

4. Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f(\text{BCLK})} - 15 [\text{ns}]$$

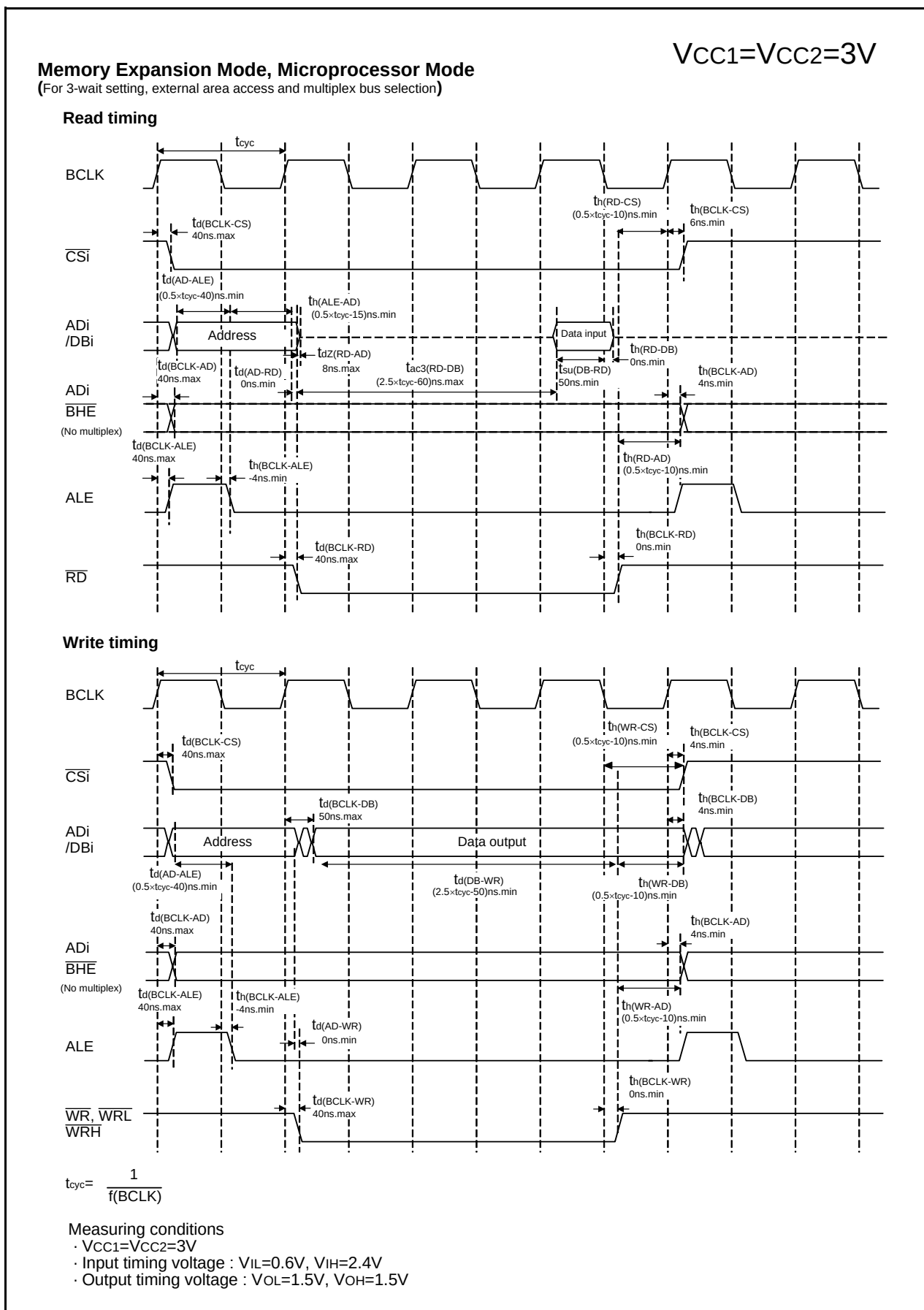


Figure 5.21 Timing Diagram (9)

Table 5.56 Power Supply Circuit Timing Characteristics

Symbol	Parameter	Measuring Condition	Standard			Unit
			Min.	Typ.	Max.	
$t_{d(P-R)}$	Time for Internal Power Supply Stabilization During Powering-On	$V_{CC1}=4.0V$ to $5.5V$			2	ms
$t_{d(R-S)}$	STOP Release Time				150	μs
$t_{d(W-S)}$	Low Power Dissipation Mode Wait Mode Release Time				150	μs

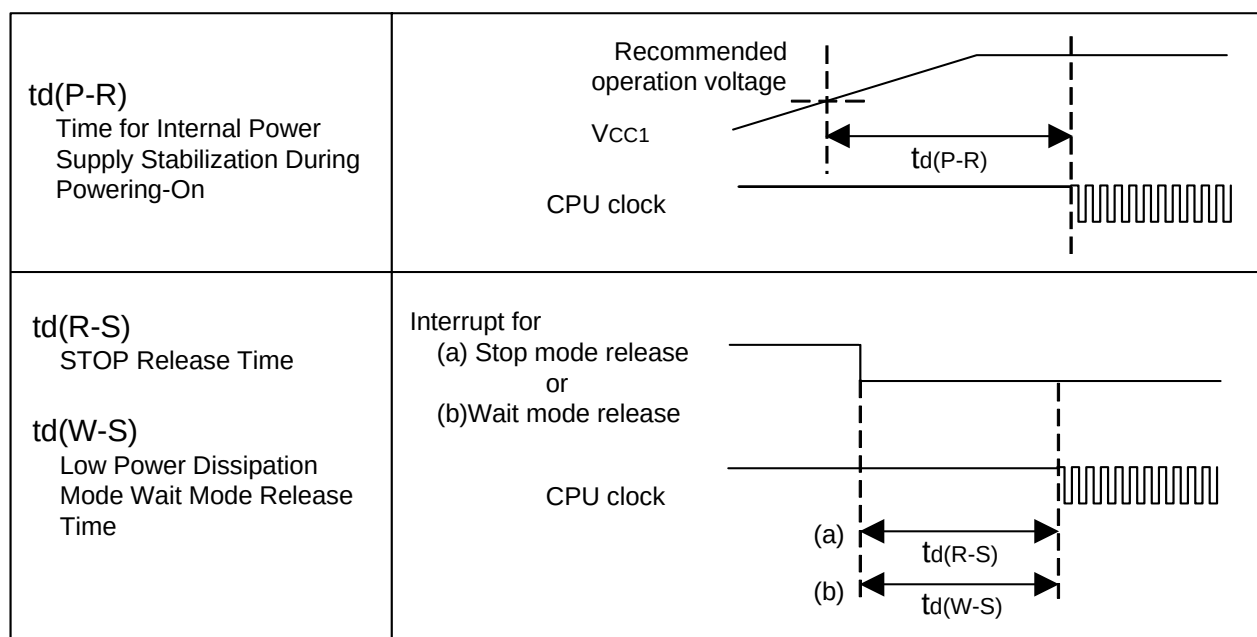
**Figure 5.22 Power Supply Circuit Timing Diagram**

Table 5.58 Electrical Characteristics (2) ⁽¹⁾

Symbol	Parameter		Measuring Condition		Standard			Unit
					Min.	Typ.	Max.	
I _{cc}	Power Supply Current (V _{CC1} =V _{CC2} =4.0V to 5.5V)	In single-chip mode, the output pins are open and other pins are V _{SS}	Mask ROM	f(BCLK)=24MHz No division, PLL operation		14	20	mA
				No division, On-chip oscillation		1		mA
			Flash Memory	f(BCLK)=24MHz, No division, PLL operation		18	27	mA
				No division, On-chip oscillation		1.8		mA
			Flash Memory Program	f(BCLK)=10MHz, V _{CC1} =5.0V		15		mA
			Flash Memory Erase	f(BCLK)=10MHz, V _{CC1} =5.0V		25		mA
			Mask ROM	f(XCIN)=32kHz Low power dissipation mode, ROM ⁽³⁾		25		μA
			Flash Memory	f(BCLK)=32kHz Low power dissipation mode, RAM ⁽³⁾		25		μA
				f(BCLK)=32kHz Low power dissipation mode, Flash Memory ⁽³⁾		420		μA
				On-chip oscillation, Wait mode		50		μA
			Mask ROM Flash Memory	f(BCLK)=32kHz Wait mode ⁽²⁾ , Oscillation capability High		7.5		μA
				f(BCLK)=32kHz Wait mode ⁽²⁾ , Oscillation capability Low		2.0		μA
				Stop mode T _{opr} =25°C		2.0	6.0	μA
				Stop mode T _{opr} =85°C			20	μA
				Stop mode T _{opr} =125°C			TBD	μA

NOTES:

1. Referenced to V_{CC1}=V_{CC2}=4.0 to 5.5V, V_{SS} = 0V at T_{opr} = -40 to 85°C / -40 to 125°C, f(BCLK)=24MHz unless otherwise specified. T version = -40 to 85°C, V version = -40 to 125°C.
2. With one timer operated using fC32.
3. This indicates the memory in which the program to be executed exists.

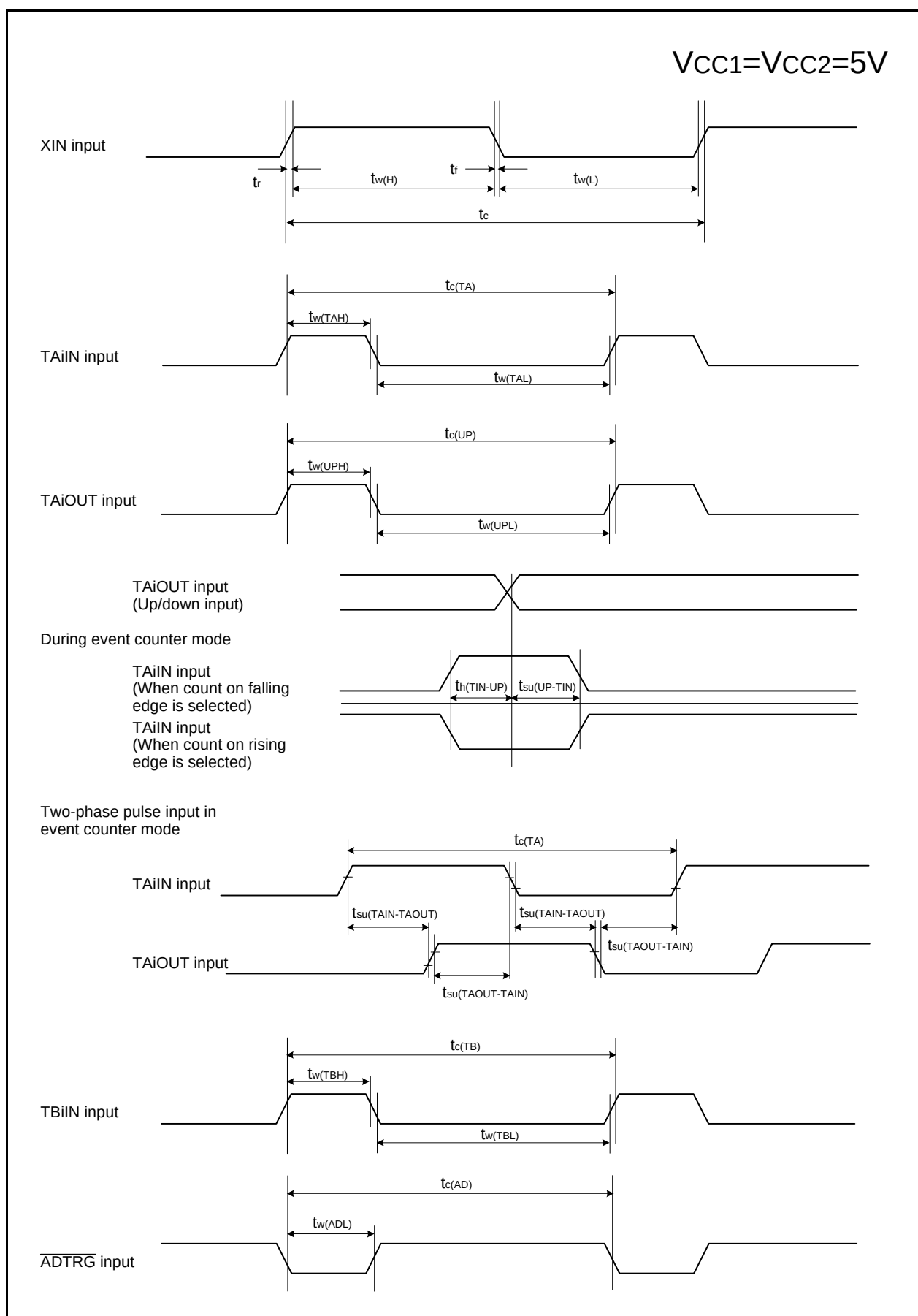


Figure 5.24 Timing Diagram (1)

REVISION HISTORY

M16C/62P Group (M16C/62P, M16C/62PT) Hardware Manual

Rev.	Date	Description	
		Page	Summary
1.10	May 28, 2003	1	Applications are partly revised.
		2	Table 1.1.1 is partly revised.
		4-5	Table 1.1.2 and 1.1.3 is partly revised. “Note 1” is partly revised.
		22	Table 1.5.3 is partly revised.
		23	Table 1.5.5 is partly revised. Table 1.5.6 is added.
		24	Table 1.5.9 is partly revised.
		30	Notes 1 and 2 in Table 1.5.26 is partly revised.
		31	Notes 1 in Table 1.5.27 is partly revised.
		30-31	Note 3 is added to “Data output hold time (refers to BCLK)” in Table 1.5.26 and 1.5.27.
		32	Note 4 is added to “th(ALE-AD)” in Table 1.5.28.
		30-32	Switching Characteristics is partly revised.
		36-39	th(WR-AD) and th(WR-DB) in Figure 1.5.5 to 1.5.8 is partly revised.
		40-41	th(ALE-AD), th(WR-CS), th(WR-DB) and th(WR-AD) in Figure 1.5.9 to 1.5.10 is partly revised.
		42	Note 2 is added to Table 1.5.29.
		47	Notes 1 and 2 in Table 1.5.45 is partly revised.
		48	Notes 1 in Table 1.5.46 is partly revised.
		47-48	Note 3 is added to “Data output hold time (refers to BCLK)” in Table 1.5.45 and 1.5.46.
		49	Note 4 is added to “th(ALE-AD)” in Table 1.5.47.
		47-48	Switching Characteristics is partly revised.
		53-56	th(WR-AD) and th(WR-DB) in Figure 1.5.15 to 1.5.18 is partly revised.
		57-58	th(ALE-AD), th(WR-CS), th(WR-DB) and th(WR-AD) in Figure 1.5.19 to 1.5.20 is partly revised.
2.00	Oct 29, 2003	-	Since high reliability version is added, a group name is revised. M16C/62 Group (M16C/62P) → M16C/62 Group (M16C/62P, M16C/62PT)
		2-4	Table 1.1 to 1.3 are revised. Note 3 is partly revised.
		2-4	Table 1.1 to 1.3 are revised. Note 3 is partly revised.
		6	Figure 1.2 Note5 is deleted.
		7-9	Table 1.4 to 1.7 Product List is partly revised.
		11	Table 1.8 and Figure 1.4 are added.
		12-15	Figure 1.5 to 1.9 ZP is added.
		17,19	Table 1.10 and 1.12 ZP is added to timer A.
		18,20	Table 1.11 and 1.13 VCC1 is added to VREF.
		30	Table 5.1 is revised.
		31-32	Table 5.2 and 5.3 are revised.

REVISION HISTORY		M16C/62P Group (M16C/62P, M16C/62PT) Hardware Manual	
Rev.	Date	Description	
		Page	Summary
		33 34,74 36 38,55 41 41-43, 58-60 44 47-48 49-50 52 53 58 61 64-65 66-67 69 70-85	Table 5.4 A-D Conversion Characteristics is revised. Table 5.5 D-A Conversion Characteristics revised. Table 5.6 to 5.7 and table 5.54 to 5.55 are revised. Table 5.11 is revised. Table 5.14 and 5.33 HLDA output deley time is deleted. Figure 5.1 is partly revised. Table 5.27 to 5.29 and table 5.46 to 48 HLDA output deley time is added. Figure 5.2 Timing Diagram (1) XIN input is added. Figure 5.5 to 5.6 Read timing DB → DBi Figure 5.7 to 5.8 Write timing DB → DBi Figure 5.10 DB → DBi Table 5.30 is revised. Figure 5.11 is partly revised. Figure 5.12 Timing Diagram (1) XIN input is added. Figure 5.15 to 5.16 Read timing DB → DBi Figure 5.17 to 5.18 Write timing DB → DBi Figure 5.20 DB → DBi Electrical Characteristics (M16C/62PT) is added.
2.10	Nov 07, 2003	8-9 23 71 72	Table 1.5 to 1.7 Product List is partly revised. Note 1 is deleted. Table 3.1 is revised. Table 5.50 is revised. Table 5.51 is deleted.
2.11	Jan 06, 2004	16 17-18 31	Table 1.9 NOTE 3 VCC1 VCC2 → VCC1 > VCC2 Table 1.10 to 1.11 NOTE 1 VCC1 VCC2 → VCC1 > VCC2 Table 5.2 Power Supply Ripple Allowable Frequency Unit MHz → kHz
2.30	Sep 01, 2004	12 18, 20 19,21 24 25 33 34 35 37	Table 1.9 and Figure 1.5 are added. Table 1.11 to 1.13 are revised. Table 1.12 to 1.14 are revised. Figure 3.1 is partly revised. Note 3 is added. Note 6 is added. Table 5.3 is revised. Note 2 in Table 5.4 is added. Table 5.5 to 5.6 is partly revised. Table 5.8 is revised. Table 5.9 is revised. Table 5.11 is revised.