Renesas Electronics America Inc - M30624FGPFP#U7C Datasheet

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	M16C/60
Core Size	16-Bit
Speed	24MHz
Connectivity	I²C, IEBus, UART/USART
Peripherals	DMA, WDT
Number of I/O	85
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	20K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 26x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-BQFP
Supplier Device Package	100-QFP (14x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/m30624fgpfp-u7c

1. Overview

The M16C/62P Group (M16C/62P, M16C/62PT) of single-chip microcomputers are built using the high performance silicon gate CMOS process using a M16C/60 Series CPU core and are packaged in a 80-pin, 100-pin and 128-pin plastic molded QFP. These single-chip microcomputers operate using sophisticated instructions featuring a high level of instruction efficiency. With 1M bytes of address space, they are capable of executing instructions at high speed. In addition, this microcomputer contains a multiplier and DMAC which combined with fast instruction processing capability, makes it suitable for control of various OA, communication, and industrial equipment which requires high-speed arithmetic/logic operations.

1.1 Applications

Audio, cameras, television, home appliance, office/communications/portable/industrial equipment, automobile, etc.

Specifications written in this manual are believed to be accurate, but are not guaranteed to be entirely free of error. Specifications in this manual may be changed for functional or performance improvements. Please make sure your manual is the latest edition.

Table 1.3 Performance Outline of M16C/62P Group (M16C/62P, M16C/62PT)(80-pin version)

	Item	Performance	
		M16C/62P	M16C/62PT(4)
CPU	Number of Basic Instructions	91 instructions	
	Minimum Instruction Execution Time	41.7ns(f(BCLK)=24MHz, VCC1=3.3 to 5.5V) 100ns(f(BCLK)=10MHz, VCC1=2.7 to 5.5V)	41.7ns(f(BCLK)=24MHz, VCC1=4.0 to 5.5V)
	Operating Mode	Single-chip mode	
	Address Space	1 Mbyte	
	Memory Capacity	See **Table 1.4 to 1.7 Product List**	
Peripheral Function	Port	Input/Output : 70 pins, Input : 1 pin	
	Multifunction Timer	Timer A : 16 bits x 5 channels (Timer A1 and A2 are internal timer), Timer B : 16 bits x 6 channels (Timer B1 is internal timer)	
	Serial Interface	2 channels Clock synchronous, UART, I2C bus(1), IEBus(2) 1 channel Clock synchronous, I2C bus(1), IEBus(2) 2 channels Clock synchronous (1 channel is only transmission)	
	A/D Converter	10-bit A/D converter: 1 circuit, 26 channels	
	D/A Converter	8 bits x 2 channels	
	DMAC	2 channels	
	CRC Calculation Circuit	CCITT-CRC	
	Watchdog Timer	15 bits x 1 channel (with prescaler)	
	Interrupt	Internal: 29 sources, External: 5 sources, Software: 4 sources, Priority level: 7 levels	
	Clock Generation Circuit	4 circuits Main clock generation circuit (*), Subclock generation circuit (*), On-chip oscillator, PLL synthesizer (*)Equipped with a built-in feedback resistor.	
	Oscillation Stop Detection Function	Stop detection of main clock oscillation, re-oscillation detection function	
	Voltage Detection Circuit	Available (option (4))	Absent
Electric Characteristics	Supply Voltage	VCC1=3.0 to 5.5 V, (f(BCLK=24MHz) VCC1=2.7 to 5.5 V, (f(BCLK=10MHz)	VCC1=4.0 to 5.5V, (f(BCLK=24MHz)
	Power Consumption	14 mA (VCC1=5V, f(BCLK)=24MHz) 8 mA (VCC1=3V, f(BCLK)=10MHz) 1.8μA (VCC1=3V, f(XCIN)=32kHz, wait mode) 0.7μA (VCC1=3V, stop mode)	14 mA (VCC1=5V, f(BCLK)=24MHz) 2.0μA (VCC1=5V, f(XCIN)=32kHz, wait mode) 0.8μA (VCC1=5V, stop mode)
Flash memory version	Program/Erase Supply Voltage	3.3 ± 0.3V or 5.0 ± 0.5V	5.0 ± 0.5V
	Program and Erase Endurance	100 times (all area) or 1,000 times (user ROM area without block A and block 1) / 10,000 times (block A, block 1) (3)	
Operating Ambient Temperature		-20 to 85°C, -40 to 85°C (3)	T version : -40 to 85°C V version : -40 to 125°C
Package		80-pin plastic mold QFP	

NOTES:
1. I2C bus is a registered trademark of Koninklijke Philips Electronics N. V.
2. IEBus is a registered trademark of NEC Electronics Corporation.
3. See **Table 1.8 and 1.9 Product Code** for the program and erase endurance, and operating ambient temperature.
   In addition 1,000 times/10,000 times are under development as of Jul., 2005. Please inquire about a release schedule.
4. All options are on request basis.

Table 1.7 Product List (4) (V version (M16C/62PT)) As of Dec. 2005

Type No.	ROM Capacity	RAM Capacity	Package Type(1)	Remarks	
M3062CM6V-XXXFP (P)	48 Kbytes	4 Kbytes	PRQP0100JB-A	Mask ROM version	V Version (High reliability 125°C version)
M3062CM6V-XXXGP (P)			PLQP0100KB-A		
M3062EM6V-XXXGP (P)			PRQP0080JA-A		
M3062CM8V-XXXFP (P)	64 Kbytes	4 Kbytes	PRQP0100JB-A		
M3062CM8V-XXXGP (P)			PLQP0100KB-A		
M3062EM8V-XXXGP (P)			PRQP0080JA-A		
M3062CMAV-XXXFP (P)	96 Kbytes	5 Kbytes	PRQP0100JB-A		
M3062CMAV-XXXGP (P)			PLQP0100KB-A		
M3062EMAV-XXXGP (P)			PRQP0080JA-A		
M3062AMCV-XXXFP (D)	128 Kbytes	10 Kbytes	PRQP0100JB-A		
M3062AMCV-XXXGP (D)			PLQP0100KB-A		
M3062BMCV-XXXGP (P)			PRQP0080JA-A		
M3062AFCVFP (D)	128K+4 Kbytes	10 Kbytes	PRQP0100JB-A	Flash memory version (2)	
M3062AFCVGP (D)			PLQP0100KB-A		
M3062BFCVGP (P)			PRQP0080JA-A		
M3062JFHVFP (P)	384K+4 Kbytes	31 Kbytes	PRQP0100JB-A		
M3062JFHVGP (P)			PLQP0100KB-A		

(D): Under development
(P): Under planning
NOTES:
1. The old package type numbers of each package type are as follows.
   PLQP0128KB-A : 128P6Q-A,
   PRQP0100JB-A : 100P6S-A,
   PLQP0100KB-A : 100P6Q-A,
   PRQP0080JA-A : 80P6S-A
2. In the flash memory version, there is 4K bytes area (block A).

Table 1.18 Pin Description (100-pin and 128-pin Version) (2)

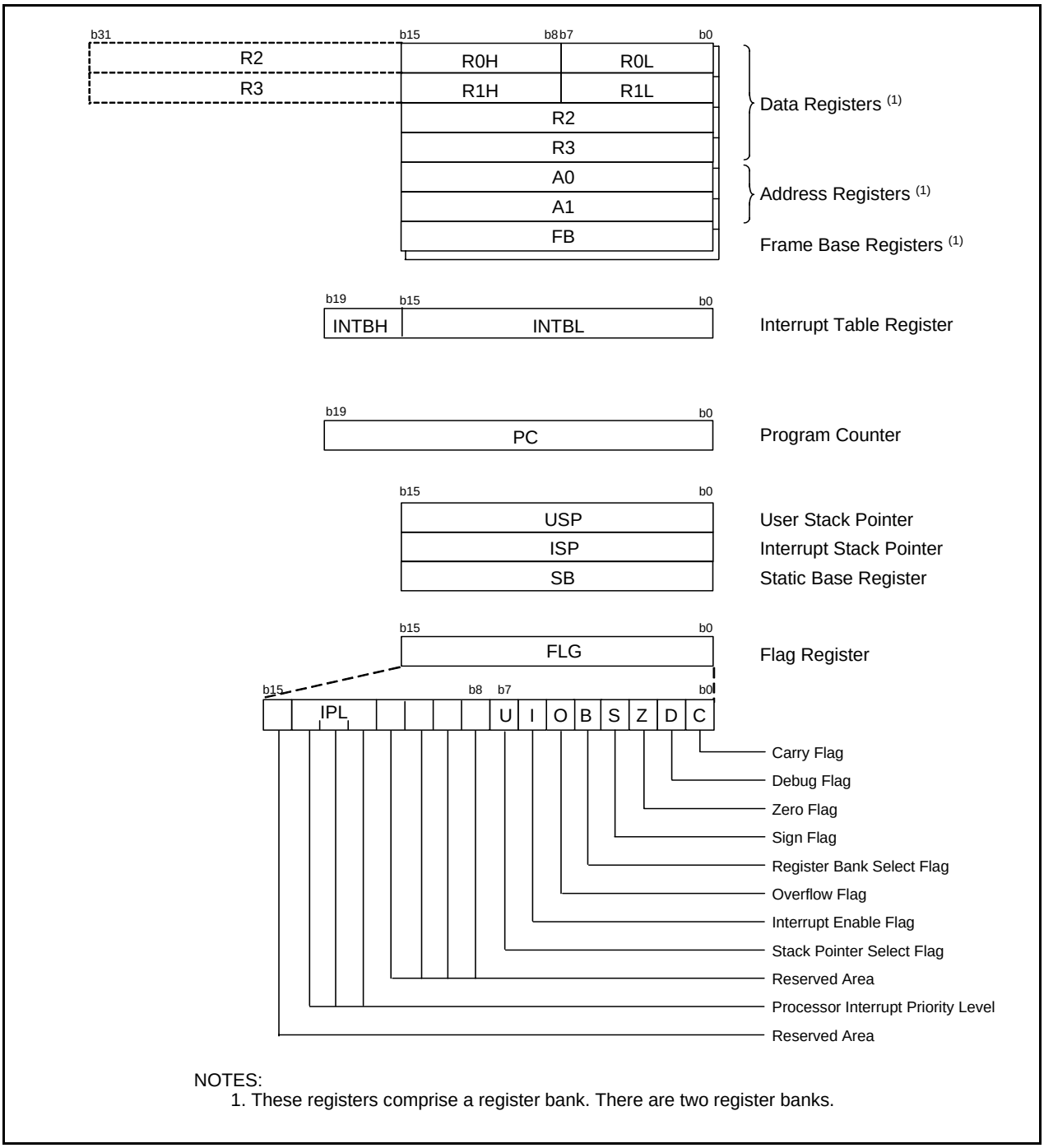
Signal Name	Pin Name	I/O Type	Power Supply(1)	Description
Main clock input	XIN	I	VCC1	I/O pins for the main clock generation circuit. Connect a ceramic resonator or crystal oscillator between XIN and XOUT (3). To use the external clock, input the clock from XIN and leave XOUT open.
Main clock output	XOUT	O	VCC1	
Sub clock input	XCIN	I	VCC1	I/O pins for a sub clock oscillation circuit. Connect a crystal oscillator between XCIN and XCOUT (3). To use the external clock, input the clock from XCIN and leave XCOUT open.
Sub clock output	XCOUT	O	VCC1	
BCLK output (2)	BCLK	O	VCC2	Outputs the BCLK signal.
Clock output	CLKOUT	O	VCC2	The clock of the same cycle as fC, f8, or f32 is outputted.
$\overline{\text{INT}}$ interrupt input	$\overline{\text{INT0}}$ to $\overline{\text{INT2}}$	I	VCC1	Input pins for the $\overline{\text{INT}}$ interrupt.
	$\overline{\text{NT3}}$ to $\overline{\text{INT5}}$	I	VCC2	
$\overline{\text{NMI}}$ interrupt input	$\overline{\text{NMI}}$	I	VCC1	Input pin for the $\overline{\text{NMI}}$ interrupt. Pin states can be read by the P8_5 bit in the P8 register.
Key input interrupt input	$\overline{\text{KI0}}$ to $\overline{\text{KI3}}$	I	VCC1	Input pins for the key input interrupt.
Timer A	TA0OUT to TA4OUT	I/O	VCC1	These are timer A0 to timer A4 I/O pins. (however, output of TA0OUT for the N-channel open drain output.)
	TA0IN to TA4IN	I	VCC1	These are timer A0 to timer A4 input pins.
	ZP	I	VCC1	Input pin for the Z-phase.
Timer B	TB0IN to TB5IN	I	VCC1	These are timer B0 to timer B5 input pins.
Three-phase motor control output	U, $\overline{\text{U}}$, V, $\overline{\text{V}}$, W, $\overline{\text{W}}$	O	VCC1	These are Three-phase motor control output pins.
Serial interface	$\overline{\text{CTS0}}$ to $\overline{\text{CTS2}}$	I	VCC1	These are send control input pins.
	$\overline{\text{RTS0}}$ to $\overline{\text{RTS2}}$	O	VCC1	These are receive control output pins.
	CLK0 to CLK4	I/O	VCC1	These are transfer clock I/O pins.
	RXD0 to RXD2	I	VCC1	These are serial data input pins.
	SIN3, SIN4	I	VCC1	These are serial data input pins.
	TXD0 to TXD2	O	VCC1	These are serial data output pins. (however, output of TXD2 for the N-channel open drain output.)
	SOUT3, SOUT4	O	VCC1	These are serial data output pins.
	CLKS1	O	VCC1	This is output pin for transfer clock output from multiple pins function.
I^2C mode	SDA0 to SDA2	I/O	VCC1	These are serial data I/O pins. (however, output of SDA2 for the N-channel open drain output.)
	SCL0 to SCL2	I/O	VCC1	These are transfer clock I/O pins. (however, output of SCL2 for the N-channel open drain output.)

I : Input O : Output I/O : Input and output

NOTES:
1. When use VCC1 > VCC2, contacts due to some points or restrictions to be checked.
2. This pin function in M16C/62PT cannot be used.
3. Ask the oscillator maker the oscillation characteristic.

2. Central Processing Unit (CPU)

Figure 2.1 shows the CPU registers. The CPU has 13 registers. Of these, R0, R1, R2, R3, A0, A1 and FB comprise a register bank. There are two register banks.



NOTES:
1. These registers comprise a register bank. There are two register banks.

Figure 2.1 Central Processing Unit Register

2.1 Data Registers (R0, R1, R2 and R3)

The R0 register consists of 16 bits, and is used mainly for transfers and arithmetic/logic operations. R1 to R3 are the same as R0.

The R0 register can be separated between high (R0H) and low (R0L) for use as two 8-bit data registers.

R1H and R1L are the same as R0H and R0L. Conversely, R2 and R0 can be combined for use as a 32-bit data register (R2R0). R3R1 is the same as R2R0.

2.2 Address Registers (A0 and A1)

The register A0 consists of 16 bits, and is used for address register indirect addressing and address register relative addressing. They also are used for transfers and logic/logic operations. A1 is the same as A0.
In some instructions, registers A1 and A0 can be combined for use as a 32-bit address register (A1A0).

2.3 Frame Base Register (FB)

FB is configured with 16 bits, and is used for FB relative addressing.

2.4 Interrupt Table Register (INTB)

INTB is configured with 20 bits, indicating the start address of an interrupt vector table.

2.5 Program Counter (PC)

PC is configured with 20 bits, indicating the address of an instruction to be executed.

2.6 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

Stack pointer (SP) comes in two types: USP and ISP, each configured with 16 bits.
Your desired type of stack pointer (USP or ISP) can be selected by the U flag of FLG.

2.7 Static Base Register (SB)

SB is configured with 16 bits, and is used for SB relative addressing.

2.8 Flag Register (FLG)

FLG consists of 11 bits, indicating the CPU status.

2.8.1 Carry Flag (C Flag)

This flag retains a carry, borrow, or shift-out bit that has occurred in the arithmetic/logic unit.

2.8.2 Debug Flag (D Flag)

The D flag is used exclusively for debugging purpose. During normal use, it must be set to “0”.

2.8.3 Zero Flag (Z Flag)

This flag is set to “1” when an arithmetic operation resulted in 0; otherwise, it is “0”.

2.8.4 Sign Flag (S Flag)

This flag is set to “1” when an arithmetic operation resulted in a negative value; otherwise, it is “0”.

2.8.5 Register Bank Select Flag (B Flag)

Register bank 0 is selected when this flag is “0” ; register bank 1 is selected when this flag is “1”.

2.8.6 Overflow Flag (O Flag)

This flag is set to “1” when the operation resulted in an overflow; otherwise, it is “0”.

2.8.7 Interrupt Enable Flag (I Flag)

This flag enables a maskable interrupt.
Maskable interrupts are disabled when the I flag is “0”, and are enabled when the I flag is “1”. The I flag is cleared to “0” when the interrupt request is accepted.

Table 5.4 A/D Conversion Characteristics (1)

Symbol	Parameter		Measuring Condition		Standard			Unit
					Min.	Typ.	Max.	
–	Resolution		$V_{REF}=V_{CC1}$				10	Bits
INL	Integral Non-Linearity Error	10bit	$V_{REF}=V_{CC1}=5V$	AN0 to AN7 input, AN0_0 to AN0_7 input, AN2_0 to AN2_7 input, ANEX0, ANEX1 input			±3	LSB
				External operation amp connection mode			±7	LSB
			$V_{REF}=V_{CC1}=3.3V$	AN0 to AN7 input, AN0_0 to AN0_7 input, AN2_0 to AN2_7 input, ANEX0, ANEX1 input			±5	LSB
				External operation amp connection mode			±7	LSB
		8bit	$V_{REF}=V_{CC1}$=5V, 3.3V				±2	LSB
–	Absolute Accuracy	10bit	$V_{REF}=V_{CC1}=5V$	AN0 to AN7 input, AN0_0 to AN0_7 input, AN2_0 to AN2_7 input, ANEX0, ANEX1 input			±3	LSB
				External operation amp connection mode			±7	LSB
			$V_{REF}=V_{CC1}=3.3V$	AN0 to AN7 input, AN0_0 to AN0_7 input, AN2_0 to AN2_7 input, ANEX0, ANEX1 input			±5	LSB
				External operation amp connection mode			±7	LSB
		8bit	$V_{REF}=V_{CC1}$=5V, 3.3V				±2	LSB
–	Tolerance Level Impedance					3		kΩ
DNL	Differential Non-Linearity Error						±1	LSB
–	Offset Error						±3	LSB
–	Gain Error						±3	LSB
R_{LADDER}	Ladder Resistance		$V_{REF}=V_{CC1}$		10		40	kΩ
t_{CONV}	10-bit Conversion Time, Sample & Hold Available		$V_{REF}=V_{CC1}$=5V, ϕAD=12MHz		2.75			µs
t_{CONV}	8-bit Conversion Time, Sample & Hold Available		$V_{REF}=V_{CC1}$=5V, ϕAD=12MHz		2.33			µs
t_{SAMP}	Sampling Time				0.25			µs
V_{REF}	Reference Voltage				2.0		V_{CC1}	V
V_{IA}	Analog Input Voltage				0		V_{REF}	V

NOTES:
1. Referenced to $V_{CC1}=AV_{CC}=V_{REF}$=3.3 to 5.5V, $V_{SS}=AV_{SS}$=0V at T_{opr} = −20 to 85°C / −40 to 85°C unless otherwise specified.
2. If $V_{CC1} > V_{CC2}$, do not use AN0_0 to AN0_7 and AN2_0 to AN2_7 as analog input pins.
3. ϕAD frequency must be 12 MHz or less. And divide the fAD if V_{CC1} is less than 4.0V, and ϕAD frequency into 10 MHz or less.
4. When sample & hold is disabled, ϕAD frequency must be 250 kHz or more, in addition to the limitation in Note 3.
   When sample & hold is enabled, ϕAD frequency must be 1MHz or more, in addition to the limitation in Note 3.

Table 5.9 Low Voltage Detection Circuit Electrical Characteristics

Symbol	Parameter	Measuring Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{det4}	Low Voltage Detection Voltage (1)	V_{CC1}=0.8V to 5.5V	3.3	3.8	4.4	V
V_{det3}	Reset Level Detection Voltage (1, 2)		2.2	2.8	3.6	V
V_{det4}-V_{det3}	Electric potential difference of Low Voltage Detection and Reset Level Detection		0.3			V
V_{det3s}	Low Voltage Reset Retention Voltage				0.8	V
V_{det3r}	Low Voltage Reset Release Voltage (3)		2.2	2.9	4.0	V

NOTES:
1. $V_{det4} > V_{det3}$.
2. Where reset level detection voltage is less than 2.7 V, if the supply power voltage is greater than the reset level detection voltage, the microcomputer operates with f(BCLK) ≤ 10MHz.
3. $V_{det3r} > V_{det3}$ is not guaranteed.
4. The voltage detection circuit is designed to use when VCC1 is set to 5V.

Table 5.10 Power Supply Circuit Timing Characteristics

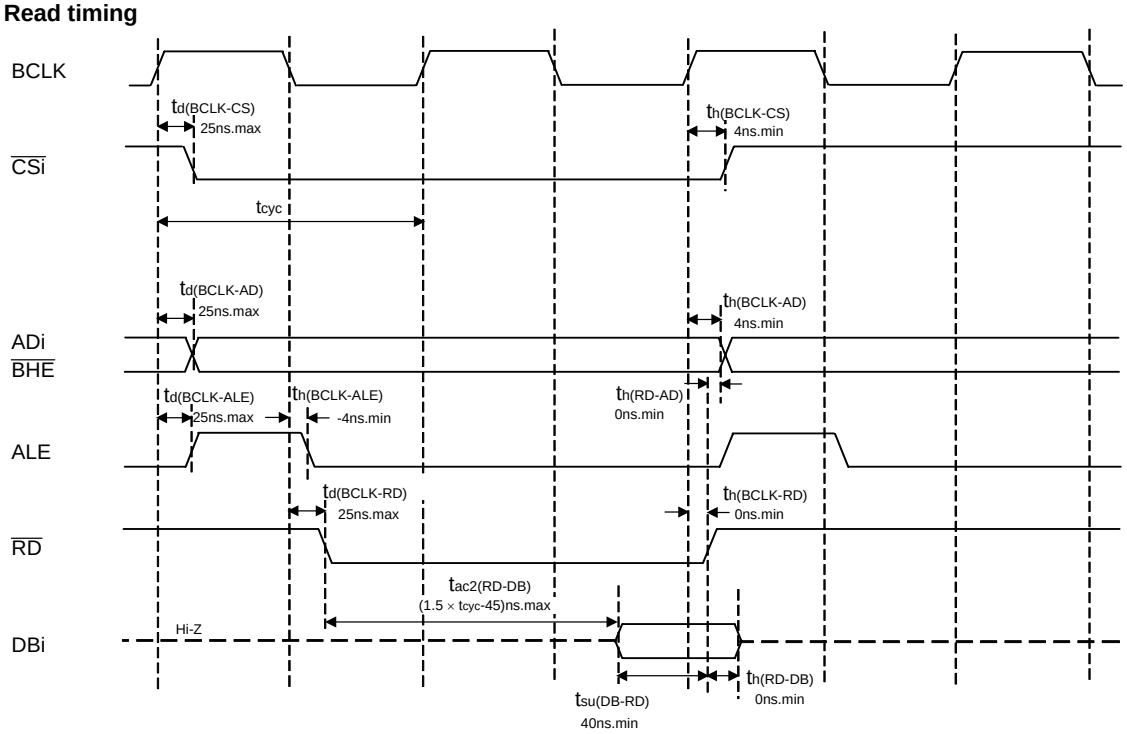
Symbol	Parameter	Measuring Condition	Standard			Unit
			Min.	Typ.	Max.	
$t_{d(P-R)}$	Time for Internal Power Supply Stabilization During Powering-On	V_{CC1}=2.7V to 5.5V			2	ms
$t_{d(R-S)}$	STOP Release Time				150	µs
$t_{d(W-S)}$	Low Power Dissipation Mode Wait Mode Release Time				150	µs
$t_{d(S-R)}$	Brown-out Detection Reset (Hardware Reset 2) Release Wait Time	V_{CC1}=V_{det3r} to 5.5V		6 (1)	20	ms
$t_{d(E-A)}$	Low Voltage Detection Circuit Operation Start Time	V_{CC1}=2.7V to 5.5V			20	µs

NOTES:
1. When V_{CC1} = 5V.

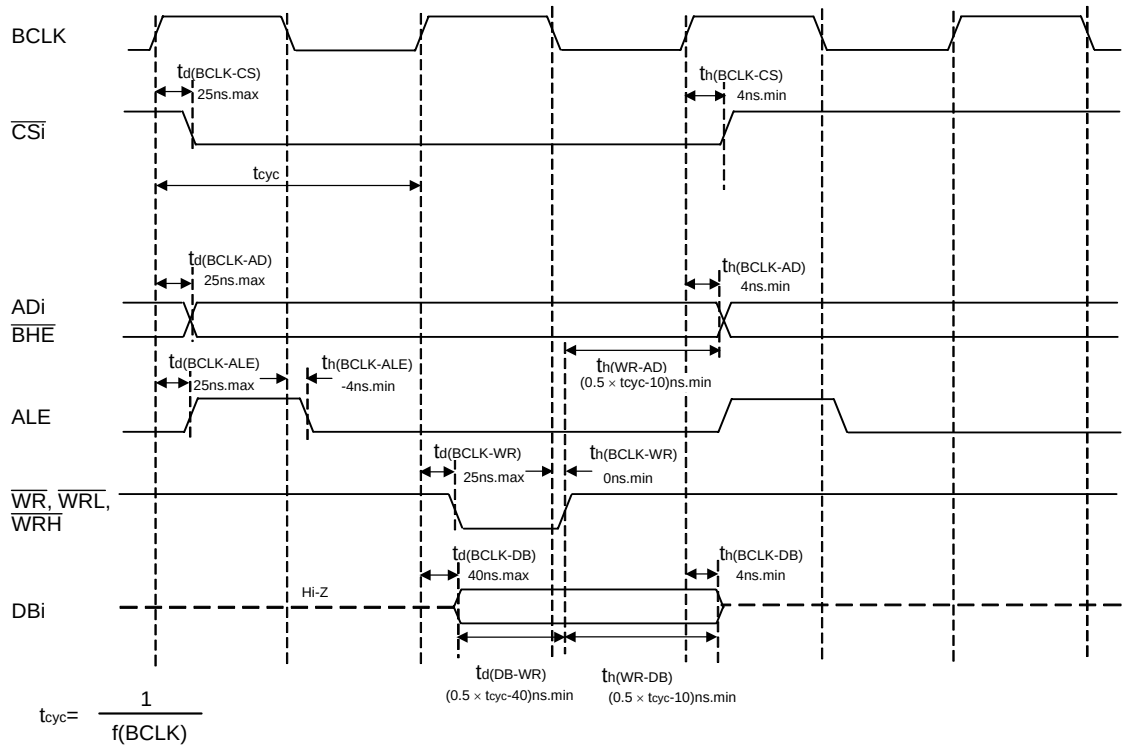
$V_{CC1}=V_{CC2}=5V$

Memory Expansion Mode, Microprocessor Mode
(for 1-wait setting and external area access**)**

Read timing



Write timing



$$t_{cyc}=\frac{1}{f(BCLK)}$$

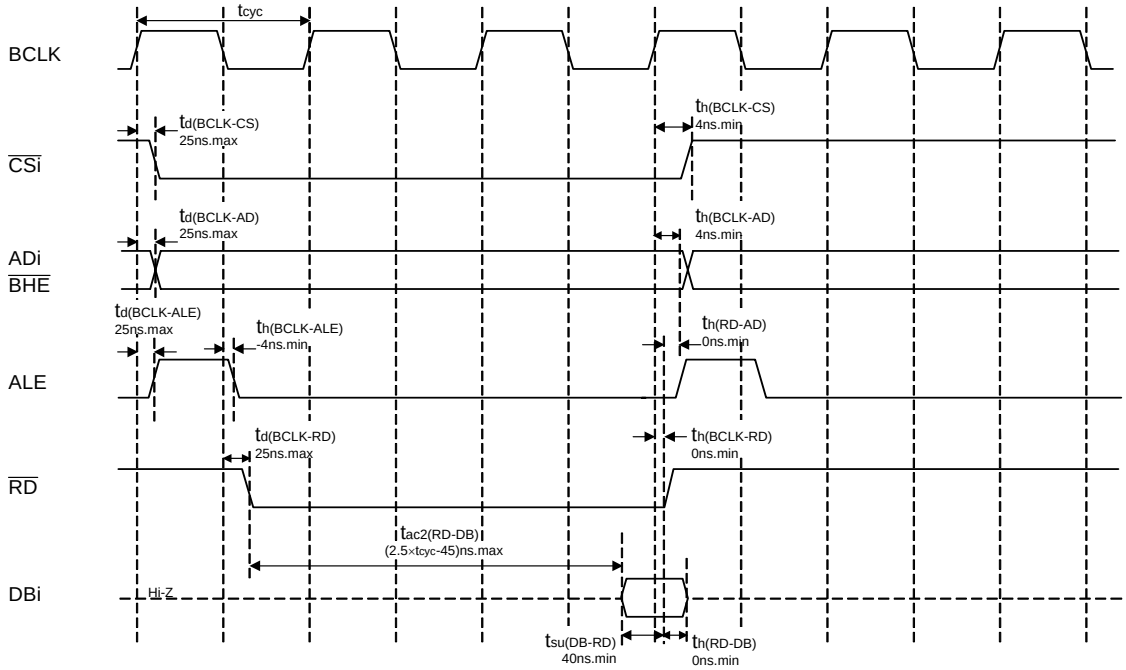
Measuring conditions
· $V_{CC1}=V_{CC2}=5V$
· Input timing voltage : $V_{IL}=0.8V$, $V_{IH}=2.0V$
· Output timing voltage : $V_{OL}=0.4V$, $V_{OH}=2.4V$

Figure 5.7 Timing Diagram (5)

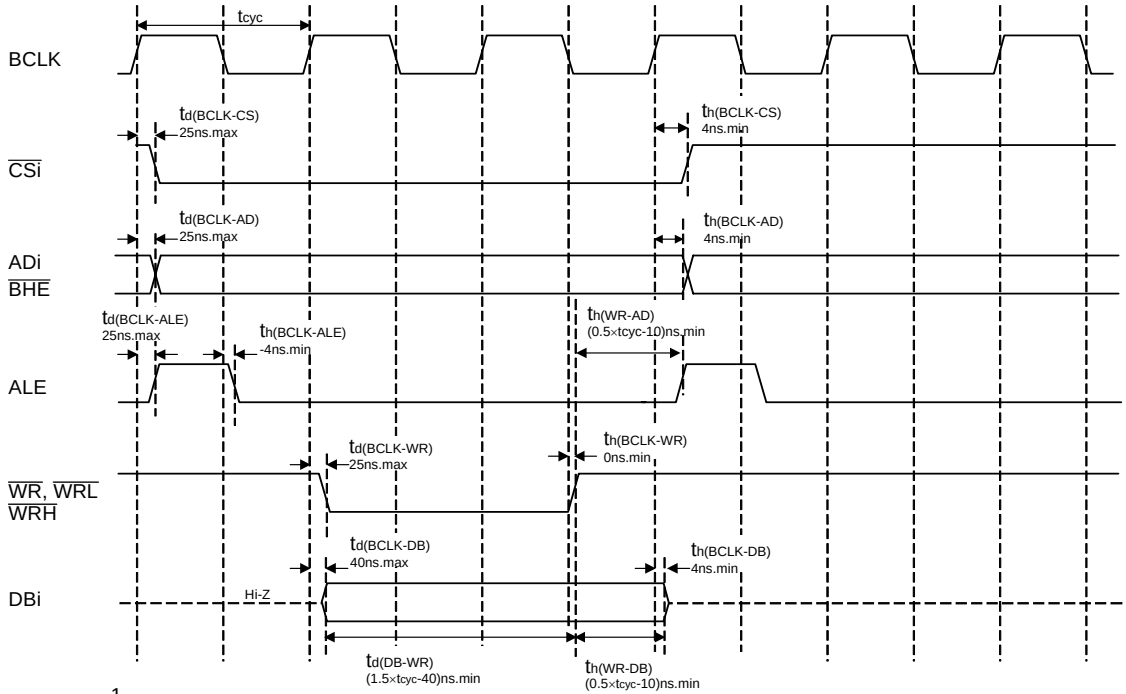
$V_{CC1}=V_{CC2}=5V$

Memory Expansion Mode, Microprocessor Mode
(for 2-wait setting and external area access**)**

Read timing



Write timing



$$T_{cyc}=\frac{1}{f(BCLK)}$$

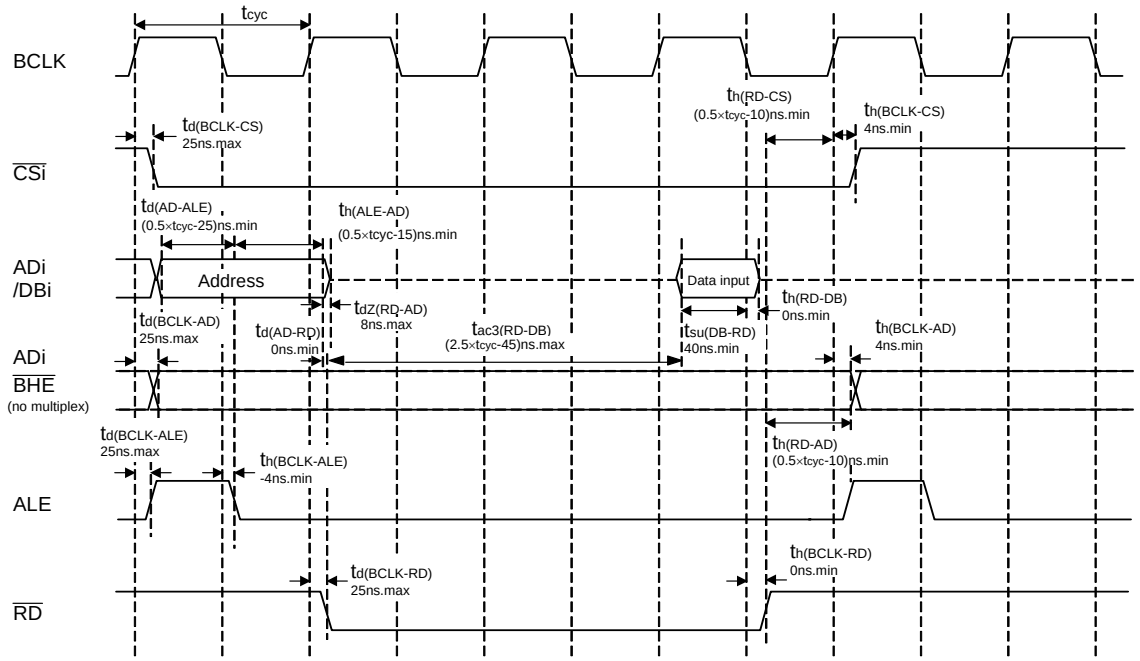
Measuring conditions
· $V_{CC1}=V_{CC2}=5V$
· Input timing voltage : $V_{IL}=0.8V$, $V_{IH}=2.0V$
· Output timing voltage : $V_{OL}=0.4V$, $V_{OH}=2.4V$

Figure 5.8 Timing Diagram (6)

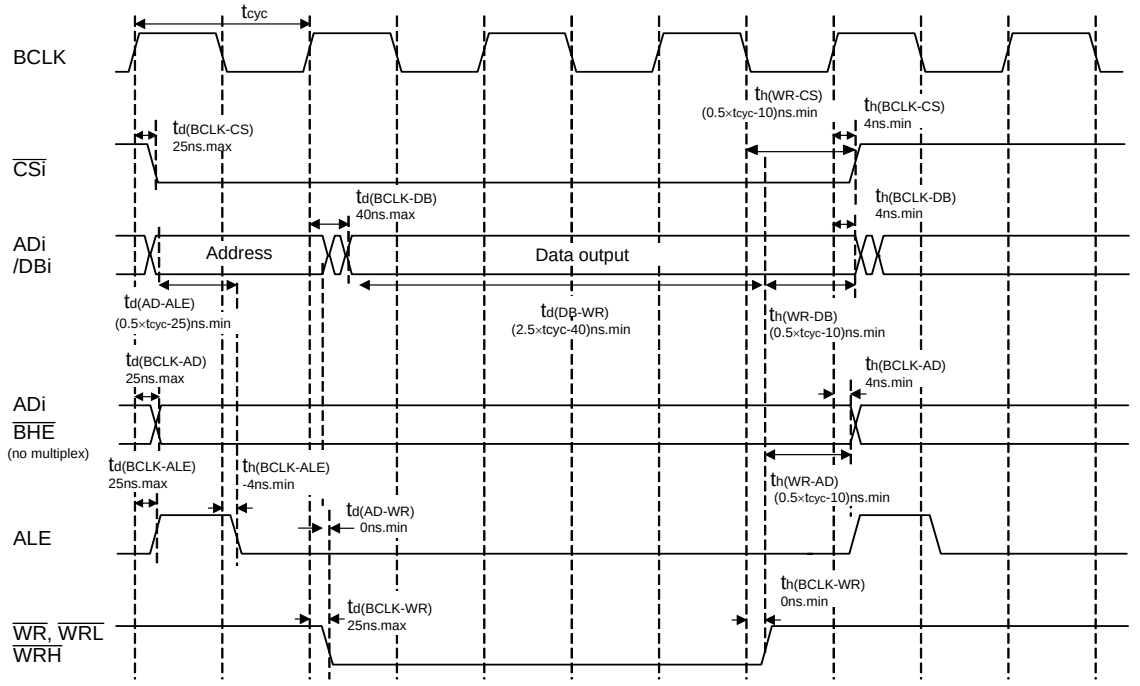
$V_{CC1}=V_{CC2}=5V$

Memory Expansion Mode, Microprocessor Mode
(For 3-wait setting, external area access and multiplex bus selection**)**

Read timing



Write timing



$$t_{cyc}=\frac{1}{f(BCLK)}$$

Measuring conditions
· $V_{CC1}=V_{CC2}=5V$
· Input timing voltage : $V_{IL}=0.8V$, $V_{IH}=2.0V$
· Output timing voltage : $V_{OL}=0.4V$, $V_{OH}=2.4V$

Figure 5.11 Timing Diagram (9)

$V_{CC1}=V_{CC2}=3V$

Table 5.30 Electrical Characteristics (1) (1)

Symbol	Parameter		Measuring Condition	Standard			Unit
				Min.	Typ.	Max.	
V_{OH}	HIGH Output Voltage (3)	P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P14_0, P14_1	I_{OH}=–1mA	V_{CC1}–0.5		V_{CC1}	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P12_0 to P12_7, P13_0 to P13_7	I_{OH}=–1mA (2)	V_{CC2}–0.5		V_{CC2}	
V_{OH}	HIGH Output Voltage XOUT	HIGHPOWER	I_{OH}=–0.1mA	V_{CC1}–0.5		V_{CC1}	V
		LOWPOWER	I_{OH}=–50µA	V_{CC1}–0.5		V_{CC1}	
	HIGH Output Voltage XCOUT	HIGHPOWER	With no load applied		2.5		V
		LOWPOWER	With no load applied		1.6		
V_{OL}	LOW Output Voltage (3)	P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P14_0, P14_1	I_{OL}=1mA			0.5	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P12_0 to P12_7, P13_0 to P13_7	I_{OL}=1mA (2)			0.5	
V_{OL}	LOW Output Voltage XOUT	HIGHPOWER	I_{OL}=0.1mA			0.5	V
		LOWPOWER	I_{OL}=50µA			0.5	
	LOW Output Voltage XCOUT	HIGHPOWER	With no load applied		0		V
		LOWPOWER	With no load applied		0		
V_{T+}-V_{T-}	Hysteresis	$\overline{HOLD}$, $\overline{RDY}$, TA0IN to TA4IN, $\overline{TB0IN}$ to $\overline{TB5IN}$, $\overline{INT0}$ to $\overline{INT5}$, $\overline{NMI}$, $\overline{ADTRG}$, $\overline{CTS0}$ to $\overline{CTS2}$, CLK0 to CLK4, TA0OUT to TA4OUT, $\overline{KI0}$ to $\overline{KI3}$, RXD0 to RXD2, SCL0 to SCL2, SDA0 to SDA2, SIN3, SIN4		0.2		0.8	V
V_{T+}-V_{T-}	Hysteresis	$\overline{RESET}$		0.2	(0.7)	1.8	V
I_{IH}	HIGH Input Current (3)	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1, XIN, $\overline{RESET}$, CNVSS, BYTE	V_I=3V			4.0	µA
I_{IL}	LOW Input Current (3)	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1, XIN, $\overline{RESET}$, CNVSS, BYTE	V_I=0V			–4.0	µA
R_{PULLUP}	Pull-Up Resistance (3)	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7,P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1	V_I=0V	50	100	500	kΩ
R_{fXIN}	Feedback Resistance XIN				3.0		MΩ
R_{fXCIN}	Feedback Resistance XCIN				25		MΩ
V_{RAM}	RAM Retention Voltage		At stop mode	2.0			V

NOTES:
1. Referenced to V_{CC1} = V_{CC2} = 2.7 to 3.3V, V_{SS} = 0V at Topr = –20 to 85°C / –40 to 85°C, f(XIN)=10MHz no wait unless otherwise specified.
2. V_{CC1} for the port P6 to P11 and P14, and V_{CC2} for the port P0 to P5 and P12 to P13
3. There is no external connections for port P1_0 to P1_7, P4_4 to P4_7, P7_2 to P7_5 and P9_1 in 80-pin version.

Table 5.31 Electrical Characteristics (2) (1)

Symbol	Parameter		Measuring Condition		Standard			Unit
					Min.	Typ.	Max.	
I_{CC}	Power Supply Current (V_{CC1}=V_{CC2}=2.7V to 3.6V)	In single-chip mode, the output pins are open and other pins are V_{SS}	Mask ROM	f(BCLK)=10MHz No division		8	11	mA
				No division, On-chip oscillation		1		mA
			Flash Memory	f(BCLK)=10MHz, No division		8	13	mA
				No division, On-chip oscillation		1.8		mA
			Flash Memory Program	f(BCLK)=10MHz, VCC1=3.0V		12		mA
			Flash Memory Erase	f(BCLK)=10MHz, VCC1=3.0V		22		mA
			Mask ROM	f(XCIN)=32kHz Low power dissipation mode, ROM (3)		25		µA
			Flash Memory	f(BCLK)=32kHz Low power dissipation mode, RAM (3)		25		µA
				f(BCLK)=32kHz Low power dissipation mode, Flash Memory (3)		420		µA
				On-chip oscillation, Wait mode		45		µA
			Mask ROM Flash Memory	f(BCLK)=32kHz Wait mode (2), Oscillation capability High		6.0		µA
				f(BCLK)=32kHz Wait mode (2), Oscillation capability Low		1.8		µA
				Stop mode Topr =25°C		0.7	3.0	µA
I_{det4}	Low Voltage Detection Dissipation Current (4)					0.6	4	µA
I_{det3}	Reset Area Detection Dissipation Current (4)					0.4	2	µA

NOTES:
1. Referenced to V_{CC1}=V_{CC2}=2.7 to 3.3V, V_{SS} = 0V at T_{opr} = –20 to 85°C / –40 to 85°C, f(BCLK)=10MHz unless otherwise specified.
2. With one timer operated using fC32.
3. This indicates the memory in which the program to be executed exists.
4. I_{det} is dissipation current when the following bit is set to “1” (detection circuit enabled).

   I_{det4}: VC27 bit in the VCR2 register

   I_{det3}: VC26 bit in the VCR2 register

$V_{CC1}=V_{CC2}=3V$

Switching Characteristics

(V_{CC1} = V_{CC2} = 3V, V_{SS} = 0V, at T_{opr} = –20 to 85°C / –40 to 85°C unless otherwise specified)

Table 5.46 Memory Expansion and Microprocessor Modes (for setting with no wait)

Symbol	Parameter		Standard		Unit
			Min.	Max.	
td(BCLK-AD)	Address Output Delay Time	See **Figure 5.12**		30	ns
th(BCLK-AD)	Address Output Hold Time (in relation to BCLK)		4		ns
th(RD-AD)	Address Output Hold Time (in relation to RD)		0		ns
th(WR-AD)	Address Output Hold Time (in relation to WR)		(NOTE 2)		ns
td(BCLK-CS)	Chip Select Output Delay Time			30	ns
th(BCLK-CS)	Chip Select Output Hold Time (in relation to BCLK)		4		ns
td(BCLK-ALE)	ALE Signal Output Delay Time			25	ns
th(BCLK-ALE)	ALE Signal Output Hold Time		–4		ns
td(BCLK-RD)	RD Signal Output Delay Time			30	ns
th(BCLK-RD)	RD Signal Output Hold Time		0		ns
td(BCLK-WR)	WR Signal Output Delay Time			30	ns
th(BCLK-WR)	WR Signal Output Hold Time		0		ns
td(BCLK-DB)	Data Output Delay Time (in relation to BCLK)			40	ns
th(BCLK-DB)	Data Output Hold Time (in relation to BCLK) (3)		4		ns
td(DB-WR)	Data Output Delay Time (in relation to WR)		(NOTE 1)		ns
th(WR-DB)	Data Output Hold Time (in relation to WR) (3)		(NOTE 2)		ns
td(BCLK-HLDA)	HLDA Output Delay Time			40	ns

NOTES:

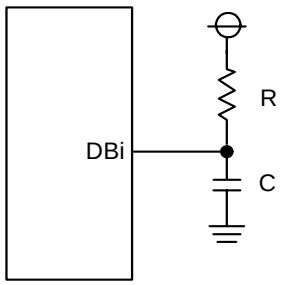
1. Calculated according to the BCLK frequency as follows:

$$\frac{0.5\times10^{9}}{f(BCLK)} - 40[ns]$$ f(BCLK) is 12.5MHz or less.

2. Calculated according to the BCLK frequency as follows:

$$\frac{0.5\times10^{9}}{f(BCLK)} - 10[ns]$$

3. This standard value shows the timing when the output is off, and does not show hold time of data bus.
   Hold time of data bus varies with capacitor volume and pull-up (pull-down) resistance value.
   Hold time of data bus is expressed in
   $t = -CR \times \ln(1 - V_{OL} / V_{CC2})$
   by a circuit of the right figure.
   For example, when $V_{OL} = 0.2V_{CC2}$, C = 30pF, R = 1kΩ, hold time of output "L" level is
   $t = -30pF \times 1k\Omega \times \ln(1 - 0.2V_{CC2} / V_{CC2})$
   = 6.7ns.



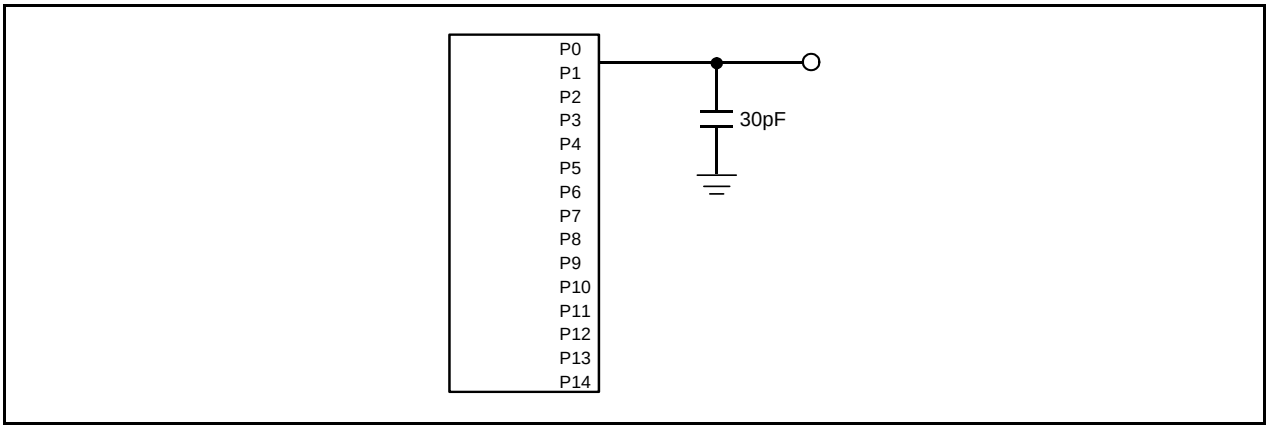


Figure 5.12 Ports P0 to P14 Measurement Circuit

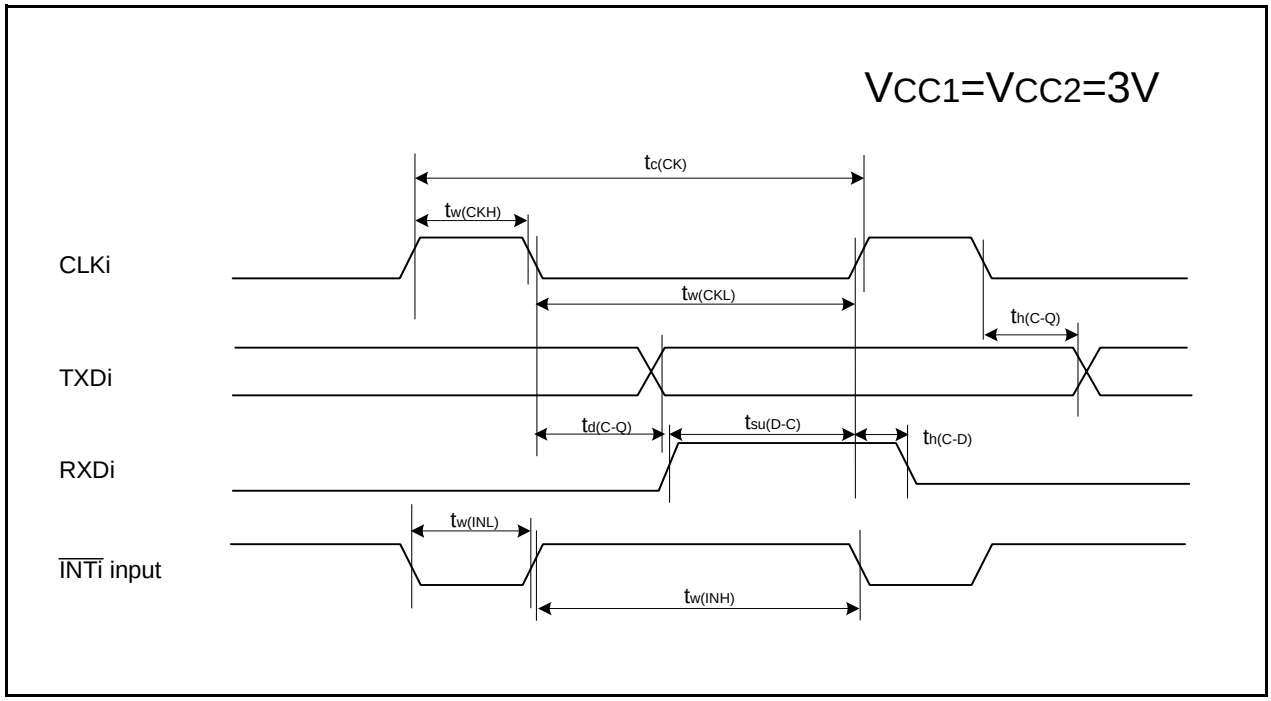
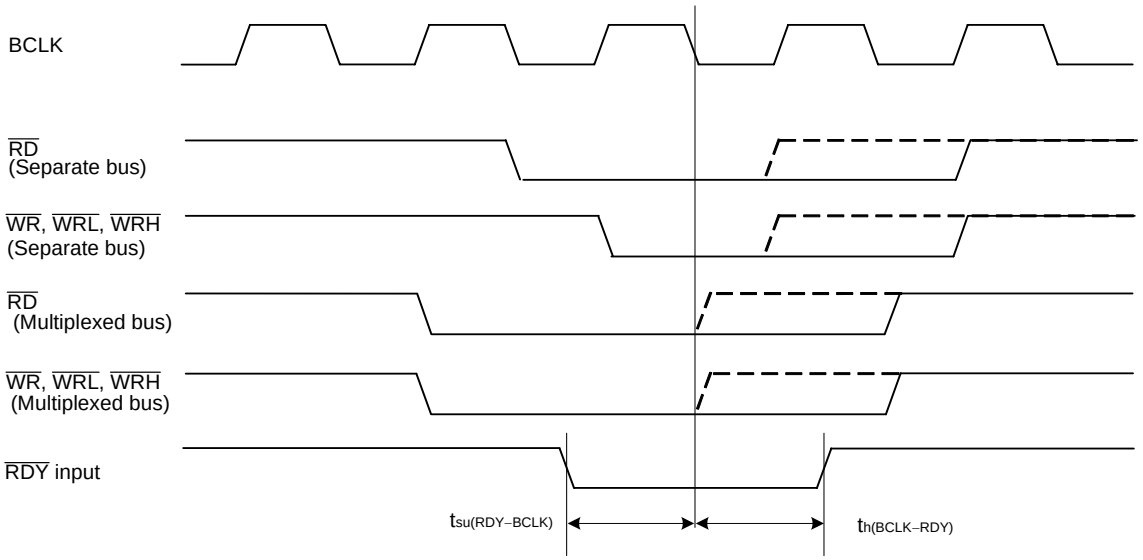


Figure 5.14 Timing Diagram (2)

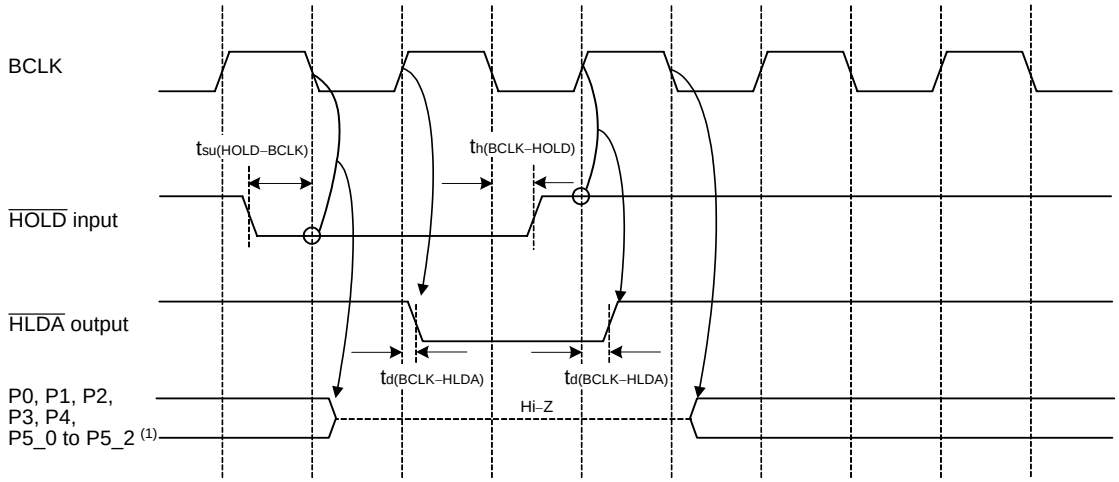
Memory Expansion Mode, Microprocessor Mode

$V_{CC1}=V_{CC2}=3V$

(Effective for setting with wait)



(Common to setting with wait and setting without wait)



NOTES:
1. These pins are set to high-impedance regardless of the input level of the BYTE pin, PM06 bit in PM0 register and PM11 bit in PM1 register.

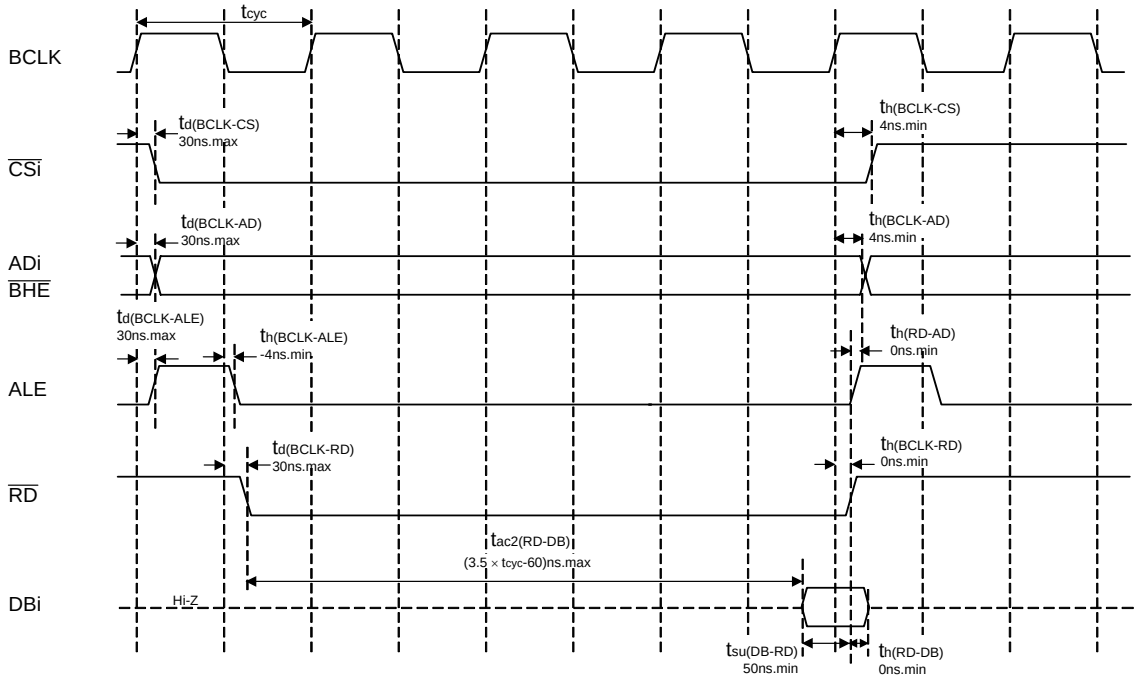
Measuring conditions :
· $V_{CC1}=V_{CC2}=3V$
· Input timing voltage : Determined with $V_{IL}=0.6V$, $V_{IH}=2.4V$
· Output timing voltage : Determined with $V_{OL}=1.5V$, $V_{OH}=1.5V$

Figure 5.15 Timing Diagram (3)

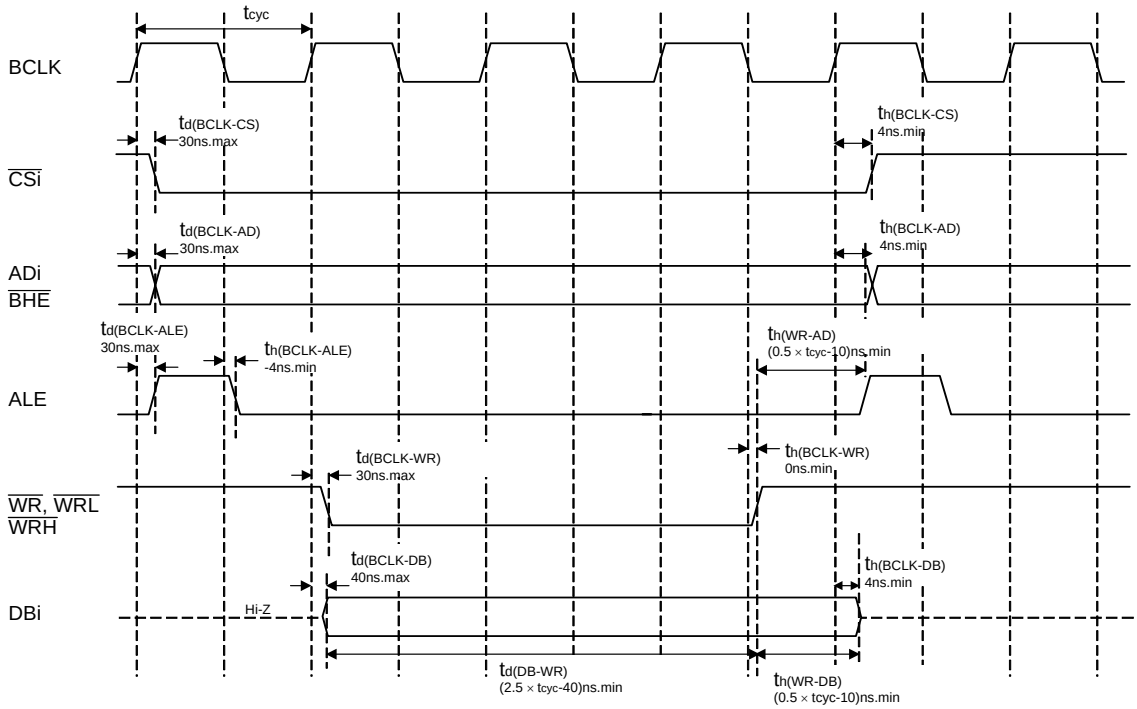
$V_{CC1} = V_{CC2} = 3V$

Memory Expansion Mode, Microprocessor Mode
(for 3-wait setting and external area access**)**

Read timing



Write timing



$$t_{cyc} = \frac{1}{f(BCLK)}$$

Measuring conditions
· V_{CC1}=V_{CC2}=3V
· Input timing voltage : V_{IL}=0.6V, V_{IH}=2.4V
· Output timing voltage : V_{OL}=1.5V, V_{OH}=1.5V

Figure 5.19 Timing Diagram (7)

V_{CC1}=V_{CC2}=5V

Timing Requirements
(V_{CC1} = V_{CC2} = 5V, V_{SS} = 0V, at T_{opr} = –40 to 85°C (T version) / –40 to 125°C (V version) unless otherwise specified)

Table 5.60 Timer A Input (Counter Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN Input Cycle Time	100		ns
$t_{w(TAH)}$	TAiIN Input HIGH Pulse Width	40		ns
$t_{w(TAL)}$	TAiIN Input LOW Pulse Width	40		ns

Table 5.61 Timer A Input (Gating Input in Timer Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN Input Cycle Time	400		ns
$t_{w(TAH)}$	TAiIN Input HIGH Pulse Width	200		ns
$t_{w(TAL)}$	TAiIN Input LOW Pulse Width	200		ns

Table 5.62 Timer A Input (External Trigger Input in One-shot Timer Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN Input Cycle Time	200		ns
$t_{w(TAH)}$	TAiIN Input HIGH Pulse Width	100		ns
$t_{w(TAL)}$	TAiIN Input LOW Pulse Width	100		ns

Table 5.63 Timer A Input (External Trigger Input in Pulse Width Modulation Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(TAH)}$	TAiIN Input HIGH Pulse Width	100		ns
$t_{w(TAL)}$	TAiIN Input LOW Pulse Width	100		ns

Table 5.64 Timer A Input (Counter Increment/Decrement Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(UP)}$	TAiOUT Input Cycle Time	2000		ns
$t_{w(UPH)}$	TAiOUT Input HIGH Pulse Width	1000		ns
$t_{w(UPL)}$	TAiOUT Input LOW Pulse Width	1000		ns
$t_{su(UP-TIN)}$	TAiOUT Input Setup Time	400		ns
$t_{h(TIN-UP)}$	TAiOUT Input Hold Time	400		ns

Table 5.65 Timer A Input (Two-phase Pulse Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN Input Cycle Time	800		ns
$t_{su(TAIN-TAOUT)}$	TAiOUT Input Setup Time	200		ns
$t_{su(TAOUT-TAIN)}$	TAiIN Input Setup Time	200		ns

$V_{CC1}=V_{CC2}=5V$

Switching Characteristics
(V_{CC1} = V_{CC2} = 5V, V_{SS} = 0V, at T_{opr} = –40 to 85°C (T version) / –40 to 125°C (V version) unless otherwise specified)

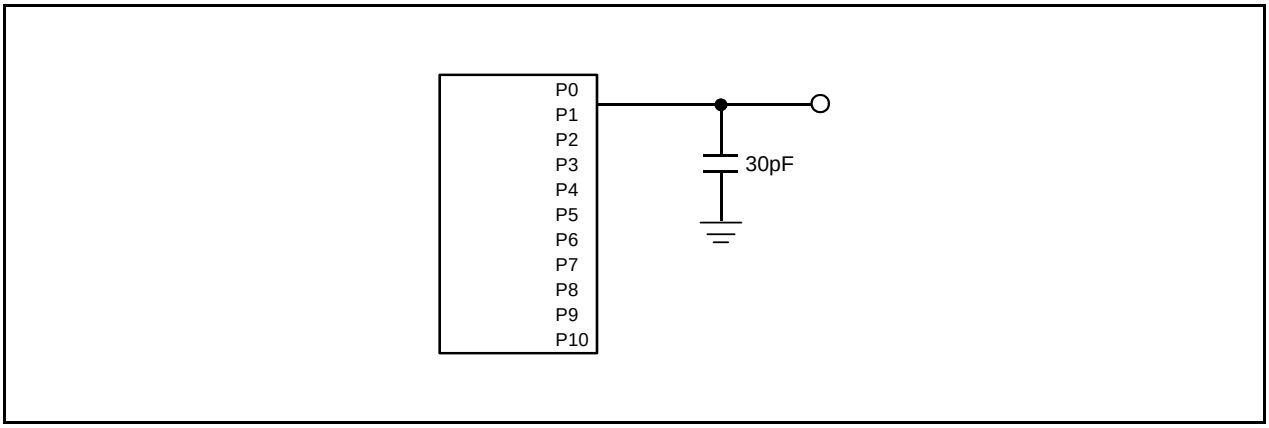


Figure 5.23 Ports P0 to P10 Measurement Circuit

Rev.	Date	Description	
		Page	Summary
		40	Table 5.24 is partly revised.
		57	Table 5.43 is partly revised.
		70	Table 5.48 is partly revised.
		72	Table 5.50 is partly revised.
		73	Table 5.53 is partly revised.
		74	Table 5.55 is revised.
		76	Table 5.57 is partly revised.
		79	Table 5.69 is partly revised.
2.41	Jan 01, 2006	-	voltage down detection reset -> brown-out detection Reset
		2-4	Tables 1.1 to 1.3 Performance outline of M16C/62P group are partly revised.
		7	Table 1.4 Product List (1) is partly revised. Note 1 is added.
		8	Table 1.5 Product List (2) is partly revised. Note 1, 2 and 3 are added.
		9	Table 1.6 Product List (3) is partly revised. Note 1 and 2 are added.
		10	Table 1.7 Product List (4) is partly revised. Note 1 and 2 are added.
		11	Figure 1.3 Type No., Memory Size, Shows RAM capacity, and Package is partly revised
		12	Table 1.8 Product Code of Flash Memory version and ROMless version for M16C/62P is partly revised.
		13	Table 1.9 Product Code of Flash Memory version for M16C/62P is partly revised.
		14	Figure 1.6 Pin Configuration (Top View) is partly revised.
		15-17	Tables 1.10 to 1.12 Pin Characteristics for 128-Pin Package are added.
		18-19	Figure 1.7 and 1.8 Pin Configuration (Top View) are partly revised.
		20-21	Tables 1.13 to 1.14 Pin Characteristics for 100-Pin Package are added.
		22	Figure 1.9 Pin Configuration (Top View) is partly revised.
		23-24	Tables 1.15 to 1.16 Pin Characteristics for 80-Pin Package are added.
		25-29	Tables 1.17 to 1.21 are partly revised.
		34	Note 4 of Table 4.1 SFR Information is partly revised.
		43	Table 5.4 A/D Conversion Characteristics is partly revised.
		45	Table 5.6 Flash Memory Version Electrical Characteristics for 100 cycle products is partly revised.
			Table 5.7 Flash Memory Version Electrical Characteristics for 10,000 cycle products is partly revised.
			Table 5.8 Flash Memory Version Program / Erase Voltage and Read Operation Voltage Characteristics is partly revised.
		46	Table 5.9 Low Voltage Detection Circuit Electrical Characteristics is partly revised.