Renesas Electronics America Inc - M30624FGPFP#U9C Datasheet

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	M16C/60
Core Size	16-Bit
Speed	24MHz
Connectivity	I²C, IEBus, UART/USART
Peripherals	DMA, WDT
Number of I/O	85
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	20K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 26x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-BQFP
Supplier Device Package	100-QFP (14x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/m30624fgpfp-u9c

1. Overview

The M16C/62P Group (M16C/62P, M16C/62PT) of single-chip microcomputers are built using the high performance silicon gate CMOS process using a M16C/60 Series CPU core and are packaged in a 80-pin, 100-pin and 128-pin plastic molded QFP. These single-chip microcomputers operate using sophisticated instructions featuring a high level of instruction efficiency. With 1M bytes of address space, they are capable of executing instructions at high speed. In addition, this microcomputer contains a multiplier and DMAC which combined with fast instruction processing capability, makes it suitable for control of various OA, communication, and industrial equipment which requires high-speed arithmetic/logic operations.

1.1 Applications

Audio, cameras, television, home appliance, office/communications/portable/industrial equipment, automobile, etc.

Specifications written in this manual are believed to be accurate, but are not guaranteed to be entirely free of error. Specifications in this manual may be changed for functional or performance improvements. Please make sure your manual is the latest edition.

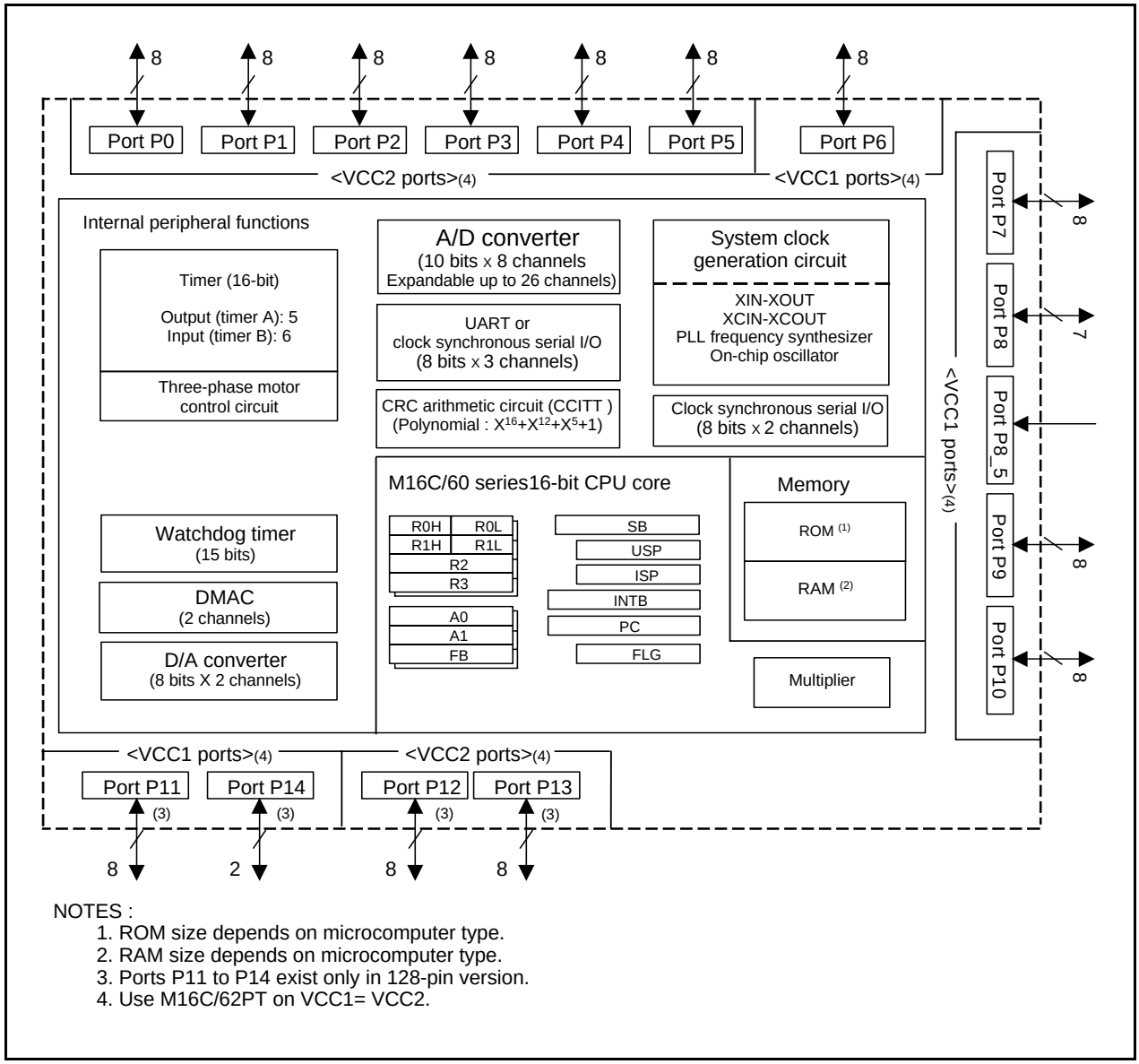
Table 1.2 Performance Outline of M16C/62P Group (M16C/62P, M16C/62PT)(100-pin version)

	Item	Performance	
		M16C/62P	M16C/62PT(4)
CPU	Number of Basic Instructions	91 instructions	
	Minimum Instruction Execution Time	41.7ns(f(BCLK)=24MHz, VCC1=3.3 to 5.5V) 100ns(f(BCLK)=10MHz, VCC1=2.7 to 5.5V)	41.7ns(f(BCLK)=24MHz, VCC1=4.0 to 5.5V)
	Operating Mode	Single-chip, memory expansion and microprocessor mode	Single-chip
	Address Space	1 Mbyte (Available to 4 Mbytes by memory space expansion function)	1 Mbyte
	Memory Capacity	See **Table 1.4 to 1.7 Product List**	
Peripheral Function	Port	Input/Output : 87 pins, Input : 1 pin	
	Multifunction Timer	Timer A : 16 bits x 5 channels, Timer B : 16 bits x 6 channels, Three phase motor control circuit	
	Serial Interface	3 channels Clock synchronous, UART, I2C bus(1), IEBus(2) 2 channels Clock synchronous	
	A/D Converter	10-bit A/D converter: 1 circuit, 26 channels	
	D/A Converter	8 bits x 2 channels	
	DMAC	2 channels	
	CRC Calculation Circuit	CCITT-CRC	
	Watchdog Timer	15 bits x 1 channel (with prescaler)	
	Interrupt	Internal: 29 sources, External: 8 sources, Software: 4 sources, Priority level: 7 levels	
	Clock Generation Circuit	4 circuits Main clock generation circuit (*), Subclock generation circuit (*), On-chip oscillator, PLL synthesizer (*)Equipped with a built-in feedback resistor.	
	Oscillation Stop Detection Function	Stop detection of main clock oscillation, re-oscillation detection function	
	Voltage Detection Circuit	Available (option (5))	Absent
Electric Characteristics	Supply Voltage	VCC1=3.0 to 5.5 V, VCC2=2.7V to VCC1 (f(BCLK=24MHz) VCC1=2.7 to 5.5 V, VCC2=2.7V to VCC1 (f(BCLK=10MHz)	VCC1=VCC2=4.0 to 5.5V (f(BCLK=24MHz)
	Power Consumption	14 mA (VCC1=VCC2=5V, f(BCLK)=24MHz) 8 mA (VCC1=VCC2=3V, f(BCLK)=10MHz) 1.8µA (VCC1=VCC2=3V, f(XCIN)=32kHz, wait mode) 0.7µA (VCC1=VCC2=3V, stop mode)	14 mA (VCC1=VCC2=5V, f(BCLK)=24MHz) 2.0µA (VCC1=VCC2=5V, f(XCIN)=32kHz, wait mode) 0.8µA (VCC1=VCC2=5V, stop mode)
Flash memory version	Program/Erase Supply Voltage	3.3±0.3 V or 5.0±0.5 V	5.0±0.5 V
	Program and Erase Endurance	100 times (all area) or 1,000 times (user ROM area without block A and block 1) / 10,000 times (block A, block 1) (3)	
Operating Ambient Temperature		-20 to 85°C, -40 to 85°C (3)	T version : -40 to 85°C V version : -40 to 125°C
Package		100-pin plastic mold QFP, LQFP	

NOTES:
1. I2C bus is a registered trademark of Koninklijke Philips Electronics N. V.
2. IEBus is a registered trademark of NEC Electronics Corporation.
3. See **Table 1.8 and 1.9 Product Code** for the program and erase endurance, and operating ambient temperature.
   In addition 1,000 times/10,000 times are under development as of Jul., 2005. Please inquire about a release schedule.
4. Use the M16C/62PT on VCC1=VCC2
5. All options are on request basis.

1.3 Block Diagram

Figure 1.1 is a M16C/62P Group (M16C/62P, M16C/62PT) 128-pin and 100-pin version Block Diagram, Figure 1.2 is a M16C/62P Group (M16C/62P, M16C/62PT) 80-pin version Block Diagram.



NOTES :
1. ROM size depends on microcomputer type.
2. RAM size depends on microcomputer type.
3. Ports P11 to P14 exist only in 128-pin version.
4. Use M16C/62PT on VCC1= VCC2.

Figure 1.1 M16C/62P Group (M16C/62P, M16C/62PT) 128-pin and 100-pin version Block Diagram

1.4 Product List

Table 1.4 to 1.7 list the product list, Figure 1.3 shows the Type No., Memory Size, and Package, Table 1.8 lists the Product Code of Flash Memory version and ROMless version for M16C/62P, and Table 1.9 lists the Product Code of Flash Memory version for M16C/62PT. Figure 1.4 shows the Marking Diagram of Flash Memory version and ROM-less version for M16C/62P (Top View), and Figure 1.5 shows the Marking Diagram of Flash Memory version for M16C/62PT (Top View) at the time of ROM order.

Table 1.4 Product List (1) (M16C/62P) As of Dec. 2005

Type No.	ROM Capacity	RAM Capacity	Package Type (1)	Remarks
M30622M6P-XXXFP	48 Kbytes	4 Kbytes	PRQP0100JB-A	Mask ROM version
M30622M6P-XXXGP			PLQP0100KB-A	
M30622M8P-XXXFP	64 Kbytes	4 Kbytes	PRQP0100JB-A	
M30622M8P-XXXGP			PLQP0100KB-A	
M30623M8P-XXXGP			PRQP0080JA-A	
M30622MAP-XXXFP	96 Kbytes	5 Kbytes	PRQP0100JB-A	
M30622MAP-XXXGP			PLQP0100KB-A	
M30623MAP-XXXGP			PRQP0080JA-A	
M30620MCP-XXXFP	128 Kbytes	10 Kbytes	PRQP0100JB-A	
M30620MCP-XXXGP			PLQP0100KB-A	
M30621MCP-XXXGP			PRQP0080JA-A	
M30622MEP-XXXFP	192 Kbytes	12 Kbytes	PRQP0100JB-A	
M30622MEP-XXXGP			PLQP0100KB-A	
M30623MEP-XXXGP			PLQP0128KB-A	
M30622MGP-XXXFP	256 Kbytes	12 Kbytes	PRQP0100JB-A	
M30622MGP-XXXGP			PLQP0100KB-A	
M30623MGP-XXXGP			PLQP0128KB-A	
M30624MGP-XXXFP		20 Kbytes	PRQP0100JB-A	
M30624MGP-XXXGP			PLQP0100KB-A	
M30625MGP-XXXGP			PLQP0128KB-A	
M30622MWP-XXXFP	320 Kbytes	16 Kbytes	PRQP0100JB-A	
M30622MWP-XXXGP			PLQP0100KB-A	
M30623MWP-XXXGP			PLQP0128KB-A	
M30624MWP-XXXFP		24 Kbytes	PRQP0100JB-A	
M30624MWP-XXXGP			PLQP0100KB-A	
M30625MWP-XXXGP			PLQP0128KB-A	
M30626MWP-XXXFP		31 Kbytes	PRQP0100JB-A	
M30626MWP-XXXGP			PLQP0100KB-A	
M30627MWP-XXXGP			PLQP0128KB-A	

(D): Under development

NOTES:

1. The old package type numbers of each package type are as follows.
   PLQP0128KB-A : 128P6Q-A,
   PRQP0100JB-A : 100P6S-A,
   PLQP0100KB-A : 100P6Q-A,
   PRQP0080JA-A : 80P6S-A

Table 1.5 Product List (2) (M16C/62P) As of Dec. 2005

Type No.	ROM Capacity	RAM Capacity	Package Type (1)	Remarks
M30622MHP-XXXFP	384 Kbytes	16 Kbytes	PRQP0100JB-A	Mask ROM version
M30622MHP-XXXGP			PLQP0100KB-A	
M30623MHP-XXXGP			PLQP0128KB-A	
M30624MHP-XXXFP		24 Kbytes	PRQP0100JB-A	
M30624MHP-XXXGP			PLQP0100KB-A	
M30625MHP-XXXGP			PLQP0128KB-A	
M30626MHP-XXXFP		31 Kbytes	PRQP0100JB-A	
M30626MHP-XXXGP			PLQP0100KB-A	
M30627MHP-XXXGP			PLQP0128KB-A	
M30626MJP-XXXFP (D)	512 Kbytes	31 Kbytes	PRQP0100JB-A	
M30626MJP-XXXGP (D)			PLQP0100KB-A	
M30627MJP-XXXGP (D)			PLQP0128KB-A	
M30622F8PFP	64K+4 Kbytes	4 Kbytes	PRQP0100JB-A	Flash memory version (2)
M30622F8PGP			PLQP0100KB-A	
M30623F8PGP			PRQP0080JA-A	
M30620FCPFP	128K+4 Kbytes	10 Kbytes	PRQP0100JB-A	
M30620FCPGP			PLQP0100KB-A	
M30621FCPGP			PRQP0080JA-A	
M3062LFGPFP(3) (D)	256K+4 Kbytes	20 Kbytes	PRQP0100JB-A	
M3062LFGPGP(3) (D)			PLQP0100KB-A	
M30625FGPGP			PLQP0128KB-A	
M30626FHPFP	384K+4 Kbytes	31 Kbytes	PRQP0100JB-A	
M30626FHPGP			PLQP0100KB-A	
M30627FHPGP			PLQP0128KB-A	
M30626FJPFP	512K+4 Kbytes	31 Kbytes	PRQP0100JB-A	
M30626FJPGP			PLQP0100KB-A	
M30627FJPGP			PLQP0128KB-A	
M30622SPFP	–	4 Kbytes	PRQP0100JB-A	ROM-less version
M30622SPGP			PLQP0100KB-A	
M30620SPFP		10 Kbytes	PRQP0100JB-A	
M30620SPGP			PLQP0100KB-A	
M30624SPFP (D)	–	20 Kbytes	PRQP0100JB-A	
M30624SPGP (D)			PLQP0100KB-A	
M30626SPFP (D)		31 Kbytes	PRQP0100JB-A	
M30626SPGP (D)			PLQP0100KB-A	

(D): Under development

NOTES:

1. The old package type numbers of each package type are as follows.
   PLQP0128KB-A : 128P6Q-A,
   PRQP0100JB-A : 100P6S-A,
   PLQP0100KB-A : 100P6Q-A,
   PRQP0080JA-A : 80P6S-A
2. In the flash memory version, there is 4K bytes area (block A).
3. Please use M3062LFGPFP and M3062LFGPGP for your new system instead of M30624FGPFP and M30624FGPGP. The M16C/62P Group (M16C/62P, M16C/62PT) hardware manual is still good for M30624FGPFP and M30624FGPGP.

M30624FGPFP	256K+4 Kbytes	20 Kbytes	PRQP0100JB-A	Flash memory version
M30624FGPGP			PLQP0100KB-A	

Table 1.7 Product List (4) (V version (M16C/62PT)) As of Dec. 2005

Type No.	ROM Capacity	RAM Capacity	Package Type(1)	Remarks	
M3062CM6V-XXXFP (P)	48 Kbytes	4 Kbytes	PRQP0100JB-A	Mask ROM version	V Version (High reliability 125°C version)
M3062CM6V-XXXGP (P)			PLQP0100KB-A		
M3062EM6V-XXXGP (P)			PRQP0080JA-A		
M3062CM8V-XXXFP (P)	64 Kbytes	4 Kbytes	PRQP0100JB-A		
M3062CM8V-XXXGP (P)			PLQP0100KB-A		
M3062EM8V-XXXGP (P)			PRQP0080JA-A		
M3062CMAV-XXXFP (P)	96 Kbytes	5 Kbytes	PRQP0100JB-A		
M3062CMAV-XXXGP (P)			PLQP0100KB-A		
M3062EMAV-XXXGP (P)			PRQP0080JA-A		
M3062AMCV-XXXFP (D)	128 Kbytes	10 Kbytes	PRQP0100JB-A		
M3062AMCV-XXXGP (D)			PLQP0100KB-A		
M3062BMCV-XXXGP (P)			PRQP0080JA-A		
M3062AFCVFP (D)	128K+4 Kbytes	10 Kbytes	PRQP0100JB-A	Flash memory version (2)	
M3062AFCVGP (D)			PLQP0100KB-A		
M3062BFCVGP (P)			PRQP0080JA-A		
M3062JFHVFP (P)	384K+4 Kbytes	31 Kbytes	PRQP0100JB-A		
M3062JFHVGP (P)			PLQP0100KB-A		

(D): Under development
(P): Under planning
NOTES:
1. The old package type numbers of each package type are as follows.
   PLQP0128KB-A : 128P6Q-A,
   PRQP0100JB-A : 100P6S-A,
   PLQP0100KB-A : 100P6Q-A,
   PRQP0080JA-A : 80P6S-A
2. In the flash memory version, there is 4K bytes area (block A).

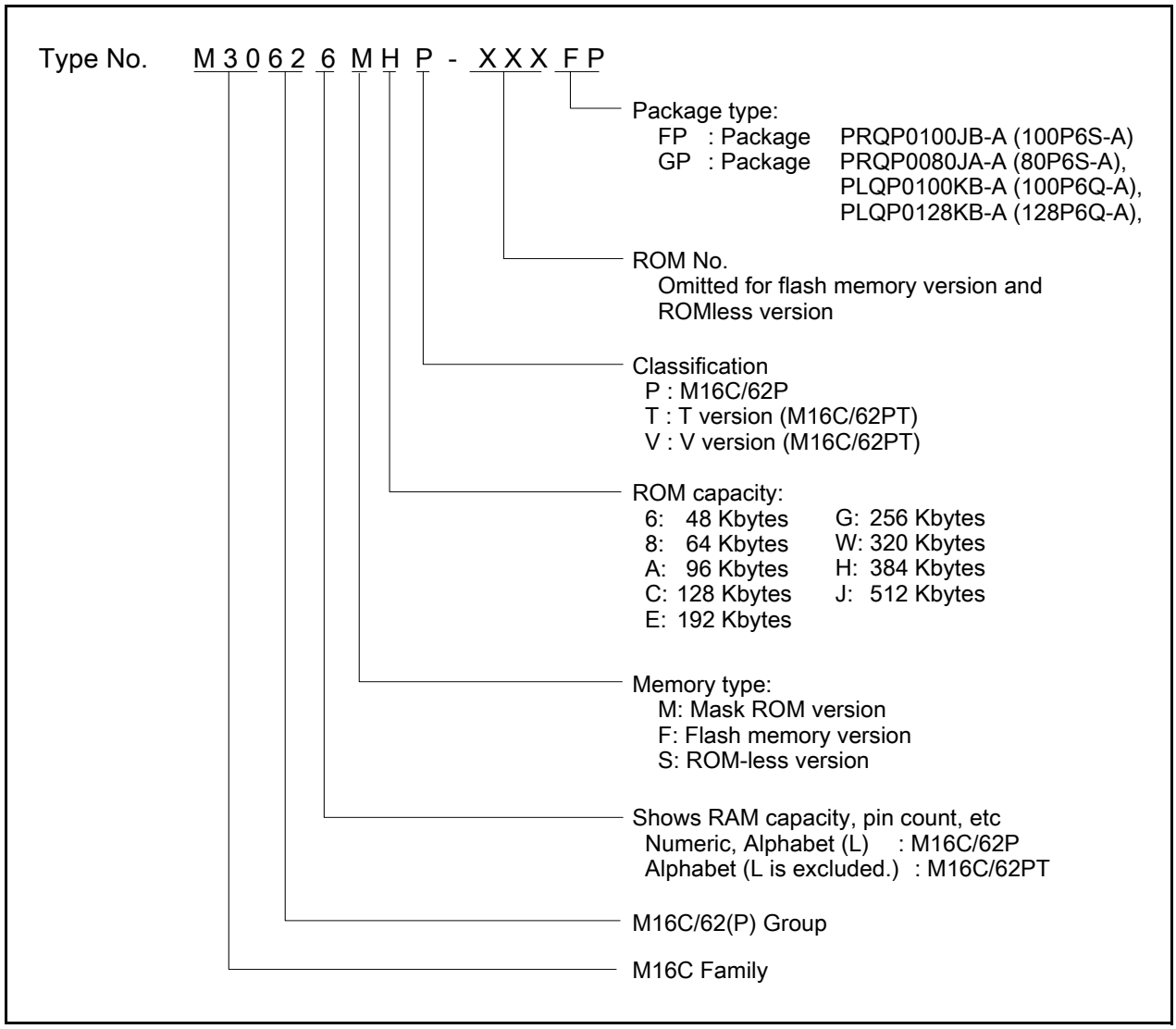
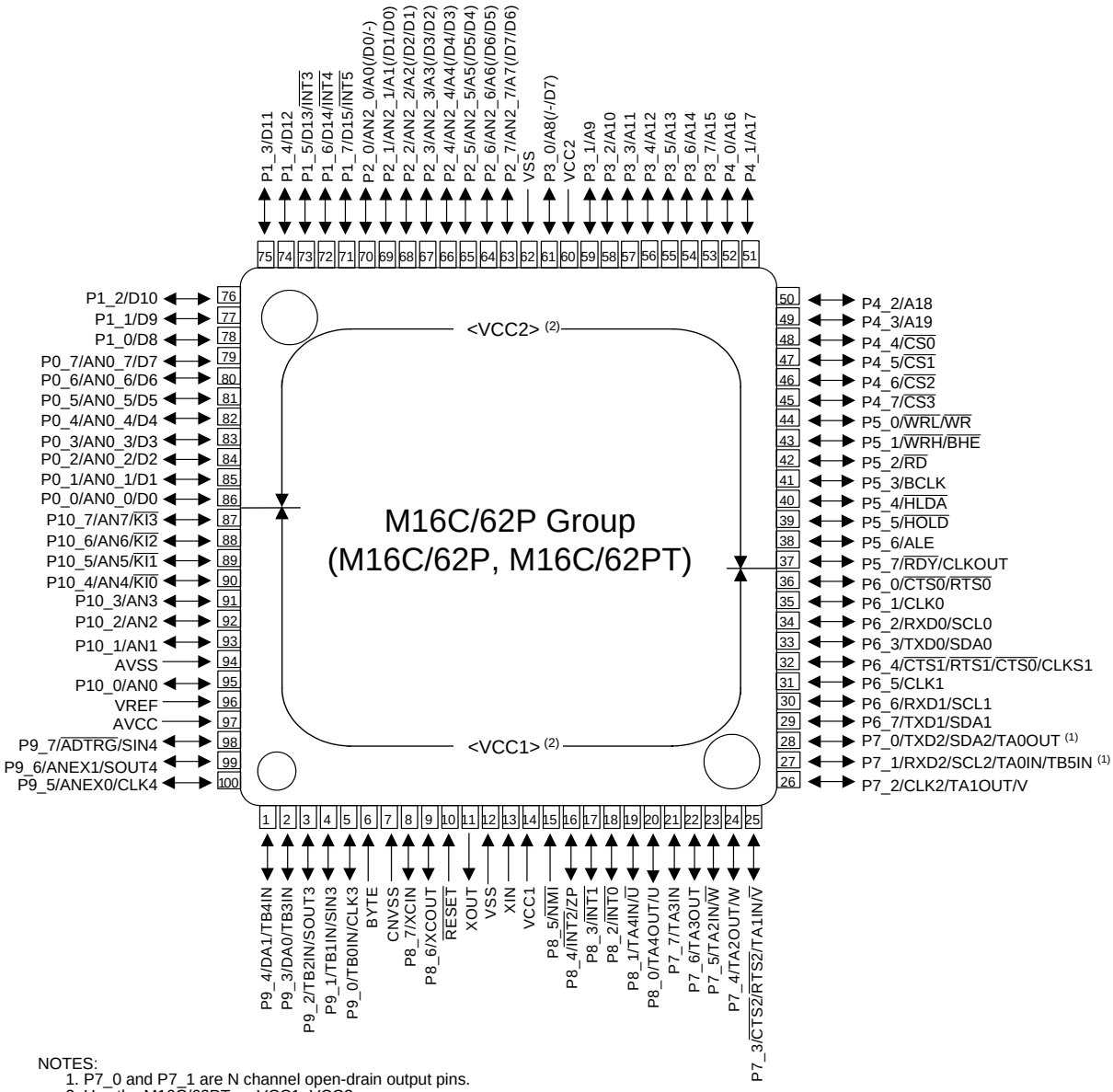


Figure 1.3 Type No., Memory Size, and Package

PIN CONFIGURATION (top view)

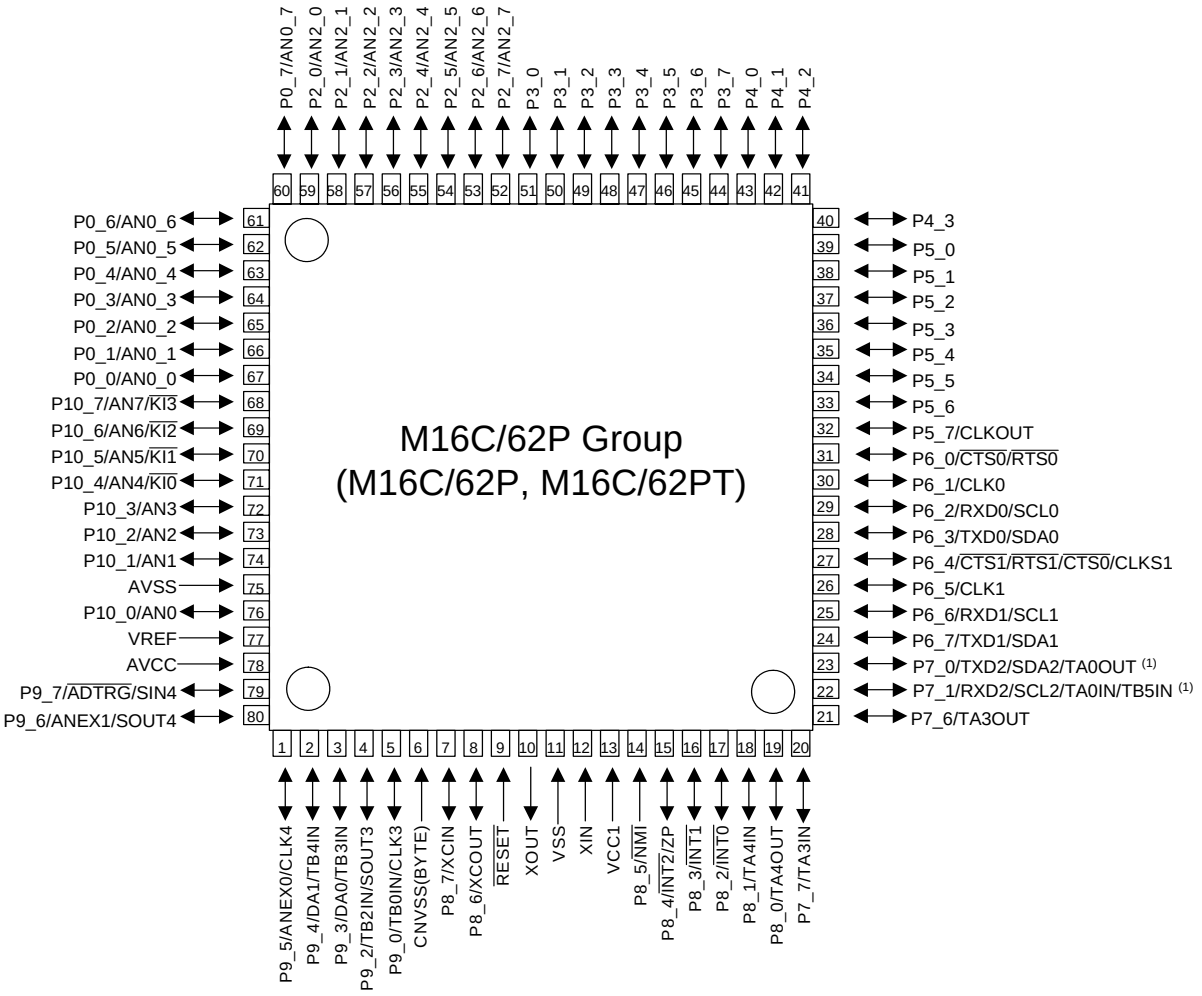


NOTES:
1. P7_0 and P7_1 are N channel open-drain output pins.
2. Use the M16C/62PT on VCC1=VCC2.

Package : PLQP0100KB-A (100P6Q-A)

Figure 1.8 Pin Configuration (Top View)

PIN CONFIGURATION (top view)



NOTES:
1. P7_0 and P7_1 are N channel open-drain output pins.

Package : PRQP0080JA-A (80P6S-A)

Figure 1.9 Pin Configuration (Top View)

Table 1.19 Pin Description (100-pin and 128-pin Version) (3)

Signal Name	Pin Name	I/O Type	Power Supply(1)	Description
Reference voltage input	VREF	I	VCC1	Applies the reference voltage for the A/D converter and D/A converter.
A/D converter	AN0 to AN7, AN0_0 to AN0_7, AN2_0 to AN2_7	I	VCC1	Analog input pins for the A/D converter.
	$\overline{\text{ADTRG}}$	I	VCC1	This is an A/D trigger input pin.
	ANEX0	I/O	VCC1	This is the extended analog input pin for the A/D converter, and is the output in external op-amp connection mode.
	ANEX1	I	VCC1	This is the extended analog input pin for the A/D converter.
D/A converter	DA0, DA1	O	VCC1	This is the output pin for the D/A converter.
I/O port	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P12_0 to P12_7 (2), P13_0 to P13_7 (2)	I/O	VCC2	8-bit I/O ports in CMOS, having a direction register to select an input or output. Each pin is set as an input port or output port. An input port can be set for a pull-up or for no pull-up in 4-bit unit by program.
	P6_0 to P6_7, P7_0 to P7_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7 (2)	I/O	VCC1	8-bit I/O ports having equivalent functions to P0. (however, output of P7_0 and P7_1 for the N-channel open drain output.)
	P8_0 to P8_4, P8_6, P8_7, P14_0, P14_1(2)	I/O	VCC1	I/O ports having equivalent functions to P0.
Input port	P8_5	I	VCC1	Input pin for the $\overline{\text{NMI}}$ interrupt. Pin states can be read by the P8_5 bit in the P8 register.

I : Input O : Output I/O : Input and output

NOTES:
1. When use VCC1 > VCC2, contacts due to some points or restrictions to be checked.
2. Ports P11 to P14 in M16C/62P (100-pin version) and M16C/62PT (100-pin version) cannot be used.

2.8.8 Stack Pointer Select Flag (U Flag)

ISP is selected when the U flag is “0”; USP is selected when the U flag is “1”.
The U flag is cleared to “0” when a hardware interrupt request is accepted or an INT instruction for software interrupt Nos. 0 to 31 is executed.

2.8.9 Processor Interrupt Priority Level (IPL)

IPL is configured with three bits, for specification of up to eight processor interrupt priority levels from level 0 to level 7.
If a requested interrupt has priority greater than IPL, the interrupt is enabled.

2.8.10 Reserved Area

When write to this bit, write “0”. When read, its content is indeterminate.

Table 4.6 SFR Information (6) (1)

Address	Register	Symbol	After Reset
03C0h 03C1h	A/D Register 0	AD0	XXh XXh
03C2h 03C3h	A/D Register 1	AD1	XXh XXh
03C4h 03C5h	A/D Register 2	AD2	XXh XXh
03C6h 03C7h	A/D Register 3	AD3	XXh XXh
03C8h 03C9h	A/D Register 4	AD4	XXh XXh
03CAh 03CBh	A/D Register 5	AD5	XXh XXh
03CCh 03CDh	A/D Register 6	AD6	XXh XXh
03CEh 03CFh	A/D Register 7	AD7	XXh XXh
03D0h			
03D1h			
03D2h			
03D3h			
03D4h	A/D Control Register 2	ADCON2	00h
03D5h			
03D6h	A/D Control Register 0	ADCON0	00000XXXb
03D7h	A/D Control Register 1	ADCON1	00h
03D8h	D/A Register 0	DA0	00h
03D9h			
03DAh	D/A Register 1	DA1	00h
03DBh			
03DCh	D/A Control Register	DACON	00h
03DDh			
03DEh	Port P14 Control Register (3)	PC14	XX00XXXXb
03DFh	Pull-Up Control Register 3 (3)	PUR3	00h
03E0h	Port P0 Register	P0	XXh
03E1h	Port P1 Register	P1	XXh
03E2h	Port P0 Direction Register	PD0	00h
03E3h	Port P1 Direction Register	PD1	00h
03E4h	Port P2 Register	P2	XXh
03E5h	Port P3 Register	P3	XXh
03E6h	Port P2 Direction Register	PD2	00h
03E7h	Port P3 Direction Register	PD3	00h
03E8h	Port P4 Register	P4	XXh
03E9h	Port P5 Register	P5	XXh
03EAh	Port P4 Direction Register	PD4	00h
03EBh	Port P5 Direction Register	PD5	00h
03ECh	Port P6 Register	P6	XXh
03EDh	Port P7 Register	P7	XXh
03EEh	Port P6 Direction Register	PD6	00h
03EFh	Port P7 Direction Register	PD7	00h
03F0h	Port P8 Register	P8	XXh
03F1h	Port P9 Register	P9	XXh
03F2h	Port P8 Direction Register	PD8	00X00000b
03F3h	Port P9 Direction Register	PD9	00h
03F4h	Port P10 Register	P10	XXh
03F5h	Port P11 Register (3)	P11	XXh
03F6h	Port P10 Direction Register	PD10	00h
03F7h	Port P11 Direction Register (3)	PD11	00h
03F8h	Port P12 Register (3)	P12	XXh
03F9h	Port P13 Register (3)	P13	XXh
03FAh	Port P12 Direction Register (3)	PD12	00h
03FBh	Port P13 Direction Register (3)	PD13	00h
03FCh	Pull-Up Control Register 0	PUR0	00h
03FDh	Pull-Up Control Register 1	PUR1	00000000b (2) 00000010b (2)
03FEh	Pull-Up Control Register 2	PUR2	00h
03FFh	Port Control Register	PCR	00h

NOTES:
1. The blank areas are reserved and cannot be accessed by users.
2. At hardware reset 1 or hardware reset 2, the register is as follows:
   - "00000000b" where "L" is inputted to the CNVSS pin
   - "00000010b" where "H" is inputted to the CNVSS pin

   At software reset, watchdog timer reset and oscillation stop detection reset, the register is as follows:
   - "00000000b" where the PM01 to PM00 bits in the PM0 register are "00b" (single-chip mode).
   - "00000010b" where the PM01 to PM00 bits in the PM0 register are "01b" (memory expansion mode) or "11b" (microprocessor mode).
3. These registers do not exist in M16C/62P (80-pin version), and M16C/62PT (80-pin version).

X : Nothing is mapped to this bit

Table 5.9 Low Voltage Detection Circuit Electrical Characteristics

Symbol	Parameter	Measuring Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{det4}	Low Voltage Detection Voltage (1)	V_{CC1}=0.8V to 5.5V	3.3	3.8	4.4	V
V_{det3}	Reset Level Detection Voltage (1, 2)		2.2	2.8	3.6	V
V_{det4}-V_{det3}	Electric potential difference of Low Voltage Detection and Reset Level Detection		0.3			V
V_{det3s}	Low Voltage Reset Retention Voltage				0.8	V
V_{det3r}	Low Voltage Reset Release Voltage (3)		2.2	2.9	4.0	V

NOTES:
1. $V_{det4} > V_{det3}$.
2. Where reset level detection voltage is less than 2.7 V, if the supply power voltage is greater than the reset level detection voltage, the microcomputer operates with f(BCLK) ≤ 10MHz.
3. $V_{det3r} > V_{det3}$ is not guaranteed.
4. The voltage detection circuit is designed to use when VCC1 is set to 5V.

Table 5.10 Power Supply Circuit Timing Characteristics

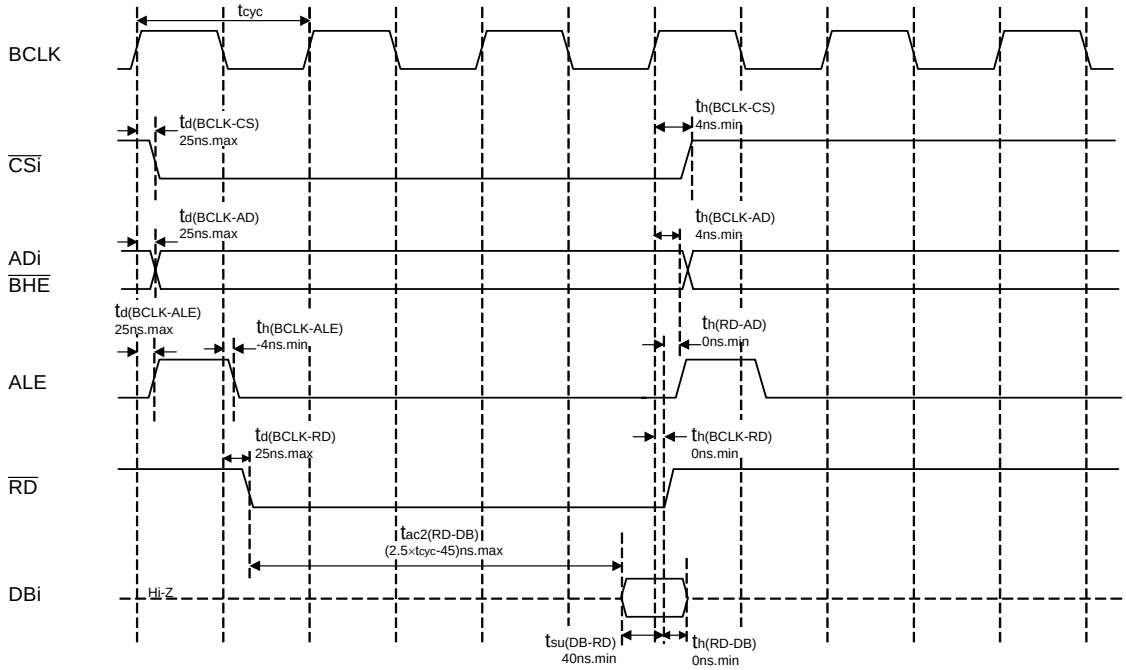
Symbol	Parameter	Measuring Condition	Standard			Unit
			Min.	Typ.	Max.	
$t_{d(P-R)}$	Time for Internal Power Supply Stabilization During Powering-On	V_{CC1}=2.7V to 5.5V			2	ms
$t_{d(R-S)}$	STOP Release Time				150	µs
$t_{d(W-S)}$	Low Power Dissipation Mode Wait Mode Release Time				150	µs
$t_{d(S-R)}$	Brown-out Detection Reset (Hardware Reset 2) Release Wait Time	V_{CC1}=V_{det3r} to 5.5V		6 (1)	20	ms
$t_{d(E-A)}$	Low Voltage Detection Circuit Operation Start Time	V_{CC1}=2.7V to 5.5V			20	µs

NOTES:
1. When V_{CC1} = 5V.

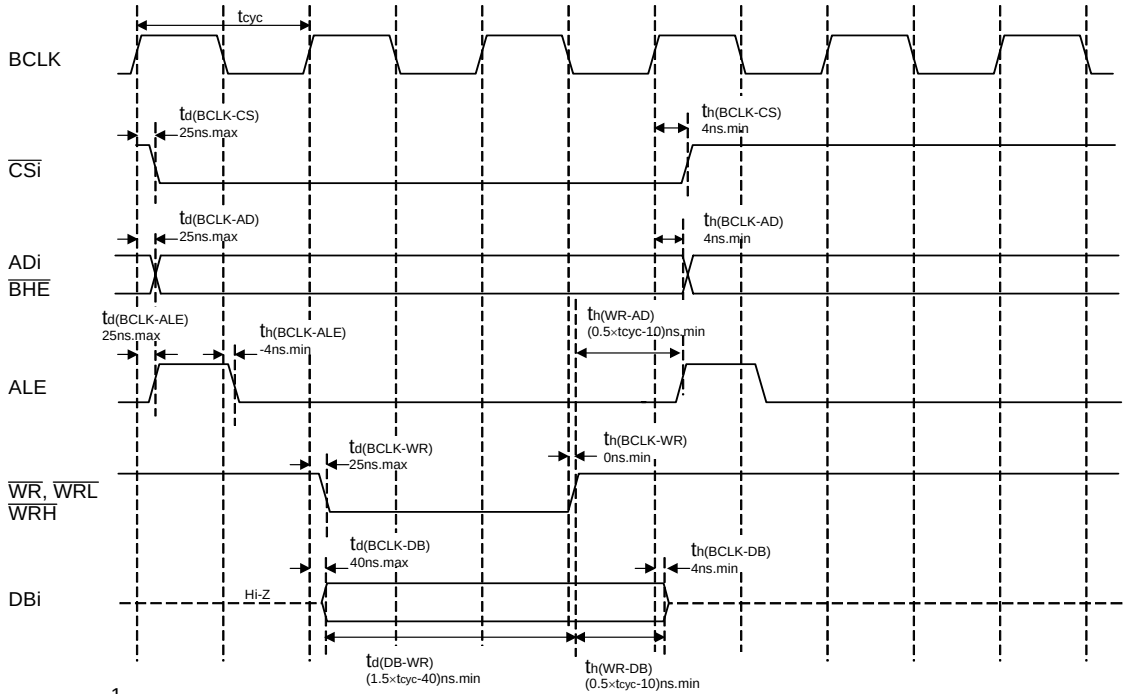
$V_{CC1}=V_{CC2}=5V$

Memory Expansion Mode, Microprocessor Mode
(for 2-wait setting and external area access**)**

Read timing



Write timing



$$T_{cyc}=\frac{1}{f(BCLK)}$$

Measuring conditions
· $V_{CC1}=V_{CC2}=5V$
· Input timing voltage : $V_{IL}=0.8V$, $V_{IH}=2.0V$
· Output timing voltage : $V_{OL}=0.4V$, $V_{OH}=2.4V$

Figure 5.8 Timing Diagram (6)

$V_{CC1}=V_{CC2}=3V$

Switching Characteristics

(V_{CC1} = V_{CC2} = 3V, V_{SS} = 0V, at T_{opr} = –20 to 85°C / –40 to 85°C unless otherwise specified)

Table 5.46 Memory Expansion and Microprocessor Modes (for setting with no wait)

Symbol	Parameter		Standard		Unit
			Min.	Max.	
td(BCLK-AD)	Address Output Delay Time	See **Figure 5.12**		30	ns
th(BCLK-AD)	Address Output Hold Time (in relation to BCLK)		4		ns
th(RD-AD)	Address Output Hold Time (in relation to RD)		0		ns
th(WR-AD)	Address Output Hold Time (in relation to WR)		(NOTE 2)		ns
td(BCLK-CS)	Chip Select Output Delay Time			30	ns
th(BCLK-CS)	Chip Select Output Hold Time (in relation to BCLK)		4		ns
td(BCLK-ALE)	ALE Signal Output Delay Time			25	ns
th(BCLK-ALE)	ALE Signal Output Hold Time		–4		ns
td(BCLK-RD)	RD Signal Output Delay Time			30	ns
th(BCLK-RD)	RD Signal Output Hold Time		0		ns
td(BCLK-WR)	WR Signal Output Delay Time			30	ns
th(BCLK-WR)	WR Signal Output Hold Time		0		ns
td(BCLK-DB)	Data Output Delay Time (in relation to BCLK)			40	ns
th(BCLK-DB)	Data Output Hold Time (in relation to BCLK) (3)		4		ns
td(DB-WR)	Data Output Delay Time (in relation to WR)		(NOTE 1)		ns
th(WR-DB)	Data Output Hold Time (in relation to WR) (3)		(NOTE 2)		ns
td(BCLK-HLDA)	HLDA Output Delay Time			40	ns

NOTES:

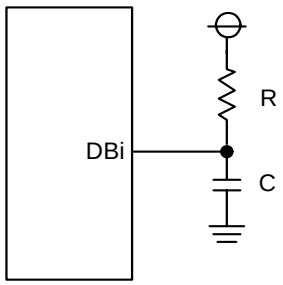
1. Calculated according to the BCLK frequency as follows:

$$\frac{0.5\times10^{9}}{f(BCLK)} - 40[ns]$$ f(BCLK) is 12.5MHz or less.

2. Calculated according to the BCLK frequency as follows:

$$\frac{0.5\times10^{9}}{f(BCLK)} - 10[ns]$$

3. This standard value shows the timing when the output is off, and does not show hold time of data bus.
   Hold time of data bus varies with capacitor volume and pull-up (pull-down) resistance value.
   Hold time of data bus is expressed in
   $t = -CR \times \ln(1 - V_{OL} / V_{CC2})$
   by a circuit of the right figure.
   For example, when $V_{OL} = 0.2V_{CC2}$, C = 30pF, R = 1kΩ, hold time of output "L" level is
   $t = -30pF \times 1k\Omega \times \ln(1 - 0.2V_{CC2} / V_{CC2})$
   = 6.7ns.



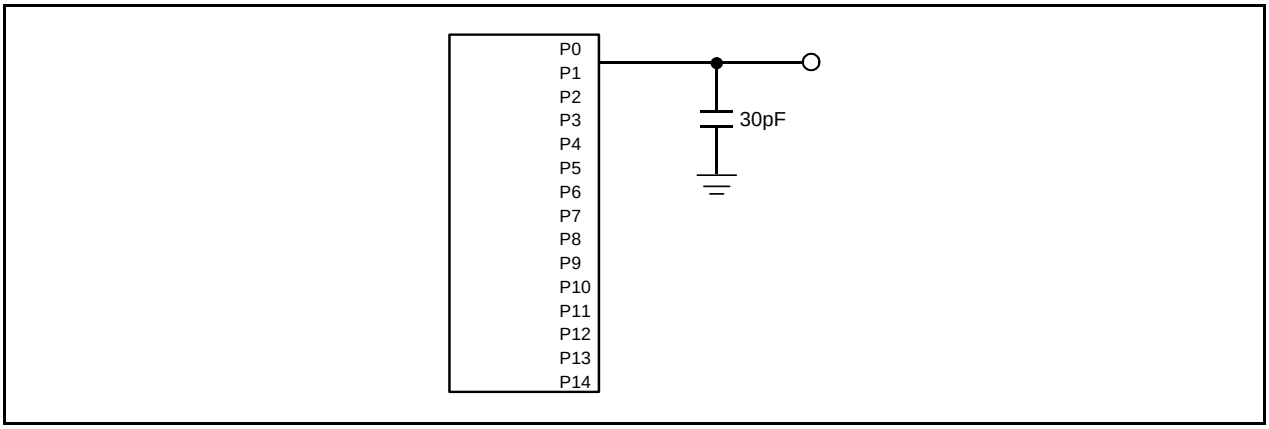


Figure 5.12 Ports P0 to P14 Measurement Circuit

5.2 Electrical Characteristics (M16C/62PT)

Table 5.49 Absolute Maximum Ratings

Symbol	Parameter		Condition	Rated Value	Unit
V_{CC1}, V_{CC2}	Supply Voltage		V_{CC1}=V_{CC2}=AVcc	–0.3 to 6.5	V
AVcc	Analog Supply Voltage		V_{CC1}=V_{CC2}=AVcc	–0.3 to 6.5	V
V_I	Input Voltage	$\overline{\text{RESET}}$, CNVSS, BYTE, P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P14_0, P14_1, VREF, XIN		–0.3 to V_{CC1}+0.3 (1)	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P12_0 to P12_7, P13_0 to P13_7		–0.3 to V_{CC2}+0.3 (1)	V
		P7_0, P7_1		–0.3 to 6.5	V
V_O	Output Voltage	P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P14_0, P14_1, XOUT		–0.3 to V_{CC1}+0.3 (1)	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P12_0 to P12_7, P13_0 to P13_7		–0.3 to V_{CC2}+0.3 (1)	V
		P7_0, P7_1		–0.3 to 6.5	V
P_d	Power Dissipation		–40°C<T_{opr}≤85°C	300	mW
			85°C<T_{opr}≤125°C	200	
T_{opr}	Operating Ambient Temperature	When the Microcomputer is Operating		–40 to 85 / –40 to 125 (2)	°C
		Flash Program Erase		0 to 60	
T_{stg}	Storage Temperature			–65 to 150	°C

NOTES:
1. There is no external connections for port P1_0 to P1_7, P4_4 to P4_7, P7_2 to P7_5 and P9_1 in 80-pin version.
2. T version = –40 to 85 °C, V version= –40 to 125 °C.

V_{CC1}=V_{CC2}=5V

Timing Requirements
(V_{CC1} = V_{CC2} = 5V, V_{SS} = 0V, at T_{opr} = –40 to 85°C (T version) / –40 to 125°C (V version) unless otherwise specified)

Table 5.60 Timer A Input (Counter Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN Input Cycle Time	100		ns
$t_{w(TAH)}$	TAiIN Input HIGH Pulse Width	40		ns
$t_{w(TAL)}$	TAiIN Input LOW Pulse Width	40		ns

Table 5.61 Timer A Input (Gating Input in Timer Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN Input Cycle Time	400		ns
$t_{w(TAH)}$	TAiIN Input HIGH Pulse Width	200		ns
$t_{w(TAL)}$	TAiIN Input LOW Pulse Width	200		ns

Table 5.62 Timer A Input (External Trigger Input in One-shot Timer Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN Input Cycle Time	200		ns
$t_{w(TAH)}$	TAiIN Input HIGH Pulse Width	100		ns
$t_{w(TAL)}$	TAiIN Input LOW Pulse Width	100		ns

Table 5.63 Timer A Input (External Trigger Input in Pulse Width Modulation Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(TAH)}$	TAiIN Input HIGH Pulse Width	100		ns
$t_{w(TAL)}$	TAiIN Input LOW Pulse Width	100		ns

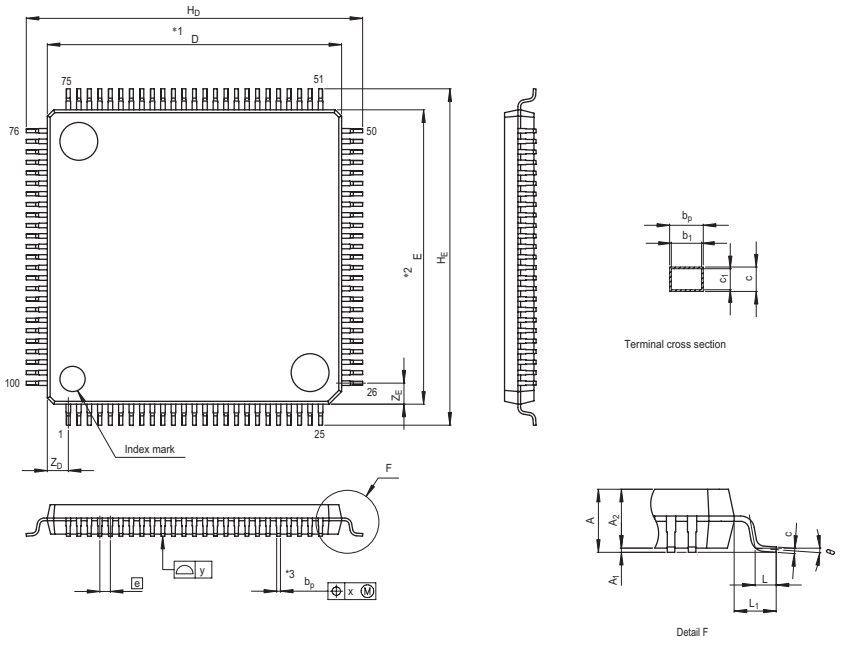
Table 5.64 Timer A Input (Counter Increment/Decrement Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(UP)}$	TAiOUT Input Cycle Time	2000		ns
$t_{w(UPH)}$	TAiOUT Input HIGH Pulse Width	1000		ns
$t_{w(UPL)}$	TAiOUT Input LOW Pulse Width	1000		ns
$t_{su(UP-TIN)}$	TAiOUT Input Setup Time	400		ns
$t_{h(TIN-UP)}$	TAiOUT Input Hold Time	400		ns

Table 5.65 Timer A Input (Two-phase Pulse Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN Input Cycle Time	800		ns
$t_{su(TAIN-TAOUT)}$	TAiOUT Input Setup Time	200		ns
$t_{su(TAOUT-TAIN)}$	TAiIN Input Setup Time	200		ns

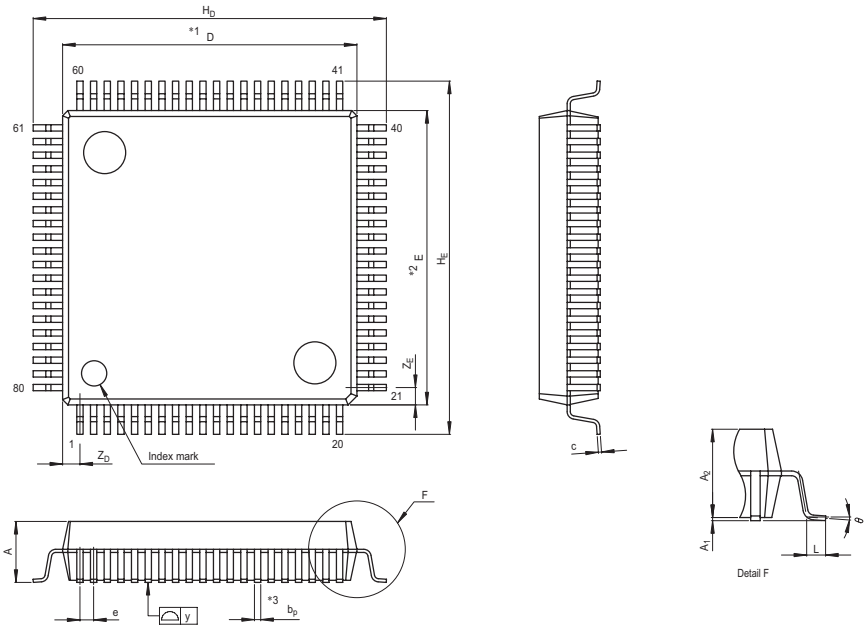
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP100-14x14-0.50	PLQP0100KB-A	100P6Q-A / FP-100U / FP-100UV	0.6g



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	13.9	14.0	14.1
E	13.9	14.0	14.1
A_2	—	1.4	—
H_D	15.8	16.0	16.2
H_E	15.8	16.0	16.2
A	—	—	1.7
A_1	0.05	0.1	0.15
b_p	0.15	0.20	0.25
b_1	—	0.18	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
Z_D	—	1.0	—
Z_E	—	1.0	—
L	0.35	0.5	0.65
L_1	—	1.0	—

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-QFP80-14x14-0.65	PRQP0080JA-A	80P6S-A	1.1g



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	13.8	14.0	14.2
E	13.8	14.0	14.2
A_2	—	2.8	—
H_D	16.5	16.8	17.1
H_E	16.5	16.8	17.1
A	—	—	3.05
A_1	0	0.1	0.2
b_p	0.25	0.3	0.4
c	0.13	0.15	0.2
θ	0°	—	10°
e	0.5	0.65	0.8
y	—	—	0.10
Z_D	—	0.825	—
Z_E	—	0.825	—
L	0.4	0.6	0.8

Rev.	Date	Description	
		Page	Summary
		40	Table 5.24 is partly revised.
		57	Table 5.43 is partly revised.
		70	Table 5.48 is partly revised.
		72	Table 5.50 is partly revised.
		73	Table 5.53 is partly revised.
		74	Table 5.55 is revised.
		76	Table 5.57 is partly revised.
		79	Table 5.69 is partly revised.
2.41	Jan 01, 2006	-	voltage down detection reset -> brown-out detection Reset
		2-4	Tables 1.1 to 1.3 Performance outline of M16C/62P group are partly revised.
		7	Table 1.4 Product List (1) is partly revised. Note 1 is added.
		8	Table 1.5 Product List (2) is partly revised. Note 1, 2 and 3 are added.
		9	Table 1.6 Product List (3) is partly revised. Note 1 and 2 are added.
		10	Table 1.7 Product List (4) is partly revised. Note 1 and 2 are added.
		11	Figure 1.3 Type No., Memory Size, Shows RAM capacity, and Package is partly revised
		12	Table 1.8 Product Code of Flash Memory version and ROMless version for M16C/62P is partly revised.
		13	Table 1.9 Product Code of Flash Memory version for M16C/62P is partly revised.
		14	Figure 1.6 Pin Configuration (Top View) is partly revised.
		15-17	Tables 1.10 to 1.12 Pin Characteristics for 128-Pin Package are added.
		18-19	Figure 1.7 and 1.8 Pin Configuration (Top View) are partly revised.
		20-21	Tables 1.13 to 1.14 Pin Characteristics for 100-Pin Package are added.
		22	Figure 1.9 Pin Configuration (Top View) is partly revised.
		23-24	Tables 1.15 to 1.16 Pin Characteristics for 80-Pin Package are added.
		25-29	Tables 1.17 to 1.21 are partly revised.
		34	Note 4 of Table 4.1 SFR Information is partly revised.
		43	Table 5.4 A/D Conversion Characteristics is partly revised.
		45	Table 5.6 Flash Memory Version Electrical Characteristics for 100 cycle products is partly revised.
			Table 5.7 Flash Memory Version Electrical Characteristics for 10,000 cycle products is partly revised.
			Table 5.8 Flash Memory Version Program / Erase Voltage and Read Operation Voltage Characteristics is partly revised.
		46	Table 5.9 Low Voltage Detection Circuit Electrical Characteristics is partly revised.

Rev.	Date	Description	
		Page	Summary
		47	Figure 5.1 Power Supply Circuit Timing Diagram is partly revised.
		48	Table 5.11 Electrical Characteristics (1) is partly deleted.
		49	Table 5.12 Electrical Characteristics (2) is partly revised.
		50	Note 1 of Table 5.13 External Clock Input (XIN input) is added.
		67	Notes 1 to 4 of Table 5.32 External Clock Input (XIN input) are added.
		85	Table 5.53 Flash Memory Version Electrical Characteristics for 100 cycle products is partly revised. Standard (Min.) is partly revised. Table 5.54 Flash Memory Version Electrical Characteristics for 10,000 cycle products is partly revised. Standard (Min.) is partly revised. Note 5 is revised. Table 23.55 Flash Memory Version Program / Erase Voltage and Read Operation Voltage Characteristics is partly revised.
		87	Table 5.57 Electrical Characteristics (1) is partly deleted.
		88	Table 5.58 Electrical Characteristics is partly revised.