



Welcome to **E-XFL.COM**

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded - Microcontrollers</u>"

Details	
Product Status	Not For New Designs
Core Processor	M16C/60
Core Size	16-Bit
Speed	24MHz
Connectivity	I ² C, IEBus, UART/USART
Peripherals	DMA, WDT
Number of I/O	85
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	20K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 26x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LFQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/m30624fgpgp-u3c

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



M16C/62P Group (M16C/62P, M16C/62PT) SINGLE-CHIP 16-BIT CMOS MICROCOMPUTER

REJ03B0001-0241 Rev.2.41 Jan 10, 2006

1. Overview

The M16C/62P Group (M16C/62P, M16C/62PT) of single-chip microcomputers are built using the high performance silicon gate CMOS process using a M16C/60 Series CPU core and are packaged in a 80-pin, 100-pin and 128-pin plastic molded QFP. These single-chip microcomputers operate using sophisticated instructions featuring a high level of instruction efficiency. With 1M bytes of address space, they are capable of executing instructions at high speed. In addition, this microcomputer contains a multiplier and DMAC which combined with fast instruction processing capability, makes it suitable for control of various OA, communication, and industrial equipment which requires high-speed arithmetic/logic operations.

1.1 Applications

Audio, cameras, television, home appliance, office/communications/portable/industrial equipment, automobile, etc

Specifications written in this manual are believed to be accurate, but are not guaranteed to be entirely free of error. Specifications in this manual may be changed for functional or performance improvements. Please make sure your manual is the latest edition.

RENESAS

Table 1.5 Product List (2) (M16C/62P)

As of Dec. 2005

		RAM		
Type No.	ROM Capacity	Capacity	Package Type (1)	Remarks
M30622MHP-XXXFP	384 Kbytes	16 Kbytes	PRQP0100JB-A	Mask ROM version
M30622MHP-XXXGP			PLQP0100KB-A	1
M30623MHP-XXXGP			PLQP0128KB-A	
M30624MHP-XXXFP		24 Kbytes	PRQP0100JB-A	1
M30624MHP-XXXGP			PLQP0100KB-A	1
M30625MHP-XXXGP			PLQP0128KB-A	1
M30626MHP-XXXFP		31 Kbytes	PRQP0100JB-A	1
M30626MHP-XXXGP			PLQP0100KB-A	
M30627MHP-XXXGP			PLQP0128KB-A	
M30626MJP-XXXFP (D)	512 Kbytes	31 Kbytes	PRQP0100JB-A	
M30626MJP-XXXGP (D)			PLQP0100KB-A	
M30627MJP-XXXGP (D)			PLQP0128KB-A	
M30622F8PFP	64K+4 Kbytes	4 Kbytes	PRQP0100JB-A	Flash memory
M30622F8PGP			PLQP0100KB-A	version (2)
M30623F8PGP			PRQP0080JA-A	
M30620FCPFP	128K+4 Kbytes	10 Kbytes	PRQP0100JB-A	1
M30620FCPGP			PLQP0100KB-A	
M30621FCPGP			PRQP0080JA-A	1
M3062LFGPFP ⁽³⁾ (D)	256K+4 Kbytes	20 Kbytes	PRQP0100JB-A	1
M3062LFGPGP ⁽³⁾ (D)			PLQP0100KB-A	1
M30625FGPGP			PLQP0128KB-A	-
M30626FHPFP	384K+4 Kbytes	31 Kbytes	PRQP0100JB-A	-
M30626FHPGP			PLQP0100KB-A	-
M30627FHPGP			PLQP0128KB-A	1
M30626FJPFP	512K+4 Kbytes	31 Kbytes	PRQP0100JB-A	1
M30626FJPGP			PLQP0100KB-A	1
M30627FJPGP			PLQP0128KB-A	1
M30622SPFP	-	4 Kbytes	PRQP0100JB-A	ROM-less version
M30622SPGP			PLQP0100KB-A	1
M30620SPFP		10 Kbytes	PRQP0100JB-A	1
M30620SPGP	7		PLQP0100KB-A	1
M30624SPFP (D)	_	20 Kbytes	PRQP0100JB-A	1
M30624SPGP (D)	1		PLQP0100KB-A	1
M30626SPFP (D)	7	31 Kbytes	PRQP0100JB-A	1
M30626SPGP (D)	<u> </u>		PLQP0100KB-A	

(D): Under development

NOTES:

1. The old package type numbers of each package type are as follows.

PLQP0128KB-A: 128P6Q-A, PRQP0100JB-A: 100P6S-A, PLQP0100KB-A: 100P6Q-A, PRQP0080JA-A: 80P6S-A

2. In the flash memory version, there is 4K bytes area (block A).

3. Please use M3062LFGPFP and M3062LFGPGP for your new system instead of M30624FGPFP and M30624FGPGP. The M16C/62P Group (M16C/62P, M16C/62PT) hardware manual is still good for M30624FGPFP and M30624FGPGP.

M30624FGPFP	256K+4 Kbytes	20 Kbytes	PRQP0100JB-A	Flash memory version
M30624FGPGP			PLQP0100KB-A	

included

Lead-free

D5

U3

U5

version

-20°C to 85°C

-40°C to 85°C

-20°C to 85°C

Internal ROM Internal ROM (User ROM Area Without Block A, (Block A, Block 1) Operating Block 1) Product Package Ambient Code Program Program Temperature Temperature Temperature and Erase and Erase Range Range Endurance Endurance 100 0°C to 60°C 100 0°C to 60°C -40°C to 85°C Flash memory D3 Lead-Version included D5 -20°C to 85°C D7 1,000 10,000 -40°C to 85°C -40°C to 85°C D9 -20°C to 85°C -20°C to 85°C 100 -40°C to 85°C U3 Lead-free 100 0°C to 60°C U5 -20°C to 85°C U7 1,000 10,000 -40°C to 85°C -40°C to 85°C U9 -20°C to 85°C -20°C to 85°C **ROM-less** D3 -40°C to 85°C Lead-

Table 1.8 Product Code of Flash Memory version and ROMless version for M16C/62P

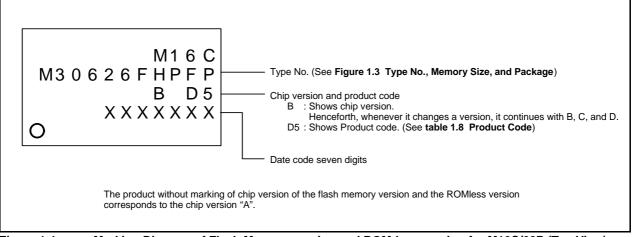


Figure 1.4 Marking Diagram of Flash Memory version and ROM-less version for M16C/62P (Top View)

Table 1.19 Pin Description (100-pin and 128-pin Version) (3)

Signal Name	Pin Name	I/O	Power	Description
		Туре	Supply ⁽¹⁾	
Reference voltage input	VREF	I	VCC1	Applies the reference voltage for the A/D converter and D/A converter.
A/D converter	AN0 to AN7, AN0_0 to AN0_7, AN2_0 to AN2_7	I	VCC1	Analog input pins for the A/D converter.
	ADTRG	I	VCC1	This is an A/D trigger input pin.
	ANEX0	I/O	VCC1	This is the extended analog input pin for the A/D converter, and is the output in external op-amp connection mode.
	ANEX1	I	VCC1	This is the extended analog input pin for the A/D converter.
D/A converter	DA0, DA1	0	VCC1	This is the output pin for the D/A converter.
I/O port	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P12_0 to P12_7 (2), P13_0 to P13_7 (2)	I/O	VCC2	8-bit I/O ports in CMOS, having a direction register to select an input or output. Each pin is set as an input port or output port. An input port can be set for a pull-up or for no pull-up in 4-bit unit by program.
	P6_0 to P6_7, P7_0 to P7_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7 (2)	I/O	VCC1	8-bit I/O ports having equivalent functions to P0. (however, output of P7_0 and P7_1 for the N-channel open drain output.)
	P8_0 to P8_4, P8_6, P8_7, P14_0, P14_1 ⁽²⁾	I/O	VCC1	I/O ports having equivalent functions to P0.
Input port	P8_5	I	VCC1	Input pin for the NMI interrupt. Pin states can be read by the P8_5 bit in the P8 register.

I : Input O : Output I/O : Input and output

NOTES:

- 1. When use VCC1 > VCC2, contacts due to some points or restrictions to be checked.
- 2. Ports P11 to P14 in M16C/62P (100-pin version) and M16C/62PT (100-pin version) cannot be used.

Table 4.2 SFR Information (2) (1)

1904245				
100415		Register	Symbol	After Reset
1904245	0040h			
100434h 1173 Interrupt Control Register 100000000000000000000000000000000000	0041h			
10045h	0042h			
0945h Timer BS Interrupt Control Register TISSIC XXXXXX000b 0948h Timer B Interrupt Control Register TISSIC XXXXXX000b 0947h Timer BS Interrupt Control Register, UNRTO BUS Collision Detection Interrupt Control Register TISSIC, UDBCNIC XXXXXX000b 0948h SILOS Interrupt Control Register, INT4 Interrupt Control Register SIC, INT5IC XXXXXX000b 0948h SILOS Interrupt Control Register INT4 Interrupt Control Register SIRC, INT5IC XXXXXX000b 0948h DIVAD Interrupt Control Register DIVIDIC XXXXXX000b 0948h DIVAD Interrupt Control Register DIVIDIC XXXXXX00b 0948h DIVAD Interrupt Control Register DIVIDIC XXXXXX00b 0948h DIVAD Interrupt Control Register DIVIDIC XXXXXX00b 0948h DIVAD Register DIVIDIC XXXXXX00b 0948h DIVAD Register DIVIDIC XXXXXX00b 0948h LAST Register DIVIDIC XXXXXX00b 0956h LART Register Interrupt Control Register DIVIDIC XXXXXX00b 0956h LART Register Interrupt	0043h			
0946h Timer 64 Hintering Control Register UART I BUS Collision Detection Interrupt Control Register T84IC, UBRONIC XXXXXX0000b 0947h Timer 58 Interrupt Control Register UART I BUS Collision Detection Interrupt Control Register SIGL, INTSIC XXXXXX0000b 0948h SIJO4 Interrupt Control Register, INT5 Interrupt Control Register SIGL, INTSIC XXXXXX000b 0948h DAM Collision Detection Interrupt Control Register BKNIC XXXXXX000b 0948h DAM Direrupt Control Register DMIC XXXXXX000b 0948h DAM Direrupt Control Register DMIC XXXXXX000b 0948h DAM Direrupt Control Register DMIC XXXXXX000b 0948h DAM Triburation Control Register RUPIC XXXXXX000b 0948h DAM Triburation Control Register RUPIC XXXXXX000b 0948h DAM Triburation Control Register ADIC XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX	0044h	INT3 Interrupt Control Register	INT3IC	XX00X000b
1984 Street 1985 Common 1985 Commo	0045h	Timer B5 Interrupt Control Register	TB5IC	XXXXX000b
00498	0046h		TB4IC, U1BCNIC	XXXXX000b
00498	0047h	Timer B3 Interrupt Control Register, UART0 BUS Collision Detection Interrupt Control Register	TB3IC, U0BCNIC	XXXXX000b
0048h UAR12 Bus Collision Defection Interrupt Control Register BCNIC XXXXX0000b 0040h DMAD Interrupt Control Register DMIIC XXXXX000b 0040h DMAI Therrupt Control Register DMIIC XXXXX000b 0040h Ky Interrupt Control Register KUPIC XXXXX000b 0044h ADIC Conversion Interrupt Control Register SZIIC XXXXX000b 0044h ADIC Tonswish Interrupt Control Register SZIIC XXXXX000b 0055h UAR12 Transmit Interrupt Control Register SZIIC XXXXX000b 0055h UAR10 Receive Interrupt Control Register SOIIC XXXXX000b 0055h UAR11 Receive Interrupt Control Register SOIIC XXXXX000b 0055h UAR11 Transmit Interrupt Control Register SOIIC XXXXX000b 0055h UAR11 Transmit Interrupt Control Register SOIIC XXXXXX000b 0055h UaR11 Transmit Interrupt Control Register STIIC XXXXXX000b 0055h Timer AD Interrupt Control Register TADIC XXXXXX000b 0055h Timer AD Interrupt Control Register TADIC<	0048h		S4IC, INT5IC	XX00X000b
004Bh DMAO Interrupt Control Register DMIIC XXXXX000b 004Ch DMAI Interrupt Control Register DMIIC XXXXX000b 004Dh Key Input Interrupt Control Register MIC XXXXX000b 004Eh AD Conversion Interrupt Control Register ADIC XXXXX000b 004Fh UART2 Transmit Interrupt Control Register SZPIC XXXXX000b 0056h UART2 Receive Interrupt Control Register SZPIC XXXXX000b 0056h UART2 Receive Interrupt Control Register SORIC XXXXX000b 0055h UART1 Receive Interrupt Control Register SORIC XXXXX000b 0055h UART1 Receive Interrupt Control Register STRIC XXXXX000b 0055h UART1 Receive Interrupt Control Register STRIC XXXXX000b 0055h Timer AD Interrupt Control Register TARIC XXXXX000b 0055h Timer AD Interrupt Control Register TARIC XXXXX000b 0056h Timer AD Interrupt Control Register TARIC XXXXX000b 0057h Timer AD Interrupt Control Register TARIC XXXXX000b <td>0049h</td> <td>SI/O3 Interrupt Control Register, INT4 Interrupt Control Register</td> <td>S3IC, INT4IC</td> <td>XX00X000b</td>	0049h	SI/O3 Interrupt Control Register, INT4 Interrupt Control Register	S3IC, INT4IC	XX00X000b
004Ch DMAI Interrupt Control Register DMIIC XXXXX000b 004Dh Ky Input Interrupt Control Register KUPIC XXXXX000b 004Eh ADI Conversion Interrupt Control Register ADIC XXXXX000b 004Fh JART 2 Transmit Interrupt Control Register S2TIC XXXXX000b 0050h UART 2 Receive Interrupt Control Register S2RIC XXXXX000b 0055h UART 0 Receive Interrupt Control Register S9TIC XXXXX000b 0052h UART 1 Receive Interrupt Control Register S0RIC XXXXX000b 0053h UART 1 Receive Interrupt Control Register S1TIC XXXXX000b 0054h UART 1 Receive Interrupt Control Register S1TIC XXXXX000b 0055h Timer AD Interrupt Control Register TADIC XXXXX000b 0055h Timer AD Interrupt Control Register TADIC XXXXX000b 0055h Timer AD Interrupt Control Register TADIC XXXXX000b 0057h Timer AD Interrupt Control Register TADIC XXXXX000b 0058h Timer AD Interrupt Control Register TADIC X	004Ah	UART2 Bus Collision Detection Interrupt Control Register	BCNIC	XXXXX000b
004BH Key Input Interrupt Control Register KUPIC XXXXX000b 004Fh JO Conversion Interrupt Control Register ADIC XXXXX000b 0056h UAR12 Receive Interrupt Control Register S2FIC XXXXX000b 0055h UAR12 Receive Interrupt Control Register S2RIC XXXXX000b 0055h UAR17 Insamit Interrupt Control Register S0RIC XXXXX000b 0055h UAR17 Insamit Interrupt Control Register S0RIC XXXXX000b 0055h UAR17 Insamit Interrupt Control Register S1RIC XXXXX000b 0055h UAR17 Receive Interrupt Control Register S1RIC XXXXX000b 0055h UAR17 Receive Interrupt Control Register TAIC XXXXX000b 0055h Timer A1 Interrupt Control Register TAIC XXXXX000b 0055h Timer A1 Interrupt Control Register TAIC XXXXX000b 0055h Timer A2 Interrupt Control Register TASIC XXXXX000b 0055h Timer A3 Interrupt Control Register TASIC XXXXX000b 0055h Timer B2 Interrupt Control Register TBIC XXX	004Bh	DMA0 Interrupt Control Register	DM0IC	XXXXX000b
004Eh A7D Conversion Interrupt Control Register ADIC XXXXXX000b 004Ph UART2 Transmit Interrupt Control Register \$2TIC XXXXXX000b 0050h UART2 Receive Interrupt Control Register \$2RIC XXXXXX000b 0051h UART0 Receive Interrupt Control Register \$5RIC XXXXXX000b 0052h UART0 Receive Interrupt Control Register \$5RIC XXXXXX000b 0053h UART1 Receive Interrupt Control Register \$5RIC XXXXXX000b 0054h UART1 Receive Interrupt Control Register \$1RIC XXXXXX000b 0055h UART1 Receive Interrupt Control Register \$1RIC XXXXXX000b 0055h Timer A1 Interrupt Control Register \$1RIC XXXXXX000b 0055h Timer A2 Interrupt Control Register \$1AIC XXXXXX000b 0057h Timer A2 Interrupt Control Register \$1AIC XXXXXX000b 0058h Timer A2 Interrupt Control Register \$1AIC XXXXXX000b 0058h Timer B2 Interrupt Control Register \$1AIC XXXXXX000b 0058h Timer B2 Interrupt Control Register \$1AIC <td>004Ch</td> <td>DMA1 Interrupt Control Register</td> <td>DM1IC</td> <td>XXXXX000b</td>	004Ch	DMA1 Interrupt Control Register	DM1IC	XXXXX000b
004Fh UART2 Transmit Interrupt Control Register \$2TIC XXXXX000b 0050h UART2 Receive Interrupt Control Register \$2RIC XXXXX000b 0051h UART0 Transmit Interrupt Control Register \$3TIC XXXXX000b 0052h UART1 Graceive Interrupt Control Register \$3RIC XXXXX000b 0053h UART1 Transmit Interrupt Control Register \$3TIC XXXXX000b 0054h UART1 Transmit Interrupt Control Register \$1TIC XXXXX000b 0055h Timer AD Interrupt Control Register \$1TIC XXXXX000b 0056h Timer AD Interrupt Control Register \$1TIC XXXXX000b 0057h Timer AD Interrupt Control Register \$1ASIC XXXXX000b 0058h Timer AD Interrupt Control Register \$1BIC XXXXX000b 0058h Timer BD Interrupt Control Register \$1BIC	004Dh	Key Input Interrupt Control Register	KUPIC	XXXXX000b
0055h UAR12 Receive Interrupt Control Register \$2RIC XXXXX000b 0051h UAR10 Transmit Interrupt Control Register \$0RIC XXXXXX00b 0052h UAR10 Receive Interrupt Control Register \$3RIC XXXXXX00b 0053h UAR11 Receive Interrupt Control Register \$1RIC XXXXXX00b 0054h UAR11 Receive Interrupt Control Register \$1RIC XXXXXX00b 0055h Timer An Interrupt Control Register \$1RIC XXXXXX00b 0056h Timer A1 Interrupt Control Register \$1AIC XXXXXX00b 0057h Timer A1 Interrupt Control Register \$1AIC XXXXXX00b 0058h Timer A2 Interrupt Control Register \$1AIC XXXXXX00b 0059h Timer A3 Interrupt Control Register \$1AIC XXXXXX00b 0059h Timer B0 Interrupt Control Register \$1AIC XXXXXX00b 0058h Timer B1 Interrupt Control Register \$1BIC XXXXXX00b 0058h Timer B2 Interrupt Control Register \$1BIC XXXXXX00b 0059h Interrupt Control Register \$1BIC XXXXXX00b <td>004Eh</td> <td>A/D Conversion Interrupt Control Register</td> <td>ADIC</td> <td>XXXXX000b</td>	004Eh	A/D Conversion Interrupt Control Register	ADIC	XXXXX000b
0051h UARTO Transmit Interrupt Control Register SOTIC XXXXX000b 0052h UARTO Receive Interrupt Control Register SORIC XXXXXX00b 0053h UARTO Receive Interrupt Control Register STRIC XXXXXX00b 0054h UARTI Transmit Interrupt Control Register STRIC XXXXXX00b 0055h Timer AD Interrupt Control Register TA0IC XXXXXX00b 0056h Timer AD Interrupt Control Register TA0IC XXXXXX00b 0057h Timer AD Interrupt Control Register TA2IC XXXXXX00b 0059h Timer BD Interrupt Control Register TBDIC XXXXXX00b 0059h Timer BD Interrupt Control Register TBDIC XXXXXX00b 005Ch Timer BD Interrupt Control Register TBDIC XXXXXX00b 005Ch Timer BD Interrupt Control Register NTOIC XXXXXXXXXXXXXXXXX	004Fh	UART2 Transmit Interrupt Control Register	S2TIC	XXXXX000b
0051h UARTO Transmit Interrupt Control Register SOTIC XXXXX000b 0052h UARTO Receive Interrupt Control Register SORIC XXXXX000b 0053h UARTO Receive Interrupt Control Register STRIC XXXXX000b 0054h UARTI Transmit Interrupt Control Register STRIC XXXXX000b 0055h Timer AD Interrupt Control Register TA0IC XXXXX000b 0056h Timer AI Interrupt Control Register TA0IC XXXXX000b 0056h Timer AI Interrupt Control Register TA2IC XXXXX000b 0057h Timer AI Interrupt Control Register TA2IC XXXXX000b 0058h Timer AI Interrupt Control Register TA4IC XXXXX000b 0059h Timer AI Interrupt Control Register TB0IC XXXXX000b 0059h Timer BI Interrupt Control Register TB0IC XXXXX000b 0059h Timer BI Interrupt Control Register TB1IC XXXXX000b 005Ch Timer BI Interrupt Control Register TB1IC XXXXX000b 005Ch Timer BI Interrupt Control Register INT0IC XX0XX000b	0050h	UART2 Receive Interrupt Control Register	S2RIC	XXXXX000b
0052h UARTO Receive Interrupt Control Register SORIC XXXXXX000b 0053h UART1 ransmit Interrupt Control Register STRIC XXXXXX00b 0054h UART1 Receive Interrupt Control Register TABIC XXXXXX00b 0055h Timer Al Interrupt Control Register TABIC XXXXXX00b 0057h Timer Al Interrupt Control Register TABIC XXXXXX00b 0057h Timer Al Interrupt Control Register TABIC XXXXXX00b 0058h Timer Bo Interrupt Control Register TBIC XXXXXX00b 0056h Timer Bo Interrupt Control Register TBIC XXXXXX00b 0055h Timer Bo Interrupt Control Register TBIC XXXXXX00b 0055h IntTO Interrupt Control Register INTOIC XXXXXX00b 0057h Interrupt Control Register INTOIC XXXXXX00b	0051h		S0TIC	XXXXX000b
0055h UART1 fransmit Interrupt Control Register STRIC XXXXX000b 0055h MART1 Receive Interrupt Control Register STRIC XXXXX000b 0055h Timer AO Interrupt Control Register TA0IC XXXXX000b 0056h Timer AO Interrupt Control Register TA2IC XXXXX000b 0057h Timer AI Interrupt Control Register TA2IC XXXXXX000b 0058h Timer AI Interrupt Control Register TA3IC XXXXXX000b 0059h Timer AI Interrupt Control Register TA3IC XXXXXX000b 0059h Timer AI Interrupt Control Register TB8IC XXXXXX000b 0058h Timer BI Interrupt Control Register TB8IC XXXXXX000b 005Ch Timer BI Interrupt Control Register TB2IC XXXXXX000b 005Ch Timer BI Interrupt Control Register INT1IC XX00X000b 005Fh INT2 Interrupt Control Register INT1IC XX00X000b 005Fh Int2 Interrupt Control Register INT2IC XX00X000b 006Ch Interrupt Control Register Int2IC XX00X00b	0052h			
0054h UART1 Receive Interrupt Control Register STRIC XXXXX000b 0055h Timer AD Interrupt Control Register TADIC XXXXX000b 0056h Timer AI Interrupt Control Register TATIC XXXXX000b 0057h Timer AI Interrupt Control Register TAZIC XXXXX000b 0058h Timer AI Interrupt Control Register TAXIC XXXXX000b 0059h Timer AI Interrupt Control Register TAXIC XXXXX000b 0059h Timer AI Interrupt Control Register TAXIC XXXXX000b 0059h Timer BI Interrupt Control Register TBIC XXXXX000b 0055h Timer BI Interrupt Control Register TBIC XXXXX000b 0055h Interrupt Control Register INTOIC XX00X000b 0055h Interrupt Control Register INTOIC XX00X000b 0056h Interrupt Control Register INTOIC XX00X000b 0067h Interrupt Control Register INTOIC XX00X000b 0068h Interrupt Control Register Interrupt Control Register Interrupt Control Register	0053h			
0055h Timer AO Interrupt Control Register TAOIC XXXXX000b 0055h Timer AI Interrupt Control Register TAIIC XXXXXX000b 0057h Timer AZ Interrupt Control Register TAZIC XXXXXX000b 0058h Timer AZ Interrupt Control Register TAZIC XXXXXX000b 0058h Timer AZ Interrupt Control Register TAZIC XXXXXX000b 0054h Timer AZ Interrupt Control Register TBOIC XXXXXX000b 0055h Timer BZ Interrupt Control Register TBIIC XXXXXX000b 0055h Timer BZ Interrupt Control Register TBZIC XXXXXX000b 0055h Timer BZ Interrupt Control Register INTOIC XXX00X000b 0055h INT1 Interrupt Control Register INT1C XXX0XX000b 0056h INT2 Interrupt Control Register INT2IC XX0XX000b 0067h INT2 Interrupt Control Register INT2IC XX0XX000b 0068h INT2 Interrupt Control Register INT2IC XX0XX000b 0068h INT2IC XX0XX000b INT2IC XX0XX00b <t< td=""><td>0054h</td><td></td><td></td><td></td></t<>	0054h			
0056h Timer A1 Interrupt Control Register TA1IC XXXXX000b 0057h Timer A2 Interrupt Control Register TA2IC XXXXX000b 0058h Timer A3 Interrupt Control Register TA3IC XXXXX000b 0058h Timer A3 Interrupt Control Register TA3IC XXXXX000b 0058h Timer A3 Interrupt Control Register TB0IC XXXXX000b 0058h Timer B3 Interrupt Control Register TB1IC XXXXX000b 0055h Timer B3 Interrupt Control Register TB2IC XXXXX000b 0055h INT0 Interrupt Control Register INT0IC XX00X000b 0055h INT1 Interrupt Control Register INT1IC XX00X000b 0056h INT2 Interrupt Control Register INT2IC XX00X000b 0060h INT2 Interrupt Control Register INT2IC XX00X000b 0060h INT2 Interrupt Control Register INT2IC XX00X000b 0060h INT2 Interrupt Control Register INT2IC XX00X000b 0066h INT2 Interrupt Control Register INT2IC XX00X000b 0066h	0055h			
0057h Timer AZ Interrupt Control Register TA2IC XXXXX000b 0058h Timer AZ Interrupt Control Register TA3IC XXXXX000b 0059h Timer AZ Interrupt Control Register TA4IC XXXXX000b 005Ah Timer BZ Interrupt Control Register TB0IC XXXXX000b 005Bh Timer BZ Interrupt Control Register TB1IC XXXXX000b 005Ch Timer BZ Interrupt Control Register TB2IC XXXXX000b 005Dh INT0 Interrupt Control Register INT0IC XX00X000b 005Eh INT1 Interrupt Control Register INT1IC XX00X000b 005Eh INT2 Interrupt Control Register INT2IC XX00X000b 006Eh INT2IC XX00X000b INT2IC XX00X00b 006Eh INT2IC XX00X00b INT2IC XX00X00b INT2IC INT2IC	0056h			
0058h Timer A3 Interrupt Control Register TA3IC XXXXX000b 0059h Timer A4 Interrupt Control Register TA4IC XXXXX000b 005Ah Timer B0 Interrupt Control Register TB0IC XXXXX000b 005Bh Timer B1 Interrupt Control Register TB1IC XXXXX000b 005Ch Timer B1 Interrupt Control Register TB2IC XXXXX000b 005Dh INT0 Interrupt Control Register INT0IC XXXXX000b 005Bh INT1 Interrupt Control Register INT0IC XX00X000b 005Fh INT2 Interrupt Control Register INT2IC XX00X000b 006Fh INT2IC XX00X000b 006Bh INT2IC XX00X000b 006Ch INT2IC XX00X000b 006Bh INT2IC XX0XX000b 006Bh INT2IC XX0XXXIII 006Bh INT2IC	0057h			
	0058h			
005Ah Timer B0 Interrupt Control Register TB0IC XXXXX000b 005Bh Timer B1 Interrupt Control Register TB1IC XXXXX000b 005Ch Timer B2 Interrupt Control Register TB2IC XXXXX000b 005Dh INT0 Interrupt Control Register INT0IC XX00X000b 005Eh INT1 Interrupt Control Register INT1IC XX00X000b 006Dh INT2 Interrupt Control Register INT2IC XX00X000b 006Dh INT2 Interrupt Control Register INT2IC XX00X000b 006Dh INT2 Interrupt Control Register INT2IC XX00X000b 006Dh INT2IC INT2IC XX00X000b 006Bh INT2IC				
0055h Timer B2 Interrupt Control Register TB1C XXXX000b 005Ch Timer B2 Interrupt Control Register TB2IC XXXXX000b 005Dh INT0 Interrupt Control Register INT0IC XX00X000b 005Fh INT1 Interrupt Control Register INT1IC XX00X000b 006Ph INT2 Interrupt Control Register INT2IC XX00X000b 0061h 0060h 0060h 0060h 0063h 0064h 0065h 0066h 0066h 0066h 0066h 0066h 0068h 0068h 0068h 0066h 006Ch 006Dh 0066h 0066h 006Fh 0070h 0070h 0070h 0077h 0073h 0078h 0078h 0077h 0078h 0078h 0078h 0077h 0078h 0078h 0078h 007Dh 007Dh 007Dh 007Dh 007Dh 007Dh 007Dh 007Dh				
005Ch Timer B2 Interrupt Control Register TB2/C XXXXX000b 005Ch INTO Interrupt Control Register INT0IC XX00X000b 005Eh INT1 Interrupt Control Register INT1IC XX00X000b 005Fh INT2 Interrupt Control Register INT2IC XX00X000b 0060h 0061h 0062h 0062h 0062h 0062h 0062h 0062h 0068h 0066h 0067h 0068h 0068h 0069h 0060h 0060h 006Ch 006Ch 006Ch 006Ch 006Eh 0070h 0070h 0071h 0073h 0074h 0078h 0078h 0077h 0078h 0078h 0078h 0077h 0078h 0078h 0078h 0077h 0078h 0078h 0078h 007Dh 007Dh 007Dh 007Dh 007Dh 007Dh 007Dh 007Dh				
005Dh INT0 Interrupt Control Register INT1IC XX00X000b 005Fh INT1 Interrupt Control Register INT1IC XX00X000b 0060h INT2 Interrupt Control Register INT2IC XX00X000b 0061h INT2 Interrupt Control Register INT2IC XX00X000b 0061h INT2 Interrupt Control Register INT2IC XX00X000b 0061h INT2 Interrupt Control Register INT2IC XX00X000b 0062h INT2IC XX00X000b 0063h INT2IC XX00X000b 0063h INT2IC XX00X000b 0064h INT2IC XX00X000b 0065h INT2IC XX00X000b 0066h INT2IC INT2IC 0068h INT2IC INT2IC <tr< td=""><td></td><td>Timer B2 Interrupt Control Register</td><td></td><td>XXXXX000b</td></tr<>		Timer B2 Interrupt Control Register		XXXXX000b
005Eh INT1 Interrupt Control Register INT2IC XX00X000b 006Fh INT2 Interrupt Control Register INT2IC XX00X000b 0060h				
005Fh INT2 Interrupt Control Register INT2IC XX00X000b 0060h				
0060h 0061h 0062h 0063h 0064h 0066h 0067h 0067h 0068h 0069h 006Ah 0060h 006Ah 0060h 006Ch 006Ch 006Ch 006Ch 006Fh 0070h 0071h 0072h 0072h 0073h 0074h 0075h 0077h 0078h 0078h 0078h 0078h 0078h 0078h 0078h 007Ah 007Ah 007Bh 007Ch 007Dh 007Dh				
0061h 0062h 0063h 0064h 0066h 0066h 0067h 0068h 0068h 0068h 0068h 0060h 006Ch 006Ch 006Ch 006Ch 0071h 0070h 0071h 0077h 0077h 0077h 0077sh 0077sh 0077sh 0077sh 0077sh 007sh		The state of the s		7.0.007.0002
0062h 0063h 0064h 0 0065h 0 0067h 0 0068h 0 0069h 0 006Ch 0 006Ch 0 006Fh 0 007th 0 007th 0 0073h 0 0076h 0 0078h 0 0079h 0 0078h 0 0078h 0 0078h 0 007Ch 0 007Dh 0				
0063h 0064h 0066h 0066h 0067h 0068h 0069h 0069h 0060h 0060h 0060h 006Ch 006Ch 006Fh 0071h 0071h 0073h 0073h 0073h 0074h 0075h 0075h 0076h 0077h 0078h 0077h 0078h				
0064h 0065h 0066h 0067h 0068h 0069h 0069h 0060h 0060h 0060h 0060h 0060h 0060h 0060h 0070h 0070h 0073h 0073h 0075h 0075h 0076h 0077h 0078h				
0065h 0066h 0067h 0068h 0069h 0069h 006Ah 006Bh 006Ch 006Ch 006Dh 006Eh 006Fh 0070h 0071h 0072h 0073h 0073h 0074h 0075h 0075h 0076h 0077h 0078h 0078h 0078h 0078h 0078h 0079h 0079h 0079h 0079h 0079h 0079h 0079h 0077h 0078h 0079h 0079h 0079h 0079h 0079h 0077h 0078h 0079h 0079h 0070h				
0066h 0067h 0068h 0069h 006Ah 006Bh 006Ch 006Ch 006Eh 006Fh 0070h 0071h 0072h 0073h 0075h 0075h 0076h 0076h 0076h 0076h 0076h 0077h 0078h 0078h 0078h 0079h 0070h 0079h 0070h 0079h 0070h 0070h 0070h 0070h 0070h 0070h				
0067h 0068h 0069h 0060h 0060h 0060h 0060h 0060h 0060h 0060h 0060h 0060h 0070h 0071h 0073h 0074h 0075h 0076h 0077h 0078h 0079h 0070h 0070h 0070h 0070h 0070h 0070h				
0068h 0069h 006Ah 006Bh 006Ch 006Dh 006Eh 006Fh 0071h 0071h 0073h 0074h 0075h 0076h 0077h 0078h 0077h				
0069h 006Ah 006Bh 006Ch 006Eh 006Fh 006Fh 0070h 0071h 0072h 0073h 0074h 0075h 0076h 0076h 0076h 0077h 0076h 0077h 0078h 0079h 0070h 0070h 0070h				
006Ah 006Bh 006Ch 006Dh 006Eh 006Fh 0070h 0071h 0072h 0072h 0073h 0074h 0075h 0076h 0077h 0078h 0079h 007Ah 007Bh 007Ch 007Ch 007Ch 007Ch 007Ch 007Eh 007Eh				
006Bh 006Ch 006Dh 006Eh 006Fh 0070h 0071h 0072h 0073h 0074h 0075h 0076h 0077h 0077h 0078h 0077h 0078h 0079h 0070h 0070h 0070h 0070h 0070h 0070h 0070h 0070h				
006Ch 006Dh 006Eh 006Fh 0070h 0070h 0071h 0072h 0073h 0074h 0075h 0076h 0076h 0076h 0076h 0076h 0076h 0076h 0076h 0077h 0078h 0078h 0078h 0079h 0070h 0070h			1	
006Dh 006Eh 006Fh 0070h 0070h 0071h 0072h 0073h 0074h 0075h 0076h 0076h 0076h 0076h 0076h 0076h 0077h 0078h 0078h 0079h 0070h 0070h 0070h			1	
006Eh 006Fh 0070h 0070h 0071h 0072h 0073h 0074h 0075h 0076h 0077h 0076h 0077h 0078h 0078h 0078h 0079h 007Ah 007Bh 007Ch 007Ch 007Ch 007Ch 007Ch 007Ch 007Ch			1	
006Fh 0070h 0071h 0071h 0072h 0073h 0074h 0074h 0075h 0076h 0077h 0078h 0079h 007Ah 007Bh 007Bh 007Ch 007Ch 007Dh 007Eh			1	
0070h 0071h 0072h 0073h 0073h 0074h 0075h 0076h 0077h 0078h 0079h 0079h 0079h 007Ah 007Bh 007Ch 007Bh 007Ch 007Ch 007Ch				†
0071h 0072h 0073h 0074h 0074h 0075h 0076h 0077h 0078h 0079h 0079h 007Ah 007Ph 007Ah 007Bh 007Ch 007Ch 007Ch 007Ch	0070h		1	
0072h 0073h 0074h 0074h 0075h 0076h 0076h 0077h 0078h 0079h 007Ah 007Bh 007Ch 007Ch 007Ch 007Ch 007Ch 007Ch			1	
0073h			1	
0074h 0075h 0076h 0077h 0078h 0078h 0078h 0078h 007Ah 007Bh 007Bh 007Ch 007Ch 007Dh			1	
0075h 0076h 0077h 0078h 0078h 0079h 007Ah 007Ah 007Ch 007Ch 007Dh				†
0076h				†
0077h 0078h 0079h 007Ah 007Bh 007Ch 007Ch 007Dh 007Ch			1	+
0078h			1	+
0079h 007Ah 007Bh 007Ch 007Dh 007Eh			1	+
007Ah 007Bh 007Ch 007Dh 007Eh			1	+
007Bh			1	+
007Ch			1	1
007Dh				1
007Eh				1
				1
	007En 007Fh			ļ

NOTES:

1. The blank areas are reserved and cannot be accessed by users.

X : Nothing is mapped to this bit

Table 4.6 SFR Information (6) (1)

Address	Register	Symbol	After Reset
03C0h	A/D Register 0	AD0	XXh
03C1h	112 112gi2121 1	1.24	XXh
03C2h	A/D Register 1	AD1	XXh
03C3h	11-11-g-11-11		XXh
03C4h	A/D Register 2	AD2	XXh
03C5h	7.15 (togistis) 2	7.52	XXh
03C6h	A/D Register 3	AD3	XXh
03C7h	1.1g	1.24	XXh
03C8h	A/D Register 4	AD4	XXh
03C9h	The stage of the s		XXh
03CAh	A/D Register 5	AD5	XXh
03CBh	, vo regions o	7.20	XXh
03CCh	A/D Register 6	AD6	XXh
03CDh	, vo regions. o	7.20	XXh
03CEh	A/D Register 7	AD7	XXh
03CFh	7 V D Trogistion 7	7.51	XXh
03D0h			7001
03D1h			
03D2h			
03D2h			
03D3H	A/D Control Register 2	ADCON2	00h
03D4H	77D Control Register 2	ADCONZ	3011
03D5h	A/D Control Register 0	ADCON0	00000XXXb
03D6h	A/D Control Register 1	ADCON0 ADCON1	00h
03D7h 03D8h	D/A Register 0	DA0	00h
03D6H	D/A Register 0	DAU	0011
03D9h 03DAh	D/A Pagister 1	I DA4	004
03DAn 03DBh	D/A Register 1	DA1	00h
	D/A Control Boniston	DACON	001-
03DCh	D/A Control Register	DACON	00h
03DDh	D (D(10) (1)	10011	100000000000000000000000000000000000000
03DEh	Port P14 Control Register (3)	PC14	XX00XXXXb
03DFh	Pull-Up Control Register 3 (3)	PUR3	00h
03E0h	Port P0 Register	P0	XXh
03E1h	Port P1 Register	P1	XXh
03E2h	Port P0 Direction Register	PD0	00h
03E3h	Port P1 Direction Register	PD1	00h
03E4h	Port P2 Register	P2	XXh
03E5h	Port P3 Register	P3	XXh
03E6h	Port P2 Direction Register	PD2	00h
03E7h	Port P3 Direction Register	PD3	00h
03E8h	Port P4 Register	P4	XXh
03E9h	Port P5 Register	P5	XXh
03EAh	Port P4 Direction Register	PD4	00h
03EBh	Port P5 Direction Register	PD5	00h
03ECh	Port P6 Register	P6	XXh
03EDh	Port P7 Register	P7	XXh
03EEh	Port P6 Direction Register	PD6	00h
03EFh	Port P7 Direction Register	PD7	00h
03F0h	Port P8 Register	P8	XXh
03F1h	Port P9 Register	P9	XXh
03F2h	Port P8 Direction Register	PD8	00X00000b
03F3h	Port P9 Direction Register	PD9	00h
03F4h	Port P10 Register	P10	XXh
03F5h	Port P11 Register (3)	P11	XXh
03F6h	Port P10 Direction Register	PD10	00h
03F7h	Port P11 Direction Register (3)	PD11	00h
03F8h	Port P12 Register (3)	P12	XXh
03F9h	Port P13 Register (3)	P13	XXh
03FAh	Port P12 Direction Register (3)	PD12	00h
03FBh	Port P13 Direction Register (3)	PD13	00h
03FCh	Pull-Up Control Register 0	PUR0	00h
		PUR1	00000000b (2)
03FDh	Pull-Up Control Register 1	1 01(1	
	Pull-Up Control Register 1 Pull-Up Control Register 2	PUR2	00000010b ⁽²⁾

NOTES:

- 1. The blank areas are reserved and cannot be accessed by users.
- At hardware reset 1 or hardware reset 2, the register is as follows:
 "00000000b" where "L" is inputted to the CNVSS pin
 "00000010b" where "H" is inputted to the CNVSS pin

 - At software reset, watchdog timer reset and oscillation stop detection reset, the register is as follows:

 - "00000000b" where the PM01 to PM00 bits in the PM0 register are "00b" (single-chip mode).
 "00000010b" where the PM01 to PM00 bits in the PM0 register are "01b" (memory expansion mode) or "11b" (microprocessor mode).
- 3. These registers do not exist in M16C/62P (80-pin version), and M16C/62PT (80-pin version).
- X : Nothing is mapped to this bit



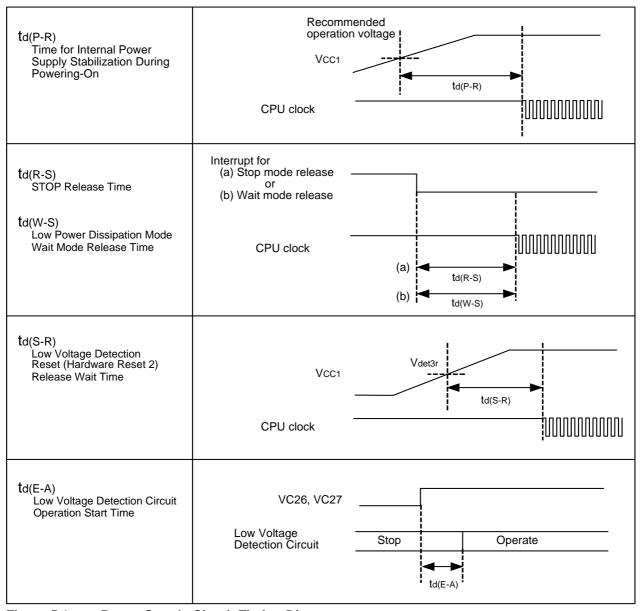


Figure 5.1 Power Supply Circuit Timing Diagram

Table 5.12 Electrical Characteristics (2) (1)

Symbol	Paramet	or.	Moos	uring Condition	,	Standar	b	Unit
Symbol	Faraniei	eı	ivieas	uning Condition	Min.	Тур.	Max.	Offic
Icc	Power Supply Current (Vcc1=Vcc2=4.0V to 5.5V)	In single-chip mode, the output	Mask ROM	f(BCLK)=24MHz No division, PLL operation		14	20	mA
	,	pins are open and other pins are Vss		No division, On-chip oscillation		1		mA
		outer puite die 1 ee	Flash Memory	f(BCLK)=24MHz, No division, PLL operation		18	27	mA
			,	No division, On-chip oscillation		1.8		mA
			Flash Memory Program	f(BCLK)=10MHz, VCC1=5.0V		15		mA
			Flash Memory Erase	f(BCLK)=10MHz, VCC1=5.0V		25		mA
			Mask ROM	f(XCIN)=32kHz Low power dissipation mode, ROM ⁽³⁾		25		μА
			Flash Memory	f(BCLK)=32kHz Low power dissipation mode, RAM ⁽³⁾		25		μА
				f(BCLK)=32kHz Low power dissipation mode, Flash Memory ⁽³⁾		420		μА
				On-chip oscillation, Wait mode		50		μА
			Mask ROM Flash Memory	f(BCLK)=32kHz Wait mode ⁽²⁾ , Oscillation capability High		7.5		μА
				f(BCLK)=32kHz Wait mode ⁽²⁾ , Oscillation capability Low		2.0		μА
				Stop mode Topr =25°C		0.8	3.0	μА
Idet4	Low Voltage Detection Diss	sipation Current (4)				0.7	4	μА
Idet3	Reset Area Detection Dissi	pation Current (4)				1.2	8	μА

- NOTES:

 1. Referenced to Vcc1=Vcc2=4.2 to 5.5V, Vss = 0V at Topr = -20 to 85°C / -40 to 85°C, f(BCLK)=24MHz unless otherwise specified.

 2. With one timer operated using fC32.

 3. This indicates the memory in which the program to be executed exists.

 4. Idea is dissipation current when the following bit is set to "1" (detection circuit enabled).

Idet4: VC27 bit in the VCR2 register Idet3: VC26 bit in the VCR2 register

Timing Requirements

(VCC1 = VCC2 = 5V, VSS = 0V, at Topr = -20 to 85°C / -40 to 85°C unless otherwise specified)

Table 5.21 Timer B Input (Counter Input in Event Counter Mode)

Symbol	Parameter	Stan	Unit	
Symbol	Oymbol I alameter		Max.	Offic
tc(TB)	TBilN Input Cycle Time (counted on one edge)	100		ns
tw(TBH)	TBilN Input HIGH Pulse Width (counted on one edge)	40		ns
tw(TBL)	TBiIN Input LOW Pulse Width (counted on one edge)	40		ns
tc(TB)	TBilN Input Cycle Time (counted on both edges)	200		ns
tw(TBH)	TBilN Input HIGH Pulse Width (counted on both edges)	80		ns
tw(TBL)	TBilN Input LOW Pulse Width (counted on both edges)	80		ns

Table 5.22 Timer B Input (Pulse Period Measurement Mode)

Symbol	Parameter		Standard		
Symbol	Falameter	Min.	Max.	Unit	
tc(TB)	TBilN Input Cycle Time	400		ns	
tw(TBH)	TBilN Input HIGH Pulse Width	200		ns	
tw(TBL)	TBilN Input LOW Pulse Width	200		ns	

Table 5.23 Timer B Input (Pulse Width Measurement Mode)

Symbol	Parameter	Stan	Unit	
Symbol	ymbol		Max.	Offic
tc(TB)	TBilN Input Cycle Time	400		ns
tw(TBH)	TBilN Input HIGH Pulse Width	200		ns
tw(TBL)	TBilN Input LOW Pulse Width	200		ns

Table 5.24 A/D Trigger Input

Symbol	Parameter	Standard		Unit
Symbol	Symbol		Max.	Offic
tc(AD)	ADTRG Input Cycle Time	1000		ns
tw(ADL)	ADTRG input LOW Pulse Width	125		ns

Table 5.25 Serial Interface

Symbol	Parameter	Star	Unit	
Symbol	Falanetei	Min.	Max.	Offic
tc(CK)	CLKi Input Cycle Time	200		ns
tw(CKH)	CLKi Input HIGH Pulse Width	100		ns
tw(CKL)	CLKi Input LOW Pulse Width	100		ns
td(C-Q)	TXDi Output Delay Time		80	ns
th(C-Q)	TXDi Hold Time	0		ns
tsu(D-C)	RXDi Input Setup Time	70		ns
th(C-D)	RXDi Input Hold Time	90		ns

Table 5.26 External Interrupt INTi Input

Symbol	Parameter	Stan	Unit		
Symbol	Falanielei	Min.	Max.	Offic	
tw(INH)	INTi Input HIGH Pulse Width	250		ns	
tw(INL)	INTi Input LOW Pulse Width	250		ns	

Switching Characteristics

(VCC1 = VCC2 = 5V, VSS = 0V, at Topr = -20 to 85°C / -40 to 85°C unless otherwise specified)

Table 5.27 Memory Expansion and Microprocessor Modes (for setting with no wait)

Symbol	nbol Parameter		Standard		Unit	
Symbol			Min.	Max.	Offic	
td(BCLK-AD)	Address Output Delay Time			25	ns	
th(BCLK-AD)	Address Output Hold Time (in relation to BCLK)		4		ns	
th(RD-AD)	Address Output Hold Time (in relation to RD)		0		ns	
th(WR-AD)	Address Output Hold Time (in relation to WR)		(NOTE 2)		ns	
td(BCLK-CS)	Chip Select Output Delay Time			25	ns	
th(BCLK-CS)	Chip Select Output Hold Time (in relation to BCLK)		4		ns	
td(BCLK-ALE)	ALE Signal Output Delay Time			15	ns	
th(BCLK-ALE)	ALE Signal Output Hold Time	0	-4		ns	
td(BCLK-RD)	RD Signal Output Delay Time	See Figure 5.2		25	ns	
th(BCLK-RD)	RD Signal Output Hold Time	i igure 3.2	0		ns	
td(BCLK-WR)	WR Signal Output Delay Time			25	ns	
th(BCLK-WR)	WR Signal Output Hold Time		0		ns	
td(BCLK-DB)	Data Output Delay Time (in relation to BCLK)			40	ns	
th(BCLK-DB)	Data Output Hold Time (in relation to BCLK) (3)		4		ns	
td(DB-WR)	Data Output Delay Time (in relation to WR)		(NOTE 1)		ns	
th(WR-DB)	Data Output Hold Time (in relation to WR) (3)		(NOTE 2)		ns	
td(BCLK-HLDA)	HLDA Output Delay Time			40	ns	

NOTES:

1. Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \text{x} 10^9}{\text{f(BCLK)}} - 40 [\text{ns}] \hspace{1cm} \text{f(BCLK) is 12.5MHz or less.}$$

2. Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{\mathsf{f}(\mathsf{BCLK})} - 10[\mathsf{ns}]$$

3. This standard value shows the timing when the output is off, and does not show hold time of data bus.

Hold time of data bus varies with capacitor volume and pull-up (pull-down) resistance value.

Hold time of data bus is expressed in

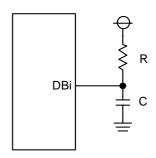
$$t = -CR X In (1-VoL / Vcc2)$$

by a circuit of the right figure.

For example, when VoL = 0.2Vcc2, C = 30pF, R = 1k Ω , hold time of output "L" level is

$$t = -30pF X 1k \Omega X In(1-0.2Vcc2 / Vcc2)$$

= 6.7 ns.



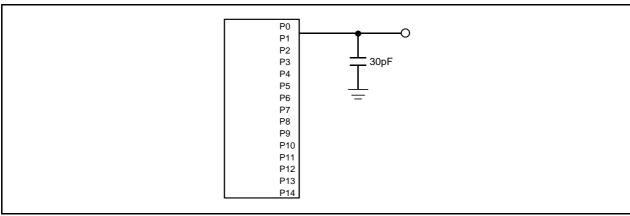


Figure 5.2 Ports P0 to P14 Measurement Circuit

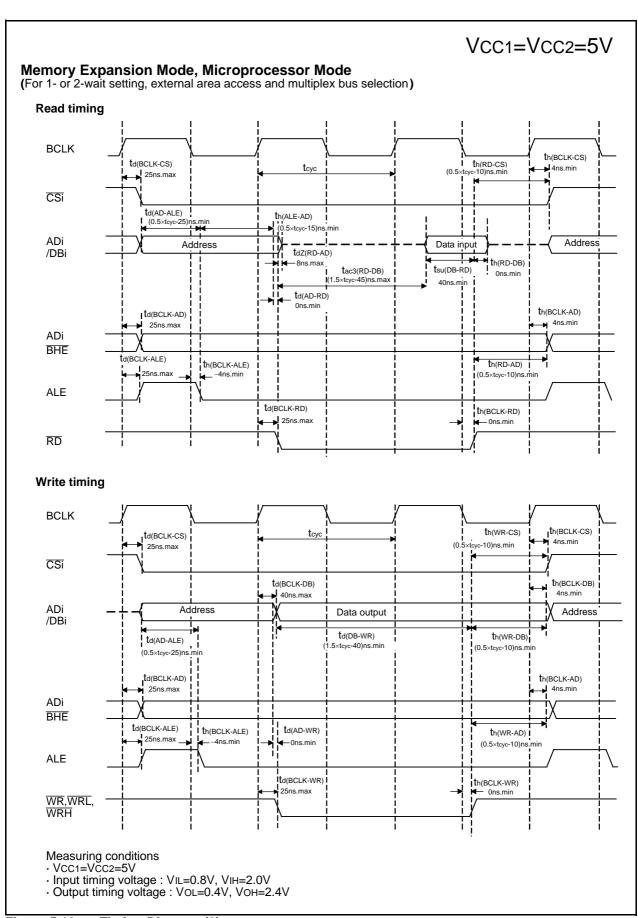


Figure 5.10 Timing Diagram (8)

Switching Characteristics

(VCC1 = VCC2 = 3V, VSS = 0V, at Topr = -20 to 85°C / -40 to 85°C unless otherwise specified)

Table 5.46 Memory Expansion and Microprocessor Modes (for setting with no wait)

Symbol	Parameter		Stan	dard	Unit
Symbol	Faianetei		Min.	Max.	Offic
td(BCLK-AD)	Address Output Delay Time			30	ns
th(BCLK-AD)	Address Output Hold Time (in relation to BCLK)		4		ns
th(RD-AD)	Address Output Hold Time (in relation to RD)		0		ns
th(WR-AD)	Address Output Hold Time (in relation to WR)		(NOTE 2)		ns
td(BCLK-CS)	Chip Select Output Delay Time			30	ns
th(BCLK-CS)	Chip Select Output Hold Time (in relation to BCLK)		4		ns
td(BCLK-ALE)	ALE Signal Output Delay Time			25	ns
th(BCLK-ALE)	ALE Signal Output Hold Time	1	-4		ns
td(BCLK-RD)	RD Signal Output Delay Time	See Figure 5.12		30	ns
th(BCLK-RD)	RD Signal Output Hold Time	Tigule 3.12	0		ns
td(BCLK-WR)	WR Signal Output Delay Time			30	ns
th(BCLK-WR)	WR Signal Output Hold Time		0		ns
td(BCLK-DB)	Data Output Delay Time (in relation to BCLK)			40	ns
th(BCLK-DB)	Data Output Hold Time (in relation to BCLK) (3)		4		ns
td(DB-WR)	Data Output Delay Time (in relation to WR)		(NOTE 1)		ns
th(WR-DB)	Data Output Hold Time (in relation to WR) (3)	7	(NOTE 2)		ns
td(BCLK-HLDA)	HLDA Output Delay Time	7		40	ns

NOTES:

1. Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \text{x} 10^9}{\text{f(BCLK)}} - 40 [\text{ns}] \hspace{1cm} \text{f(BCLK) is 12.5MHz or less.}$$

2. Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f(BCLK)} - 10[ns]$$

3. This standard value shows the timing when the output is off, and does not show hold time of data bus.

Hold time of data bus varies with capacitor volume and pull-up (pull-down) resistance value.

Hold time of data bus is expressed in

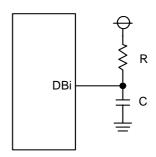
$$t = -CR X In (1-VoL / Vcc2)$$

by a circuit of the right figure.

For example, when VoL = 0.2Vcc2, C = 30pF, R = 1k Ω , hold time of output "L" level is

$$t = -30pF X 1k \Omega X In(1-0.2Vcc2 / Vcc2)$$

= 6.7 ns.



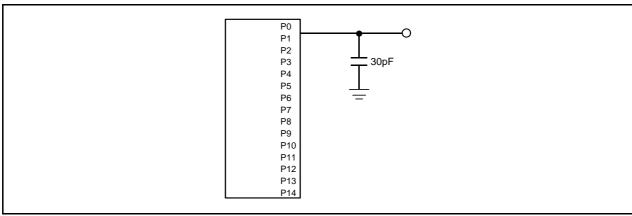


Figure 5.12 Ports P0 to P14 Measurement Circuit

Page 70 of 96

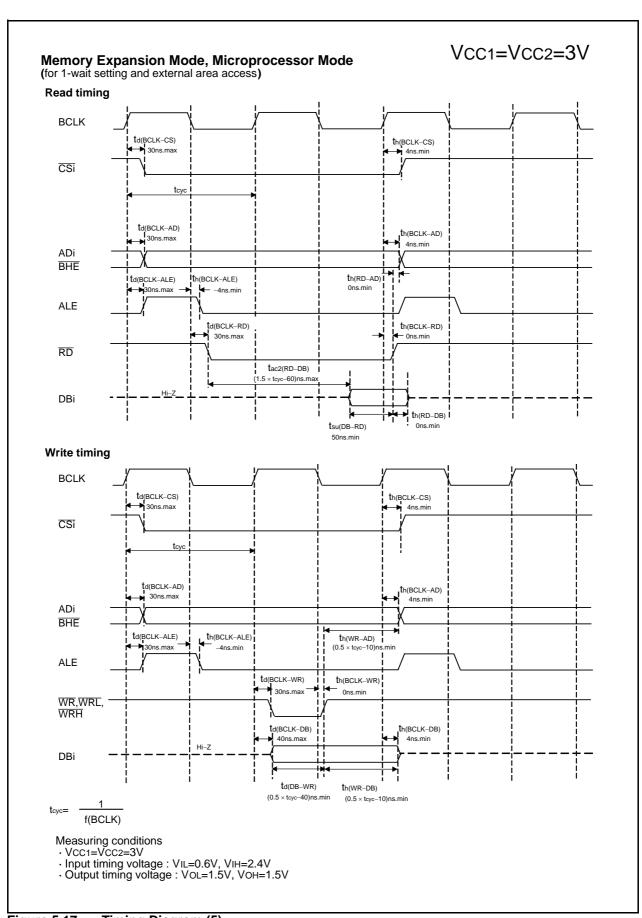


Figure 5.17 Timing Diagram (5)

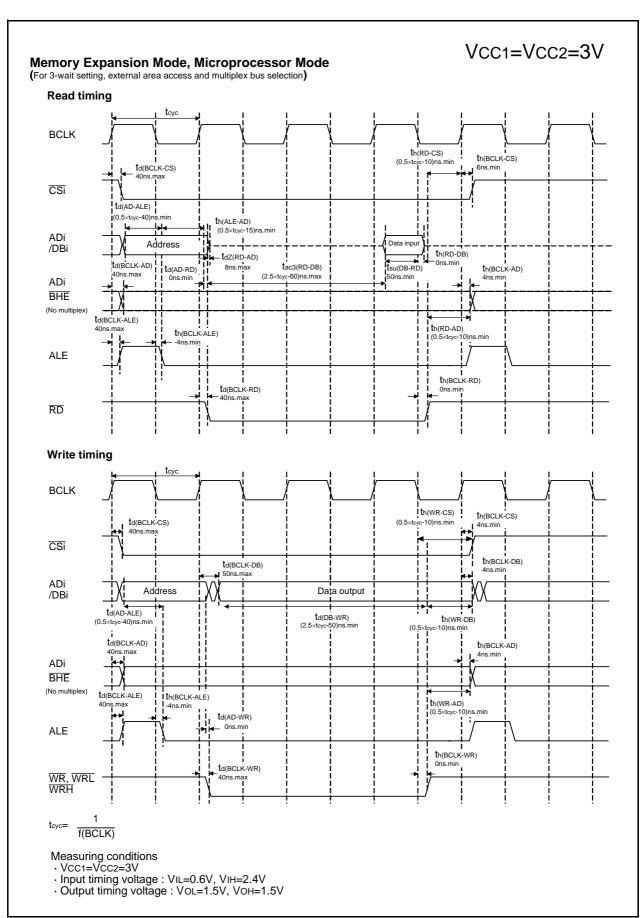


Figure 5.21 Timing Diagram (9)

5.2 Electrical Characteristics (M16C/62PT)

Table 5.49 Absolute Maximum Ratings

Symbol		Parameter	Condition	Rated Value	Unit
VCC1, VCC2	Supply Voltage		Vcc1=Vcc2=AVcc	-0.3 to 6.5	V
AVcc	Analog Supply Voltage		Vcc1=Vcc2=AVcc	-0.3 to 6.5	V
Vı	Input Voltage	RESET, CNVSS, BYTE, P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P14_0, P14_1, VREF, XIN		-0.3 to Vcc1+0.3 (1)	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P12_0 to P12_7, P13_0 to P13_7		-0.3 to Vcc2+0.3 ⁽¹⁾	V
		P7_0, P7_1		-0.3 to 6.5	V
Vo	Output Voltage	P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P14_0, P14_1, XOUT		-0.3 to Vcc1+0.3 ⁽¹⁾	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P12_0 to P12_7, P13_0 to P13_7		-0.3 to Vcc2+0.3 ⁽¹⁾	٧
		P7_0, P7_1		-0.3 to 6.5	V
Pd	Power Dissipation	on	-40°C <topr≤85°c< td=""><td>300</td><td>mW</td></topr≤85°c<>	300	mW
			85°C <topr≤125°c< td=""><td>200</td><td>IIIVV</td></topr≤125°c<>	200	IIIVV
Topr	Operating Ambient	When the Microcomputer is Operating		-40 to 85 / -40 to 125	°C
	Temperature	Flash Program Erase		0 to 60	
Tstg	Storage Temper	ature		-65 to 150	°C

NOTES:

- 1. There is no external connections for port P1_0 to P1_7, P4_4 to P4_7, P7_2 to P7_5 and P9_1 in 80-pin version.
- 2. T version = -40 to 85 °C, V version = -40 to 125 °C.

	•			•	, ,	,	
Symbol	Parameter		Standard			Unit	
Symbol			Min.	Тур.	Max.	Offic	
_	Program and Erase Endurance (3)		100			cycle	
_	Word Program Time (Vcc1=5.0V)	Word Program Time (Vcc1=5.0V)			200	μS	
_	Lock Bit Program Time		25	200	μS		
_	Block Erase Time	4-Kbyte block	4	0.3	4	S	
_	(Vcc1=5.0V)	8-Kbyte block		0.3	4	S	
_		32-Kbyte block		0.5	4	S	
_		64-Kbyte block		0.8	4	S	
-	Erase All Unlocked Blocks Time (2)				4×n	S	
tps	Flash Memory Circuit Stabilization Wait Ti	me			15	μS	
_	Data Hold Time (5)		20			year	

Table 5.53 Flash Memory Version Electrical Characteristics (1) for 100 cycle products (B, U)

Table 5.54 Flash Memory Version Electrical Characteristics (6) for 10,000 cycle products (B7, U7) (Block A and Block 1 (7))

Symbol	Parameter			Unit		
Symbol			Min.	Тур.	Max.	Offic
-	Program and Erase Endurance (3, 8, 9)		10,000 (4)			cycle
=	Word Program Time (Vcc1=5.0V)		25		μS	
-	Lock Bit Program Time			25		μS
	Block Erase Time (Vcc1=5.0V)	4-Kbyte block	4	0.3		s
tps	Flash Memory Circuit Stabilization Wait Time				15	μS
-	Data Hold Time (5)		20			year

NOTES:

- 1. Referenced to Vcc1=4.5 to 5.5V at Topr = 0 to 60 °C unless otherwise specified.
- 2. n denotes the number of block erases.
- In denotes the number of block erases.
 Program and Erase Endurance refers to the number of times a block erase can be performed.
 If the program and erase endurance is n (n=100, 1,000, or 10,000), each block can be erased n times.
 For example, if a 4 Kbytes block A is erased after writing 1 word data 2,048 times, each to a different address, this counts as one program and erase endurance. Data cannot be written to the same address more than once without erasing the block. (Rewrite prohibited)
- 4. Maximum number of E/W cycles for which operation is guaranteed.

Page 85 of 96

- 5. Ta (ambient temperature)=55 °C. As to the data hold time except Ta=55 °C, please contact Renesas Technology Corp. or an authorized Renesas Technology Corp. product distributor.
- 6. Referenced to Vcc1 = 4.5 to 5.5V at Topr = -40 to 85 °C (B7, U7 (T version)) / -40 to 125 °C (B7, U7 (V version)) unless otherwise specified.
- 7. Table 5.54 applies for block A or block 1 program and erase endurance > 1,000. Otherwise, use Table 5.53.
- 8. To reduce the number of program and erase endurance when working with systems requiring numerous rewrites, write to unused word addresses within the block instead of rewrite. Erase block only after all possible addresses are used. For example, an 8-word program can be written 256 times maximum before erase becomes necessary.
 Maintaining an equal number of erasure between block A and block 1 will also improve efficiency. It is important to track the total number of times erasure is used.
- 9. Should erase error occur during block erase, attempt to execute clear status register command, then block erase command at least three times until erase error disappears.
- 10. Set the PM17 bit in the PM1 register to "1" (wait state) when executing more than 100 times rewrites (B7 and U7).
- 11. Customers desiring E/W failure rate information should contact their Renesas technical support representative.

Table 5.55 Flash Memory Version Program/Erase Voltage and Read Operation Voltage Characteristics (at Topr = 0 to 60 $^{\circ}$ C(B, U), Topr = -40 to 85 $^{\circ}$ C (B7, U7 (T version)) / -40 to 125 $^{\circ}$ C (B7, U7 (V version))

Flash Program, Erase Voltage	Flash Read Operation Voltage
$VCC1 = 5.0 V \pm 0.5 V$	Vcc1=4.0 to 5.5 V

Table 5.57 Electrical Characteristics (1) (1)

Symbol		Parameter		Measuring Condition	Standard			Unit
Cymbol				Wedsuming Condition	Min.	Тур.	Max.	Onne
Vон	HIGH Output Voltage (2)	P6_0 to P6_7, P7_2 to P7_7 P8_6, P8_7, P9_0 to P9_7, P11_0 to P11_7, P14_0, P14	P10_0 to P10_7,	IOH=-5mA	Vcc1-2.0		VCC1	V
		P0_0 to P0_7, P1_0 to P1_7 P3_0 to P3_7, P4_0 to P4_7 P12_0 to P12_7, P13_0 to P	7, P5_0 to P5_7,	IOH=-5mA	Vcc2-2.0		VCC2	V
Vон	HIGH Output Voltage (2)	P6_0 to P6_7, P7_2 to P7_7 P8_6, P8_7, P9_0 to P9_7, P11_0 to P11_7, P14_0, P14_0	P10_0 to P10_7,	ΟΗ=-200μΑ	Vcc1-0.3		Vcc1	V
		P0_0 to P0_7, P1_0 to P1_7 P3_0 to P3_7, P4_0 to P4_7 P12_0 to P12_7, P13_0 to P	7, P5_0 to P5_7,	ΙΟΗ=-200μΑ	Vcc2-0.3		VCC2	V
Vон	HIGH Outpu	t Voltage XOUT	HIGHPOWER	IOH=-1mA	Vcc1-2.0		Vcc1	V
			LOWPOWER	IOH=-0.5mA	Vcc1-2.0		Vcc1	V
	HIGH Outpu	t Voltage XCOUT	HIGHPOWER	With no load applied		2.5		.,
			LOWPOWER	With no load applied		1.6		V
Vol	LOW Output Voltage (2)	P6_0 to P6_7, P7_0 to P7_7 P8_6, P8_7, P9_0 to P9_7, P11_0 to P11_7, P14_0, P14	P10_0 to P10_7,	IOL=5mA			2.0	V
		P0_0 to P0_7, P1_0 to P1_7 P3_0 to P3_7, P4_0 to P4_7 P12_0 to P12_7, P13_0 to P	7, P5_0 to P5_7,	IOL=5mA			2.0	V
Vol	L LOW Output Voltage (2) P6_0 to P6_7, P7_0 to P9_P11_0 to P11_7, P14_0, P0_0 to P0_7, P1_0 to P12_0 to P12_7, P13_0 to P12_7,		P10_0 to P10_7,	IOL=200μA			0.45	V
			7, P5_0 to P5_7,	IOL=200μA			0.45	V
Vol	LOW Output	Voltage XOUT	HIGHPOWER	IOL=1mA			2.0	.,
			LOWPOWER	IOL=0.5mA			2.0	V
	LOW Output	Voltage XCOUT	HIGHPOWER	With no load applied		0		.,
			LOWPOWER	With no load applied		0		V
VT+-VT-	Hysteresis	HOLD, RDY, TA0IN to TA4II INT0 to INT5, NMI, ADTRG, TA0OUT to TA4OUT, KI0 to SCL0 to SCL2, SDA0 to SDA	CTS0 to CTS2, CLK0 to CLK4, KI3, RXD0 to RXD2,		0.2		1.0	V
VT+-VT-	Hysteresis	RESET			0.2		2.5	V
lін	HIGH Input Current (2)		P12_7, P13_0 to P13_7,	VI=5V			5.0	μА
lı∟	LOW Input Current (2)			VI=0V			-5.0	μА
RPULLUP	Pull-Up Resistance (2)	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7,		VI=0V	30	50	170	kΩ
RfXIN	Feedback Re	esistance XIN				1.5		МΩ
RfXCIN	Feedback Re	Feedback Resistance XCIN				15		МΩ
VRAM	RAM Retent	ion Voltage		At stop mode	2.0			V

NOTES:

1. Referenced to Vcc1=Vcc2=4.0 to 5.5V, Vss = 0V at Topr = -40 to 85°C / -40 to 125°C, f(BCLK)=24MHz unless otherwise specified. T version = -40 to 85°C, V version = -40 to 125°C.

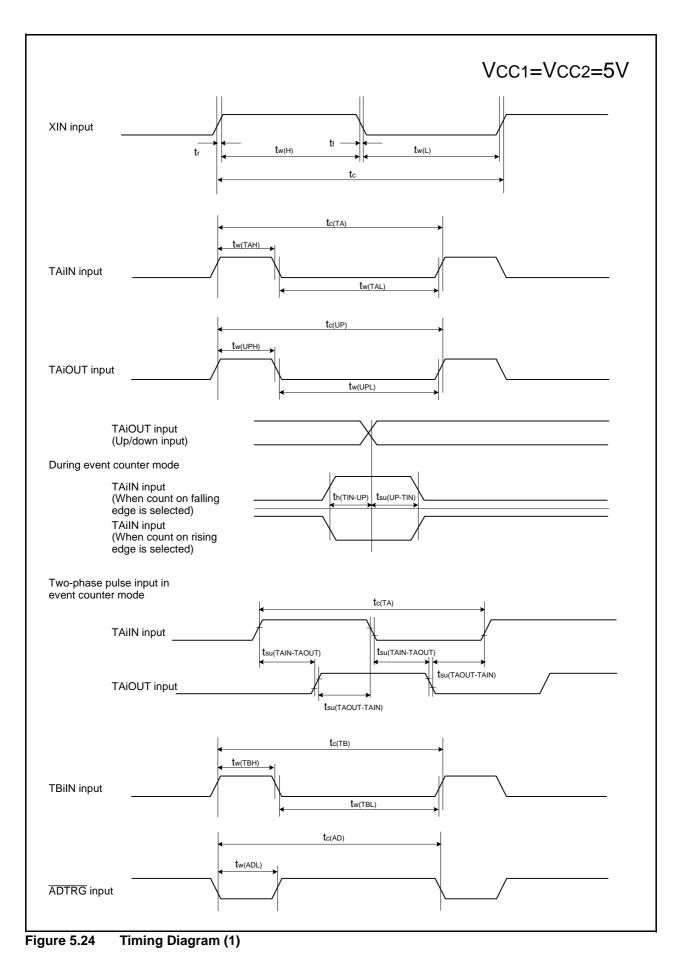
2. There is no external connections for port P1_0 to P1_7, P4_4 to P4_7, P7_2 to P7_5 and P9_1 in 80-pin version.

Timing Requirements

(VCC1 = VCC2 = 5V, Vss = 0V, at T_{opr} = -40 to 85°C (T version) / -40 to 125°C (V version) unless otherwise specified)

Table 5.59 External Clock Input (XIN input)

Symbol	Parameter	Stan	Unit	
Symbol	Faianietei	Min.	Max.	Offic
tc	External Clock Input Cycle Time		ns	
tw(H)	External Clock Input HIGH Pulse Width	25		ns
tw(L)	External Clock Input LOW Pulse Width 25			
tr	External Clock Rise Time		15	ns
tf	External Clock Fall Time		15	ns



RENESAS

REVISION HISTORY

Pov	Data		Description
Rev.	Date	Page	Summary
1.10	May 28, 2003	1	Applications are partly revised.
		2	Table 1.1.1 is partly revised.
		4-5	Table 1.1.2 and 1.1.3 is partly revised.
			"Note 1" is partly revised.
		22	Table 1.5.3 is partly revised.
		23	Table 1.5.5 is partly revised.
			Table 1.5.6 is added.
		24	Table 1.5.9 is partly revised.
		30	Notes 1 and 2 in Table 1.5.26 is partly revised.
		31	Notes 1 in Table 1.5.27 is partly revised.
		30-31	Note 3 is added to "Data output hold time (refers to BCLK)" in Table 1.5.26 and 1.5.27.
		32	Note 4 is added to "th(ALE-AD)" in Table 1.5.28.
		30-32	Switching Characteristics is partly revised.
		36-39	th(WR-AD) and th(WR-DB) in Figure 1.5.5 to 1.5.8 is partly revised.
		40-41	th(ALE-AD), th(WR-CS), th(WR-DB) and th(WR-AD) in Figure 1.5.9 to
		42	1.5.10 is partly revised.
			Note 2 is added to Table 1.5.29.
		47	Notes 1 and 2 in Table 1.5.45 is partly revised.
		48 47-48	Notes 1 in Table 1.5.46 is partly revised.
		47-40	Note 3 is added to "Data output hold time (refers to BCLK)" in Table
		49	1.5.45 and 1.5.46.
		49 47-48	Note 4 is added to "th(ALE-AD)" in Table 1.5.47. Switching Characteristics is partly revised.
		_	th(WR-AD) and th(WR-DB) in Figure 1.5.15 to 1.5.18 is partly revised.
		57-58	th(ALE-AD), th(WR-CS), th(WR-DB) and th(WR-AD) in Figure 1.5.19 to
			1.5.20 is partly revised.
2.00	Oct 29, 2003	-	Since high reliability version is added, a group name is revised. M16C/62 Group (M16C/62P) → M16C/62 Group (M16C/62P, M16C/62PT)
		2-4	Table 1.1 to 1.3 are revised. Note 3 is partly revised.
		2-4	Table 1.1 to 1.3 are revised.
			Note 3 is partly revised.
		6	Figure 1.2 Note5 is deleted.
		7-9	Table 1.4 to 1.7 Product List is partly revised.
		11	Table 1.8 and Figure 1.4 are added.
		12-15	Figure 1.5 to 1.9 ZP is added. Table 1.10 and 1.12 ZP is added to timer A.
		17,19	
		18,20 30	Table 1.11 and 1.13 VCC1 is added to VREF. Table 5.1 is revised.
		31-32	
		01-02	Table 5.2 and 5.3 are revised.