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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded - Microcontrollers</u>"

Details	
Product Status	Obsolete
Core Processor	M16C/60
Core Size	16-Bit
Speed	24MHz
Connectivity	I ² C, IEBus, UART/USART
Peripherals	DMA, WDT
Number of I/O	50
Program Memory Size	-
Program Memory Type	ROMIess
EEPROM Size	-
RAM Size	20K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 26x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-BQFP
Supplier Device Package	100-QFP (14x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/m30624spfp-u5c

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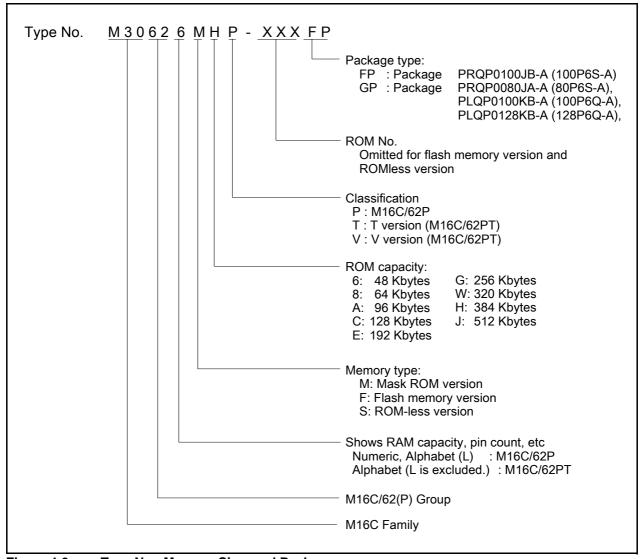


Figure 1.3 Type No., Memory Size, and Package

Pin Characteristics for 100-Pin Package (1) **Table 1.13**

Pin FP	No. GP	Control Pin	Port	Interrupt Pin	Timer Pin	UART Pin	Analog Pin	Bus Control Pin
1	99		P9_6	-		SOUT4	ANEX1	
2	100		P9_5			CLK4	ANEX0	
3	1		P9_4		TB4IN	OLIV	DA1	
4	2		P9_3		TB3IN		DA0	
5	3		P9_2		TB2IN	SOUT3	DAO	
6	4		P9_1		TB1IN	SIN3		
7	5		P9_0		TB0IN	CLK3		
8	6	BYTE						
9	7	CNVSS						
10	8	XCIN	P8_7					
11	9	XCOUT	P8_6					
12	10	RESET						
13	11	XOUT						
14	12	VSS						
15	13	XIN						
16	14	VCC1						
17	15		P8_5	NMI				
18	16		P8_4	INT2	ZP			
19	17		P8_3	ĪNT1				
20	18		P8_2	ĪNT0				
21	19		P8_1		TA4IN/U			
22	20		P8_0		TA4OUT/U			
23	21		P7_7		TA3IN			
24	22		P7_6		TA3OUT			
25	23		P7_5		TA2IN/W			
26	24		P7_4		TA2OUT/W			
27	25		P7_3		TA1IN/V	CTS2/RTS2		
28	26		P7_2		TA1OUT/V	CLK2		
29	27		P7_1		TA0IN/TB5IN	RXD2/SCL2		
30	28		P7_0		TA0OUT	TXD2/SDA2		
31	29		P6_7			TXD1/SDA1		
32	30		P6_6			RXD1/SCL1		
33	31		P6_5			CLK1		
34	32		P6_4			CTS1/RTS1/CTS0/CLKS1		
35	33		P6_3			TXD0/SDA0		
36	34		P6_2			RXD0/SCL0		
37	35		P6_1			CLK0		
38	36		P6_0			CTS0/RTS0		
39	37		P5_7					RDY/CLKOUT
40	38		P5_6					ALE
41	39		P5_5					HOLD
42	40		P5_4					HLAD
43	41		P5_3	1				BCLK
44	42		P5_2					RD
45	43		P5_1					WRH/BHE
46	44							WRL/WR
			P5_0					
47	45		P4_7					CS3
48	46		P4_6	ļ				CS2
49	47		P4_5					CS1
50	48		P4_4					CS0

Pin Characteristics for 100-Pin Package (2) **Table 1.14**

Table				ensues ioi i		g- (=)		1
Pin FP	No. GP	Control Pin	Port	Interrupt Pin	Timer Pin	UART Pin	Analog Pin	Bus Control Pin
51	49		P4_3					A19
52	50		P4_2					A18
53	51		P4_1					A17
54	52		P4_0					A16
55	53		P3_7					A15
56	54		P3_6					A14
57	55		P3_5					A13
58	56		P3_4					A12
59	57		P3_3					A11
60	58		P3_2					A10
61	59		P3_1					A9
62	60	VCC2						
63	61		P3_0					A8(/-/D7)
64	62	VSS						
65	63		P2_7				AN2_7	A7(/D7/D6)
66	64		P2_6				AN2_6	A6(/D6/D5)
67	65		P2_5				AN2_5	A5(/D5/D4)
68	66		P2_4				AN2_4	A4(/D4/D3)
69	67		P2_3				AN2_3	A3(/D3/D2)
70 71	68 69		P2_2 P2_1				AN2_2 AN2_1	A2(/D2/D1) A1(/D1/D0)
72	70		P2_0				AN2_1 AN2_0	A0(/D0/-)
73	71			INT5			74142_0	D15
+			P1_7					
74	72		P1_6	INT4				D14
75	73		P1_5	INT3				D13
76	74		P1_4					D12
77	75		P1_3					D11
78	76		P1_2					D10
79	77		P1_1					D9
80	78		P1_0					D8
81	79		P0_7				AN0_7	D7
82	80		P0_6				AN0_6	D6
83	81		P0_5				AN0_5	D5
84	82		P0_4				AN0_4	D4
85	83		P0_3				AN0_3	D3
86	84		P0_2				AN0_2	D2
87	85		P0_1				AN0_1	D1
88	86		P0_0	 			AN0_0	D0
89	87		P10_7	KI3			AN7	
90	88		P10_6	KI2			AN6	
91	89		P10_5	KI1			AN5	
92	90		P10_4	KI0			AN4	
93	91		P10_3				AN3	
94	92		P10_2				AN2	
95	93		P10_1				AN1	
96	94	AVSS						
97	95		P10_0				AN0	
98	96	VREF						
99	97	AVCC						
100	98		P9_7			SIN4	ADTRG	
		l .		1		L		1

Table 1.15 Pin Characteristics for 80-Pin Package (1)

Pin No.	Control Pin		Interrupt Pin	Timer Pin	UART Pin	Analog Pin	Bus Control Pin
1		P9_5			CLK4	ANEX0	
2		P9_4		TB4IN		DA1	
3		P9_3		TB3IN		DA0	
4		P9_2		TB2IN	SOUT3		
5		P9_0		TB0IN	CLK3		
6	CNVSS (BYTE)						
7	XCIN	P8_7					
8	XCOUT	P8_6					
9	RESET						
10	XOUT						
11	VSS						
12	XIN						
13	VCC1		l				
14		P8_5	NMI				
15		P8_4	ĪNT2	ZP			
16		P8_3	ĪNT1				
17		P8_2	ĪNT0				
18		P8_1		TA4IN			
19		P8_0		TA4OUT			
20		P7_7		TA3IN			
21		P7_6		TA3OUT			
22		P7_1		TA0IN/TB5IN	RXD2/SCL2		
23		P7_0		TA0OUT	TXD2/SDA2		
24		P6_7			TXD1/SDA1		
25		P6_6			RXD1/SCL1		
26		P6_5			CLK1		
27		P6_4			CTS1/RTS1/CTS0/CLKS1		
28		P6_3			TXD0/SDA0		
29		P6_2			RXD0/SCL0		
30		P6_1			CLK0		
31		P6_0			CTS0/RTS0		
32		P5_7					CLKOUT
33		P5_6					
34		P5_5					
35		P5_4					
36		P5_3					
37		P5_2					
38		P5_1					
39		P5_0					
40							
		P4_3					
41		P4_2					
42		P4_1					
43		P4_0					
44		P3_7					
45		P3_6					
46		P3_5					
47		P3_4					
48		P3_3					
49		P3_2				1	
50		P3_1		1			
50		J_	j	<u> </u>		j	1

Table 1.21 Pin Description (80-pin Version) (2)

Signal Name	Pin Name	I/O	Power	Description
Reference voltage input	VREF	Type	Supply ⁽¹⁾ VCC1	Applies the reference voltage for the A/D converter and D/A converter.
A/D converter	AN0 to AN7, AN0_0 to AN0_7, AN2_0 to AN2_7	I	VCC1	Analog input pins for the A/D converter.
	ADTRG	I	VCC1	This is an A/D trigger input pin.
	ANEX0	I/O	VCC1	This is the extended analog input pin for the A/D converter, and is the output in external op-amp connection mode.
	ANEX1	I	VCC1	This is the extended analog input pin for the A/D converter.
D/A converter	DA0, DA1	0	VCC1	This is the output pin for the D/A converter.
I/O port ⁽¹⁾	P0_0 to P0_7, P2_0 to P2_7, P3_0 to P3_7, P5_0 to P5_7, P6_0 to P6_7, P10_0 to P10_7	I/O	VCC1	8-bit I/O ports in CMOS, having a direction register to select an input or output. Each pin is set as an input port or output port. An input port can be set for a pull-up or for no pull-up in 4-bit unit by program.
	P8_0 to P8_4, P8_6, P8_7, P9_0, P9_2 to P9_7	I/O	VCC1	I/O ports having equivalent functions to P0.
	P4_0 to P4_3, P7_0, P7_1, P7_6, P7_7	I/O	VCC1	I/O ports having equivalent functions to P0. (however, output of P7_0 and P7_1 for the N-channel open drain output.)
Input port	P8_5	I	VCC1	Input pin for the NMI interrupt. Pin states can be read by the P8_5 bit in the P8 register.

I: Input O: Output I/O: Input and output

NOTES:

1. There is no external connections for port P1, P4_4 to P4_7, P7_2 to P7_5 and P9_1 in 80-pin version. Set the direction bits in these ports to "1" (output mode), and set the output data to "0" ("L") using the program.

2.2 Address Registers (A0 and A1)

The register A0 consists of 16 bits, and is used for address register indirect addressing and address register relative addressing. They also are used for transfers and logic/logic operations. A1 is the same as A0. In some instructions, registers A1 and A0 can be combined for use as a 32-bit address register (A1A0).

2.3 Frame Base Register (FB)

FB is configured with 16 bits, and is used for FB relative addressing.

2.4 Interrupt Table Register (INTB)

INTB is configured with 20 bits, indicating the start address of an interrupt vector table.

2.5 Program Counter (PC)

PC is configured with 20 bits, indicating the address of an instruction to be executed.

2.6 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

Stack pointer (SP) comes in two types: USP and ISP, each configured with 16 bits. Your desired type of stack pointer (USP or ISP) can be selected by the U flag of FLG.

2.7 Static Base Register (SB)

SB is configured with 16 bits, and is used for SB relative addressing.

2.8 Flag Register (FLG)

FLG consists of 11 bits, indicating the CPU status.

2.8.1 Carry Flag (C Flag)

This flag retains a carry, borrow, or shift-out bit that has occurred in the arithmetic/logic unit.

2.8.2 Debug Flag (D Flag)

The D flag is used exclusively for debugging purpose. During normal use, it must be set to "0".

2.8.3 Zero Flag (Z Flag)

This flag is set to "1" when an arithmetic operation resulted in 0; otherwise, it is "0".

2.8.4 Sign Flag (S Flag)

This flag is set to "1" when an arithmetic operation resulted in a negative value; otherwise, it is "0".

2.8.5 Register Bank Select Flag (B Flag)

Register bank 0 is selected when this flag is "0"; register bank 1 is selected when this flag is "1".

2.8.6 Overflow Flag (O Flag)

This flag is set to "1" when the operation resulted in an overflow; otherwise, it is "0".

2.8.7 Interrupt Enable Flag (I Flag)

This flag enables a maskable interrupt.

Maskable interrupts are disabled when the I flag is "0", and are enabled when the I flag is "1". The I flag is cleared to "0" when the interrupt request is accepted.



Table 4.2 SFR Information (2) (1)

1904245				
100415		Register	Symbol	After Reset
1904245	0040h			
100434h 1173 Interrupt Control Register 100000000000000000000000000000000000	0041h			
10045h	0042h			
0945h Timer BS Interrupt Control Register TISSIC XXXXXX000b 0948h Timer B Interrupt Control Register TISSIC XXXXXX000b 0947h Timer BS Interrupt Control Register, UNRTO BUS Collision Detection Interrupt Control Register TISSIC, UDBCNIC XXXXXX000b 0948h SILOS Interrupt Control Register, INT4 Interrupt Control Register SIC, INT5IC XXXXXX000b 0948h SILOS Interrupt Control Register (INT4 Interrupt Control Register SIRC, INT5IC XXXXXX000b 0948h DIVAD Interrupt Control Register DIVIDIO XXXXXX000b 0948h DIVAD Interrupt Control Register DIVIDIO XXXXXX00b 0948h DIVAD Interrupt Control Register DIVIDIO XXXXXX00b 0948h DIVAD Interrupt Control Register DIVIDIO XXXXXX00b 0948h DIVAD Register DIVIDIO XXXXXX00b 0948h DIVAD Register SITIC XXXXXX00b 0948h LAST Register SITIC XXXXXX00b 0956h LART Register Interrupt Control Register SITIC XXXXXX00b 0956h LART Register Interrupt Cont	0043h			
0946h Timer 64 Hintering Control Register UART I BUS Collision Detection Interrupt Control Register T84IC, UBRONIC XXXXXX0000b 0947h Timer 58 Interrupt Control Register UART I BUS Collision Detection Interrupt Control Register SIGL, INTSIC XXXXXX0000b 0948h SIJO4 Interrupt Control Register, INT5 Interrupt Control Register SIGL, INTSIC XXXXXX000b 0948h DAM Collision Detection Interrupt Control Register BKNIC XXXXXX000b 0948h DAM Direrupt Control Register DMIC XXXXXX000b 0948h DAM Direrupt Control Register DMIC XXXXXX000b 0948h DAM Direrupt Control Register DMIC XXXXXX000b 0948h DAM Tribut Interrupt Control Register RUPIC XXXXXX000b 0948h DAM Tribut Interrupt Control Register ADIC XXXXXXX00b 0948h DAM Tribut Interrupt Control Register ADIC XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX	0044h	INT3 Interrupt Control Register	INT3IC	XX00X000b
1984 Street 1985 Common 1985 Commo	0045h	Timer B5 Interrupt Control Register	TB5IC	XXXXX000b
00498	0046h		TB4IC, U1BCNIC	XXXXX000b
00498	0047h	Timer B3 Interrupt Control Register, UART0 BUS Collision Detection Interrupt Control Register	TB3IC, U0BCNIC	XXXXX000b
0048h UAR12 Bus Collision Defection Interrupt Control Register BCNIC XXXXX0000b 0040h DMAD Interrupt Control Register DMIIC XXXXX000b 0040h DMAI Therrupt Control Register DMIIC XXXXX000b 0040h Ky Interrupt Control Register KUPIC XXXXX000b 0044h ADIC Conversion Interrupt Control Register SZIIC XXXXX000b 0044h ADIC Tonswish Interrupt Control Register SZIIC XXXXX000b 0055h UAR12 Transmit Interrupt Control Register SZIIC XXXXX000b 0055h UAR10 Receive Interrupt Control Register SOIIC XXXXX000b 0055h UAR11 Receive Interrupt Control Register SOIIC XXXXX000b 0055h UAR11 Transmit Interrupt Control Register SOIIC XXXXX000b 0055h UAR11 Transmit Interrupt Control Register SOIIC XXXXXX000b 0055h UaR11 Transmit Interrupt Control Register STIIC XXXXXX000b 0055h Timer AD Interrupt Control Register TADIC XXXXXX000b 0055h Timer AD Interrupt Control Register TADIC<	0048h		S4IC, INT5IC	XX00X000b
004Bh DMAO Interrupt Control Register DMIIC XXXXX000b 004Ch DMAI Interrupt Control Register DMIIC XXXXX000b 004Dh Key Input Interrupt Control Register MIC XXXXX000b 004Eh AD Conversion Interrupt Control Register ADIC XXXXX000b 004Fh UART2 Transmit Interrupt Control Register SZPIC XXXXX000b 0056h UART2 Receive Interrupt Control Register SZPIC XXXXX000b 0055h UART2 Receive Interrupt Control Register SORIC XXXXX000b 0055h UART1 Receive Interrupt Control Register SORIC XXXXX000b 0055h UART1 Receive Interrupt Control Register STRIC XXXXX000b 0055h UART1 Receive Interrupt Control Register STRIC XXXXX000b 0055h Timer AD Interrupt Control Register TARIC XXXXX000b 0055h Timer AI Interrupt Control Register TARIC XXXXX000b 0056h Timer AI Interrupt Control Register TARIC XXXXX000b 0057h Timer AI Interrupt Control Register TARIC XXXXX000b <td>0049h</td> <td>SI/O3 Interrupt Control Register, INT4 Interrupt Control Register</td> <td>S3IC, INT4IC</td> <td>XX00X000b</td>	0049h	SI/O3 Interrupt Control Register, INT4 Interrupt Control Register	S3IC, INT4IC	XX00X000b
004Ch DMAI Interrupt Control Register DMIIC XXXXX000b 004Dh Ky Input Interrupt Control Register KUPIC XXXXX000b 004Eh ADI Conversion Interrupt Control Register ADIC XXXXX000b 004Fh JART 2 Transmit Interrupt Control Register S2TIC XXXXX000b 0050h UART 2 Receive Interrupt Control Register S2RIC XXXXX000b 0055h UART 0 Receive Interrupt Control Register S9TIC XXXXX000b 0052h UART 1 Receive Interrupt Control Register S0RIC XXXXX000b 0053h UART 1 Receive Interrupt Control Register S1TIC XXXXX000b 0054h UART 1 Receive Interrupt Control Register S1TIC XXXXX000b 0055h Timer AD Interrupt Control Register TADIC XXXXX000b 0055h Timer AD Interrupt Control Register TADIC XXXXX000b 0055h Timer AD Interrupt Control Register TADIC XXXXX000b 0057h Timer AD Interrupt Control Register TADIC XXXXX000b 0058h Timer AD Interrupt Control Register TADIC X	004Ah	UART2 Bus Collision Detection Interrupt Control Register	BCNIC	XXXXX000b
004BH Key Input Interrupt Control Register KUPIC XXXXX000b 004Fh JO Conversion Interrupt Control Register ADIC XXXXX000b 0056h UAR12 Receive Interrupt Control Register S2FIC XXXXX000b 0055h UAR12 Receive Interrupt Control Register S2RIC XXXXX000b 0055h UAR17 Insamit Interrupt Control Register S0RIC XXXXX000b 0055h UAR17 Insamit Interrupt Control Register S0RIC XXXXX000b 0055h UAR17 Insamit Interrupt Control Register S1RIC XXXXX000b 0055h UAR17 Receive Interrupt Control Register S1RIC XXXXX000b 0055h UAR17 Receive Interrupt Control Register TAIC XXXXX000b 0055h Timer A1 Interrupt Control Register TAIC XXXXX000b 0055h Timer A1 Interrupt Control Register TAIC XXXXX000b 0055h Timer A2 Interrupt Control Register TASIC XXXXX000b 0055h Timer A3 Interrupt Control Register TASIC XXXXX000b 0055h Timer B2 Interrupt Control Register TBIC XXX	004Bh	DMA0 Interrupt Control Register	DM0IC	XXXXX000b
004Eh A7D Conversion Interrupt Control Register ADIC XXXXXX000b 004Ph UART2 Transmit Interrupt Control Register \$2TIC XXXXXX000b 0050h UART2 Receive Interrupt Control Register \$2RIC XXXXXX000b 0051h UART0 Receive Interrupt Control Register \$5RIC XXXXXX000b 0052h UART0 Receive Interrupt Control Register \$5RIC XXXXXX000b 0053h UART1 Receive Interrupt Control Register \$5RIC XXXXXX000b 0054h UART1 Receive Interrupt Control Register \$1RIC XXXXXX000b 0055h UART1 Receive Interrupt Control Register \$1RIC XXXXXX000b 0055h Timer A1 Interrupt Control Register \$1RIC XXXXXX000b 0055h Timer A2 Interrupt Control Register \$1AIC XXXXXX000b 0057h Timer A2 Interrupt Control Register \$1AIC XXXXXX000b 0058h Timer A2 Interrupt Control Register \$1AIC XXXXXX000b 0058h Timer B2 Interrupt Control Register \$1AIC XXXXXX000b 0058h Timer B2 Interrupt Control Register \$1AIC <td>004Ch</td> <td>DMA1 Interrupt Control Register</td> <td>DM1IC</td> <td>XXXXX000b</td>	004Ch	DMA1 Interrupt Control Register	DM1IC	XXXXX000b
004Fh UART2 Transmit Interrupt Control Register \$2TIC XXXXX000b 0050h UART2 Receive Interrupt Control Register \$2RIC XXXXX000b 0051h UART0 Transmit Interrupt Control Register \$3TIC XXXXX000b 0052h UART1 Graceive Interrupt Control Register \$3RIC XXXXX000b 0053h UART1 Transmit Interrupt Control Register \$3TIC XXXXX000b 0054h UART1 Transmit Interrupt Control Register \$1TIC XXXXX000b 0055h Timer AD Interrupt Control Register \$1TIC XXXXX000b 0056h Timer AD Interrupt Control Register \$1TIC XXXXX000b 0057h Timer AD Interrupt Control Register \$1ASIC XXXXX000b 0058h Timer AD Interrupt Control Register \$1BIC XXXXX000b 0058h Timer BD Interrupt Control Register \$1BIC	004Dh	Key Input Interrupt Control Register	KUPIC	XXXXX000b
0055h UAR12 Receive Interrupt Control Register \$2RIC XXXXX000b 0051h UAR10 Transmit Interrupt Control Register \$0RIC XXXXXX00b 0052h UAR10 Receive Interrupt Control Register \$3RIC XXXXXX00b 0053h UAR11 Receive Interrupt Control Register \$1RIC XXXXXX00b 0054h UAR11 Receive Interrupt Control Register \$1RIC XXXXXX00b 0055h Timer An Interrupt Control Register \$1RIC XXXXXX00b 0056h Timer A1 Interrupt Control Register \$1AIC XXXXXX00b 0057h Timer A1 Interrupt Control Register \$1AIC XXXXXX00b 0058h Timer A3 Interrupt Control Register \$1AIC XXXXXX00b 0059h Timer A3 Interrupt Control Register \$1AIC XXXXXX00b 0059h Timer B0 Interrupt Control Register \$1AIC XXXXXX00b 0058h Timer B1 Interrupt Control Register \$1BIC XXXXXX00b 0058h Timer B2 Interrupt Control Register \$1BIC XXXXXX00b 0059h Interrupt Control Register \$1BIC XXXXXX00b <td>004Eh</td> <td>A/D Conversion Interrupt Control Register</td> <td>ADIC</td> <td>XXXXX000b</td>	004Eh	A/D Conversion Interrupt Control Register	ADIC	XXXXX000b
0051h UARTO Transmit Interrupt Control Register SOTIC XXXXX000b 0052h UARTO Receive Interrupt Control Register SORIC XXXXXX00b 0053h UARTO Receive Interrupt Control Register STRIC XXXXXX00b 0054h UARTI Transmit Interrupt Control Register STRIC XXXXXX00b 0055h Timer AD Interrupt Control Register TA0IC XXXXXX00b 0056h Timer AD Interrupt Control Register TA0IC XXXXXX00b 0057h Timer AD Interrupt Control Register TA2IC XXXXXX00b 0058h Timer AD Interrupt Control Register TA2IC XXXXXX00b 0059h Timer AD Interrupt Control Register TA2IC XXXXXX00b 0059h Timer AD Interrupt Control Register TA2IC XXXXXX00b 0058h Timer BD Interrupt Control Register TBDIC XXXXXX00b 0056h Timer BD Interrupt Control Register TBTIC XXXXXX00b 0056h Timer BD Interrupt Control Register NT0IC XXXXXX00b 0056h Timer BD Interrupt Control Register NT0IC XXXXXXXXXXXXXXXXX	004Fh	UART2 Transmit Interrupt Control Register	S2TIC	XXXXX000b
0051h UARTO Transmit Interrupt Control Register SOTIC XXXXX000b 0052h UARTO Receive Interrupt Control Register SORIC XXXXX000b 0053h UARTO Receive Interrupt Control Register STRIC XXXXX000b 0054h UARTI Transmit Interrupt Control Register STRIC XXXXX000b 0055h Timer AD Interrupt Control Register TA0IC XXXXX000b 0056h Timer AI Interrupt Control Register TA0IC XXXXX000b 0056h Timer AI Interrupt Control Register TA2IC XXXXX000b 0057h Timer AI Interrupt Control Register TA2IC XXXXX000b 0058h Timer AI Interrupt Control Register TA3IC XXXXX000b 0059h Timer AI Interrupt Control Register TA4IC XXXXX000b 0059h Timer BI Interrupt Control Register TBIC XXXXX000b 0059h Timer BI Interrupt Control Register TBIC XXXXX000b 005Ch Timer BI Interrupt Control Register TBIC XXXXX000b 005Ch Timer BI Interrupt Control Register INTIC XX0XXX000b	0050h	UART2 Receive Interrupt Control Register	S2RIC	XXXXX000b
0052h UARTO Receive Interrupt Control Register SORIC XXXXXX000b 0053h UART1 ransmit Interrupt Control Register STRIC XXXXXX00b 0054h UART1 Receive Interrupt Control Register TABIC XXXXXX00b 0055h Timer Al Interrupt Control Register TABIC XXXXXX00b 0057h Timer Al Interrupt Control Register TABIC XXXXXX00b 0057h Timer Al Interrupt Control Register TABIC XXXXXX00b 0058h Timer Bo Interrupt Control Register TBIC XXXXXX00b 0056h Timer Bo Interrupt Control Register TBIC XXXXXX00b 0055h Timer Bo Interrupt Control Register TBIC XXXXXX00b 0055h IntTO Interrupt Control Register INTOIC XXXXXX00b 0057h Interrupt Control Register INTOIC XXXXXX00b	0051h		S0TIC	XXXXX000b
0055h UART1 fransmit Interrupt Control Register STRIC XXXXX000b 0055h MART1 Receive Interrupt Control Register STRIC XXXXX000b 0055h Timer AO Interrupt Control Register TA0IC XXXXX000b 0056h Timer AO Interrupt Control Register TA2IC XXXXX000b 0057h Timer AI Interrupt Control Register TA2IC XXXXXX000b 0058h Timer AI Interrupt Control Register TA3IC XXXXXX000b 0059h Timer AI Interrupt Control Register TA3IC XXXXXX000b 0059h Timer AI Interrupt Control Register TB8IC XXXXXX000b 0058h Timer BI Interrupt Control Register TB8IC XXXXXX000b 005Ch Timer BI Interrupt Control Register TB2IC XXXXXX000b 005Ch Timer BI Interrupt Control Register INT1IC XX00X000b 005Fh INT2 Interrupt Control Register INT1IC XX00X000b 005Fh Int2 Interrupt Control Register INT2IC XX00X000b 006Bh Interrupt Control Register Int2IC XX00X00b	0052h			
0054h UART1 Receive Interrupt Control Register STRIC XXXXX000b 0055h Timer AD Interrupt Control Register TADIC XXXXX000b 0056h Timer AI Interrupt Control Register TATIC XXXXX000b 0057h Timer AI Interrupt Control Register TAZIC XXXXX000b 0058h Timer AI Interrupt Control Register TAXIC XXXXX000b 0059h Timer AI Interrupt Control Register TAXIC XXXXX000b 0059h Timer AI Interrupt Control Register TAXIC XXXXX000b 0059h Timer BI Interrupt Control Register TBIC XXXXX000b 0055h Timer BI Interrupt Control Register TBIC XXXXX000b 0055h Interrupt Control Register INTOIC XXXXX000b 0055h Interrupt Control Register INTOIC XXXXX000b 0056h Interrupt Control Register INTOIC XXXXX000b 0057h Interrupt Control Register INTOIC XXXXX000b 0068h Interrupt Control Register Interrupt Control Register Interrupt Control Register	0053h			
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0058h Timer A3 Interrupt Control Register TA3IC XXXXX000b 0059h Timer A4 Interrupt Control Register TA4IC XXXXX000b 005Ah Timer B0 Interrupt Control Register TB0IC XXXXX000b 005Bh Timer B1 Interrupt Control Register TB1IC XXXXX000b 005Ch Timer B1 Interrupt Control Register TB2IC XXXXX000b 005Dh INT0 Interrupt Control Register INT0IC XXXXX000b 005Bh INT1 Interrupt Control Register INT0IC XX00X000b 005Fh INT2 Interrupt Control Register INT2IC XX00X000b 006Fh INT2IC XX00X000b 006Bh INT2IC XX00X000b 006Ch INT2IC XX00X000b 006Bh INT2IC XX0XX000b 006Bh INT2IC XX0XXX00b 006Bh INT2IC	0057h			
	0058h			
005Ah Timer B0 Interrupt Control Register TB0IC XXXXX000b 005Bh Timer B1 Interrupt Control Register TB1IC XXXXX000b 005Ch Timer B2 Interrupt Control Register TB2IC XXXXX000b 005Dh INT0 Interrupt Control Register INT0IC XX00X000b 005Eh INT1 Interrupt Control Register INT1IC XX00X000b 006Dh INT2 Interrupt Control Register INT2IC XX00X000b 006Dh INT2 Interrupt Control Register INT2IC XX00X000b 006Dh INT2 Interrupt Control Register INT2IC XX00X000b 006Dh INT2IC INT2IC XX00X000b 006Bh INT2IC				
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0078h			1	+
0079h 007Ah 007Bh 007Ch 007Dh 007Eh			1	+
007Ah 007Bh 007Ch 007Dh 007Eh			1	+
007Bh			1	+
007Ch			1	1
007Dh				1
007Eh				1
				1
	007En 007Fh			ļ

NOTES:

1. The blank areas are reserved and cannot be accessed by users.

X : Nothing is mapped to this bit

5. Electrical Characteristics

5.1 Electrical Characteristics (M16C/62P)

Table 5.1 Absolute Maximum Ratings

Symbol		Parameter	Condition	Rated Value	Unit
VCC1, VCC2	Supply Voltage		Vcc1=AVcc	-0.3 to 6.5	V
Vcc2	Supply Voltage		Vcc2	-0.3 to Vcc1+0.1	V
AVcc	Analog Supply V	/oltage	Vcc1=AVcc	-0.3 to 6.5	V
Vı	Input Voltage	RESET, CNVSS, BYTE, P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P14_0, P14_1, VREF, XIN		-0.3 to Vcc1+0.3 ⁽¹⁾	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P12_0 to P12_7, P13_0 to P13_7		-0.3 to Vcc2+0.3 ⁽¹⁾	V
	P7_0, P7_1			-0.3 to 6.5	V
Vo	Output Voltage	P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P14_0, P14_1, XOUT		-0.3 to Vcc1+0.3 ⁽¹⁾	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P12_0 to P12_7, P13_0 to P13_7		-0.3 to Vcc2+0.3 ⁽¹⁾	V
		P7_0, P7_1		-0.3 to 6.5	V
Pd	Power Dissipation	on	–40°C <topr≤85°c< td=""><td>300</td><td>mW</td></topr≤85°c<>	300	mW
Topr	Operating Ambient	When the Microcomputer is Operating		-20 to 85 / -40 to 85	°C
	Temperature	Flash Program Erase		0 to 60	
Tstg	Storage Temper	rature		-65 to 150	°C

NOTES:

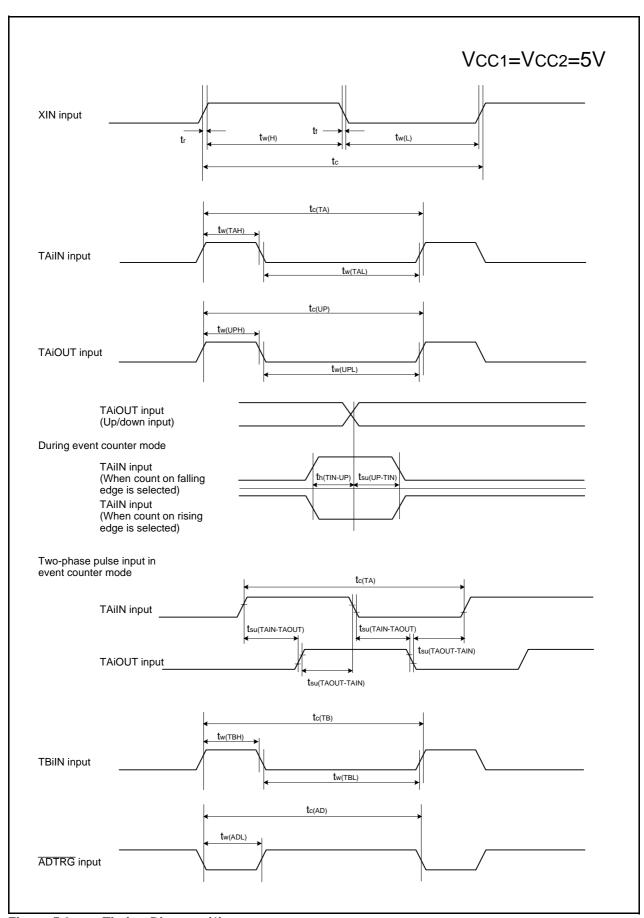
1. There is no external connections for port P1_0 to P1_7, P4_4 to P4_7, P7_2 to P7_5 and P9_1 in 80-pin version.

Table 5.4 A/D Conversion Characteristics (1)

Symbol	Parame	tor		Measuring Condition	Standard			Unit
Symbol	i didiliotoi					Тур.	Max.	
-	Resolution		VREF=VCC1				10	Bits
INL	Integral Non-Linearity Error	10bit	VREF= VCC1= 5V	AN0 to AN7 input, AN0_0 to AN0_7 input, AN2_0 to AN2_7 input, ANEX0, ANEX1 input			±3	LSB
				External operation amp connection mode			±7	LSB
			VREF= VCC1= 3.3V	AN0 to AN7 input, AN0_0 to AN0_7 input, AN2_0 to AN2_7 input, ANEX0, ANEX1 input			±5	LSB
				External operation amp connection mode			±7	LSB
		8bit	VREF=VCC1=5V, 3.3V				±2	LSB
_	Absolute Accuracy	10bit	VREF= VCC1= 5V	AN0 to AN7 input, AN0_0 to AN0_7 input, AN2_0 to AN2_7 input, ANEX0, ANEX1 input			±3	LSB
				External operation amp connection mode			±7	LSB
		VREF= VCC1 =3.3V	AN0 to AN7 input, AN0_0 to AN0_7 input, AN2_0 to AN2_7 input, ANEX0, ANEX1 input			±5	LSB	
				External operation amp connection mode			±7	LSB
		8bit	VREF=VCC1=5V, 3.3V				±2	LSB
-	Tolerance Level Impeda	ance				3		kΩ
DNL	Differential Non-Linearit	y Error					±1	LSB
-	Offset Error						±3	LSB
_	Gain Error						±3	LSB
RLADDER	Ladder Resistance		VREF=V	/cc1	10		40	kΩ
tconv	10-bit Conversion Time, Sample & Hold Available		VREF=V	/cc1=5V, φAD=12MHz	2.75			μS
tconv	8-bit Conversion Time, S Available	Sample & Hold	VREF=VCC1=5V,		2.33			μS
tsamp	Sampling Time				0.25			μS
VREF	Reference Voltage				2.0		Vcc1	V
VIA	Analog Input Voltage				0		VREF	V

NOTES:

- 1. Referenced to Vcc1=AVcc=VREF=3.3 to 5.5V, Vss=AVss=0V at Topr = -20 to 85°C / -40 to 85°C unless otherwise specified.
- 2. If Vcc1 > Vcc2, do not use AN0_0 to AN0_7 and AN2_0 to AN2_7 as analog input pins.
- 3. φAD frequency must be 12 MHz or less. And divide the fAD if Vcc1 is less than 4.0V, and φAD frequency into 10 MHz or less.
- When sample & hold is disabled, φAD frequency must be 250 kHz or more, in addition to the limitation in Note 3.
 When sample & hold is enabled, φAD frequency must be 1MHz or more, in addition to the limitation in Note 3.



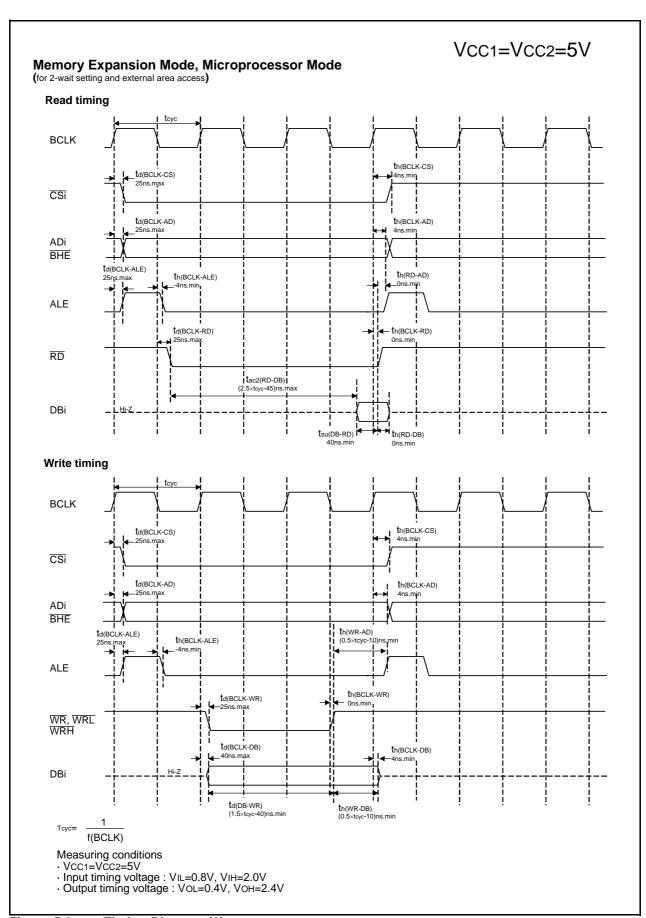


Figure 5.8 Timing Diagram (6)

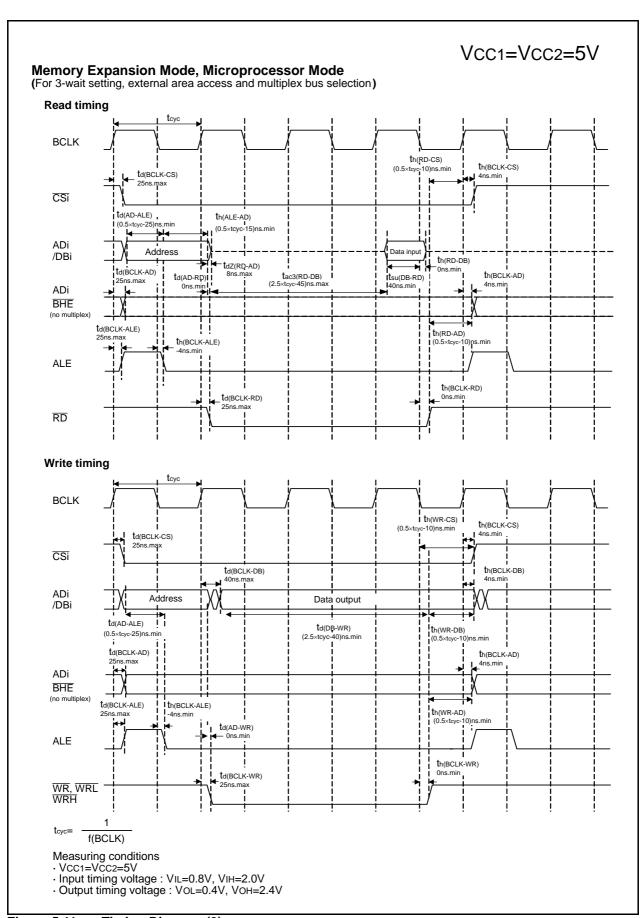


Figure 5.11 Timing Diagram (9)

VCC1=VCC2=3V

Switching Characteristics

(VCC1 = VCC2 = 3V, VSS = 0V, at Topr = -20 to 85°C / -40 to 85°C unless otherwise specified)

Table 5.46 Memory Expansion and Microprocessor Modes (for setting with no wait)

Symbol	Parameter		Stan	dard	Unit
Symbol	Falameter		Min.	Max.	Offic
td(BCLK-AD)	Address Output Delay Time			30	ns
th(BCLK-AD)	Address Output Hold Time (in relation to BCLK)		4		ns
th(RD-AD)	Address Output Hold Time (in relation to RD)		0		ns
th(WR-AD)	Address Output Hold Time (in relation to WR)		(NOTE 2)		ns
td(BCLK-CS)	Chip Select Output Delay Time			30	ns
th(BCLK-CS)	Chip Select Output Hold Time (in relation to BCLK)		4		ns
td(BCLK-ALE)	ALE Signal Output Delay Time			25	ns
th(BCLK-ALE)	ALE Signal Output Hold Time	1	-4		ns
td(BCLK-RD)	RD Signal Output Delay Time	See Figure 5.12		30	ns
th(BCLK-RD)	RD Signal Output Hold Time	Tigule 3.12	0		ns
td(BCLK-WR)	WR Signal Output Delay Time			30	ns
th(BCLK-WR)	WR Signal Output Hold Time		0		ns
td(BCLK-DB)	Data Output Delay Time (in relation to BCLK)			40	ns
th(BCLK-DB)	Data Output Hold Time (in relation to BCLK) (3)		4		ns
td(DB-WR)	Data Output Delay Time (in relation to WR)		(NOTE 1)		ns
th(WR-DB)	Data Output Hold Time (in relation to WR) (3)	7	(NOTE 2)		ns
td(BCLK-HLDA)	HLDA Output Delay Time	7		40	ns

NOTES:

1. Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \text{x} 10^9}{\text{f(BCLK)}} - 40 [\text{ns}] \hspace{1cm} \text{f(BCLK) is 12.5MHz or less.}$$

2. Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f(BCLK)} - 10[ns]$$

3. This standard value shows the timing when the output is off, and does not show hold time of data bus.

Hold time of data bus varies with capacitor volume and pull-up (pull-down) resistance value.

Hold time of data bus is expressed in

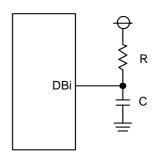
$$t = -CR X In (1-VoL / Vcc2)$$

by a circuit of the right figure.

For example, when VoL = 0.2Vcc2, C = 30pF, R = 1k Ω , hold time of output "L" level is

$$t = -30pF X 1k \Omega X In(1-0.2Vcc2 / Vcc2)$$

= 6.7 ns.



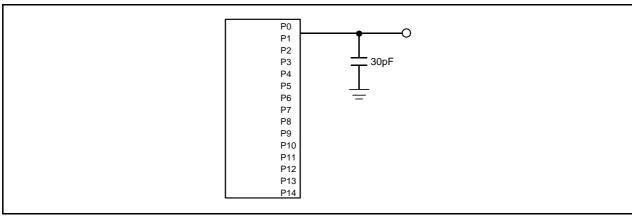


Figure 5.12 Ports P0 to P14 Measurement Circuit

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VCC1=VCC2=3V

Switching Characteristics

(VCC1 = VCC2 = 5V, VSS = 0V, at Topr = -20 to 85°C / -40 to 85°C unless otherwise specified)

Table 5.48 Memory Expansion and Microprocessor Modes (for 2- to 3-wait setting, external area access and multiplex bus selection)

Courselp ad	Davanatas		Stan	dard	Unit
Symbol	Parameter		Min.	Max.	Unit
td(BCLK-AD)	Address Output Delay Time			50	ns
th(BCLK-AD)	Address Output Hold Time (in relation to BCLK)		4		ns
th(RD-AD)	Address Output Hold Time (in relation to RD)		(NOTE 1)		ns
th(WR-AD)	Address Output Hold Time (in relation to WR)		(NOTE 1)		ns
td(BCLK-CS)	Chip Select Output Delay Time			50	ns
th(BCLK-CS)	Chip Select Output Hold Time (in relation to BCLK)		4		ns
th(RD-CS)	Chip Select Output Hold Time (in relation to RD)		(NOTE 1)		ns
th(WR-CS)	Chip Select Output Hold Time (in relation to WR)		(NOTE 1)		ns
td(BCLK-RD)	RD Signal Output Delay Time			40	ns
th(BCLK-RD)	RD Signal Output Hold Time		0		ns
td(BCLK-WR)	WR Signal Output Delay Time			40	ns
th(BCLK-WR)	WR Signal Output Hold Time	See	0		ns
td(BCLK-DB)	Data Output Delay Time (in relation to BCLK)	Figure 5.12		50	ns
th(BCLK-DB)	Data Output Hold Time (in relation to BCLK)		4		ns
td(DB-WR)	Data Output Delay Time (in relation to WR)		(NOTE 2)		ns
th(WR-DB)	Data Output Hold Time (in relation to WR)		(NOTE 1)		ns
td(BCLK-HLDA)	HLDA Output Delay Time			40	ns
td(BCLK-ALE)	ALE Signal Output Delay Time (in relation to BCLK)			25	ns
th(BCLK-ALE)	ALE Signal Output Hold Time (in relation to BCLK)		-4		ns
td(AD-ALE)	ALE Signal Output Delay Time (in relation to Address)		(NOTE 3)		ns
th(AD-ALE)	ALE Signal Output Hold Time (in relation to Address)		(NOTE 4)		ns
td(AD-RD)	RD Signal Output Delay From the End of Address		0		ns
td(AD-WR)	WR Signal Output Delay From the End of Address		0		ns
tdz(RD-AD)	Address Output Floating Start Time			8	ns

NOTES:

1. Calculated according to the BCLK frequency as follows:

$$\frac{0.5x10^9}{f(BCLK)} - 10[ns]$$

2. Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \text{x} 10^9}{\text{f(BCLK)}} - 50 [\text{ns}] \qquad \qquad \text{n is "2" for 2-wait setting, "3" for 3-wait setting.}$$

3. Calculated according to the BCLK frequency as follows:

$$\frac{0.5x10^9}{f(BCLK)}-40[\text{ns}]$$

4. Calculated according to the BCLK frequency as follows:

$$\frac{0.5x10^9}{f(BCLK)} - 15[ns]$$

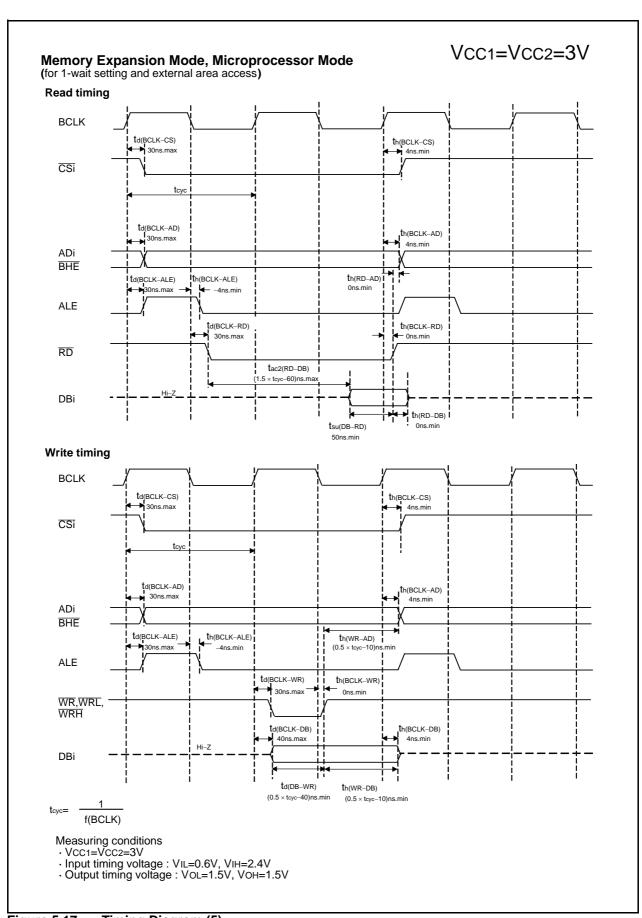


Figure 5.17 Timing Diagram (5)

	•			, ,	, ,	,	
Symbol	Parameter			Standard			
Symbol	Faiametei	Min.	Тур.	Max.	Unit		
_	Program and Erase Endurance (3)	100			cycle		
_	Word Program Time (Vcc1=5.0V)		25	200	μS		
_	Lock Bit Program Time		25	200	μS		
_	Block Erase Time	4-Kbyte block	4	0.3	4	S	
_	(Vcc1=5.0V)	8-Kbyte block		0.3	4	S	
_		32-Kbyte block		0.5	4	S	
_		64-Kbyte block		0.8	4	S	
_	Erase All Unlocked Blocks Time (2)				4×n	S	
tps	Flash Memory Circuit Stabilization Wait T	ime			15	μS	
_	Data Hold Time (5)		20			year	

Table 5.53 Flash Memory Version Electrical Characteristics (1) for 100 cycle products (B, U)

Table 5.54 Flash Memory Version Electrical Characteristics (6) for 10,000 cycle products (B7, U7) (Block A and Block 1 (7))

Symbol	Parameter		Standard			
Symbol	Falanielei	Min.	Тур.	Max.	Unit	
=	Program and Erase Endurance (3, 8, 9)	10,000 (4)			cycle	
=	Word Program Time (Vcc1=5.0V)		25		μS	
=	Lock Bit Program Time		25		μS	
	Block Erase Time (Vcc1=5.0V)	4-Kbyte block	4	0.3		s
tps	Flash Memory Circuit Stabilization Wait Time				15	μS
-	Data Hold Time (5)		20			year

NOTES:

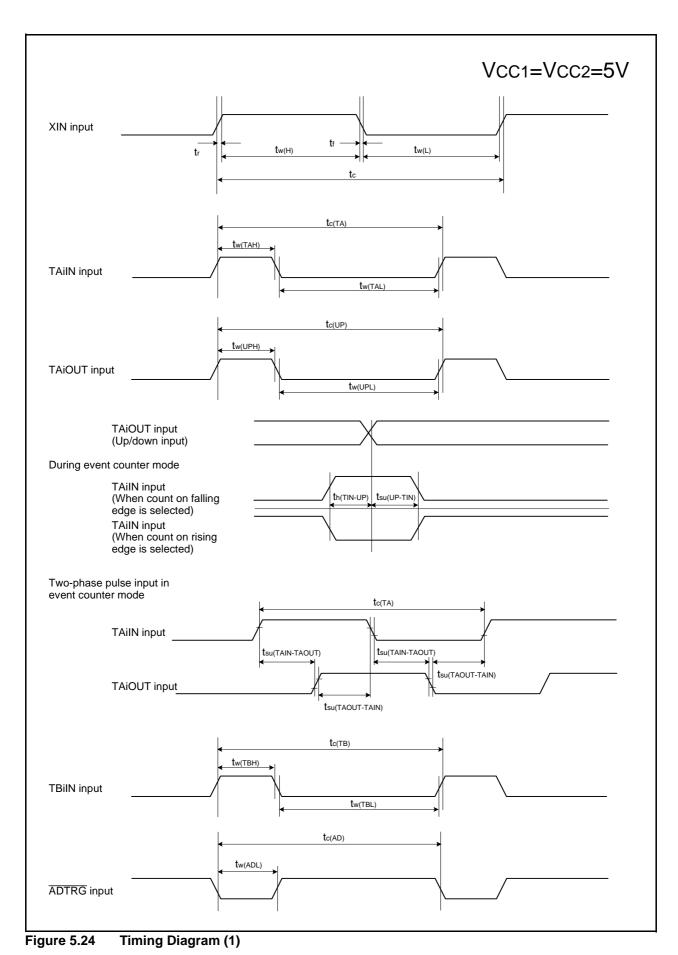
- 1. Referenced to Vcc1=4.5 to 5.5V at Topr = 0 to 60 °C unless otherwise specified.
- 2. n denotes the number of block erases.
- In denotes the number of block erases.
 Program and Erase Endurance refers to the number of times a block erase can be performed.
 If the program and erase endurance is n (n=100, 1,000, or 10,000), each block can be erased n times.
 For example, if a 4 Kbytes block A is erased after writing 1 word data 2,048 times, each to a different address, this counts as one program and erase endurance. Data cannot be written to the same address more than once without erasing the block. (Rewrite prohibited)
- 4. Maximum number of E/W cycles for which operation is guaranteed.

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- 5. Ta (ambient temperature)=55 °C. As to the data hold time except Ta=55 °C, please contact Renesas Technology Corp. or an authorized Renesas Technology Corp. product distributor.
- 6. Referenced to Vcc1 = 4.5 to 5.5V at Topr = -40 to 85 °C (B7, U7 (T version)) / -40 to 125 °C (B7, U7 (V version)) unless otherwise specified.
- 7. Table 5.54 applies for block A or block 1 program and erase endurance > 1,000. Otherwise, use Table 5.53.
- 8. To reduce the number of program and erase endurance when working with systems requiring numerous rewrites, write to unused word addresses within the block instead of rewrite. Erase block only after all possible addresses are used. For example, an 8-word program can be written 256 times maximum before erase becomes necessary.
 Maintaining an equal number of erasure between block A and block 1 will also improve efficiency. It is important to track the total number of times erasure is used.
- 9. Should erase error occur during block erase, attempt to execute clear status register command, then block erase command at least three times until erase error disappears.
- 10. Set the PM17 bit in the PM1 register to "1" (wait state) when executing more than 100 times rewrites (B7 and U7).
- 11. Customers desiring E/W failure rate information should contact their Renesas technical support representative.

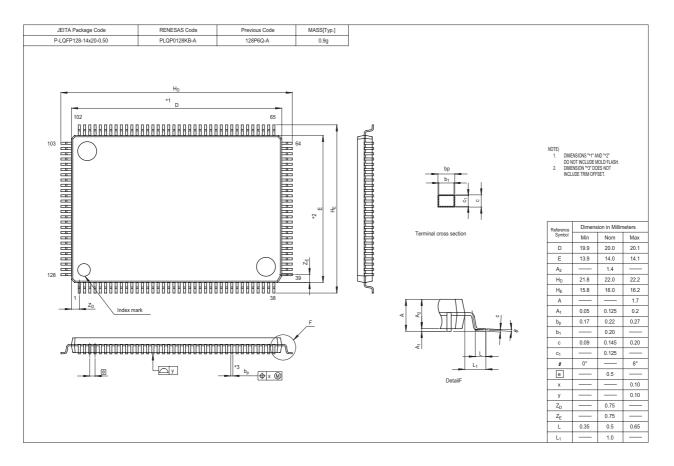
Table 5.55 Flash Memory Version Program/Erase Voltage and Read Operation Voltage Characteristics (at Topr = 0 to 60 $^{\circ}$ C(B, U), Topr = -40 to 85 $^{\circ}$ C (B7, U7 (T version)) / -40 to 125 $^{\circ}$ C (B7, U7 (V version))

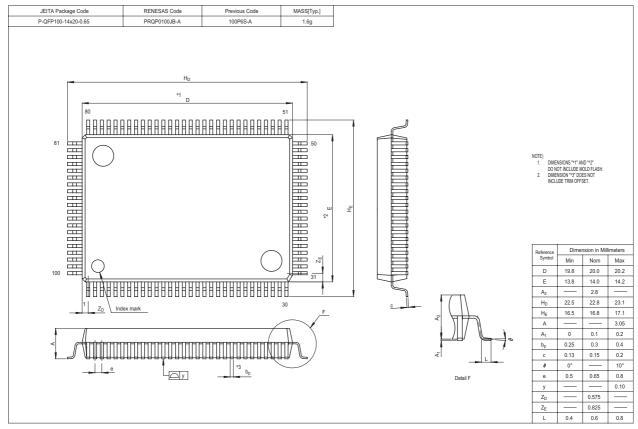
Flash Program, Erase Voltage	Flash Read Operation Voltage
$VCC1 = 5.0 V \pm 0.5 V$	Vcc1=4.0 to 5.5 V



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Appendix 1.Package Dimensions





REVISION HISTORY			RY	M16C/62P Group (M16C/62P, M16C/62PT) Hardware Manual		
Dov	Date			Description		
Rev.		Page		Summary		
		40	Table 5.2	4 is partly revised.		
		57	Table 5.4	3 is partly revised.		
		70		8 is partly revised.		
		72		0 is partly revised.		
		73		3 is partly revised.		
		74 70	Table 5.55 is revised. Table 5.57 is partly revised. Table 5.69 is partly revised.			
		76 79				
2.41	Jan 01, 2006	-		own detection reset -> brown-out detection Reset		
2.41	Jan 01, 2000	2.4				
		2-4	Tables 1.1 to 1.3 Performance outline of M16C/62P group are partly revised. Table 1.4 Product List (1) is partly revised. Note 1 is added. Table 1.5 Product List (2) is partly revised. Note 1, 2 and 3 are added.			
		7				
		8				
		9		Product List (3) is partly revised. ad 2 are added.		
		10		Product List (4) is partly revised. d 2 are added.		
		11	Figure 1.3	B Type No., Memory Size, Shows RAM capacity, and Package is ised		
		12	Table 1.8	Product Code of Flash Memory version and ROMless version for P is partly revised.		
		13		Product Code of Flash Memory version for M16C/62P is partly		
		14	Figure 1.6	6 Pin Configuration (Top View) is partly revised.		
		15-17	Tables 1.	10 to 1.12 Pin Characteristics for 128-Pin Package are added.		
		18-19	Figure 1.7	7 and 1.8 Pin Configuration (Top View) are partly revised.		
		20-21	_	13 to 1.14 Pin Characteristics for 100-Pin Package are added.		
		22		9 Pin Configuration (Top View) is partly revised.		
		23-24		15 to 1.16 Pin Characteristics for 80-Pin Package are added.		
		25-29		17 to 1.21 are partly revised.		
		34		Table 4.1 SFR Information is partly revised.		
		43		A/D Conversion Characteristics is partly revised.		
		45	Table 5.6	Flash Memory Version Electrical Characteristics for 100 cycle is partly revised.		
			Table 5.7	Flash Memory Version Electrical Characteristics for 10,000 cycle is partly revised.		
			Table 5.8	Flash Memory Version Program / Erase Voltage and Read Noltage Characteristics is partly revised.		
		46		Low Voltage Detection Circuit Electrical Characteristics is partly		

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