# Renesas Electronics America Inc - M30625FGPGP#U3C Datasheet

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | M16C/60 |
| Core Size | 16-Bit |
| Speed | 24MHz |
| Connectivity | I²C, IEBus, UART/USART |
| Peripherals | DMA, WDT |
| Number of I/O | 113 |
| Program Memory Size | 256KB (256K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 20K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.7V ~ 5.5V |
| Data Converters | A/D 26x10b; D/A 2x8b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 128-LQFP |
| Supplier Device Package | 128-LFQFP (14x20) |
| Purchase URL | https://www.e-xfl.com/product-detail/renesas-electronics-america/m30625fgpgp-u3c |

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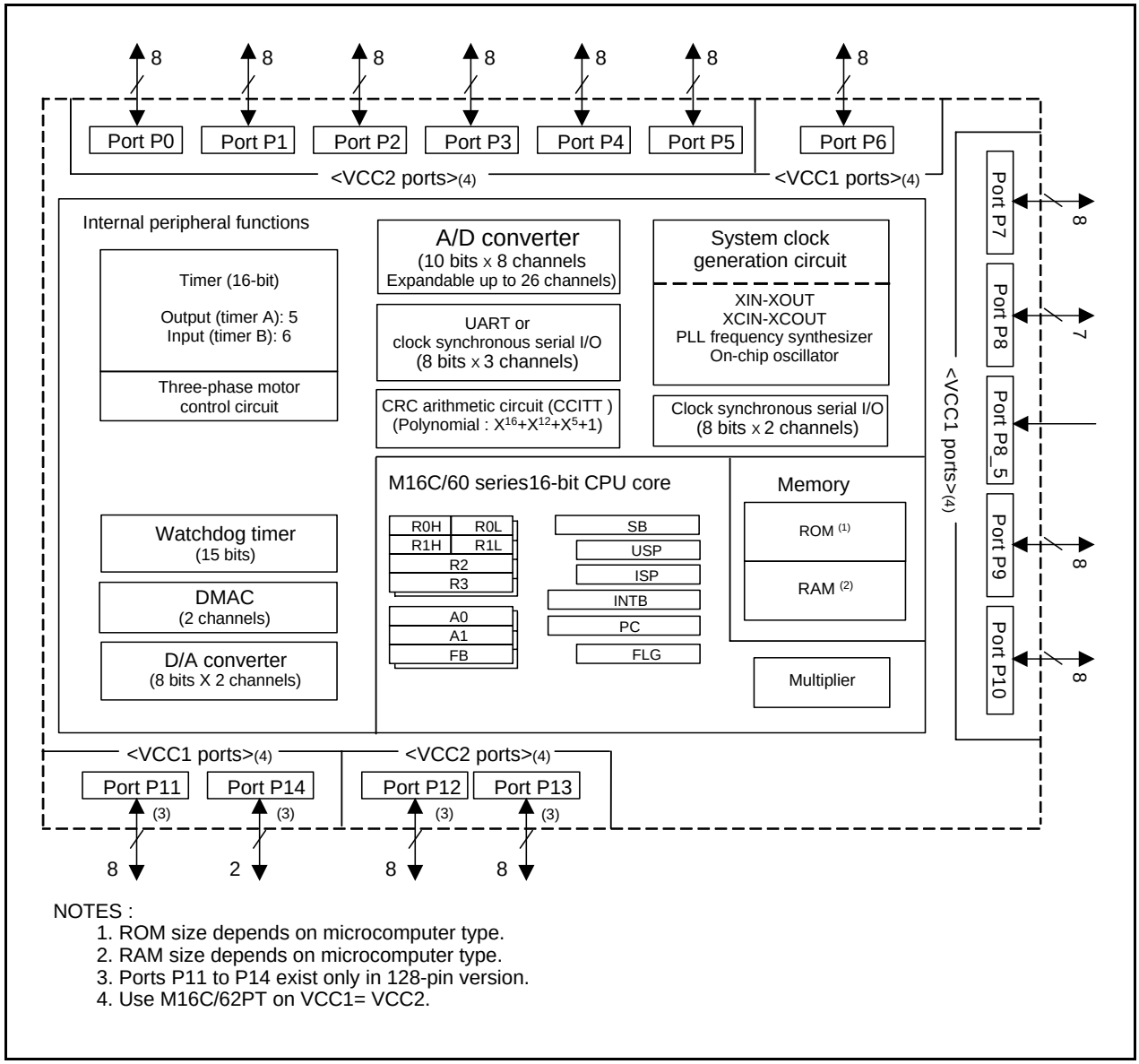
## 1.3 Block Diagram

Figure 1.1 is a M16C/62P Group (M16C/62P, M16C/62PT) 128-pin and 100-pin version Block Diagram, Figure 1.2 is a M16C/62P Group (M16C/62P, M16C/62PT) 80-pin version Block Diagram.




NOTES :
1. ROM size depends on microcomputer type.
2. RAM size depends on microcomputer type.
3. Ports P11 to P14 exist only in 128-pin version.
4. Use M16C/62PT on VCC1= VCC2.

**Figure 1.1 M16C/62P Group (M16C/62P, M16C/62PT) 128-pin and 100-pin version Block Diagram**

## 1.5 Pin Configuration

Figures 1.6 to 1.9 show the Pin Configuration (Top View).

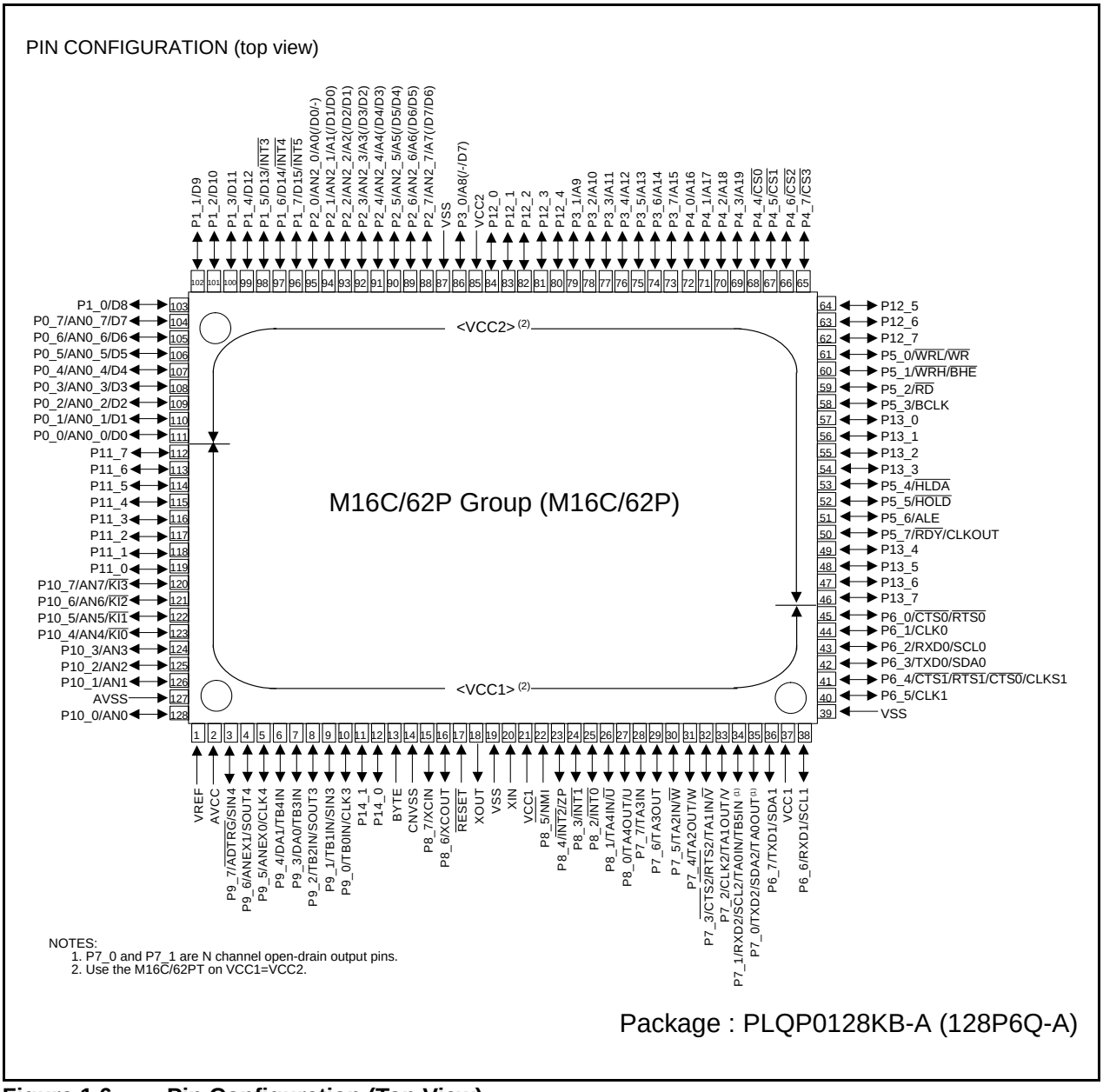



**Figure 1.6 Pin Configuration (Top View)**

**Table 1.16 Pin Characteristics for 80-Pin Package (2)**

| Pin No. | Control Pin | Port | Interrupt Pin | Timer Pin | UART Pin | Analog Pin | Bus Control Pin |
|---|---|---|---|---|---|---|---|
| 51 | | P3_0 | | | | | |
| 52 | | P2_7 | | | | AN2_7 | |
| 53 | | P2_6 | | | | AN2_6 | |
| 54 | | P2_5 | | | | AN2_5 | |
| 55 | | P2_4 | | | | AN2_4 | |
| 56 | | P2_3 | | | | AN2_3 | |
| 57 | | P2_2 | | | | AN2_2 | |
| 58 | | P2_1 | | | | AN2_1 | |
| 59 | | P2_0 | | | | AN2_0 | |
| 60 | | P0_7 | | | | AN0_7 | |
| 61 | | P0_6 | | | | AN0_6 | |
| 62 | | P0_5 | | | | AN0_5 | |
| 63 | | P0_4 | | | | AN0_4 | |
| 64 | | P0_3 | | | | AN0_3 | |
| 65 | | P0_2 | | | | AN0_2 | |
| 66 | | P0_1 | | | | AN0_1 | |
| 67 | | P0_0 | | | | AN0_0 | |
| 68 | | P10_7 | $\overline{KI3}$ | | | AN7 | |
| 69 | | P10_6 | $\overline{KI2}$ | | | AN6 | |
| 70 | | P10_5 | $\overline{KI1}$ | | | AN5 | |
| 71 | | P10_4 | $\overline{KI0}$ | | | AN4 | |
| 72 | | P10_3 | | | | AN3 | |
| 73 | | P10_2 | | | | AN2 | |
| 74 | | P10_1 | | | | AN1 | |
| 75 | AVSS | | | | | | |
| 76 | | P10_0 | | | | AN0 | |
| 77 | VREF | | | | | | |
| 78 | AVCC | | | | | | |
| 79 | | P9_7 | | | SIN4 | $\overline{ADTRG}$ | |
| 80 | | P9_6 | | | SOUT4 | ANEX1 | |

**Table 1.20 Pin Description (80-pin Version) (1)** (1)

| Signal Name | Pin Name | I/O Type | Power Supply | Description |
|---|---|---|---|---|
| Power supply input | VCC1, VSS | I | – | Apply 2.7 to 5.5 V to the VCC1 pin and 0 V to the VSS pin. (1, 2) |
| Analog power supply input | AVCC<br>AVSS | I | VCC1 | Applies the power supply for the A/D converter. Connect the AVCC pin to VCC1. Connect the AVSS pin to VSS. |
| Reset input | $\overline{\text{RESET}}$ | I | VCC1 | The microcomputer is in a reset state when applying "L" to the this pin. |
| CNVSS | CNVSS<br>(BYTE) | I | VCC1 | Switches processor mode. Connect this pin to VSS to when after a reset to start up in single-chip mode. Connect this pin to VCC1 to start up in microprocessor mode. As for the BYTE pin of the 80-pin versions, pull-up processing is performed within the microcomputer. |
| Main clock input | XIN | I | VCC1 | I/O pins for the main clock generation circuit. Connect a ceramic resonator or crystal oscillator between XIN and XOUT (3). To use the external clock, input the clock from XIN and leave XOUT open. |
| Main clock output | XOUT | O | VCC1 | |
| Sub clock input | XCIN | I | VCC1 | I/O pins for a sub clock oscillation circuit. Connect a crystal oscillator between XCIN and XCOUT (3). To use the external clock, input the clock from XCIN and leave XCOUT open. |
| Sub clock output | XCOUT | O | VCC1 | |
| Clock output | CLKOUT | O | VCC2 | The clock of the same cycle as fC, f8, or f32 is outputted. |
| $\overline{\text{INT}}$ interrupt input | $\overline{\text{INT0}}$ to $\overline{\text{INT2}}$ | I | VCC1 | Input pins for the $\overline{\text{INT}}$ interrupt. |
| $\overline{\text{NMI}}$ interrupt input | $\overline{\text{NMI}}$ | I | VCC1 | Input pin for the $\overline{\text{NMI}}$ interrupt. |
| Key input interrupt input | $\overline{\text{KI0}}$ to $\overline{\text{KI3}}$ | I | VCC1 | Input pins for the key input interrupt. |
| Timer A | TA0OUT,<br>TA3OUT,<br>TA4OUT | I/O | VCC1 | These are Timer A0,Timer A3 and Timer A4 I/O pins. (however, output of TA0OUT for the N-channel open drain output.) |
| | TA0IN, TA3IN,<br>TA4IN | I | VCC1 | These are Timer A0, Timer A3 and Timer A4 input pins. |
| | ZP | I | VCC1 | Input pin for the Z-phase. |
| Timer B | TB0IN, TB2IN<br>to TB5IN | I | VCC1 | These are Timer B0, Timer B2 to Timer B5 input pins. |
| Serial interface | $\overline{\text{CTS0}}$ to $\overline{\text{CTS1}}$ | I | VCC1 | These are send control input pins. |
| | $\overline{\text{RTS0}}$ to $\overline{\text{RTS1}}$ | O | VCC1 | These are receive control output pins. |
| | CLK0, CLK1,<br>CLK3, CLK4 | I/O | VCC1 | These are transfer clock I/O pins. |
| | RXD0 to RXD2 | I | VCC1 | These are serial data input pins. |
| | SIN4 | I | VCC1 | This is serial data input pin. |
| | TXD0 to TXD2 | O | VCC1 | These are serial data output pins. (however, output of TXD2 for the N-channel open drain output.) |
| | SOUT3,<br>SOUT4 | O | VCC1 | These are serial data output pins. |
| | CLKS1 | O | VCC1 | This is output pin for transfer clock output from multiple pins function. |
| $I^2C$ mode | SDA0 to SDA2 | I/O | VCC1 | These are serial data I/O pins. (however, output of SDA2 for the N-channel open drain output.) |
| | SCL0 to SCL2 | I/O | VCC1 | These are transfer clock I/O pins. (however, output of SCL2 for the N-channel open drain output.) |

I : Input O : Output I/O : Input and output

NOTES:
1. In this manual, hereafter, VCC refers to VCC1 unless otherwise noted.
2. In M16C/62PT, apply 4.0 to 5.5 V to the VCC1 pin.
3. Ask the oscillator maker the oscillation characteristic.

**Table 4.2 SFR Information (2)** (1)

| Address | Register | Symbol | After Reset |
|---|---|---|---|
| 0040h | | | |
| 0041h | | | |
| 0042h | | | |
| 0043h | | | |
| 0044h | INT3 Interrupt Control Register | INT3IC | XX00X000b |
| 0045h | Timer B5 Interrupt Control Register | TB5IC | XXXXX000b |
| 0046h | Timer B4 Interrupt Control Register, UART1 BUS Collision Detection Interrupt Control Register | TB4IC, U1BCNIC | XXXXX000b |
| 0047h | Timer B3 Interrupt Control Register, UART0 BUS Collision Detection Interrupt Control Register | TB3IC, U0BCNIC | XXXXX000b |
| 0048h | SI/O4 Interrupt Control Register, INT5 Interrupt Control Register | S4IC, INT5IC | XX00X000b |
| 0049h | SI/O3 Interrupt Control Register, INT4 Interrupt Control Register | S3IC, INT4IC | XX00X000b |
| 004Ah | UART2 Bus Collision Detection Interrupt Control Register | BCNIC | XXXXX000b |
| 004Bh | DMA0 Interrupt Control Register | DM0IC | XXXXX000b |
| 004Ch | DMA1 Interrupt Control Register | DM1IC | XXXXX000b |
| 004Dh | Key Input Interrupt Control Register | KUPIC | XXXXX000b |
| 004Eh | A/D Conversion Interrupt Control Register | ADIC | XXXXX000b |
| 004Fh | UART2 Transmit Interrupt Control Register | S2TIC | XXXXX000b |
| 0050h | UART2 Receive Interrupt Control Register | S2RIC | XXXXX000b |
| 0051h | UART0 Transmit Interrupt Control Register | S0TIC | XXXXX000b |
| 0052h | UART0 Receive Interrupt Control Register | S0RIC | XXXXX000b |
| 0053h | UART1 Transmit Interrupt Control Register | S1TIC | XXXXX000b |
| 0054h | UART1 Receive Interrupt Control Register | S1RIC | XXXXX000b |
| 0055h | Timer A0 Interrupt Control Register | TA0IC | XXXXX000b |
| 0056h | Timer A1 Interrupt Control Register | TA1IC | XXXXX000b |
| 0057h | Timer A2 Interrupt Control Register | TA2IC | XXXXX000b |
| 0058h | Timer A3 Interrupt Control Register | TA3IC | XXXXX000b |
| 0059h | Timer A4 Interrupt Control Register | TA4IC | XXXXX000b |
| 005Ah | Timer B0 Interrupt Control Register | TB0IC | XXXXX000b |
| 005Bh | Timer B1 Interrupt Control Register | TB1IC | XXXXX000b |
| 005Ch | Timer B2 Interrupt Control Register | TB2IC | XXXXX000b |
| 005Dh | INT0 Interrupt Control Register | INT0IC | XX00X000b |
| 005Eh | INT1 Interrupt Control Register | INT1IC | XX00X000b |
| 005Fh | INT2 Interrupt Control Register | INT2IC | XX00X000b |
| 0060h | | | |
| 0061h | | | |
| 0062h | | | |
| 0063h | | | |
| 0064h | | | |
| 0065h | | | |
| 0066h | | | |
| 0067h | | | |
| 0068h | | | |
| 0069h | | | |
| 006Ah | | | |
| 006Bh | | | |
| 006Ch | | | |
| 006Dh | | | |
| 006Eh | | | |
| 006Fh | | | |
| 0070h | | | |
| 0071h | | | |
| 0072h | | | |
| 0073h | | | |
| 0074h | | | |
| 0075h | | | |
| 0076h | | | |
| 0077h | | | |
| 0078h | | | |
| 0079h | | | |
| 007Ah | | | |
| 007Bh | | | |
| 007Ch | | | |
| 007Dh | | | |
| 007Eh | | | |
| 007Fh | | | |

NOTES:
1. The blank areas are reserved and cannot be accessed by users.

X : Nothing is mapped to this bit

**Table 5.2 Recommended Operating Conditions (1)** (1)

| Symbol | Parameter | | Standard | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| $V_{CC1}$, $V_{CC2}$ | Supply Voltage ($V_{CC1} \geq V_{CC2}$) | | 2.7 | 5.0 | 5.5 | V |
| AVcc | Analog Supply Voltage | | | $V_{CC1}$ | | V |
| Vss | Supply Voltage | | | 0 | | V |
| AVss | Analog Supply Voltage | | | 0 | | V |
| $V_{IH}$ | HIGH Input Voltage | P3_1 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P12_0 to P12_7, P13_0 to P13_7 | 0.8$V_{CC2}$ | | $V_{CC2}$ | V |
| | | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 (during single-chip mode) | 0.8$V_{CC2}$ | | $V_{CC2}$ | V |
| | | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 (data input during memory expansion and microprocessor mode) | 0.5$V_{CC2}$ | | $V_{CC2}$ | V |
| | | P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P14_0, P14_1, XIN, $\overline{RESET}$, CNVSS, BYTE | 0.8$V_{CC1}$ | | $V_{CC1}$ | V |
| | | P7_0, P7_1 | 0.8$V_{CC1}$ | | 6.5 | V |
| $V_{IL}$ | LOW Input Voltage | P3_1 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P12_0 to P12_7, P13_0 to P13_7 | 0 | | 0.2$V_{CC2}$ | V |
| | | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 (during single-chip mode) | 0 | | 0.2$V_{CC2}$ | V |
| | | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 (data input during memory expansion and microprocessor mode) | 0 | | 0.16$V_{CC2}$ | V |
| | | P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P14_0, P14_1, XIN, $\overline{RESET}$, CNVSS, BYTE | 0 | | 0.2$V_{CC}$ | V |
| $I_{OH(peak)}$ | HIGH Peak Output Current | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1 | | | –10.0 | mA |
| $I_{OH(avg)}$ | HIGH Average Output Current | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1 | | | –5.0 | mA |
| $I_{OL(peak)}$ | LOW Peak Output Current | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1 | | | 10.0 | mA |
| $I_{OL(avg)}$ | LOW Average Output Current | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1 | | | 5.0 | mA |

NOTES:

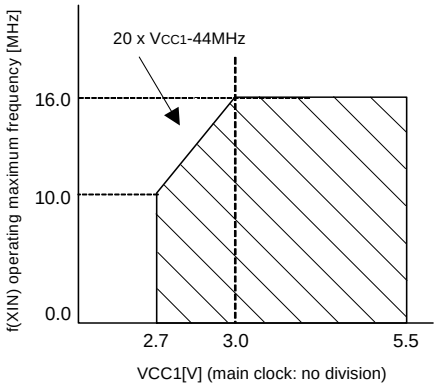
1. Referenced to $V_{CC1}$ = $V_{CC2}$ = 2.7 to 5.5V at $T_{opr}$ = –20 to 85°C / –40 to 85°C unless otherwise specified.
2. The Average Output Current is the mean value within 100ms.
3. The total $I_{OL(peak)}$ for ports P0, P1, P2, P8_6, P8_7, P9, P10, P11, P14_0, and P14_1 must be 80mA max. The total $I_{OL(peak)}$ for ports P3, P4, P5, P6, P7, P8_0 to P8_4, P12, and P13 must be 80mA max. The total $I_{OH(peak)}$ for ports P0, P1, and P2 must be –40mA max. The total $I_{OH(peak)}$ for ports P3, P4, P5, P12, and P13 must be –40mA max. The total $I_{OH(peak)}$ for ports P6, P7, and P8_0 to P8_4 must be –40mA max. The total $I_{OH(peak)}$ for ports P8_6, P8_7, P9, P10, P14_0, and P14_1 must be –40mA max. Set Average Output Current to 1/2 of peak. The total $I_{OH(peak)}$ for ports P8_6, P8_7, P9 , P10, P11, P14_0, and P14_1 must be –40mA max.
   As for 80-pin version, the total $I_{OL(peak)}$ for all ports and $I_{OH(peak)}$ must be 80mA. max. due to one $V_{CC}$ and one $V_{SS}$.
4. There is no external connections for port P1_0 to P1_7, P4_4 to P4_7, P7_2 to P7_5 and P9_1 in 80-pin version.

**Table 5.3 Recommended Operating Conditions (2)** (1)

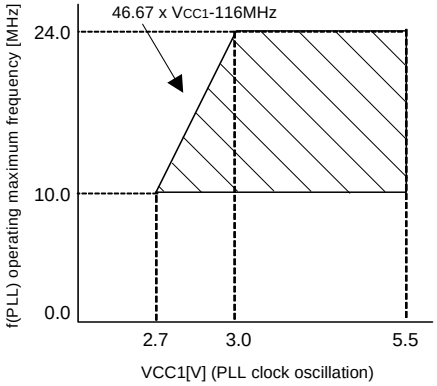
| Symbol | Parameter | | Standard | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| f(XIN) | Main Clock Input Oscillation Frequency (2) | $V_{CC1}$=3.0V to 5.5V | 0 | | 16 | MHz |
| | | $V_{CC1}$=2.7V to 3.0V | 0 | | $20\times V_{CC1}-44$ | MHz |
| f(XCIN) | Sub-Clock Oscillation Frequency | | | 32.768 | 50 | kHz |
| f(Ring) | On-chip Oscillation Frequency | | 0.5 | 1 | 2 | MHz |
| f(PLL) | PLL Clock Oscillation Frequency (2) | $V_{CC1}$=3.0V to 5.5V | 10 | | 24 | MHz |
| | | $V_{CC1}$=2.7V to 3.0V | 10 | | $46.67\times V_{CC1}-116$ | MHz |
| f(BCLK) | CPU Operation Clock | | 0 | | 24 | MHz |
| $t_{SU}$(PLL) | PLL Frequency Synthesizer Stabilization Wait Time | $V_{CC1}$=5.5V | | | 20 | ms |
| | | $V_{CC1}$=3.0V | | | 50 | ms |

NOTES:
1. Referenced to $V_{CC1}$ = $V_{CC2}$ = 2.7 to 5.5V at $T_{opr}$ = –20 to 85°C / –40 to 85°C unless otherwise specified.
2. Relationship between main clock oscillation frequency, and supply voltage.

Main clock input oscillation frequency




PLL clock oscillation frequency



# $V_{CC1}=V_{CC2}=5V$

**Table 5.11 Electrical Characteristics (1)** (1)

| Symbol | Parameter | | | Measuring Condition | Standard | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min. | Typ. | Max. | |
| $V_{OH}$ | HIGH Output Voltage (3) | P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P14_0, P14_1 | | $I_{OH}$=−5mA | $V_{CC1}$−2.0 | | $V_{CC1}$ | V |
| | | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P12_0 to P12_7, P13_0 to P13_7 | | $I_{OH}$=−5mA (2) | $V_{CC2}$−2.0 | | $V_{CC2}$ | |
| $V_{OH}$ | HIGH Output Voltage (3) | P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P14_0, P14_1 | | $I_{OH}$=−200μA | $V_{CC1}$−0.3 | | $V_{CC1}$ | V |
| | | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P12_0 to P12_7, P13_0 to P13_7 | | $I_{OH}$=−200μA (2) | $V_{CC2}$−0.3 | | $V_{CC2}$ | |
| $V_{OH}$ | HIGH Output Voltage XOUT | | HIGHPOWER | $I_{OH}$=−1mA | $V_{CC1}$−2.0 | | $V_{CC1}$ | V |
| | | | LOWPOWER | $I_{OH}$=−0.5mA | $V_{CC1}$−2.0 | | $V_{CC1}$ | |
| | HIGH Output Voltage XCOUT | | HIGHPOWER | With no load applied | | 2.5 | | V |
| | | | LOWPOWER | With no load applied | | 1.6 | | |
| $V_{OL}$ | LOW Output Voltage (3) | P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P14_0, P14_1 | | $I_{OL}$=5mA | | | 2.0 | V |
| | | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P12_0 to P12_7, P13_0 to P13_7 | | $I_{OL}$=5mA (2) | | | 2.0 | |
| $V_{OL}$ | LOW Output Voltage (3) | P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P14_0, P14_1 | | $I_{OL}$=200μA | | | 0.45 | V |
| | | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P12_0 to P12_7, P13_0 to P13_7 | | $I_{OL}$=200μA (2) | | | 0.45 | |
| $V_{OL}$ | LOW Output Voltage XOUT | | HIGHPOWER | $I_{OL}$=1mA | | | 2.0 | V |
| | | | LOWPOWER | $I_{OL}$=0.5mA | | | 2.0 | |
| | LOW Output Voltage XCOUT | | HIGHPOWER | With no load applied | | 0 | | V |
| | | | LOWPOWER | With no load applied | | 0 | | |
| $V_{T+}$-$V_{T-}$ | Hysteresis | $\overline{HOLD}$, $\overline{RDY}$, TA0IN to TA4IN, TB0IN to TB5IN, $\overline{INT0}$ to $\overline{INT5}$, $\overline{NMI}$, $\overline{ADTRG}$, $\overline{CTS0}$ to $\overline{CTS2}$, CLK0 to CLK4, TA0OUT to TA4OUT, $\overline{KI0}$ to $\overline{KI3}$, RXD0 to RXD2, SCL0 to SCL2, SDA0 to SDA2, SIN3, SIN4 | | | 0.2 | | 1.0 | V |
| $V_{T+}$-$V_{T-}$ | Hysteresis | $\overline{RESET}$ | | | 0.2 | | 2.5 | V |
| $I_{IH}$ | HIGH Input Current (3) | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1, XIN, $\overline{RESET}$, CNVSS, BYTE | | $V_I$=5V | | | 5.0 | μA |
| $I_{IL}$ | LOW Input Current (3) | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7,P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1, XIN, $\overline{RESET}$, CNVSS, BYTE | | $V_I$=0V | | | −5.0 | μA |
| $R_{PULLUP}$ | Pull-Up Resistance (3) | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7,P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1 | | $V_I$=0V | 30 | 50 | 170 | kΩ |
| $R_{fXIN}$ | Feedback Resistance XIN | | | | | 1.5 | | MΩ |
| $R_{fXCIN}$ | Feedback Resistance XCIN | | | | | 15 | | MΩ |
| $V_{RAM}$ | RAM Retention Voltage | | | At stop mode | 2.0 | | | V |

NOTES:
1. Referenced to $V_{CC1}$=$V_{CC2}$=4.2 to 5.5V, $V_{SS}$ = 0V at $T_{opr}$ = −20 to 85°C / −40 to 85°C, f(BCLK)=24MHz unless otherwise specified.
2. Where the product is used at $V_{CC1}$ = 5 V and $V_{CC2}$ = 3 V, refer to the 3 V version value for the pin specified value on $V_{CC2}$ port side.
3. There is no external connections for port P1_0 to P1_7, P4_4 to P4_7, P7_2 to P7_5 and P9_1 in 80-pin version.

# $V_{CC1}=V_{CC2}=5V$

## Switching Characteristics

**($V_{CC1}$ = $V_{CC2}$ = 5V, $V_{SS}$ = 0V, at $T_{opr}$ = –20 to 85°C / –40 to 85°C unless otherwise specified)**

**Table 5.27 Memory Expansion and Microprocessor Modes (for setting with no wait)**

| Symbol | Parameter | | Standard | | Unit |
|---|---|---|---|---|---|
| | | | Min. | Max. | |
| td(BCLK-AD) | Address Output Delay Time | See **Figure 5.2** | | 25 | ns |
| th(BCLK-AD) | Address Output Hold Time (in relation to BCLK) | | 4 | | ns |
| th(RD-AD) | Address Output Hold Time (in relation to RD) | | 0 | | ns |
| th(WR-AD) | Address Output Hold Time (in relation to WR) | | (NOTE 2) | | ns |
| td(BCLK-CS) | Chip Select Output Delay Time | | | 25 | ns |
| th(BCLK-CS) | Chip Select Output Hold Time (in relation to BCLK) | | 4 | | ns |
| td(BCLK-ALE) | ALE Signal Output Delay Time | | | 15 | ns |
| th(BCLK-ALE) | ALE Signal Output Hold Time | | –4 | | ns |
| td(BCLK-RD) | RD Signal Output Delay Time | | | 25 | ns |
| th(BCLK-RD) | RD Signal Output Hold Time | | 0 | | ns |
| td(BCLK-WR) | WR Signal Output Delay Time | | | 25 | ns |
| th(BCLK-WR) | WR Signal Output Hold Time | | 0 | | ns |
| td(BCLK-DB) | Data Output Delay Time (in relation to BCLK) | | | 40 | ns |
| th(BCLK-DB) | Data Output Hold Time (in relation to BCLK) (3) | | 4 | | ns |
| td(DB-WR) | Data Output Delay Time (in relation to WR) | | (NOTE 1) | | ns |
| th(WR-DB) | Data Output Hold Time (in relation to WR) (3) | | (NOTE 2) | | ns |
| td(BCLK-HLDA) | HLDA Output Delay Time | | | 40 | ns |

NOTES:

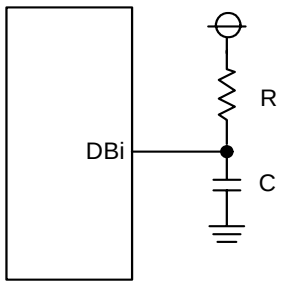
1. Calculated according to the BCLK frequency as follows:

$$\frac{0.5\times10^{9}}{f(BCLK)} - 40[ns]$$ f(BCLK) is 12.5MHz or less.

2. Calculated according to the BCLK frequency as follows:

$$\frac{0.5\times10^{9}}{f(BCLK)} - 10[ns]$$

3. This standard value shows the timing when the output is off, and does not show hold time of data bus.
   Hold time of data bus varies with capacitor volume and pull-up (pull-down) resistance value.
   Hold time of data bus is expressed in
   $t = -CR \times \ln(1 - V_{OL} / V_{CC2})$
   by a circuit of the right figure.
   For example, when $V_{OL} = 0.2V_{CC2}$, C = 30pF, R = 1kΩ, hold time of output "L" level is
   $t = -30pF \times 1k\Omega \times \ln(1 - 0.2V_{CC2} / V_{CC2})$
   = 6.7ns.



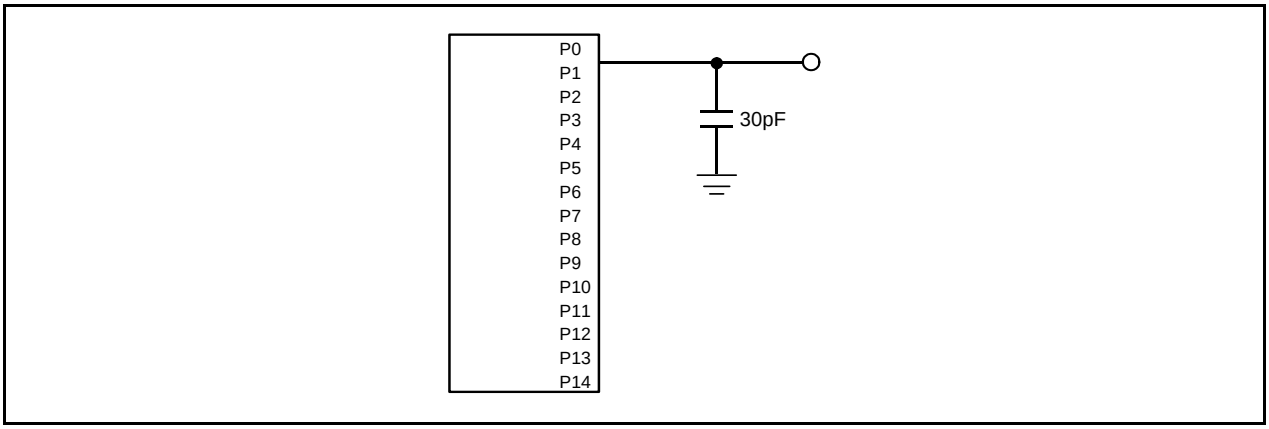




**Figure 5.2 Ports P0 to P14 Measurement Circuit**

# $V_{CC1}=V_{CC2}=5V$

## Switching Characteristics

**($V_{CC1}$ = $V_{CC2}$ = 5V, $V_{SS}$ = 0V, at $T_{opr}$ = –20 to 85°C / –40 to 85°C unless otherwise specified)**

**Table 5.28 Memory Expansion and Microprocessor Modes (for 1- to 3-wait setting and external area access)**

| Symbol | Parameter | | Standard | | Unit |
|---|---|---|---|---|---|
| | | | Min. | Max. | |
| $t_{d(BCLK-AD)}$ | Address Output Delay Time | See **Figure 5.2** | | 25 | ns |
| $t_{h(BCLK-AD)}$ | Address Output Hold Time (in relation to BCLK) | | 4 | | ns |
| $t_{h(RD-AD)}$ | Address Output Hold Time (in relation to RD) | | 0 | | ns |
| $t_{h(WR-AD)}$ | Address Output Hold Time (in relation to WR) | | (NOTE 2) | | ns |
| $t_{d(BCLK-CS)}$ | Chip Select Output Delay Time | | | 25 | ns |
| $t_{h(BCLK-CS)}$ | Chip Select Output Hold Time (in relation to BCLK) | | 4 | | ns |
| $t_{d(BCLK-ALE)}$ | ALE Signal Output Delay Time | | | 15 | ns |
| $t_{h(BCLK-ALE)}$ | ALE Signal Output Hold Time | | -4 | | ns |
| $t_{d(BCLK-RD)}$ | RD Signal Output Delay Time | | | 25 | ns |
| $t_{h(BCLK-RD)}$ | RD Signal Output Hold Time | | 0 | | ns |
| $t_{d(BCLK-WR)}$ | WR Signal Output Delay Time | | | 25 | ns |
| $t_{h(BCLK-WR)}$ | WR Signal Output Hold Time | | 0 | | ns |
| $t_{d(BCLK-DB)}$ | Data Output Delay Time (in relation to BCLK) | | | 40 | ns |
| $t_{h(BCLK-DB)}$ | Data Output Hold Time (in relation to BCLK) (3) | | 4 | | ns |
| $t_{d(DB-WR)}$ | Data Output Delay Time (in relation to WR) | | (NOTE 1) | | ns |
| th(WR-DB) | Data Output Hold Time (in relation to WR)(3) | | (NOTE 2) | | ns |
| $t_{d(BCLK-HLDA)}$ | HLDA Output Delay Time | | | 40 | ns |

NOTES:

1. Calculated according to the BCLK frequency as follows:

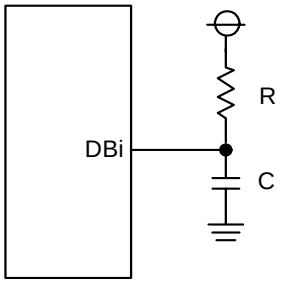
$$\frac{(n-0.5)\times 10^9}{f(BCLK)} - 40[ns]$$

n is “1” for 1-wait setting, “2” for 2-wait setting and “3” for 3-wait setting.
(BCLK) is 12.5MHz or less.

2. Calculated according to the BCLK frequency as follows:

$$\frac{0.5\times 10^9}{f(BCLK)} - 10[ns]$$

3. This standard value shows the timing when the output is off, and does not show hold time of data bus.
Hold time of data bus varies with capacitor volume and pull-up (pull-down) resistance value.
Hold time of data bus is expressed in
$t = -CR \times \ln(1 - V_{OL} / V_{CC2})$
by a circuit of the right figure.
For example, when $V_{OL}$ = 0.2$V_{CC2}$, C = 30pF, R = 1kΩ, hold time of output ”L” level is
$t = -30pF \times 1k\Omega \times \ln(1 - 0.2V_{CC2} / V_{CC2})$
= 6.7ns.



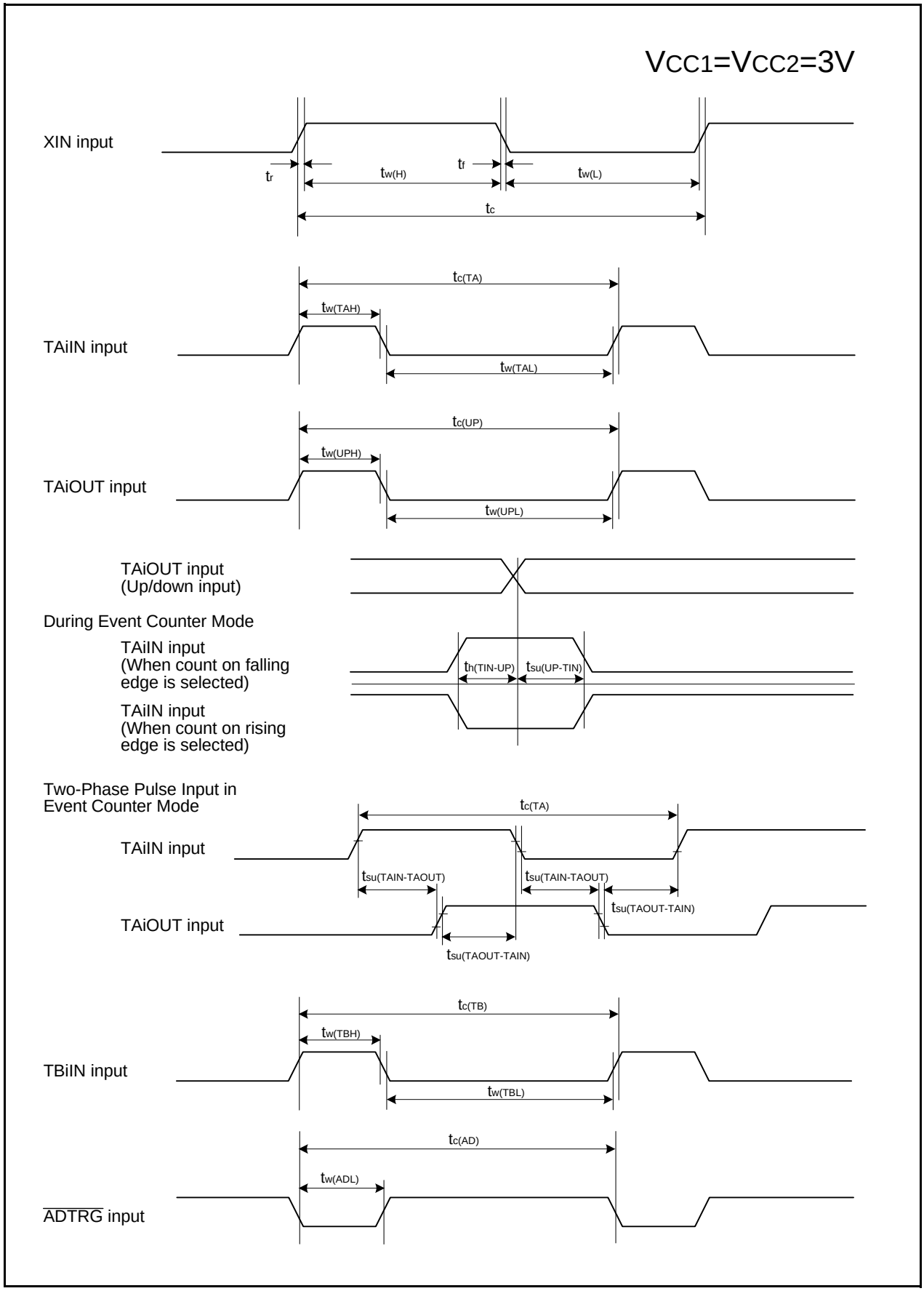
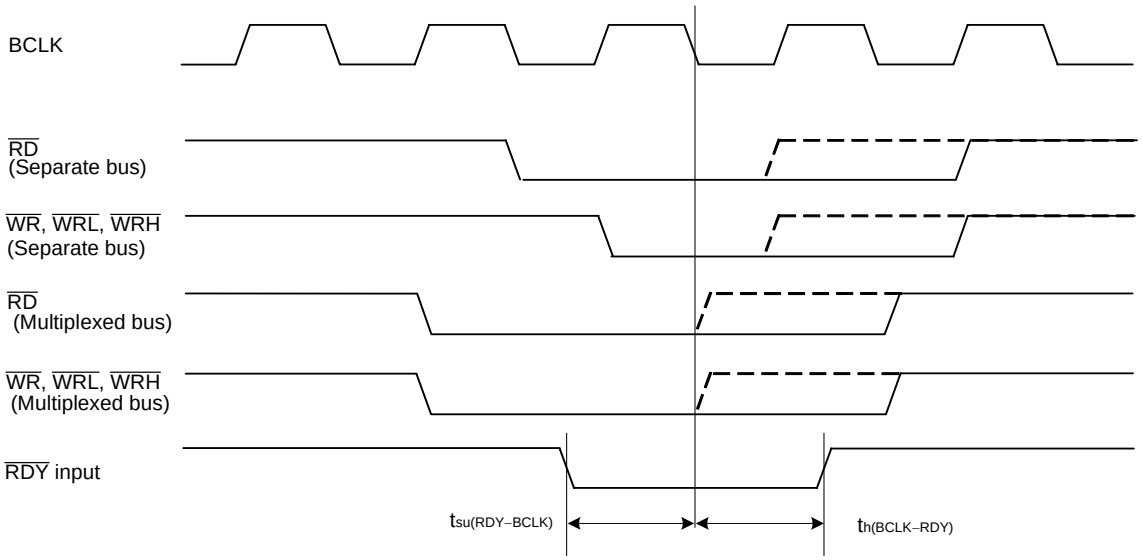



**Figure 5.13 Timing Diagram (1)**

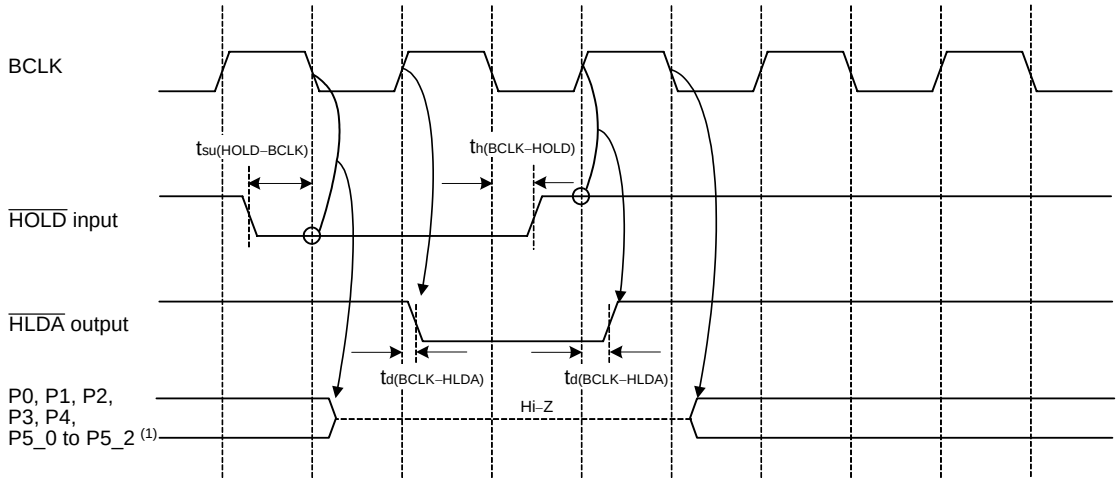
**Memory Expansion Mode, Microprocessor Mode**

$V_{CC1}=V_{CC2}=3V$

(Effective for setting with wait)




(Common to setting with wait and setting without wait)




NOTES:
1. These pins are set to high-impedance regardless of the input level of the BYTE pin, PM06 bit in PM0 register and PM11 bit in PM1 register.

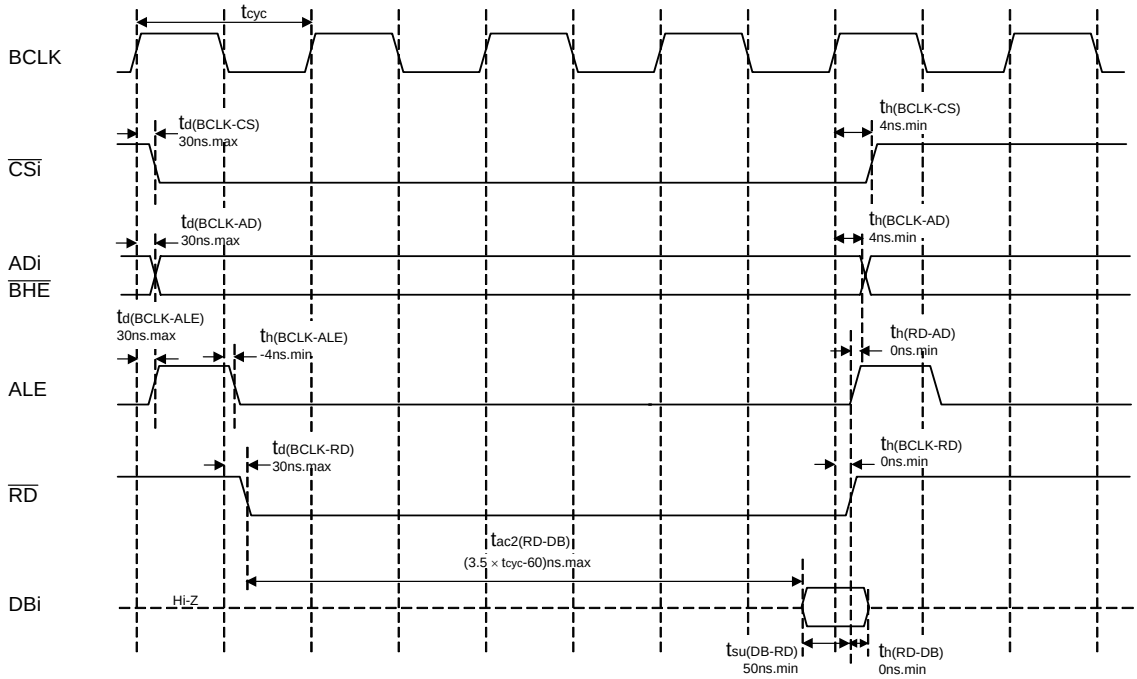
Measuring conditions :
· $V_{CC1}=V_{CC2}=3V$
· Input timing voltage : Determined with $V_{IL}=0.6V$, $V_{IH}=2.4V$
· Output timing voltage : Determined with $V_{OL}=1.5V$, $V_{OH}=1.5V$

**Figure 5.15 Timing Diagram (3)**

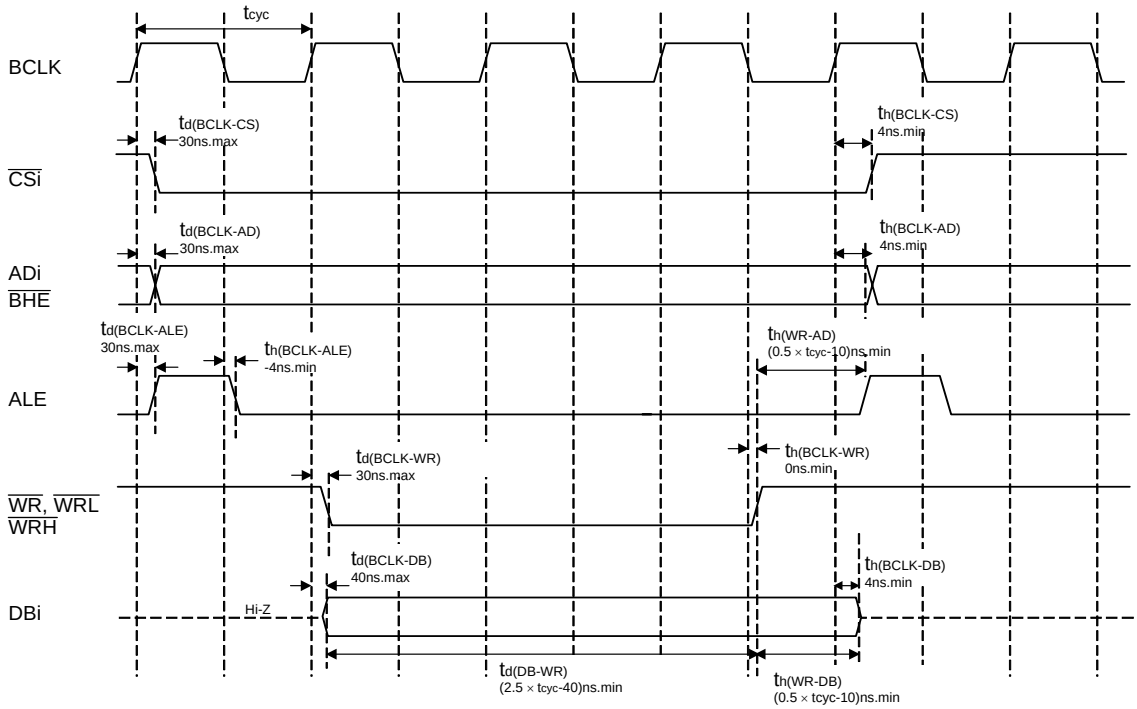
$V_{CC1} = V_{CC2} = 3V$

**Memory Expansion Mode, Microprocessor Mode**
**(**for 3-wait setting and external area access**)**

**Read timing**




**Write timing**




$$t_{cyc} = \frac{1}{f(BCLK)}$$

Measuring conditions
· $V_{CC1}$=$V_{CC2}$=3V
· Input timing voltage : $V_{IL}$=0.6V, $V_{IH}$=2.4V
· Output timing voltage : $V_{OL}$=1.5V, $V_{OH}$=1.5V

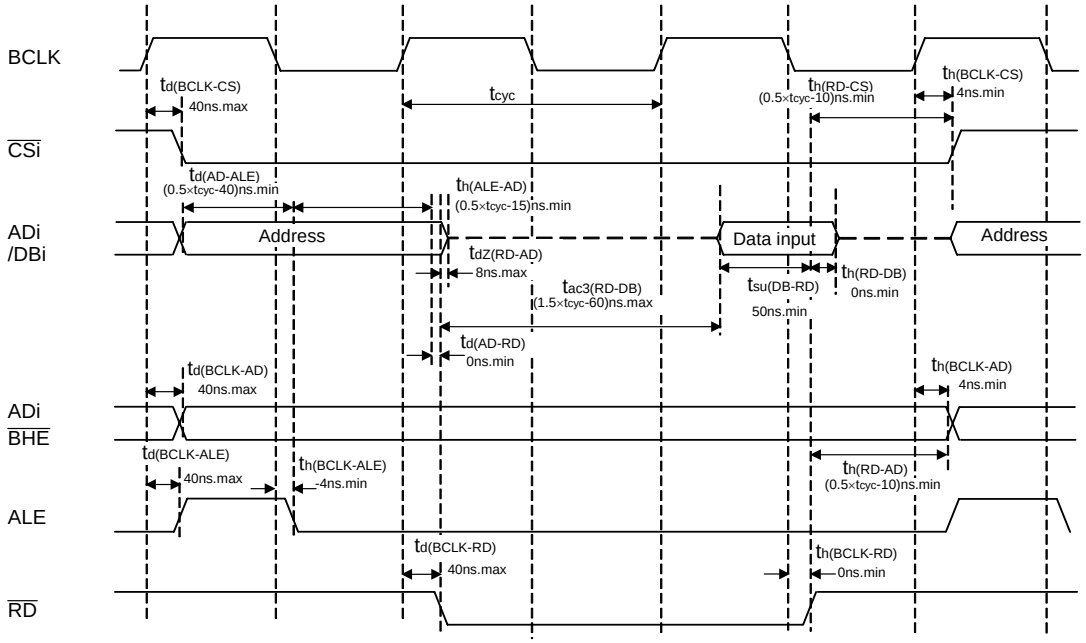
**Figure 5.19 Timing Diagram (7)**

## Memory Expansion Mode, Microprocessor Mode

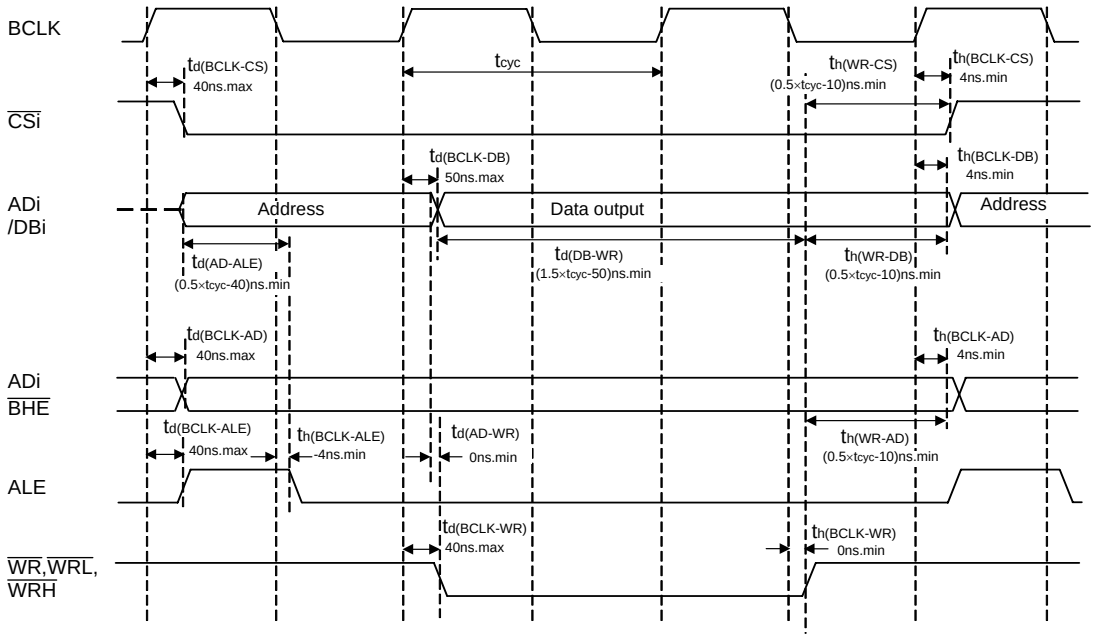
$V_{CC1}=V_{CC2}=3V$

**(**For 2-wait setting, external area access and multiplex bus selection**)**

**Read timing**




**Write timing**




$$t_{cyc}=\frac{1}{f(BCLK)}$$

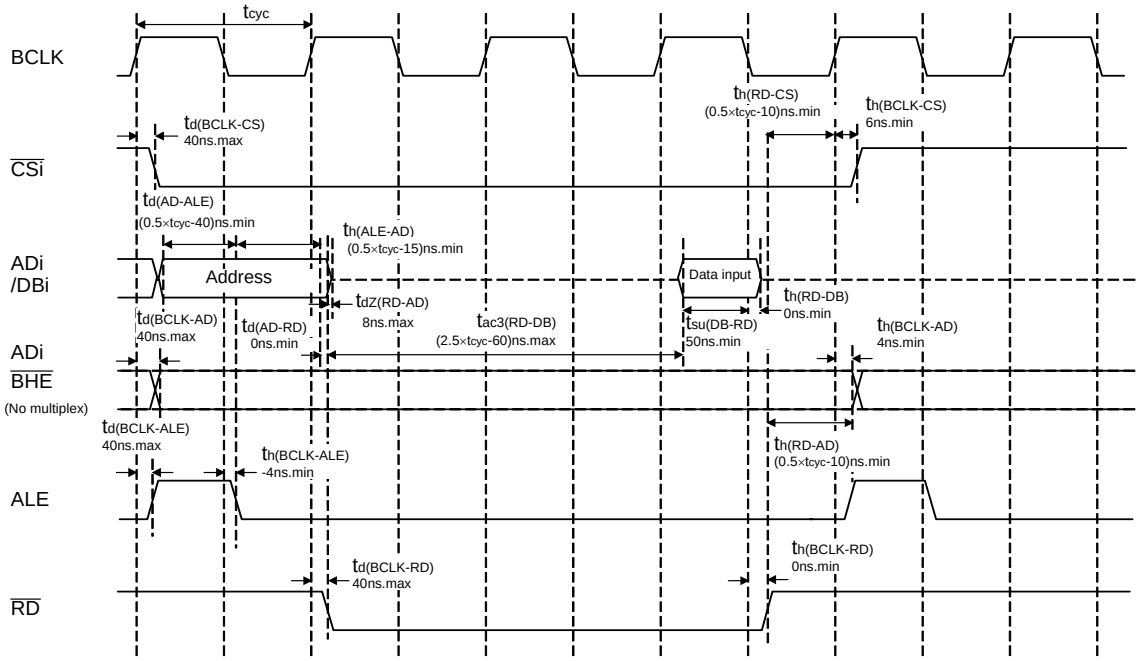
Measuring conditions
- $V_{CC1}=V_{CC2}=3V$
- Input timing voltage : $V_{IL}=0.6V$, $V_{IH}=2.4V$
- Output timing voltage : $V_{OL}=1.5V$, $V_{OH}=1.5V$

**Figure 5.20 Timing Diagram (8)**

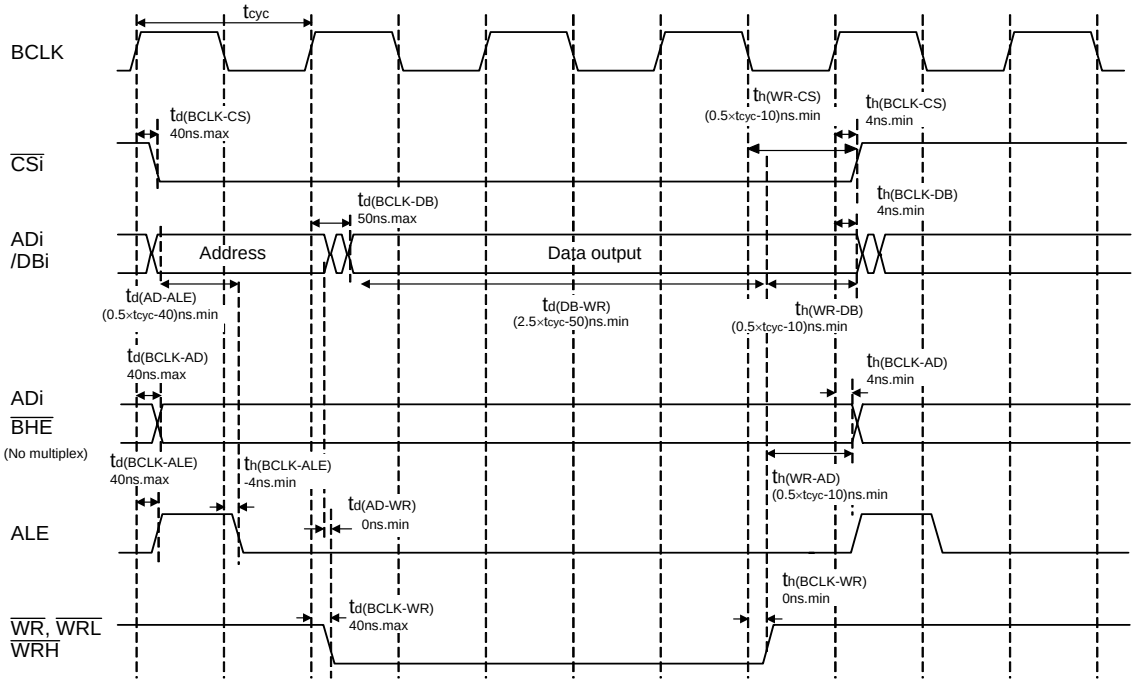
$V_{CC1}=V_{CC2}=3V$

**Memory Expansion Mode, Microprocessor Mode**
(For 3-wait setting, external area access and multiplex bus selection)

**Read timing**




**Write timing**




$$t_{cyc}=\frac{1}{f(BCLK)}$$

Measuring conditions
- $V_{CC1}=V_{CC2}=3V$
- Input timing voltage : $V_{IL}=0.6V$, $V_{IH}=2.4V$
- Output timing voltage : $V_{OL}=1.5V$, $V_{OH}=1.5V$

**Figure 5.21 Timing Diagram (9)**

**Table 5.51 A/D Conversion Characteristics** (1)

| Symbol | Parameter | | Measuring Condition | | Standard | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min. | Typ. | Max. | |
| – | Resolution | | $V_{REF}=V_{CC1}$ | | | | 10 | Bits |
| INL | Integral Non-Linearity Error | 10bit | $V_{REF}=V_{CC1}=5V$ | AN0 to AN7 input, AN0_0 to AN0_7 input, AN2_0 to AN2_7 input, ANEX0, ANEX1 input | | | ±3 | LSB |
| | | | | External operation amp connection mode | | | ±7 | LSB |
| | | 8bit | $V_{REF}=V_{CC1}=5V$ | | | | ±2 | LSB |
| – | Absolute Accuracy | 10bit | $V_{REF}=V_{CC1}=5V$ | AN0 to AN7 input, AN0_0 to AN0_7 input, AN2_0 to AN2_7 input, ANEX0, ANEX1 input | | | ±3 | LSB |
| | | | | External operation amp connection mode | | | ±7 | LSB |
| | | 8bit | $V_{REF}=V_{CC1}=5V$ | | | | ±2 | LSB |
| – | Tolerance Level Impedance | | | | | 3 | | kΩ |
| DNL | Differential Non-Linearity Error | | | | | | ±1 | LSB |
| – | Offset Error | | | | | | ±3 | LSB |
| – | Gain Error | | | | | | ±3 | LSB |
| $R_{LADDER}$ | Ladder Resistance | | $V_{REF}=V_{CC1}$ | | 10 | | 40 | kΩ |
| $t_{CONV}$ | 10-bit Conversion Time, Sample & Hold Function Available | | $V_{REF}=V_{CC1}=5V$, ϕAD=12MHz | | 2.75 | | | µs |
| $t_{CONV}$ | 8-bit Conversion Time, Sample & Hold Function Available | | $V_{REF}=V_{CC1}=5V$, ϕAD=12MHz | | 2.33 | | | µs |
| $t_{SAMP}$ | Sampling Time | | | | 0.25 | | | µs |
| $V_{REF}$ | Reference Voltage | | | | 2.0 | | $V_{CC1}$ | V |
| $V_{IA}$ | Analog Input Voltage | | | | 0 | | $V_{REF}$ | V |

NOTES:
1. Referenced to $V_{CC1}=AV_{CC}=V_{REF}=4.0$ to 5.5V, $V_{SS}=AV_{SS}=0V$ at $T_{opr}$ = –40 to 85°C / –40 to 125°C unless otherwise specified. T version = –40 to 85°C, V version =–40 to 125°C
2. ϕAD frequency must be 12 MHz or less.
3. When sample & hold is disabled, ϕAD frequency must be 250 kHz or more, in addition to the limitation in Note 2. When sample & hold is enabled, ϕAD frequency must be 1MHz or more, in addition to the limitation in Note 2.

**Table 5.52 D/A Conversion Characteristics** (1)

| Symbol | Parameter | Measuring Condition | Standard | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| – | Resolution | | | | 8 | Bits |
| – | Absolute Accuracy | | | | 1.0 | % |
| $t_{SU}$ | Setup Time | | | | 3 | µs |
| $R_O$ | Output Resistance | | 4 | 10 | 20 | kΩ |
| $I_{VREF}$ | Reference Power Supply Input Current | (NOTE 2) | | | 1.5 | mA |

NOTES:
1. Referenced to $V_{CC1}=V_{REF}=4.0$ to 5.5V, $V_{SS}=AV_{SS}=0V$ at $T_{opr}$ = –40 to 85°C / –40 to 125°C unless otherwise specified. T version = –40 to 85°C, V version =–40 to 125°C
2. This applies when using one D/A converter, with the D/A register for the unused D/A converter set to “00h”. The resistor ladder of the A/D converter is not included. Also, when D/A register contents are not “00h”, the $I_{VREF}$ will flow even if Vref id disconnected by the A/D control register.

# $V_{CC1}$=$V_{CC2}$=5V

**Timing Requirements**
**($V_{CC1}$ = $V_{CC2}$ = 5V, $V_{SS}$ = 0V, at $T_{opr}$ = –40 to 85°C (T version) / –40 to 125°C (V version) unless otherwise specified)**

**Table 5.60 Timer A Input (Counter Input in Event Counter Mode)**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(TA)}$ | TAiIN Input Cycle Time | 100 | | ns |
| $t_{w(TAH)}$ | TAiIN Input HIGH Pulse Width | 40 | | ns |
| $t_{w(TAL)}$ | TAiIN Input LOW Pulse Width | 40 | | ns |

**Table 5.61 Timer A Input (Gating Input in Timer Mode)**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(TA)}$ | TAiIN Input Cycle Time | 400 | | ns |
| $t_{w(TAH)}$ | TAiIN Input HIGH Pulse Width | 200 | | ns |
| $t_{w(TAL)}$ | TAiIN Input LOW Pulse Width | 200 | | ns |

**Table 5.62 Timer A Input (External Trigger Input in One-shot Timer Mode)**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(TA)}$ | TAiIN Input Cycle Time | 200 | | ns |
| $t_{w(TAH)}$ | TAiIN Input HIGH Pulse Width | 100 | | ns |
| $t_{w(TAL)}$ | TAiIN Input LOW Pulse Width | 100 | | ns |

**Table 5.63 Timer A Input (External Trigger Input in Pulse Width Modulation Mode)**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{w(TAH)}$ | TAiIN Input HIGH Pulse Width | 100 | | ns |
| $t_{w(TAL)}$ | TAiIN Input LOW Pulse Width | 100 | | ns |

**Table 5.64 Timer A Input (Counter Increment/Decrement Input in Event Counter Mode)**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(UP)}$ | TAiOUT Input Cycle Time | 2000 | | ns |
| $t_{w(UPH)}$ | TAiOUT Input HIGH Pulse Width | 1000 | | ns |
| $t_{w(UPL)}$ | TAiOUT Input LOW Pulse Width | 1000 | | ns |
| $t_{su(UP-TIN)}$ | TAiOUT Input Setup Time | 400 | | ns |
| $t_{h(TIN-UP)}$ | TAiOUT Input Hold Time | 400 | | ns |

**Table 5.65 Timer A Input (Two-phase Pulse Input in Event Counter Mode)**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(TA)}$ | TAiIN Input Cycle Time | 800 | | ns |
| $t_{su(TAIN-TAOUT)}$ | TAiOUT Input Setup Time | 200 | | ns |
| $t_{su(TAOUT-TAIN)}$ | TAiIN Input Setup Time | 200 | | ns |

# $V_{CC1}$=$V_{CC2}$=5V

**Timing Requirements**
**($V_{CC1}$ = $V_{CC2}$ = 5V, $V_{SS}$ = 0V, at $T_{opr}$ = –40 to 85°C (T version) / –40 to 125°C (V version) unless otherwise specified)**

**Table 5.66 Timer B Input (Counter Input in Event Counter Mode)**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(TB)}$ | TBiIN Input Cycle Time (counted on one edge) | 100 | | ns |
| $t_{w(TBH)}$ | TBiIN Input HIGH Pulse Width (counted on one edge) | 40 | | ns |
| $t_{w(TBL)}$ | TBiIN Input LOW Pulse Width (counted on one edge) | 40 | | ns |
| $t_{c(TB)}$ | TBiIN Input Cycle Time (counted on both edges) | 200 | | ns |
| $t_{w(TBH)}$ | TBiIN Input HIGH Pulse Width (counted on both edges) | 80 | | ns |
| $t_{w(TBL)}$ | TBiIN Input LOW Pulse Width (counted on both edges) | 80 | | ns |

**Table 5.67 Timer B Input (Pulse Period Measurement Mode)**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(TB)}$ | TBiIN Input Cycle Time | 400 | | ns |
| $t_{w(TBH)}$ | TBiIN Input HIGH Pulse Width | 200 | | ns |
| $t_{w(TBL)}$ | TBiIN Input LOW Pulse Width | 200 | | ns |

**Table 5.68 Timer B Input (Pulse Width Measurement Mode)**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(TB)}$ | TBiIN Input Cycle Time | 400 | | ns |
| $t_{w(TBH)}$ | TBiIN Input HIGH Pulse Width | 200 | | ns |
| $t_{w(TBL)}$ | TBiIN Input LOW Pulse Width | 200 | | ns |

**Table 5.69 A/D Trigger Input**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(AD)}$ | $\overline{\text{ADTRG}}$ Input Cycle Time | 1000 | | ns |
| $t_{w(ADL)}$ | $\overline{\text{ADTRG}}$ input LOW Pulse Width | 125 | | ns |

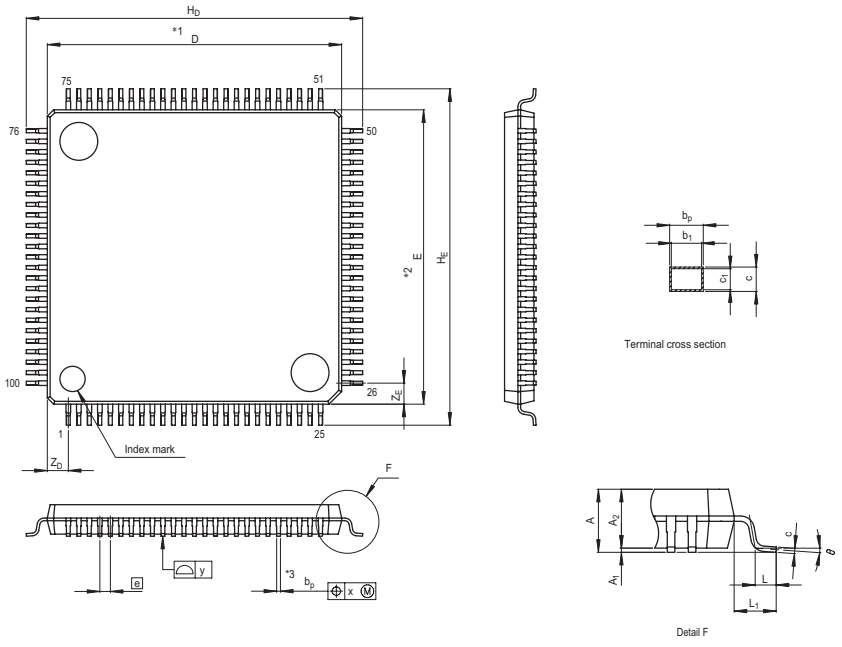
**Table 5.70 Serial Interface**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(CK)}$ | CLKi Input Cycle Time | 200 | | ns |
| $t_{w(CKH)}$ | CLKi Input HIGH Pulse Width | 100 | | ns |
| $t_{w(CKL)}$ | CLKi Input LOW Pulse Width | 100 | | ns |
| $t_{d(C-Q)}$ | TXDi Output Delay Time | | 80 | ns |
| $t_{h(C-Q)}$ | TXDi Hold Time | 0 | | ns |
| $t_{su(D-C)}$ | RXDi Input Setup Time | 70 | | ns |
| $t_{h(C-D)}$ | RXDi Input Hold Time | 90 | | ns |

**Table 5.71 External Interrupt $\overline{\text{INTi}}$ Input**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{w(INH)}$ | $\overline{\text{INTi}}$ Input HIGH Pulse Width | 250 | | ns |
| $t_{w(INL)}$ | $\overline{\text{INTi}}$ Input LOW Pulse Width | 250 | | ns |

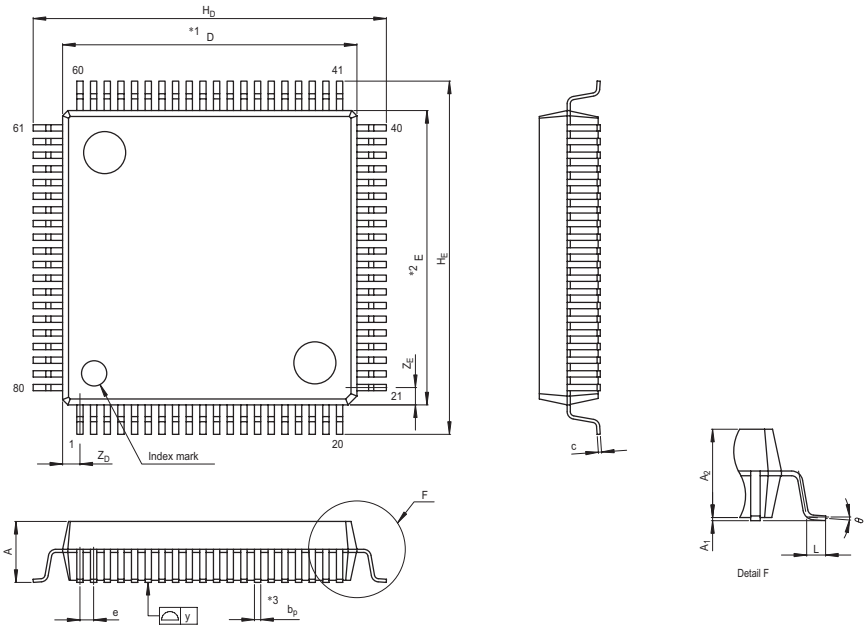
| JEITA Package Code | RENESAS Code | Previous Code | MASS[Typ.] |
|---|---|---|---|
| P-LQFP100-14x14-0.50 | PLQP0100KB-A | 100P6Q-A / FP-100U / FP-100UV | 0.6g |




NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

| Reference Symbol | Dimension in Millimeters | | |
|---|---|---|---|
| | Min | Nom | Max |
| D | 13.9 | 14.0 | 14.1 |
| E | 13.9 | 14.0 | 14.1 |
| $A_2$ | — | 1.4 | — |
| $H_D$ | 15.8 | 16.0 | 16.2 |
| $H_E$ | 15.8 | 16.0 | 16.2 |
| A | — | — | 1.7 |
| $A_1$ | 0.05 | 0.1 | 0.15 |
| $b_p$ | 0.15 | 0.20 | 0.25 |
| $b_1$ | — | 0.18 | — |
| c | 0.09 | 0.145 | 0.20 |
| $c_1$ | — | 0.125 | — |
| θ | 0° | — | 8° |
| e | — | 0.5 | — |
| x | — | — | 0.08 |
| y | — | — | 0.08 |
| $Z_D$ | — | 1.0 | — |
| $Z_E$ | — | 1.0 | — |
| L | 0.35 | 0.5 | 0.65 |
| $L_1$ | — | 1.0 | — |

| JEITA Package Code | RENESAS Code | Previous Code | MASS[Typ.] |
|---|---|---|---|
| P-QFP80-14x14-0.65 | PRQP0080JA-A | 80P6S-A | 1.1g |




NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

| Reference Symbol | Dimension in Millimeters | | |
|---|---|---|---|
| | Min | Nom | Max |
| D | 13.8 | 14.0 | 14.2 |
| E | 13.8 | 14.0 | 14.2 |
| $A_2$ | — | 2.8 | — |
| $H_D$ | 16.5 | 16.8 | 17.1 |
| $H_E$ | 16.5 | 16.8 | 17.1 |
| A | — | — | 3.05 |
| $A_1$ | 0 | 0.1 | 0.2 |
| $b_p$ | 0.25 | 0.3 | 0.4 |
| c | 0.13 | 0.15 | 0.2 |
| θ | 0° | — | 10° |
| e | 0.5 | 0.65 | 0.8 |
| y | — | — | 0.10 |
| $Z_D$ | — | 0.825 | — |
| $Z_E$ | — | 0.825 | — |
| L | 0.4 | 0.6 | 0.8 |