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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Not For New Designs
Core Processor	M16C/60
Core Size	16-Bit
Speed	24MHz
Connectivity	I ² C, IEBus, UART/USART
Peripherals	DMA, WDT
Number of I/O	113
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	20K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 26x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	128-LQFP
Supplier Device Package	128-LFQFP (14x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/m30625fgpgp-u5c

1.2 Performance Outline

Table 1.1 to 1.3 list Performance Outline of M16C/62P Group (M16C/62P, M16C/62PT)(128-pin version).

Table 1.1 Performance Outline of M16C/62P Group (M16C/62P, M16C/62PT)(128-pin version)

	Item	Performance
		M16C/62P
CPU	Number of Basic Instructions	91 instructions
	Minimum Instruction Execution Time	41.7ns(f(BCLK)=24MHz, VCC1=3.3 to 5.5V) 100ns(f(BCLK)=10MHz, VCC1=2.7 to 5.5V)
	Operating Mode	Single-chip, memory expansion and microprocessor mode
	Address Space	1 Mbyte (Available to 4 Mbytes by memory space expansion function)
	Memory Capacity	See Table 1.4 to 1.5 Product List
Peripheral Function	Port	Input/Output : 113 pins, Input : 1 pin
	Multifunction Timer	Timer A : 16 bits x 5 channels, Timer B : 16 bits x 6 channels, Three phase motor control circuit
	Serial Interface	3 channels Clock synchronous, UART, I ² C bus ⁽¹⁾ , IEBus ⁽²⁾ 2 channels Clock synchronous
	A/D Converter	10-bit A/D converter: 1 circuit, 26 channels
	D/A Converter	8 bits x 2 channels
	DMAC	2 channels
	CRC Calculation Circuit	CCITT-CRC
	Watchdog Timer	15 bits x 1 channel (with prescaler)
	Interrupt	Internal: 29 sources, External: 8 sources, Software: 4 sources, Priority level: 7 levels
	Clock Generation Circuit	4 circuits Main clock generation circuit (*), Subclock generation circuit (*), On-chip oscillator, PLL synthesizer (*)Equipped with a built-in feedback resistor.
	Oscillation Stop Detection Function	Stop detection of main clock oscillation, re-oscillation detection function
	Voltage Detection Circuit	Available (option ⁽⁴⁾)
Electric Characteristics	Supply Voltage	VCC1=3.0 to 5.5 V, VCC2=2.7V to VCC1 (f(BCLK)=24MHz) VCC1=2.7 to 5.5 V, VCC2=2.7V to VCC1 (f(BCLK)=10MHz)
	Power Consumption	14 mA (VCC1=VCC2=5V, f(BCLK)=24MHz) 8 mA (VCC1=VCC2=3V, f(BCLK)=10MHz) 1.8μA (VCC1=VCC2=3V, f(XCIN)=32kHz, wait mode) 0.7μA (VCC1=VCC2=3V, stop mode)
Flash memory version	Program/Erase Supply Voltage	3.3±0.3 V or 5.0±0.5 V
	Program and Erase Endurance	100 times (all area) or 1,000 times (user ROM area without block A and block 1) / 10,000 times (block A, block 1) ⁽³⁾
Operating Ambient Temperature		-20 to 85°C, -40 to 85°C ⁽³⁾
Package		128-pin plastic mold LQFP

NOTES:

1. I²C bus is a registered trademark of Koninklijke Philips Electronics N. V.
2. IEBus is a registered trademark of NEC Electronics Corporation.
3. See **Table 1.8 Product Code** for the program and erase endurance, and operating ambient temperature. In addition 1,000 times/10,000 times are under development as of Jul., 2005. Please inquire about a release schedule.
4. All options are on request basis.

1.3 Block Diagram

Figure 1.1 is a M16C/62P Group (M16C/62P, M16C/62PT) 128-pin and 100-pin version Block Diagram,
Figure 1.2 is a M16C/62P Group (M16C/62P, M16C/62PT) 80-pin version Block Diagram.

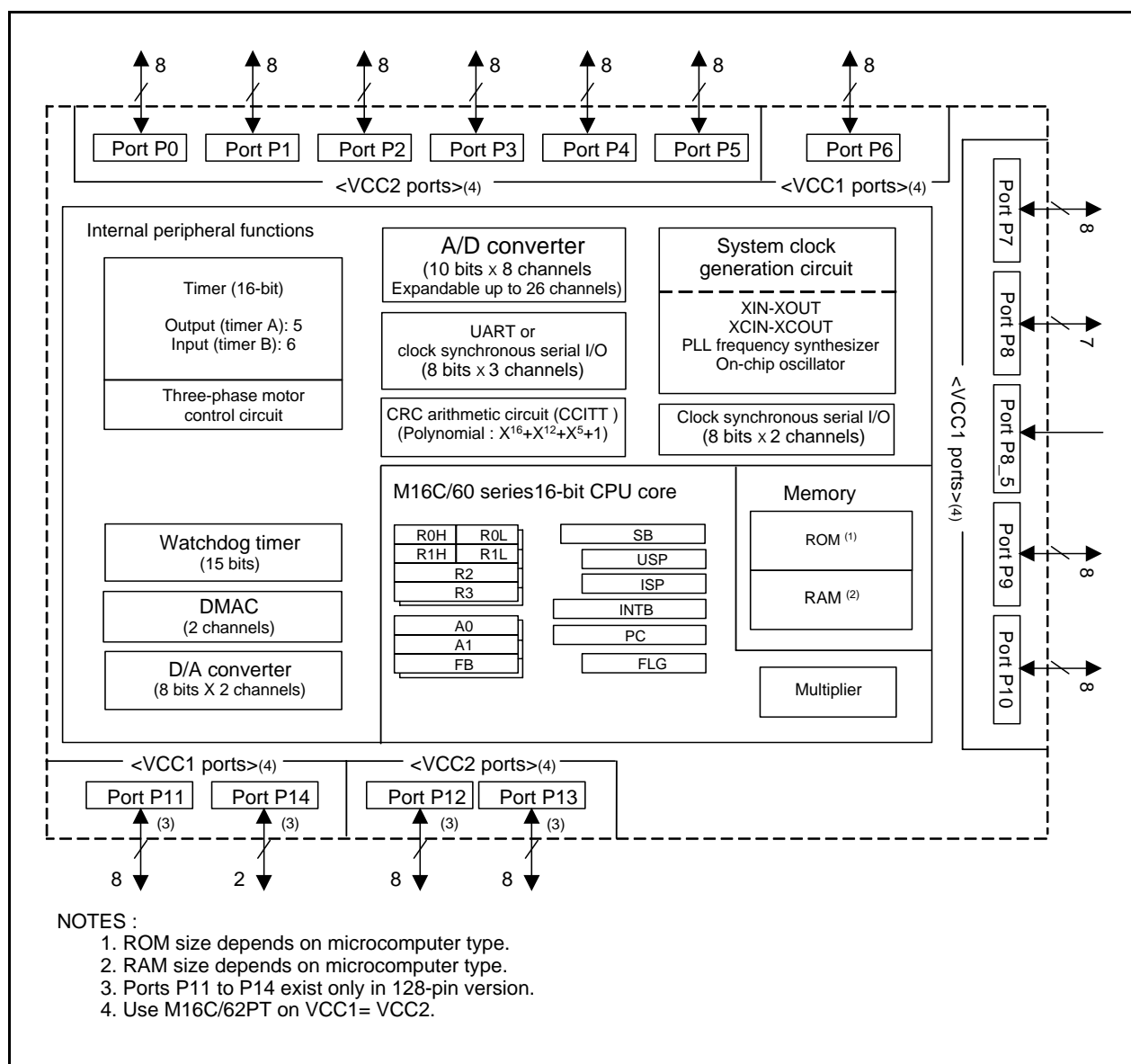


Figure 1.1 M16C/62P Group (M16C/62P, M16C/62PT) 128-pin and 100-pin version Block Diagram

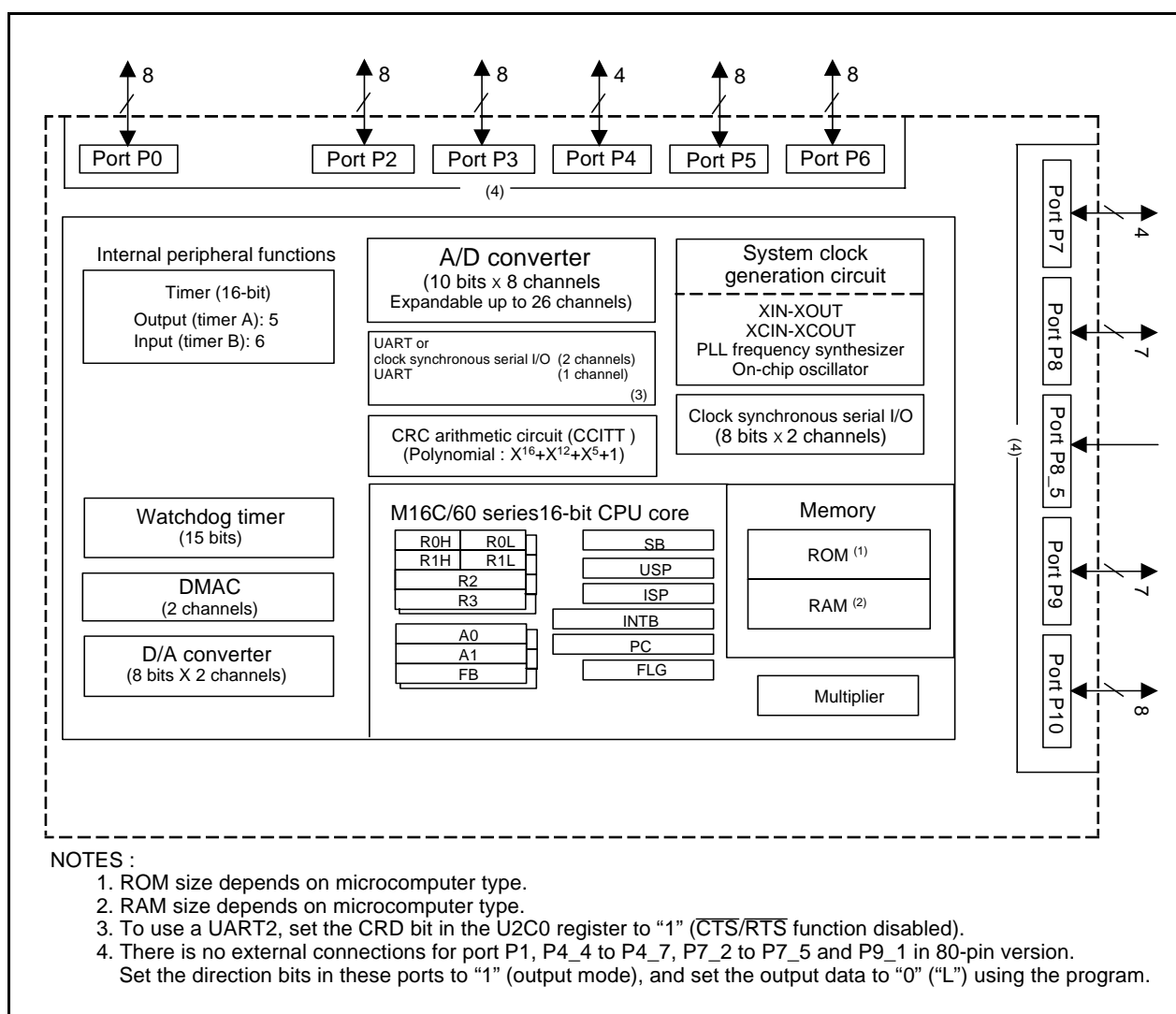


Figure 1.2 M16C/62P Group (M16C/62P, M16C/62PT) 80-pin version Block Diagram

Table 1.8 Product Code of Flash Memory version and ROMless version for M16C/62P

	Product Code	Package	Internal ROM (User ROM Area Without Block A, Block 1)		Internal ROM (Block A, Block 1)		Operating Ambient Temperature
			Program and Erase Endurance	Temperature Range	Program and Erase Endurance	Temperature Range	
Flash memory Version	D3	Lead-included	100	0°C to 60°C	100	0°C to 60°C	-40°C to 85°C
	D5						-20°C to 85°C
	D7		1,000		10,000	-40°C to 85°C	-40°C to 85°C
	D9					-20°C to 85°C	-20°C to 85°C
	U3	Lead-free	100		100	0°C to 60°C	-40°C to 85°C
	U5					-20°C to 85°C	
	U7		1,000		10,000	-40°C to 85°C	-40°C to 85°C
	U9					-20°C to 85°C	-20°C to 85°C
ROM-less version	D3	Lead-included	—	—	—	—	-40°C to 85°C
	D5		—	—	—	—	-20°C to 85°C
	U3	Lead-free	—	—	—	—	-40°C to 85°C
	U5		—	—	—	—	-20°C to 85°C

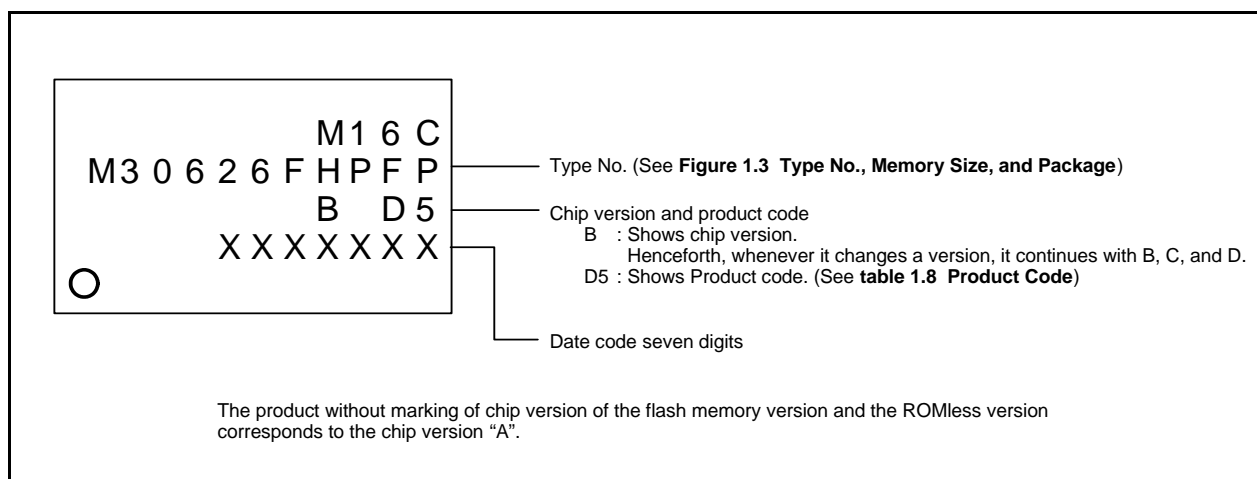
**Figure 1.4 Marking Diagram of Flash Memory version and ROM-less version for M16C/62P (Top View)**

Table 1.11 Pin Characteristics for 128-Pin Package (2)

Pin No.	Control Pin	Port	Interrupt Pin	Timer Pin	UART Pin	Analog Pin	Bus Control Pin
51		P5_6					ALE
52		P5_5					$\overline{\text{HOLD}}$
53		P5_4					$\overline{\text{HLDA}}$
54		P13_3					
55		P13_2					
56		P13_1					
57		P13_0					
58		P5_3					BCLK
59		P5_2					$\overline{\text{RD}}$
60		P5_1					$\overline{\text{WRH/BHE}}$
61		P5_0					$\overline{\text{WRL/WR}}$
62		P12_7					
63		P12_6					
64		P12_5					
65		P4_7					$\overline{\text{CS3}}$
66		P4_6					$\overline{\text{CS2}}$
67		P4_5					$\overline{\text{CS1}}$
68		P4_4					$\overline{\text{CS0}}$
69		P4_3					A19
70		P4_2					A18
71		P4_1					A17
72		P4_0					A16
73		P3_7					A15
74		P3_6					A14
75		P3_5					A13
76		P3_4					A12
77		P3_3					A11
78		P3_2					A10
79		P3_1					A9
80		P12_4					
81		P12_3					
82		P12_2					
83		P12_1					
84		P12_0					
85	VCC2						
86		P3_0					A8(/-/D7)
87	VSS						
88		P2_7				AN2_7	A7(/D7/D6)
89		P2_6				AN2_6	A6(/D6/D5)
90		P2_5				AN2_5	A5(/D5/D4)
91		P2_4				AN2_4	A4(/D4/D3)
92		P2_3				AN2_3	A3(/D3/D2)
93		P2_2				AN2_2	A2(/D2/D1)
94		P2_1				AN2_1	A1(/D1/D0)
95		P2_0				AN2_0	A0(/D0/-)
96		P1_7	$\overline{\text{INT5}}$				D15
97		P1_6	$\overline{\text{INT4}}$				D14
98		P1_5	$\overline{\text{INT3}}$				D13
99		P1_4					D12
100		P1_3					D11

5. Electrical Characteristics

5.1 Electrical Characteristics (M16C/62P)

Table 5.1 Absolute Maximum Ratings

Symbol	Parameter		Condition	Rated Value	Unit
V _{CC1} , V _{CC2}	Supply Voltage		V _{CC1} =AV _{CC}	−0.3 to 6.5	V
V _{CC2}	Supply Voltage		V _{CC2}	−0.3 to V _{CC1} +0.1	V
AV _{CC}	Analog Supply Voltage		V _{CC1} =AV _{CC}	−0.3 to 6.5	V
V _I	Input Voltage	RESET, CNVSS, BYTE, P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P14_0, P14_1, VREF, XIN		−0.3 to V _{CC1} +0.3 ⁽¹⁾	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P12_0 to P12_7, P13_0 to P13_7		−0.3 to V _{CC2} +0.3 ⁽¹⁾	V
		P7_0, P7_1		−0.3 to 6.5	V
V _O	Output Voltage	P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P14_0, P14_1, XOUT		−0.3 to V _{CC1} +0.3 ⁽¹⁾	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P12_0 to P12_7, P13_0 to P13_7		−0.3 to V _{CC2} +0.3 ⁽¹⁾	V
		P7_0, P7_1		−0.3 to 6.5	V
P _d	Power Dissipation		−40°C<T _{opr} ≤85°C	300	mW
T _{opr}	Operating Ambient Temperature	When the Microcomputer is Operating		−20 to 85 / −40 to 85	°C
		Flash Program Erase		0 to 60	
T _{stg}	Storage Temperature			−65 to 150	°C

NOTES:

1. There is no external connections for port P1_0 to P1_7, P4_4 to P4_7, P7_2 to P7_5 and P9_1 in 80-pin version.

Table 5.5 D/A Conversion Characteristics ⁽¹⁾

Symbol	Parameter	Measuring Condition	Standard			Unit
			Min.	Typ.	Max.	
–	Resolution				8	Bits
–	Absolute Accuracy				1.0	%
t _{su}	Setup Time				3	μs
R _o	Output Resistance		4	10	20	kΩ
I _{VREF}	Reference Power Supply Input Current	(NOTE 2)			1.5	mA

NOTES:

1. Referenced to V_{CC1}=V_{REF}=3.3 to 5.5V, V_{SS}=A_{VSS}=0V at T_{opr} = –20 to 85°C / –40 to 85°C unless otherwise specified.
2. This applies when using one D/A converter, with the D/A register for the unused D/A converter set to “00h”. The resistor ladder of the A/D converter is not included. Also, when D/A register contents are not “00h”, the I_{VREF} will flow even if V_{ref} is disconnected by the A/D control register.

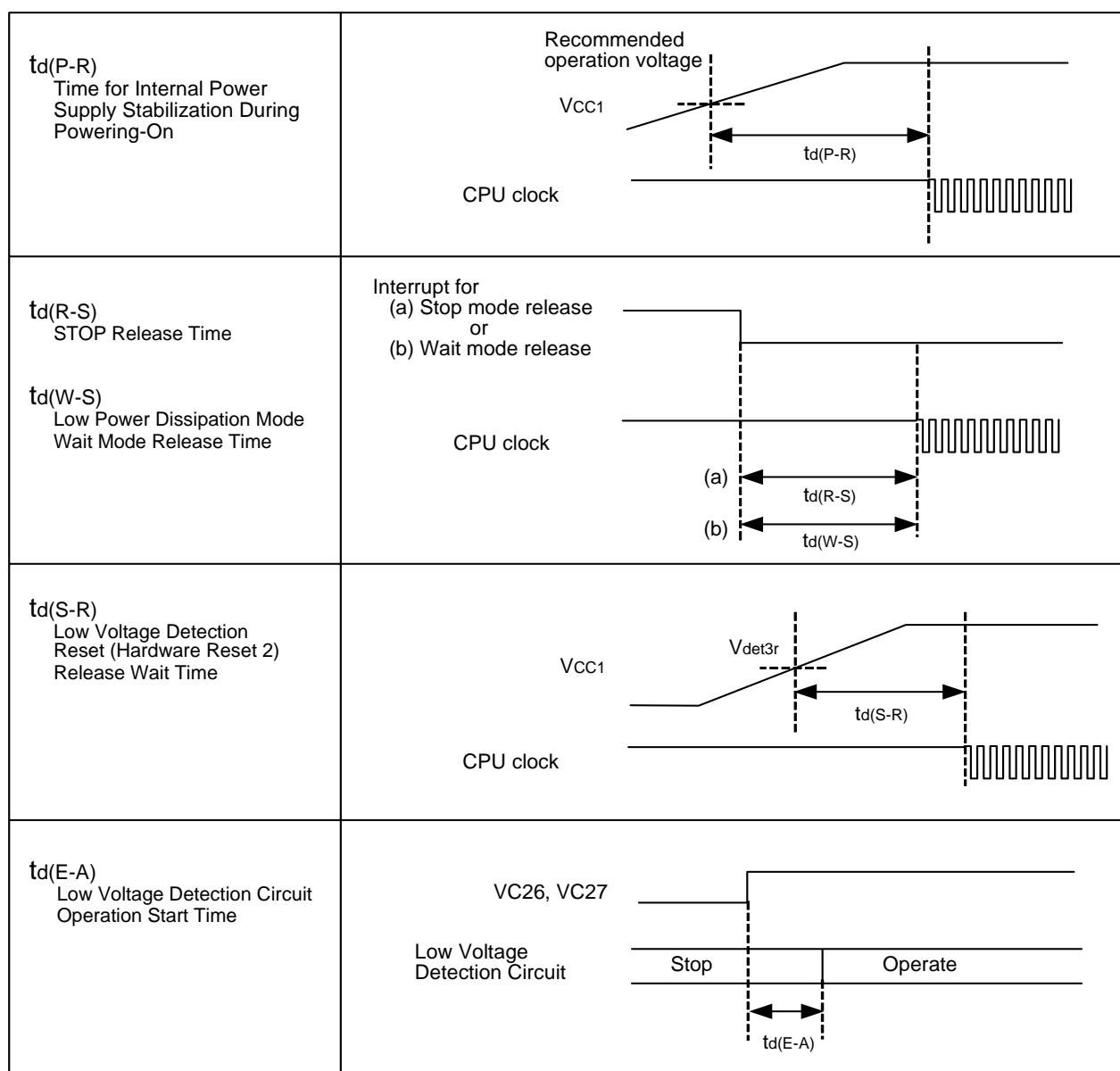


Figure 5.1 Power Supply Circuit Timing Diagram

$$V_{CC1}=V_{CC2}=5V$$

Table 5.11 Electrical Characteristics (1) (1)

Symbol	Parameter		Measuring Condition	Standard			Unit
				Min.	Typ.	Max.	
VOH	HIGH Output Voltage (3)	P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P14_0, P14_1	IOH=−5mA	VCC1−2.0		VCC1	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P12_0 to P12_7, P13_0 to P13_7	IOH=−5mA (2)	VCC2−2.0		VCC2	
VOH	HIGH Output Voltage (3)	P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P14_0, P14_1	OH=−200μA	VCC1−0.3		VCC1	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P12_0 to P12_7, P13_0 to P13_7	IOH=−200μA (2)	VCC2−0.3		VCC2	
VOH	HIGH Output Voltage XOUT	HIGHPOWER	IOH=−1mA	VCC1−2.0		VCC1	V
		LOWPOWER	IOH=−0.5mA	VCC1−2.0		VCC1	
	HIGH Output Voltage XCOUT	HIGHPOWER	With no load applied		2.5		V
		LOWPOWER	With no load applied		1.6		
VOL	LOW Output Voltage (3)	P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P14_0, P14_1	IOL=5mA			2.0	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P12_0 to P12_7, P13_0 to P13_7	IOL=5mA (2)			2.0	
VOL	LOW Output Voltage (3)	P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P14_0, P14_1	IOL=200μA			0.45	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P12_0 to P12_7, P13_0 to P13_7	IOL=200μA (2)			0.45	
VOL	LOW Output Voltage XOUT	HIGHPOWER	IOL=1mA			2.0	V
		LOWPOWER	IOL=0.5mA			2.0	
	LOW Output Voltage XCOUT	HIGHPOWER	With no load applied		0		V
		LOWPOWER	With no load applied		0		
VT+−VT−	Hysteresis	HOLD, RDY, TA0IN to TA4IN, TB0IN to TB5IN, INT0 to INT5, NMI, ADTRG, CTS0 to CTS2, CLK0 to CLK4, TA0OUT to TA4OUT, KI0 to KI3, RXD0 to RXD2, SCL0 to SCL2, SDA0 to SDA2, SIN3, SIN4		0.2		1.0	V
VT+−VT−	Hysteresis	RESET		0.2		2.5	V
I _{IH}	HIGH Input Current (3)	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1, XIN, RESET, CNVSS, BYTE	VI=5V			5.0	μA
I _{IL}	LOW Input Current (3)	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1, XIN, RESET, CNVSS, BYTE	VI=0V			−5.0	μA
RPULLUP	Pull-Up Resistance (3)	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1	VI=0V	30	50	170	kΩ
R _{I_{XIN}}	Feedback Resistance XIN				1.5		MΩ
R _{I_{XCIN}}	Feedback Resistance XCIN				15		MΩ
V _{RAM}	RAM Retention Voltage		At stop mode	2.0			V

NOTES:

1. Referenced to VCC1=VCC2=4.2 to 5.5V, VSS = 0V at T_{opr} = −20 to 85°C / −40 to 85°C, f(BCLK)=24MHz unless otherwise specified.
2. Where the product is used at VCC1 = 5 V and VCC2 = 3 V, refer to the 3 V version value for the pin specified value on VCC2 port side.
3. There is no external connections for port P1_0 to P1_7, P4_4 to P4_7, P7_2 to P7_5 and P9_1 in 80-pin version.

Table 5.12 Electrical Characteristics (2) ⁽¹⁾

Symbol	Parameter		Measuring Condition		Standard			Unit
					Min.	Typ.	Max.	
Icc	Power Supply Current (Vcc1=Vcc2=4.0V to 5.5V)	In single-chip mode, the output pins are open and other pins are Vss	Mask ROM	f(BCLK)=24MHz No division, PLL operation		14	20	mA
				No division, On-chip oscillation		1		mA
			Flash Memory	f(BCLK)=24MHz, No division, PLL operation		18	27	mA
				No division, On-chip oscillation		1.8		mA
			Flash Memory Program	f(BCLK)=10MHz, VCC1=5.0V		15		mA
			Flash Memory Erase	f(BCLK)=10MHz, VCC1=5.0V		25		mA
			Mask ROM	f(XCIN)=32kHz Low power dissipation mode, ROM ⁽³⁾		25		μA
			Flash Memory	f(BCLK)=32kHz Low power dissipation mode, RAM ⁽³⁾		25		μA
				f(BCLK)=32kHz Low power dissipation mode, Flash Memory ⁽³⁾		420		μA
				On-chip oscillation, Wait mode		50		μA
			Mask ROM Flash Memory	f(BCLK)=32kHz Wait mode ⁽²⁾ , Oscillation capability High		7.5		μA
				f(BCLK)=32kHz Wait mode ⁽²⁾ , Oscillation capability Low		2.0		μA
				Stop mode Topr =25°C		0.8	3.0	μA
Idet4	Low Voltage Detection Dissipation Current ⁽⁴⁾					0.7	4	μA
Idet3	Reset Area Detection Dissipation Current ⁽⁴⁾					1.2	8	μA

NOTES:

1. Referenced to V_{CC1}=V_{CC2}=4.2 to 5.5V, V_{SS} = 0V at T_{opr} = -20 to 85°C / -40 to 85°C, f(BCLK)=24MHz unless otherwise specified.
2. With one timer operated using fC32.
3. This indicates the memory in which the program to be executed exists.
4. I_{det} is dissipation current when the following bit is set to "1" (detection circuit enabled).
I_{det4}: VC27 bit in the VCR2 register
I_{det3}: VC26 bit in the VCR2 register

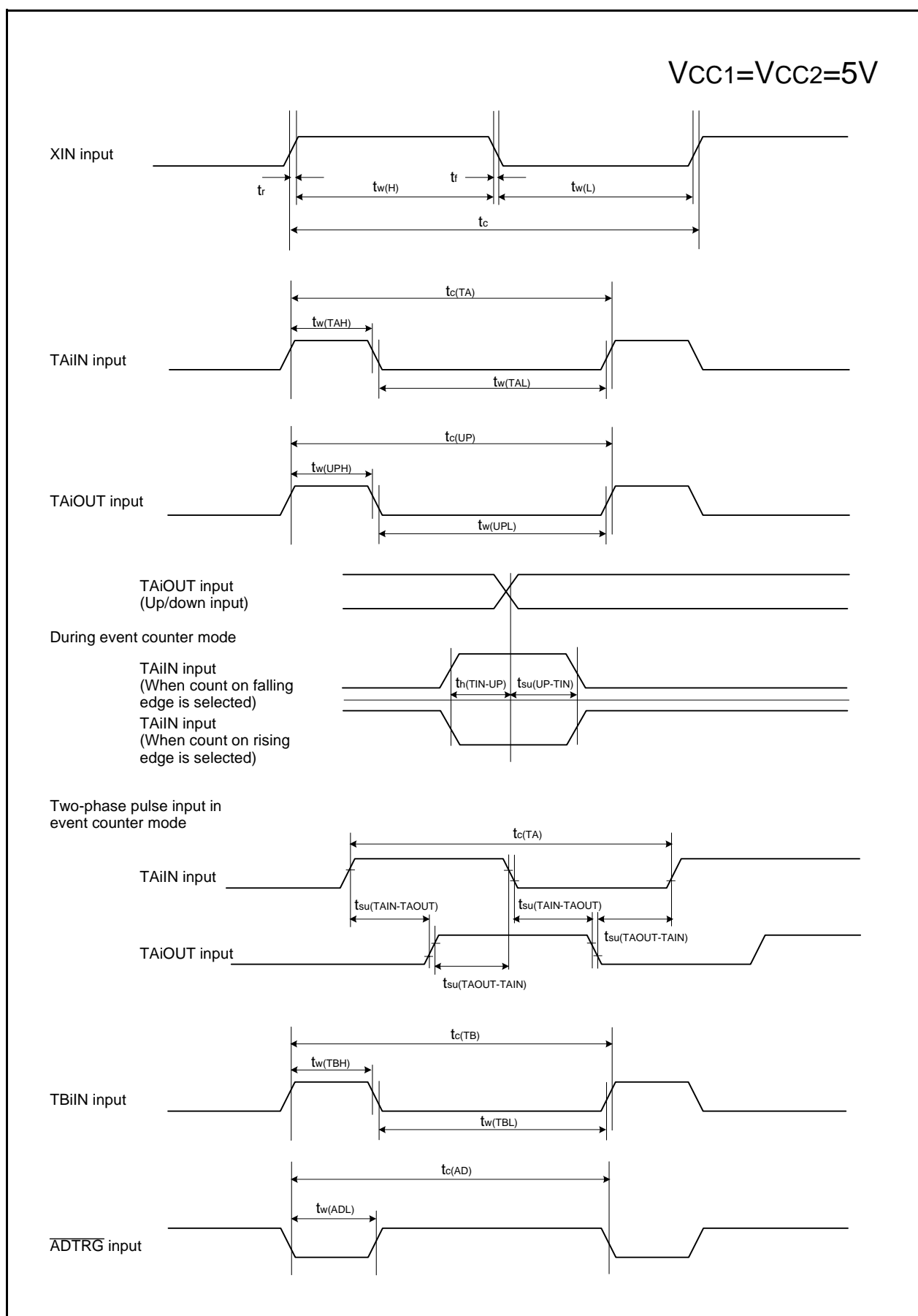
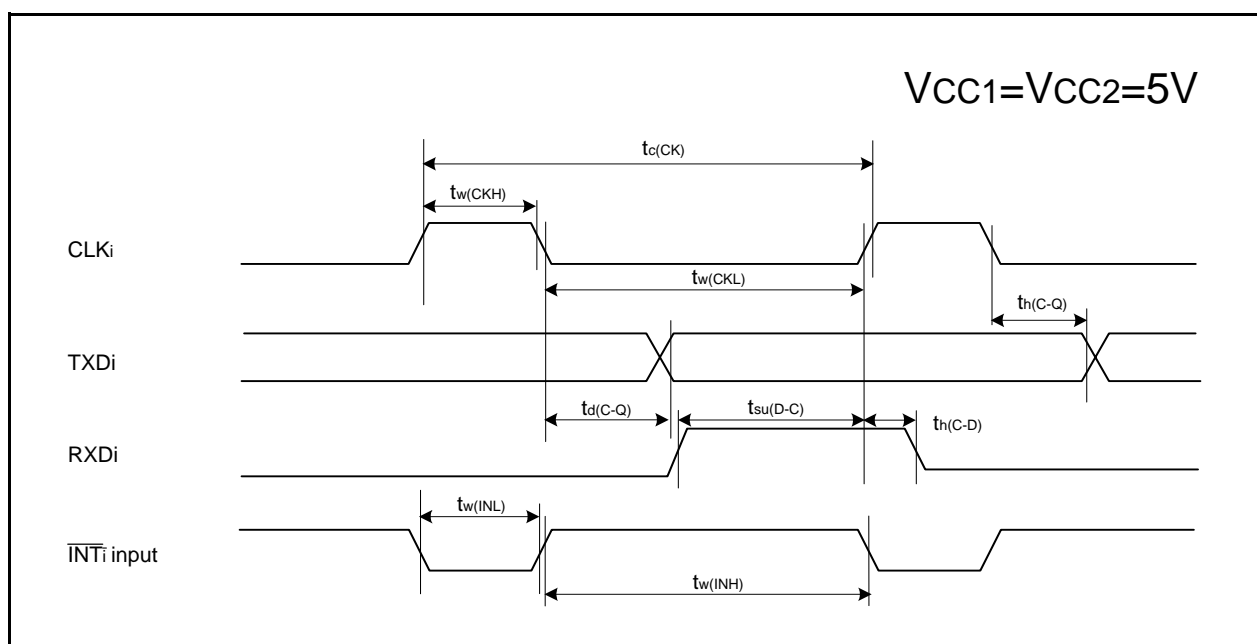


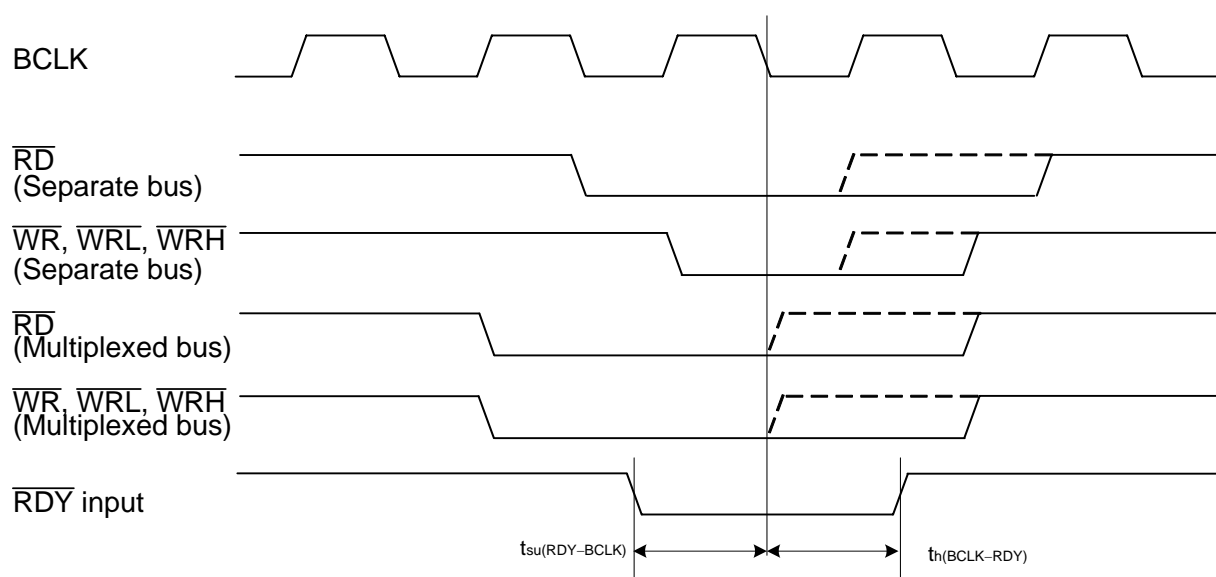
Figure 5.3 Timing Diagram (1)

**Figure 5.4** Timing Diagram (2)

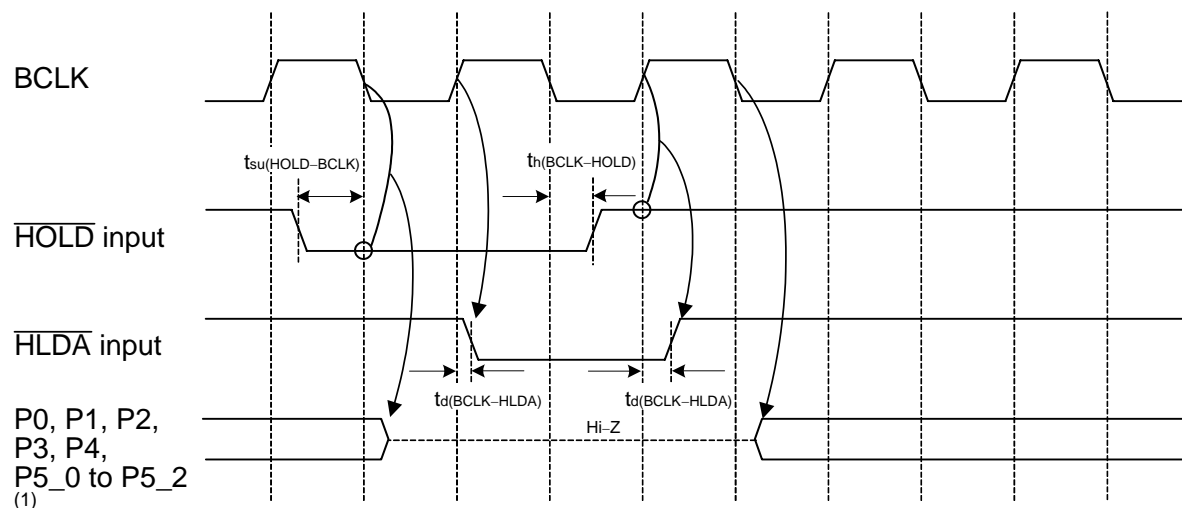
Memory Expansion Mode, Microprocessor Mode

(Effective for setting with wait)

$V_{CC1}=V_{CC2}=5V$



(Common to setting with wait and setting without wait)



NOTES:

1. These pins are set to high-impedance regardless of the input level of the BYTE pin, PM06 bit in PM0 register and PM11 bit in PM1 register.

- Measuring conditions :
- $V_{CC1}=V_{CC2}=5V$
- Input timing voltage : Determined with $V_{IL}=1.0V$, $V_{IH}=4.0V$
- Output timing voltage : Determined with $V_{OL}=2.5V$, $V_{OH}=2.5V$

Figure 5.5 Timing Diagram (3)

$$V_{CC1}=V_{CC2}=3V$$

Table 5.30 Electrical Characteristics (1) ⁽¹⁾

Symbol	Parameter		Measuring Condition	Standard			Unit
				Min.	Typ.	Max.	
VOH	HIGH Output Voltage ⁽³⁾	P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P14_0, P14_1	IOH=−1mA	VCC1−0.5		VCC1	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P12_0 to P12_7, P13_0 to P13_7	IOH=−1mA ⁽²⁾	VCC2−0.5		VCC2	
VOH	HIGH Output Voltage XOUT	HIGHPOWER	IOH=−0.1mA	VCC1−0.5		VCC1	V
		LOWPOWER	IOH=−50μA	VCC1−0.5		VCC1	
	HIGH Output Voltage XCOUT	HIGHPOWER	With no load applied		2.5		V
		LOWPOWER	With no load applied		1.6		
VOL	LOW Output Voltage ⁽³⁾	P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P14_0, P14_1	IOL=1mA			0.5	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P12_0 to P12_7, P13_0 to P13_7	IOL=1mA ⁽²⁾			0.5	
VOL	LOW Output Voltage XOUT	HIGHPOWER	IOL=0.1mA			0.5	V
		LOWPOWER	IOL=50μA			0.5	
	LOW Output Voltage XCOUT	HIGHPOWER	With no load applied		0		V
		LOWPOWER	With no load applied		0		
VT+−VT−	Hysteresis	HOLD, RDY, TA0IN to TA4IN, TB0IN to TB5IN, INT0 to INT5, NMI, ADTRG, CTS0 to CTS2, CLK0 to CLK4, TA0OUT to TA4OUT, KI0 to KI3, RXD0 to RXD2, SCL0 to SCL2, SDA0 to SDA2, SIN3, SIN4		0.2		0.8	V
VT+−VT−	Hysteresis	RESET		0.2	(0.7)	1.8	V
IiH	HIGH Input Current ⁽³⁾	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1, XIN, RESET, CNVSS, BYTE	VI=3V			4.0	μA
IiL	LOW Input Current ⁽³⁾	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1, XIN, RESET, CNVSS, BYTE	VI=0V			−4.0	μA
RPULLUP	Pull-Up Resistance ⁽³⁾	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1	VI=0V	50	100	500	kΩ
RfXIN	Feedback Resistance XIN				3.0		MΩ
RfXCIN	Feedback Resistance XCIN				25		MΩ
VRAM	RAM Retention Voltage		At stop mode	2.0			V

NOTES:

1. Referenced to VCC1 = VCC2 = 2.7 to 3.3V, VSS = 0V at T_{opr} = −20 to 85°C / −40 to 85°C, f(XIN)=10MHz no wait unless otherwise specified.
2. VCC1 for the port P6 to P11 and P14, and VCC2 for the port P0 to P5 and P12 to P13
3. There is no external connections for port P1_0 to P1_7, P4_4 to P4_7, P7_2 to P7_5 and P9_1 in 80-pin version.

Table 5.31 Electrical Characteristics (2) ⁽¹⁾

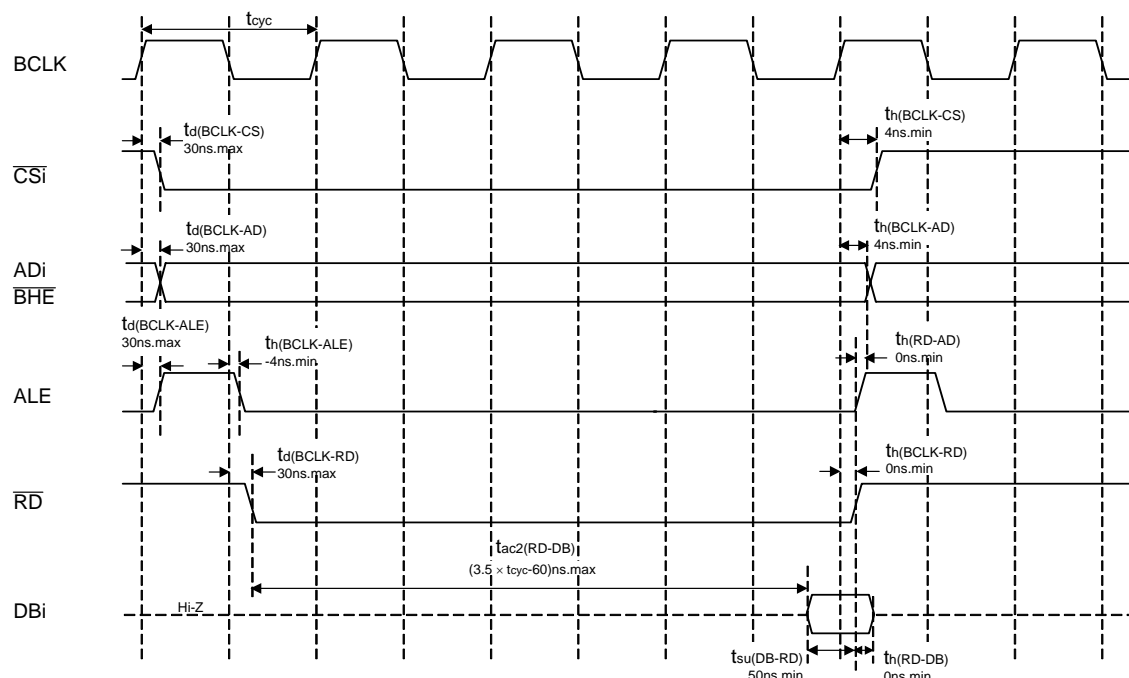
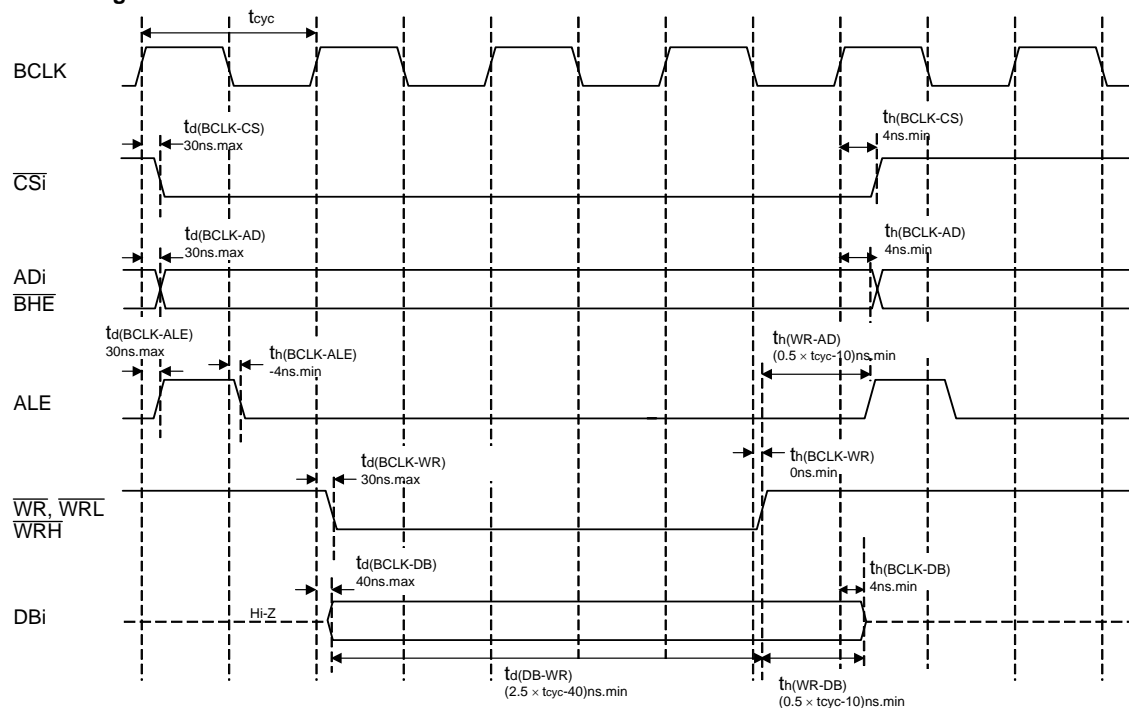
Symbol	Parameter		Measuring Condition		Standard			Unit
					Min.	Typ.	Max.	
Icc	Power Supply Current (Vcc1=Vcc2=2.7V to 3.6V)	In single-chip mode, the output pins are open and other pins are Vss	Mask ROM	f(BCLK)=10MHz No division		8	11	mA
				No division, On-chip oscillation		1		mA
			Flash Memory	f(BCLK)=10MHz, No division		8	13	mA
				No division, On-chip oscillation		1.8		mA
			Flash Memory Program	f(BCLK)=10MHz, VCC1=3.0V		12		mA
			Flash Memory Erase	f(BCLK)=10MHz, VCC1=3.0V		22		mA
			Mask ROM	f(XCIN)=32kHz Low power dissipation mode, ROM ⁽³⁾		25		μA
			Flash Memory	f(BCLK)=32kHz Low power dissipation mode, RAM ⁽³⁾		25		μA
				f(BCLK)=32kHz Low power dissipation mode, Flash Memory ⁽³⁾		420		μA
				On-chip oscillation, Wait mode		45		μA
			Mask ROM Flash Memory	f(BCLK)=32kHz Wait mode ⁽²⁾ , Oscillation capability High		6.0		μA
				f(BCLK)=32kHz Wait mode ⁽²⁾ , Oscillation capability Low		1.8		μA
				Stop mode Topr =25°C		0.7	3.0	μA
Idet4	Low Voltage Detection Dissipation Current ⁽⁴⁾					0.6	4	μA
Idet3	Reset Area Detection Dissipation Current ⁽⁴⁾					0.4	2	μA

NOTES:

1. Referenced to V_{CC1}=V_{CC2}=2.7 to 3.3V, V_{SS} = 0V at T_{opr} = -20 to 85°C / -40 to 85°C, f(BCLK)=10MHz unless otherwise specified.
2. With one timer operated using fC32.
3. This indicates the memory in which the program to be executed exists.
4. I_{det} is dissipation current when the following bit is set to "1" (detection circuit enabled).
I_{det4}: VC27 bit in the VCR2 register
I_{det3}: VC26 bit in the VCR2 register

Memory Expansion Mode, Microprocessor Mode
 (for 3-wait setting and external area access)

$$V_{CC1} = V_{CC2} = 3V$$

Read timing

Write timing


$$t_{cyc} = \frac{1}{f(BCLK)}$$

Measuring conditions

- $V_{CC1}=V_{CC2}=3V$
- Input timing voltage : $V_{IL}=0.6V$, $V_{IH}=2.4V$
- Output timing voltage : $V_{OL}=1.5V$, $V_{OH}=1.5V$

Figure 5.19 Timing Diagram (7)

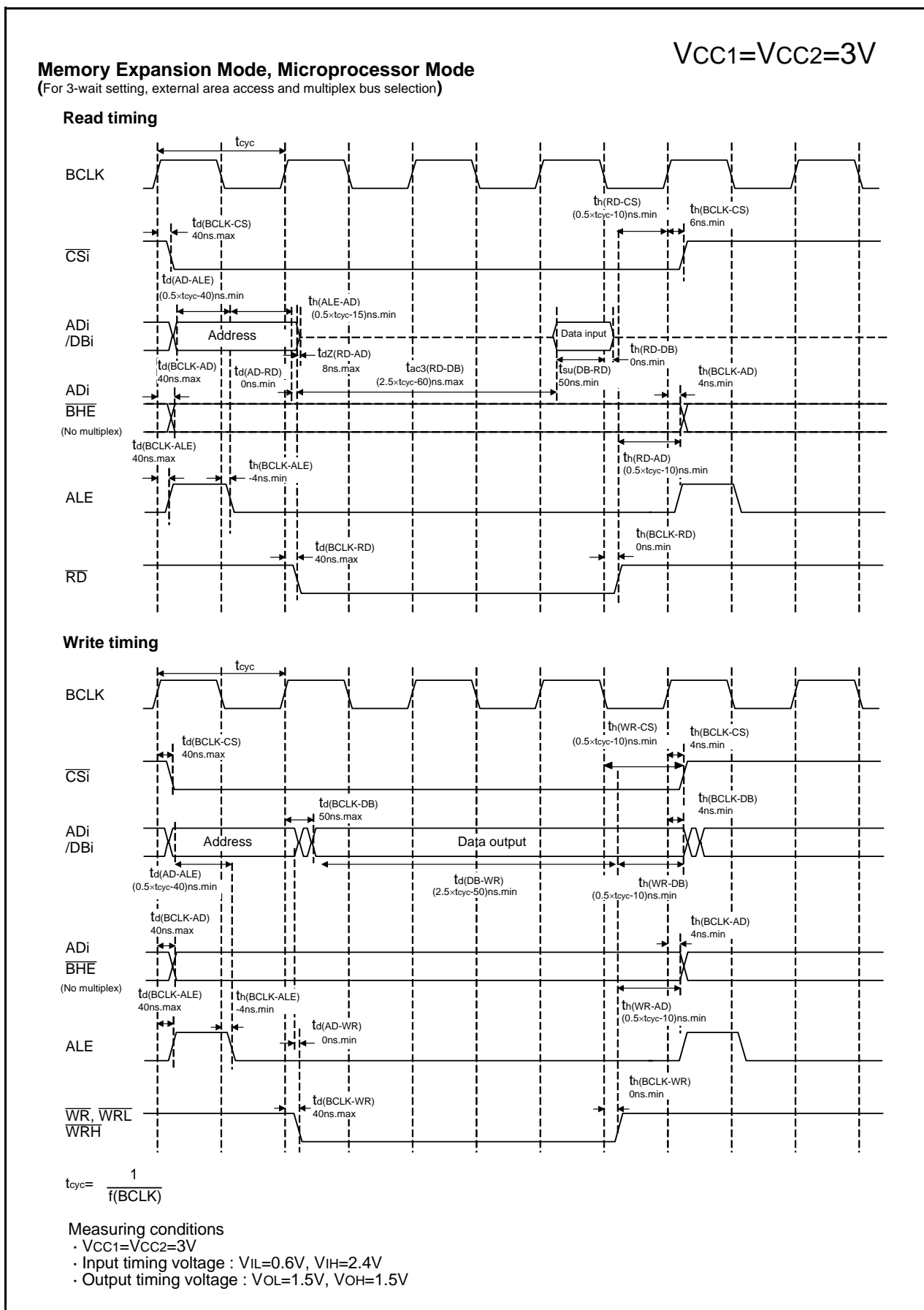


Figure 5.21 Timing Diagram (9)

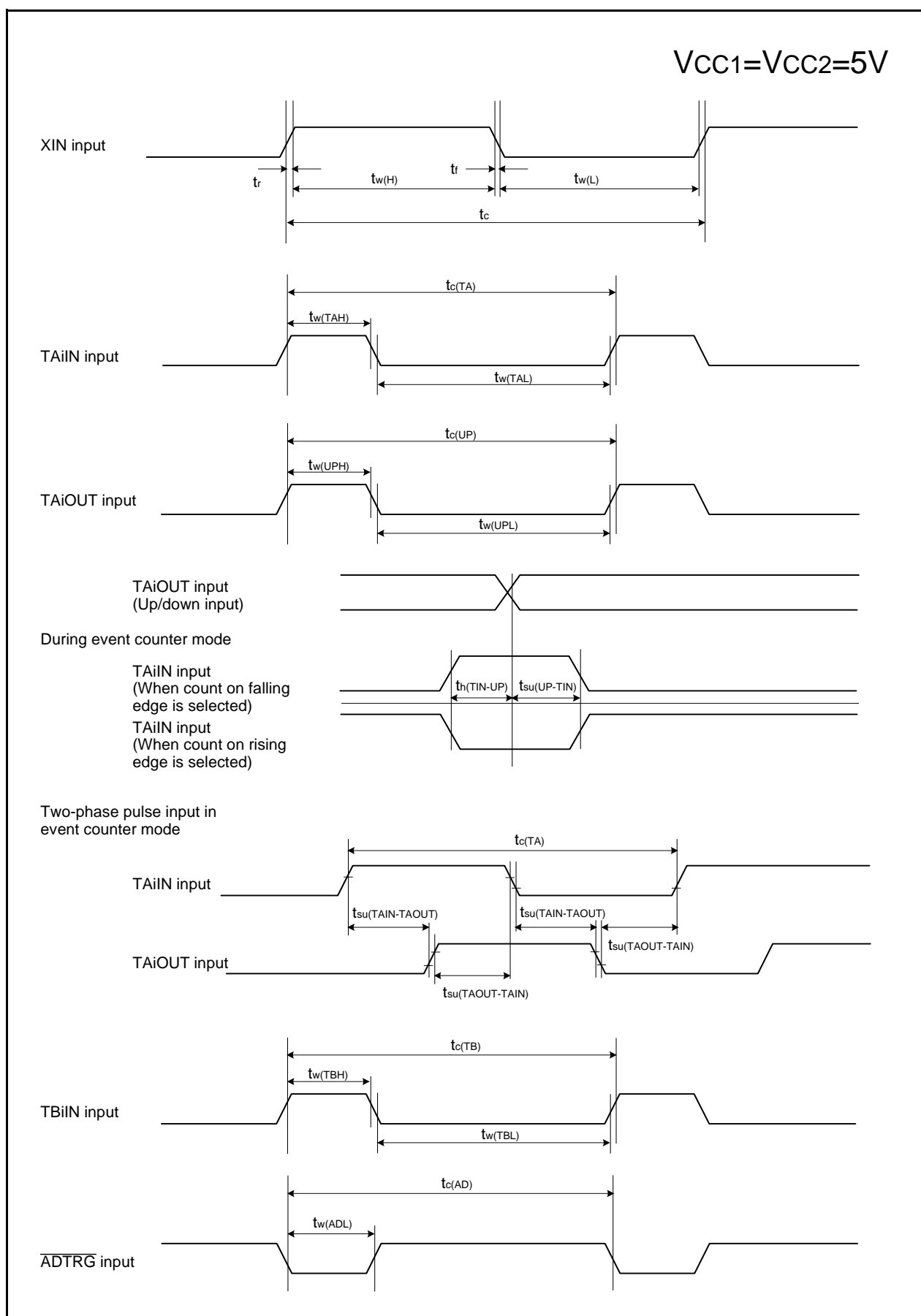


Figure 5.24 Timing Diagram (1)

REVISION HISTORY		M16C/62P Group (M16C/62P, M16C/62PT) Hardware Manual	
Rev.	Date	Description	
		Page	Summary
		33 34,74 36 38,55 41 41-43, 58-60 44 47-48 49-50 52 53 58 61 64-65 66-67 69 70-85	Table 5.4 A-D Conversion Characteristics is revised. Table 5.5 D-A Conversion Characteristics revised. Table 5.6 to 5.7 and table 5.54 to 5.55 are revised. Table 5.11 is revised. Table 5.14 and 5.33 HLDA output deley time is deleted. Figure 5.1 is partly revised. Table 5.27 to 5.29 and table 5.46 to 48 HLDA output deley time is added. Figure 5.2 Timing Diagram (1) XIN input is added. Figure 5.5 to 5.6 Read timing DB → DBi Figure 5.7 to 5.8 Write timing DB → DBi Figure 5.10 DB → DBi Table 5.30 is revised. Figure 5.11 is partly revised. Figure 5.12 Timing Diagram (1) XIN input is added. Figure 5.15 to 5.16 Read timing DB → DBi Figure 5.17 to 5.18 Write timing DB → DBi Figure 5.20 DB → DBi Electrical Characteristics (M16C/62PT) is added.
2.10	Nov 07, 2003	8-9 23 71 72	Table 1.5 to 1.7 Product List is partly revised. Note 1 is deleted. Table 3.1 is revised. Table 5.50 is revised. Table 5.51 is deleted.
2.11	Jan 06, 2004	16 17-18 31	Table 1.9 NOTE 3 VCC1 VCC2 → VCC1 > VCC2 Table 1.10 to 1.11 NOTE 1 VCC1 VCC2 → VCC1 > VCC2 Table 5.2 Power Supply Ripple Allowable Frequency Unit MHz → kHz
2.30	Sep 01, 2004	12 18, 20 19,21 24 25 33 34 35 37	Table 1.9 and Figure 1.5 are added. Table 1.11 to 1.13 are revised. Table 1.12 to 1.14 are revised. Figure 3.1 is partly revised. Note 3 is added. Note 6 is added. Table 5.3 is revised. Note 2 in Table 5.4 is added. Table 5.5 to 5.6 is partly revised. Table 5.8 is revised. Table 5.9 is revised. Table 5.11 is revised.

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