Renesas Electronics America Inc - M30625FGPGP#U7C Datasheet

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	M16C/60
Core Size	16-Bit
Speed	24MHz
Connectivity	I²C, IEBus, UART/USART
Peripherals	DMA, WDT
Number of I/O	113
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	20K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 26x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	128-LQFP
Supplier Device Package	128-LFQFP (14x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/m30625fgpgp-u7c

Table 1.2 Performance Outline of M16C/62P Group (M16C/62P, M16C/62PT)(100-pin version)

	Item	Performance	
		M16C/62P	M16C/62PT(4)
CPU	Number of Basic Instructions	91 instructions	
	Minimum Instruction Execution Time	41.7ns(f(BCLK)=24MHz, VCC1=3.3 to 5.5V) 100ns(f(BCLK)=10MHz, VCC1=2.7 to 5.5V)	41.7ns(f(BCLK)=24MHz, VCC1=4.0 to 5.5V)
	Operating Mode	Single-chip, memory expansion and microprocessor mode	Single-chip
	Address Space	1 Mbyte (Available to 4 Mbytes by memory space expansion function)	1 Mbyte
	Memory Capacity	See **Table 1.4 to 1.7 Product List**	
Peripheral Function	Port	Input/Output : 87 pins, Input : 1 pin	
	Multifunction Timer	Timer A : 16 bits x 5 channels, Timer B : 16 bits x 6 channels, Three phase motor control circuit	
	Serial Interface	3 channels Clock synchronous, UART, I2C bus(1), IEBus(2) 2 channels Clock synchronous	
	A/D Converter	10-bit A/D converter: 1 circuit, 26 channels	
	D/A Converter	8 bits x 2 channels	
	DMAC	2 channels	
	CRC Calculation Circuit	CCITT-CRC	
	Watchdog Timer	15 bits x 1 channel (with prescaler)	
	Interrupt	Internal: 29 sources, External: 8 sources, Software: 4 sources, Priority level: 7 levels	
	Clock Generation Circuit	4 circuits Main clock generation circuit (*), Subclock generation circuit (*), On-chip oscillator, PLL synthesizer (*)Equipped with a built-in feedback resistor.	
	Oscillation Stop Detection Function	Stop detection of main clock oscillation, re-oscillation detection function	
	Voltage Detection Circuit	Available (option (5))	Absent
Electric Characteristics	Supply Voltage	VCC1=3.0 to 5.5 V, VCC2=2.7V to VCC1 (f(BCLK=24MHz) VCC1=2.7 to 5.5 V, VCC2=2.7V to VCC1 (f(BCLK=10MHz)	VCC1=VCC2=4.0 to 5.5V (f(BCLK=24MHz)
	Power Consumption	14 mA (VCC1=VCC2=5V, f(BCLK)=24MHz) 8 mA (VCC1=VCC2=3V, f(BCLK)=10MHz) 1.8µA (VCC1=VCC2=3V, f(XCIN)=32kHz, wait mode) 0.7µA (VCC1=VCC2=3V, stop mode)	14 mA (VCC1=VCC2=5V, f(BCLK)=24MHz) 2.0µA (VCC1=VCC2=5V, f(XCIN)=32kHz, wait mode) 0.8µA (VCC1=VCC2=5V, stop mode)
Flash memory version	Program/Erase Supply Voltage	3.3±0.3 V or 5.0±0.5 V	5.0±0.5 V
	Program and Erase Endurance	100 times (all area) or 1,000 times (user ROM area without block A and block 1) / 10,000 times (block A, block 1) (3)	
Operating Ambient Temperature		-20 to 85°C, -40 to 85°C (3)	T version : -40 to 85°C V version : -40 to 125°C
Package		100-pin plastic mold QFP, LQFP	

NOTES:
1. I2C bus is a registered trademark of Koninklijke Philips Electronics N. V.
2. IEBus is a registered trademark of NEC Electronics Corporation.
3. See **Table 1.8 and 1.9 Product Code** for the program and erase endurance, and operating ambient temperature.
   In addition 1,000 times/10,000 times are under development as of Jul., 2005. Please inquire about a release schedule.
4. Use the M16C/62PT on VCC1=VCC2
5. All options are on request basis.

Table 1.3 Performance Outline of M16C/62P Group (M16C/62P, M16C/62PT)(80-pin version)

	Item	Performance	
		M16C/62P	M16C/62PT(4)
CPU	Number of Basic Instructions	91 instructions	
	Minimum Instruction Execution Time	41.7ns(f(BCLK)=24MHz, VCC1=3.3 to 5.5V) 100ns(f(BCLK)=10MHz, VCC1=2.7 to 5.5V)	41.7ns(f(BCLK)=24MHz, VCC1=4.0 to 5.5V)
	Operating Mode	Single-chip mode	
	Address Space	1 Mbyte	
	Memory Capacity	See **Table 1.4 to 1.7 Product List**	
Peripheral Function	Port	Input/Output : 70 pins, Input : 1 pin	
	Multifunction Timer	Timer A : 16 bits x 5 channels (Timer A1 and A2 are internal timer), Timer B : 16 bits x 6 channels (Timer B1 is internal timer)	
	Serial Interface	2 channels Clock synchronous, UART, I2C bus(1), IEBus(2) 1 channel Clock synchronous, I2C bus(1), IEBus(2) 2 channels Clock synchronous (1 channel is only transmission)	
	A/D Converter	10-bit A/D converter: 1 circuit, 26 channels	
	D/A Converter	8 bits x 2 channels	
	DMAC	2 channels	
	CRC Calculation Circuit	CCITT-CRC	
	Watchdog Timer	15 bits x 1 channel (with prescaler)	
	Interrupt	Internal: 29 sources, External: 5 sources, Software: 4 sources, Priority level: 7 levels	
	Clock Generation Circuit	4 circuits Main clock generation circuit (*), Subclock generation circuit (*), On-chip oscillator, PLL synthesizer (*)Equipped with a built-in feedback resistor.	
	Oscillation Stop Detection Function	Stop detection of main clock oscillation, re-oscillation detection function	
	Voltage Detection Circuit	Available (option (4))	Absent
Electric Characteristics	Supply Voltage	VCC1=3.0 to 5.5 V, (f(BCLK=24MHz) VCC1=2.7 to 5.5 V, (f(BCLK=10MHz)	VCC1=4.0 to 5.5V, (f(BCLK=24MHz)
	Power Consumption	14 mA (VCC1=5V, f(BCLK)=24MHz) 8 mA (VCC1=3V, f(BCLK)=10MHz) 1.8μA (VCC1=3V, f(XCIN)=32kHz, wait mode) 0.7μA (VCC1=3V, stop mode)	14 mA (VCC1=5V, f(BCLK)=24MHz) 2.0μA (VCC1=5V, f(XCIN)=32kHz, wait mode) 0.8μA (VCC1=5V, stop mode)
Flash memory version	Program/Erase Supply Voltage	3.3 ± 0.3V or 5.0 ± 0.5V	5.0 ± 0.5V
	Program and Erase Endurance	100 times (all area) or 1,000 times (user ROM area without block A and block 1) / 10,000 times (block A, block 1) (3)	
Operating Ambient Temperature		-20 to 85°C, -40 to 85°C (3)	T version : -40 to 85°C V version : -40 to 125°C
Package		80-pin plastic mold QFP	

NOTES:
1. I2C bus is a registered trademark of Koninklijke Philips Electronics N. V.
2. IEBus is a registered trademark of NEC Electronics Corporation.
3. See **Table 1.8 and 1.9 Product Code** for the program and erase endurance, and operating ambient temperature.
   In addition 1,000 times/10,000 times are under development as of Jul., 2005. Please inquire about a release schedule.
4. All options are on request basis.

Table 1.8 Product Code of Flash Memory version and ROMless version for M16C/62P

	Product Code	Package	Internal ROM (User ROM Area Without Block A, Block 1)		Internal ROM (Block A, Block 1)		Operating Ambient Temperature
			Program and Erase Endurance	Temperature Range	Program and Erase Endurance	Temperature Range	
Flash memory Version	D3	Lead-included	100	0°C to 60°C	100	0°C to 60°C	-40°C to 85°C
	D5						-20°C to 85°C
	D7		1,000		10,000	-40°C to 85°C	-40°C to 85°C
	D9					-20°C to 85°C	-20°C to 85°C
	U3	Lead-free	100		100	0°C to 60°C	-40°C to 85°C
	U5						-20°C to 85°C
	U7		1,000		10,000	-40°C to 85°C	-40°C to 85°C
	U9					-20°C to 85°C	-20°C to 85°C
ROM-less version	D3	Lead-included	–	–	–	–	-40°C to 85°C
	D5						-20°C to 85°C
	U3	Lead-free	–	–	–	–	-40°C to 85°C
	U5						-20°C to 85°C

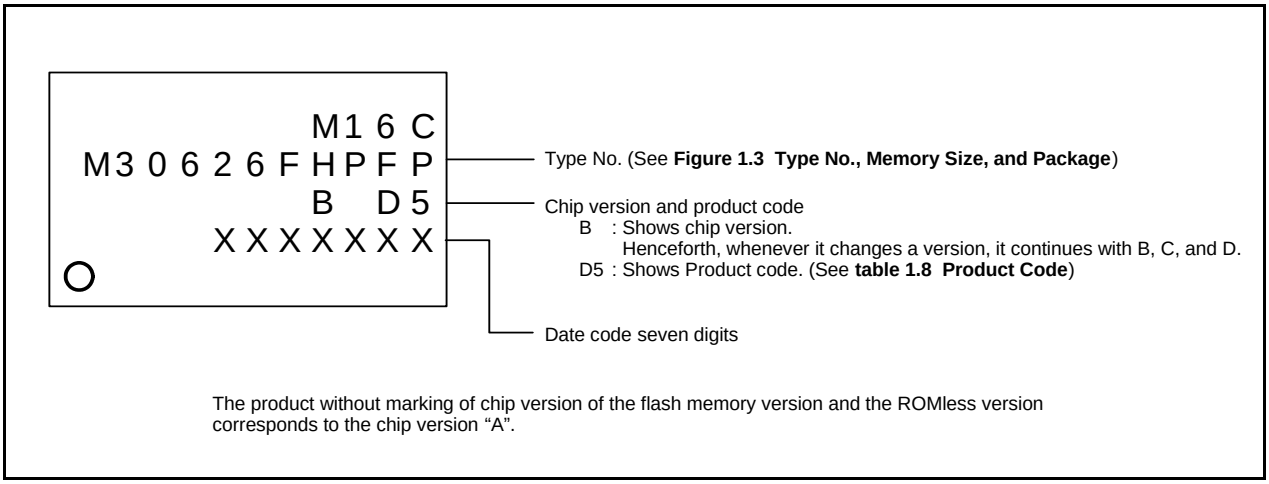


Figure 1.4 Marking Diagram of Flash Memory version and ROM-less version for M16C/62P (Top View)

1.5 Pin Configuration

Figures 1.6 to 1.9 show the Pin Configuration (Top View).

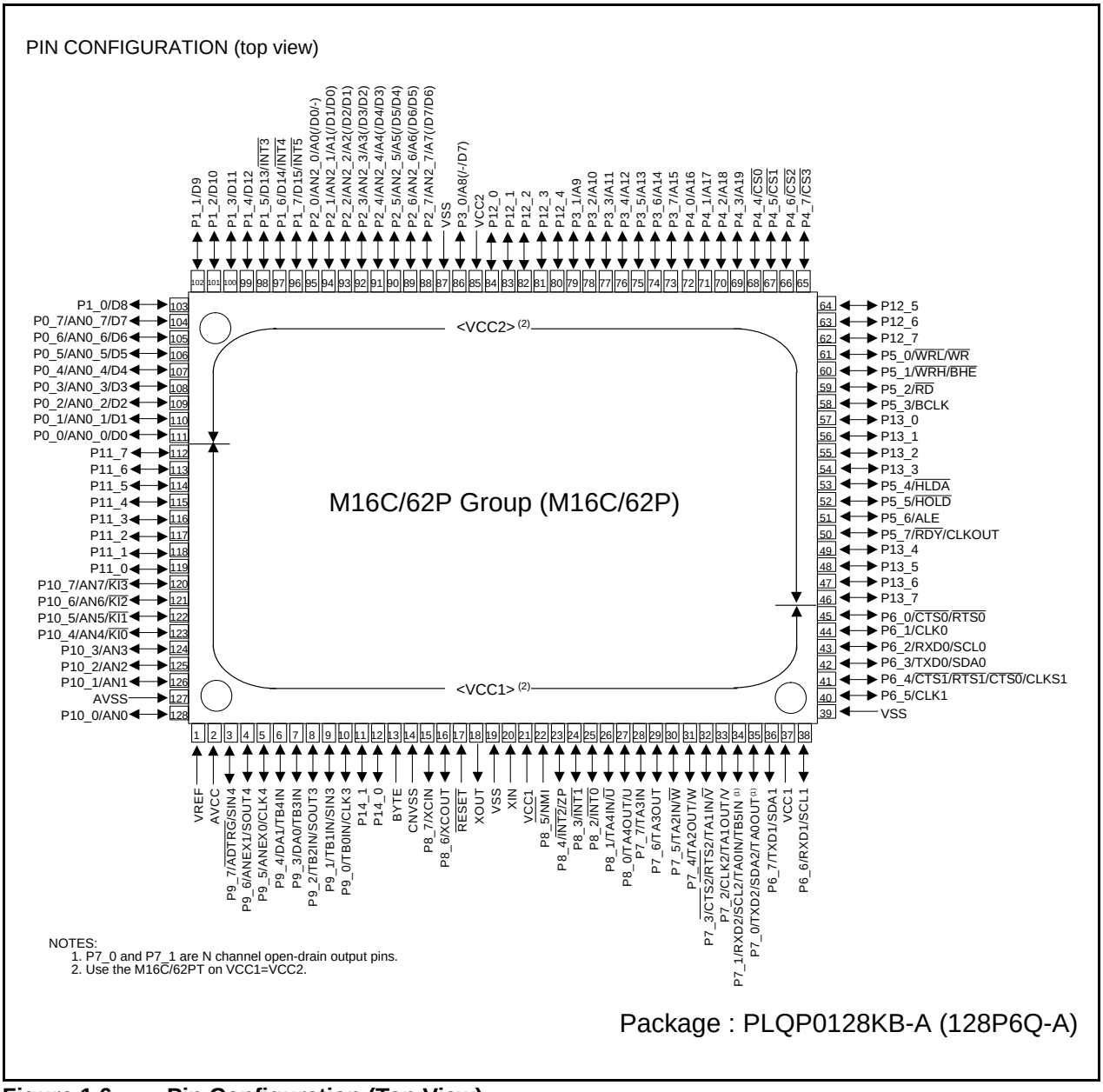


Figure 1.6 Pin Configuration (Top View)

Table 1.11 Pin Characteristics for 128-Pin Package (2)

Pin No.	Control Pin	Port	Interrupt Pin	Timer Pin	UART Pin	Analog Pin	Bus Control Pin
51		P5_6					ALE
52		P5_5					$\overline{\text{HOLD}}$
53		P5_4					$\overline{\text{HLDA}}$
54		P13_3					
55		P13_2					
56		P13_1					
57		P13_0					
58		P5_3					BCLK
59		P5_2					$\overline{\text{RD}}$
60		P5_1					$\overline{\text{WRH}}$/$\overline{\text{BHE}}$
61		P5_0					$\overline{\text{WRL}}$/$\overline{\text{WR}}$
62		P12_7					
63		P12_6					
64		P12_5					
65		P4_7					$\overline{\text{CS3}}$
66		P4_6					$\overline{\text{CS2}}$
67		P4_5					$\overline{\text{CS1}}$
68		P4_4					$\overline{\text{CS0}}$
69		P4_3					A19
70		P4_2					A18
71		P4_1					A17
72		P4_0					A16
73		P3_7					A15
74		P3_6					A14
75		P3_5					A13
76		P3_4					A12
77		P3_3					A11
78		P3_2					A10
79		P3_1					A9
80		P12_4					
81		P12_3					
82		P12_2					
83		P12_1					
84		P12_0					
85	VCC2						
86		P3_0					A8(/-/D7)
87	VSS						
88		P2_7				AN2_7	A7(/D7/D6)
89		P2_6				AN2_6	A6(/D6/D5)
90		P2_5				AN2_5	A5(/D5/D4)
91		P2_4				AN2_4	A4(/D4/D3)
92		P2_3				AN2_3	A3(/D3/D2)
93		P2_2				AN2_2	A2(/D2/D1)
94		P2_1				AN2_1	A1(/D1/D0)
95		P2_0				AN2_0	A0(/D0/-)
96		P1_7	$\overline{\text{INT5}}$				D15
97		P1_6	$\overline{\text{INT4}}$				D14
98		P1_5	$\overline{\text{INT3}}$				D13
99		P1_4					D12
100		P1_3					D11

Table 1.20 Pin Description (80-pin Version) (1) (1)

Signal Name	Pin Name	I/O Type	Power Supply	Description
Power supply input	VCC1, VSS	I	–	Apply 2.7 to 5.5 V to the VCC1 pin and 0 V to the VSS pin. (1, 2)
Analog power supply input	AVCC AVSS	I	VCC1	Applies the power supply for the A/D converter. Connect the AVCC pin to VCC1. Connect the AVSS pin to VSS.
Reset input	$\overline{\text{RESET}}$	I	VCC1	The microcomputer is in a reset state when applying "L" to the this pin.
CNVSS	CNVSS (BYTE)	I	VCC1	Switches processor mode. Connect this pin to VSS to when after a reset to start up in single-chip mode. Connect this pin to VCC1 to start up in microprocessor mode. As for the BYTE pin of the 80-pin versions, pull-up processing is performed within the microcomputer.
Main clock input	XIN	I	VCC1	I/O pins for the main clock generation circuit. Connect a ceramic resonator or crystal oscillator between XIN and XOUT (3). To use the external clock, input the clock from XIN and leave XOUT open.
Main clock output	XOUT	O	VCC1	
Sub clock input	XCIN	I	VCC1	I/O pins for a sub clock oscillation circuit. Connect a crystal oscillator between XCIN and XCOUT (3). To use the external clock, input the clock from XCIN and leave XCOUT open.
Sub clock output	XCOUT	O	VCC1	
Clock output	CLKOUT	O	VCC2	The clock of the same cycle as fC, f8, or f32 is outputted.
$\overline{\text{INT}}$ interrupt input	$\overline{\text{INT0}}$ to $\overline{\text{INT2}}$	I	VCC1	Input pins for the $\overline{\text{INT}}$ interrupt.
$\overline{\text{NMI}}$ interrupt input	$\overline{\text{NMI}}$	I	VCC1	Input pin for the $\overline{\text{NMI}}$ interrupt.
Key input interrupt input	$\overline{\text{KI0}}$ to $\overline{\text{KI3}}$	I	VCC1	Input pins for the key input interrupt.
Timer A	TA0OUT, TA3OUT, TA4OUT	I/O	VCC1	These are Timer A0,Timer A3 and Timer A4 I/O pins. (however, output of TA0OUT for the N-channel open drain output.)
	TA0IN, TA3IN, TA4IN	I	VCC1	These are Timer A0, Timer A3 and Timer A4 input pins.
	ZP	I	VCC1	Input pin for the Z-phase.
Timer B	TB0IN, TB2IN to TB5IN	I	VCC1	These are Timer B0, Timer B2 to Timer B5 input pins.
Serial interface	$\overline{\text{CTS0}}$ to $\overline{\text{CTS1}}$	I	VCC1	These are send control input pins.
	$\overline{\text{RTS0}}$ to $\overline{\text{RTS1}}$	O	VCC1	These are receive control output pins.
	CLK0, CLK1, CLK3, CLK4	I/O	VCC1	These are transfer clock I/O pins.
	RXD0 to RXD2	I	VCC1	These are serial data input pins.
	SIN4	I	VCC1	This is serial data input pin.
	TXD0 to TXD2	O	VCC1	These are serial data output pins. (however, output of TXD2 for the N-channel open drain output.)
	SOUT3, SOUT4	O	VCC1	These are serial data output pins.
	CLKS1	O	VCC1	This is output pin for transfer clock output from multiple pins function.
I^2C mode	SDA0 to SDA2	I/O	VCC1	These are serial data I/O pins. (however, output of SDA2 for the N-channel open drain output.)
	SCL0 to SCL2	I/O	VCC1	These are transfer clock I/O pins. (however, output of SCL2 for the N-channel open drain output.)

I : Input O : Output I/O : Input and output

NOTES:
1. In this manual, hereafter, VCC refers to VCC1 unless otherwise noted.
2. In M16C/62PT, apply 4.0 to 5.5 V to the VCC1 pin.
3. Ask the oscillator maker the oscillation characteristic.

Table 4.4 SFR Information (4) (1)

Address	Register	Symbol	After Reset
0340h	Timer B3, 4, 5 Count Start Flag	TBSR	000XXXXXb
0341h			
0342h	Timer A1-1 Register	TA11	XXh
0343h			XXh
0344h	Timer A2-1 Register	TA21	XXh
0345h			XXh
0346h	Timer A4-1 Register	TA41	XXh
0347h			XXh
0348h	Three-Phase PWM Control Register 0	INVC0	00h
0349h	Three-Phase PWM Control Register 1	INVC1	00h
034Ah	Three-Phase Output Buffer Register 0	IDB0	00h
034Bh	Three-Phase Output Buffer Register 1	IDB1	00h
034Ch	Dead Time Timer	DTT	XXh
034Dh	Timer B2 Interrupt Occurrence Frequency Set Counter	ICTB2	XXh
034Eh			
034Fh			
0350h	Timer B3 Register	TB3	XXh
0351h			XXh
0352h	Timer B4 Register	TB4	XXh
0353h			XXh
0354h	Timer B5 Register	TB5	XXh
0355h			XXh
0356h			
0357h			
0358h			
0359h			
035Ah			
035Bh	Timer B3 Mode Register	TB3MR	00XX0000b
035Ch	Timer B4 Mode Register	TB4MR	00XX0000b
035Dh	Timer B5 Mode Register	TB5MR	00XX0000b
035Eh	Interrupt Factor Select Register 2	IFSR2A	00XXXXXXb
035Fh	Interrupt Factor Select Register	IFSR	00h
0360h	SI/O3 Transmit/Receive Register	S3TRR	XXh
0361h			
0362h	SI/O3 Control Register	S3C	01000000b
0363h	SI/O3 Bit Rate Generator	S3BRG	XXh
0364h	SI/O4 Transmit/Receive Register	S4TRR	XXh
0365h			
0366h	SI/O4 Control Register	S4C	01000000b
0367h	SI/O4 Bit Rate Generator	S4BRG	XXh
0368h			
0369h			
036Ah			
036Bh			
036Ch	UART0 Special Mode Register 4	U0SMR4	00h
036Dh	UART0 Special Mode Register 3	U0SMR3	000X0X0Xb
036Eh	UART0 Special Mode Register 2	U0SMR2	X0000000b
036Fh	UART0 Special Mode Register	U0SMR	X0000000b
0370h	UART1 Special Mode Register 4	U1SMR4	00h
0371h	UART1 Special Mode Register 3	U1SMR3	000X0X0Xb
0372h	UART1 Special Mode Register 2	U1SMR2	X0000000b
0373h	UART1 Special Mode Register	U1SMR	X0000000b
0374h	UART2 Special Mode Register 4	U2SMR4	00h
0375h	UART2 Special Mode Register 3	U2SMR3	000X0X0Xb
0376h	UART2 Special Mode Register 2	U2SMR2	X0000000b
0377h	UART2 Special Mode Register	U2SMR	X0000000b
0378h	UART2 Transmit/Receive Mode Register	U2MR	00h
0379h	UART2 Bit Rate Generator	U2BRG	XXh
037Ah	UART2 Transmit Buffer Register	U2TB	XXh
037Bh			XXh
037Ch	UART2 Transmit/Receive Control Register 0	U2C0	00001000b
037Dh	UART2 Transmit/Receive Control Register 1	U2C1	00000010b
037Eh	UART2 Receive Buffer Register	U2RB	XXh
037Fh			XXh

NOTES:
1. The blank areas are reserved and cannot be accessed by users.

X : Nothing is mapped to this bit

Table 5.6 Flash Memory Version Electrical Characteristics (1) for 100 cycle products (D3, D5, U3, U5)

Symbol	Parameter		Standard			Unit
			Min.	Typ.	Max.	
–	Program and Erase Endurance (3)		100			cycle
–	Word Program Time (V_{CC1}=5.0V)			25	200	µs
–	Lock Bit Program Time			25	200	µs
–	Block Erase Time (V_{CC1}=5.0V)	4-Kbyte block		0.3	4	s
–		8-Kbyte block		0.3	4	s
–		32-Kbyte block		0.5	4	s
–		64-Kbyte block		0.8	4	s
–	Erase All Unlocked Blocks Time (2)				4×n	s
t_{PS}	Flash Memory Circuit Stabilization Wait Time				15	µs
–	Data Hold Time (5)		10			year

Table 5.7 Flash Memory Version Electrical Characteristics (6) for 10,000 cycle products (D7, D9, U7, U9) (Block A and Block 1 (7))

Symbol	Parameter		Standard			Unit
			Min.	Typ.	Max.	
–	Program and Erase Endurance (3, 8, 9)		10,000 (4)			cycle
–	Word Program Time (V_{CC1}=5.0V)			25		µs
–	Lock Bit Program Time			25		µs
–	Block Erase Time (V_{CC1}=5.0V)	4-Kbyte block		0.3		s
t_{PS}	Flash Memory Circuit Stabilization Wait Time				15	µs
–	Data Hold Time (5)		10			year

NOTES:
1. Referenced to V_{CC1}=4.5 to 5.5V, 3.0 to 3.6V at Topr = 0 to 60 °C (D3, D5, U3, U5) unless otherwise specified.
2. n denotes the number of block erases.
3. Program and Erase Endurance refers to the number of times a block erase can be performed.
   If the program and erase endurance is n (n=100, 1,000, or 10,000), each block can be erased n times.
   For example, if a 4 Kbytes block A is erased after writing 1 word data 2,048 times, each to a different address, this counts as one program and erase endurance. Data cannot be written to the same address more than once without erasing the block. (Rewrite prohibited)
4. Maximum number of E/W cycles for which operation is guaranteed.
5. Topr = -40 to 85 °C (D3, D7, U3, U7) / -20 to 85 °C (D5, D9, U5, U9).
6. Referenced to V_{CC1} = 4.5 to 5.5V, 3.0 to 3.6V at T_{opr} = -40 to 85 °C (D7, U7) / -20 to 85 °C (D9, U9) unless otherwise specified.
7. Table 5.7 applies for block A or block 1 program and erase endurance > 1,000. Otherwise, use Table 5.6.
8. To reduce the number of program and erase endurance when working with systems requiring numerous rewrites, write to unused word addresses within the block instead of rewrite. Erase block only after all possible addresses are used. For example, an 8-word program can be written 256 times maximum before erase becomes necessary.
   Maintaining an equal number of erasure between block A and block 1 will also improve efficiency. It is important to track the total number of times erasure is used.
9. Should erase error occur during block erase, attempt to execute clear status register command, then block erase command at least three times until erase error disappears.
10. Set the PM17 bit in the PM1 register to “1” (wait state) when executing more than 100 times rewrites (D7, D9, U7 and U9).
11. Customers desiring E/W failure rate information should contact their Renesas technical support representative.

Table 5.8 Flash Memory Version Program / Erase Voltage and Read Operation Voltage Characteristics (at T_{opr} = 0 to 60 °C(D3, D5, U3, U5), T_{opr} = -40 to 85 °C(D7, U7) / T_{opr} = -20 to 85 °C(D9, U9))

Flash Program, Erase Voltage	Flash Read Operation Voltage
V_{CC1} = 3.3 V ± 0.3 V or 5.0 V ± 0.5 V	V_{CC1}=2.7 to 5.5 V

Table 5.9 Low Voltage Detection Circuit Electrical Characteristics

Symbol	Parameter	Measuring Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{det4}	Low Voltage Detection Voltage (1)	V_{CC1}=0.8V to 5.5V	3.3	3.8	4.4	V
V_{det3}	Reset Level Detection Voltage (1, 2)		2.2	2.8	3.6	V
V_{det4}-V_{det3}	Electric potential difference of Low Voltage Detection and Reset Level Detection		0.3			V
V_{det3s}	Low Voltage Reset Retention Voltage				0.8	V
V_{det3r}	Low Voltage Reset Release Voltage (3)		2.2	2.9	4.0	V

NOTES:
1. $V_{det4} > V_{det3}$.
2. Where reset level detection voltage is less than 2.7 V, if the supply power voltage is greater than the reset level detection voltage, the microcomputer operates with f(BCLK) ≤ 10MHz.
3. $V_{det3r} > V_{det3}$ is not guaranteed.
4. The voltage detection circuit is designed to use when VCC1 is set to 5V.

Table 5.10 Power Supply Circuit Timing Characteristics

Symbol	Parameter	Measuring Condition	Standard			Unit
			Min.	Typ.	Max.	
$t_{d(P-R)}$	Time for Internal Power Supply Stabilization During Powering-On	V_{CC1}=2.7V to 5.5V			2	ms
$t_{d(R-S)}$	STOP Release Time				150	µs
$t_{d(W-S)}$	Low Power Dissipation Mode Wait Mode Release Time				150	µs
$t_{d(S-R)}$	Brown-out Detection Reset (Hardware Reset 2) Release Wait Time	V_{CC1}=V_{det3r} to 5.5V		6 (1)	20	ms
$t_{d(E-A)}$	Low Voltage Detection Circuit Operation Start Time	V_{CC1}=2.7V to 5.5V			20	µs

NOTES:
1. When V_{CC1} = 5V.

$V_{CC1}=V_{CC2}=5V$

Table 5.11 Electrical Characteristics (1) (1)

Symbol	Parameter			Measuring Condition	Standard			Unit
					Min.	Typ.	Max.	
V_{OH}	HIGH Output Voltage (3)	P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P14_0, P14_1		I_{OH}=−5mA	V_{CC1}−2.0		V_{CC1}	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P12_0 to P12_7, P13_0 to P13_7		I_{OH}=−5mA (2)	V_{CC2}−2.0		V_{CC2}	
V_{OH}	HIGH Output Voltage (3)	P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P14_0, P14_1		I_{OH}=−200μA	V_{CC1}−0.3		V_{CC1}	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P12_0 to P12_7, P13_0 to P13_7		I_{OH}=−200μA (2)	V_{CC2}−0.3		V_{CC2}	
V_{OH}	HIGH Output Voltage XOUT		HIGHPOWER	I_{OH}=−1mA	V_{CC1}−2.0		V_{CC1}	V
			LOWPOWER	I_{OH}=−0.5mA	V_{CC1}−2.0		V_{CC1}	
	HIGH Output Voltage XCOUT		HIGHPOWER	With no load applied		2.5		V
			LOWPOWER	With no load applied		1.6		
V_{OL}	LOW Output Voltage (3)	P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P14_0, P14_1		I_{OL}=5mA			2.0	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P12_0 to P12_7, P13_0 to P13_7		I_{OL}=5mA (2)			2.0	
V_{OL}	LOW Output Voltage (3)	P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P14_0, P14_1		I_{OL}=200μA			0.45	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P12_0 to P12_7, P13_0 to P13_7		I_{OL}=200μA (2)			0.45	
V_{OL}	LOW Output Voltage XOUT		HIGHPOWER	I_{OL}=1mA			2.0	V
			LOWPOWER	I_{OL}=0.5mA			2.0	
	LOW Output Voltage XCOUT		HIGHPOWER	With no load applied		0		V
			LOWPOWER	With no load applied		0		
V_{T+}-V_{T-}	Hysteresis	$\overline{HOLD}$, $\overline{RDY}$, TA0IN to TA4IN, TB0IN to TB5IN, $\overline{INT0}$ to $\overline{INT5}$, $\overline{NMI}$, $\overline{ADTRG}$, $\overline{CTS0}$ to $\overline{CTS2}$, CLK0 to CLK4, TA0OUT to TA4OUT, $\overline{KI0}$ to $\overline{KI3}$, RXD0 to RXD2, SCL0 to SCL2, SDA0 to SDA2, SIN3, SIN4			0.2		1.0	V
V_{T+}-V_{T-}	Hysteresis	$\overline{RESET}$			0.2		2.5	V
I_{IH}	HIGH Input Current (3)	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1, XIN, $\overline{RESET}$, CNVSS, BYTE		V_I=5V			5.0	μA
I_{IL}	LOW Input Current (3)	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7,P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1, XIN, $\overline{RESET}$, CNVSS, BYTE		V_I=0V			−5.0	μA
R_{PULLUP}	Pull-Up Resistance (3)	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7,P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1		V_I=0V	30	50	170	kΩ
R_{fXIN}	Feedback Resistance XIN					1.5		MΩ
R_{fXCIN}	Feedback Resistance XCIN					15		MΩ
V_{RAM}	RAM Retention Voltage			At stop mode	2.0			V

NOTES:
1. Referenced to V_{CC1}=V_{CC2}=4.2 to 5.5V, V_{SS} = 0V at T_{opr} = −20 to 85°C / −40 to 85°C, f(BCLK)=24MHz unless otherwise specified.
2. Where the product is used at V_{CC1} = 5 V and V_{CC2} = 3 V, refer to the 3 V version value for the pin specified value on V_{CC2} port side.
3. There is no external connections for port P1_0 to P1_7, P4_4 to P4_7, P7_2 to P7_5 and P9_1 in 80-pin version.

$V_{CC1}=V_{CC2}=5V$

Timing Requirements
(V_{CC1} = V_{CC2} = 5V, V_{SS} = 0V, at T_{opr} = –20 to 85°C / –40 to 85°C unless otherwise specified)

Table 5.21 Timer B Input (Counter Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN Input Cycle Time (counted on one edge)	100		ns
$t_{w(TBH)}$	TBiIN Input HIGH Pulse Width (counted on one edge)	40		ns
$t_{w(TBL)}$	TBiIN Input LOW Pulse Width (counted on one edge)	40		ns
$t_{c(TB)}$	TBiIN Input Cycle Time (counted on both edges)	200		ns
$t_{w(TBH)}$	TBiIN Input HIGH Pulse Width (counted on both edges)	80		ns
$t_{w(TBL)}$	TBiIN Input LOW Pulse Width (counted on both edges)	80		ns

Table 5.22 Timer B Input (Pulse Period Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN Input Cycle Time	400		ns
$t_{w(TBH)}$	TBiIN Input HIGH Pulse Width	200		ns
$t_{w(TBL)}$	TBiIN Input LOW Pulse Width	200		ns

Table 5.23 Timer B Input (Pulse Width Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN Input Cycle Time	400		ns
$t_{w(TBH)}$	TBiIN Input HIGH Pulse Width	200		ns
$t_{w(TBL)}$	TBiIN Input LOW Pulse Width	200		ns

Table 5.24 A/D Trigger Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(AD)}$	$\overline{\text{ADTRG}}$ Input Cycle Time	1000		ns
$t_{w(ADL)}$	$\overline{\text{ADTRG}}$ input LOW Pulse Width	125		ns

Table 5.25 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi Input Cycle Time	200		ns
$t_{w(CKH)}$	CLKi Input HIGH Pulse Width	100		ns
$t_{w(CKL)}$	CLKi Input LOW Pulse Width	100		ns
$t_{d(C-Q)}$	TXDi Output Delay Time		80	ns
$t_{h(C-Q)}$	TXDi Hold Time	0		ns
$t_{su(D-C)}$	RXDi Input Setup Time	70		ns
$t_{h(C-D)}$	RXDi Input Hold Time	90		ns

Table 5.26 External Interrupt $\overline{\text{INTi}}$ Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(INH)}$	$\overline{\text{INTi}}$ Input HIGH Pulse Width	250		ns
$t_{w(INL)}$	$\overline{\text{INTi}}$ Input LOW Pulse Width	250		ns

$V_{CC1}=V_{CC2}=5V$

Switching Characteristics

(V_{CC1} = V_{CC2} = 5V, V_{SS} = 0V, at T_{opr} = –20 to 85°C / –40 to 85°C unless otherwise specified)

Table 5.29 Memory Expansion and Microprocessor Modes (for 2- to 3-wait setting, external area access and multiplex bus selection)

Symbol	Parameter		Standard		Unit
			Min.	Max.	
td(BCLK-AD)	Address Output Delay Time	See **Figure 5.2**		25	ns
th(BCLK-AD)	Address Output Hold Time (in relation to BCLK)		4		ns
th(RD-AD)	Address Output Hold Time (in relation to RD)		(NOTE 1)		ns
th(WR-AD)	Address Output Hold Time (in relation to WR)		(NOTE 1)		ns
td(BCLK-CS)	Chip Select Output Delay Time			25	ns
th(BCLK-CS)	Chip Select Output Hold Time (in relation to BCLK)		4		ns
th(RD-CS)	Chip Select Output Hold Time (in relation to RD)		(NOTE 1)		ns
th(WR-CS)	Chip Select Output Hold Time (in relation to WR)		(NOTE 1)		ns
td(BCLK-RD)	RD Signal Output Delay Time			25	ns
th(BCLK-RD)	RD Signal Output Hold Time		0		ns
td(BCLK-WR)	WR Signal Output Delay Time			25	ns
th(BCLK-WR)	WR Signal Output Hold Time		0		ns
td(BCLK-DB)	Data Output Delay Time (in relation to BCLK)			40	ns
th(BCLK-DB)	Data Output Hold Time (in relation to BCLK)		4		ns
td(DB-WR)	Data Output Delay Time (in relation to WR)		(NOTE 2)		ns
th(WR-DB)	Data Output Hold Time (in relation to WR)		(NOTE 1)		ns
td(BCLK-HLDA)	HLDA Output Delay Time			40	ns
td(BCLK-ALE)	ALE Signal Output Delay Time (in relation to BCLK)			15	ns
th(BCLK-ALE)	ALE Signal Output Hold Time (in relation to BCLK)		–4		ns
td(AD-ALE)	ALE Signal Output Delay Time (in relation to Address)		(NOTE 3)		ns
th(AD-ALE)	ALE Signal Output Hold Time (in relation to Address)		(NOTE 4)		ns
td(AD-RD)	RD Signal Output Delay From the End of Address		0		ns
td(AD-WR)	WR Signal Output Delay From the End of Address		0		ns
tdz(RD-AD)	Address Output Floating Start Time			8	ns

NOTES:

1. Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f(BCLK)} - 10[ns]$$

2. Calculated according to the BCLK frequency as follows:

$$\frac{(n-0.5) \times 10^9}{f(BCLK)} - 40[ns]$$

n is “2” for 2-wait setting, “3” for 3-wait setting.

3. Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f(BCLK)} - 25[ns]$$

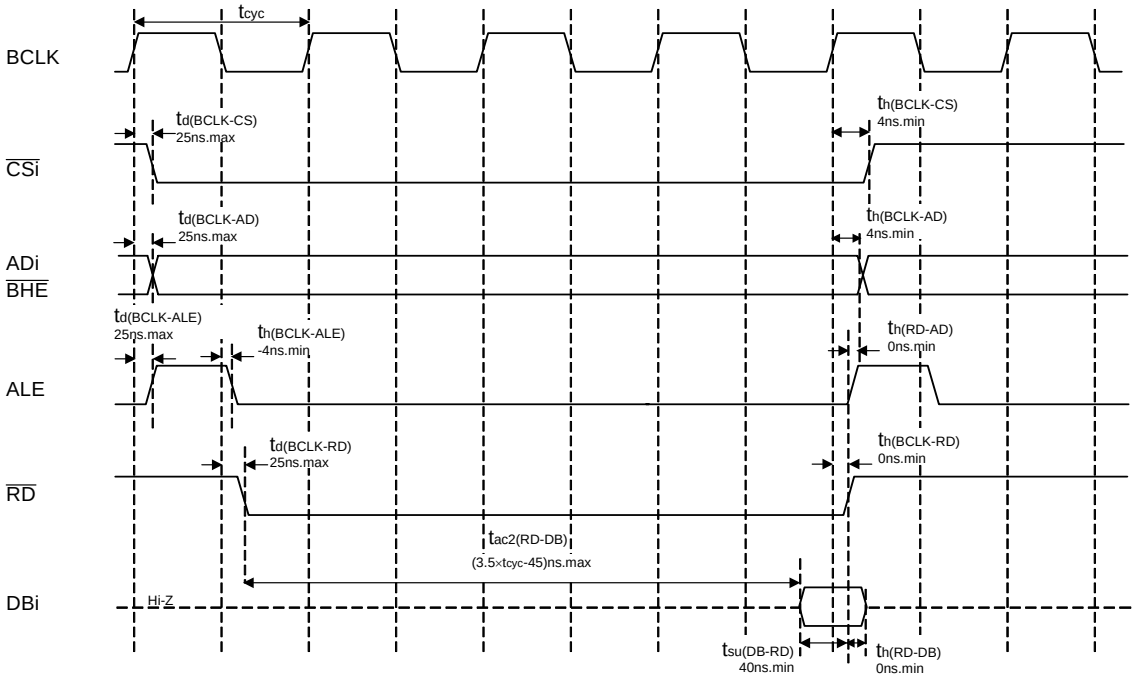
4. Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f(BCLK)} - 15[ns]$$

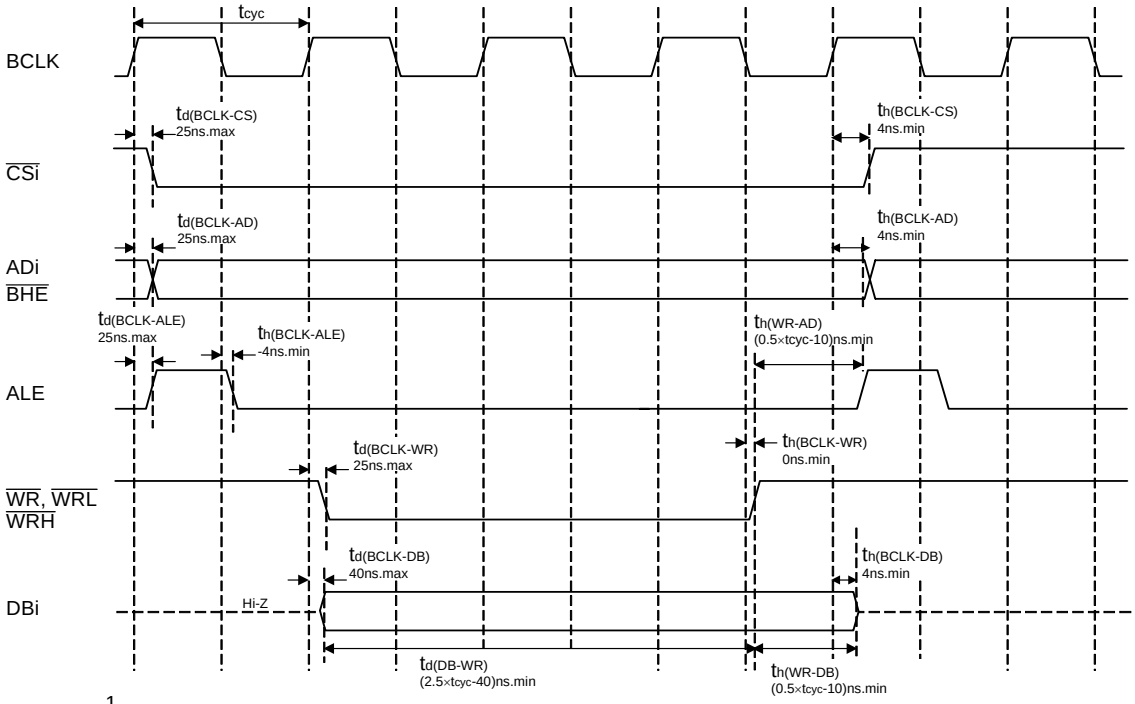
Memory Expansion Mode, Microprocessor Mode
(for 3-wait setting and external area access**)**

$V_{CC1}=V_{CC2}=5V$

Read timing



Write timing



$$t_{cyc}=\frac{1}{f(BCLK)}$$

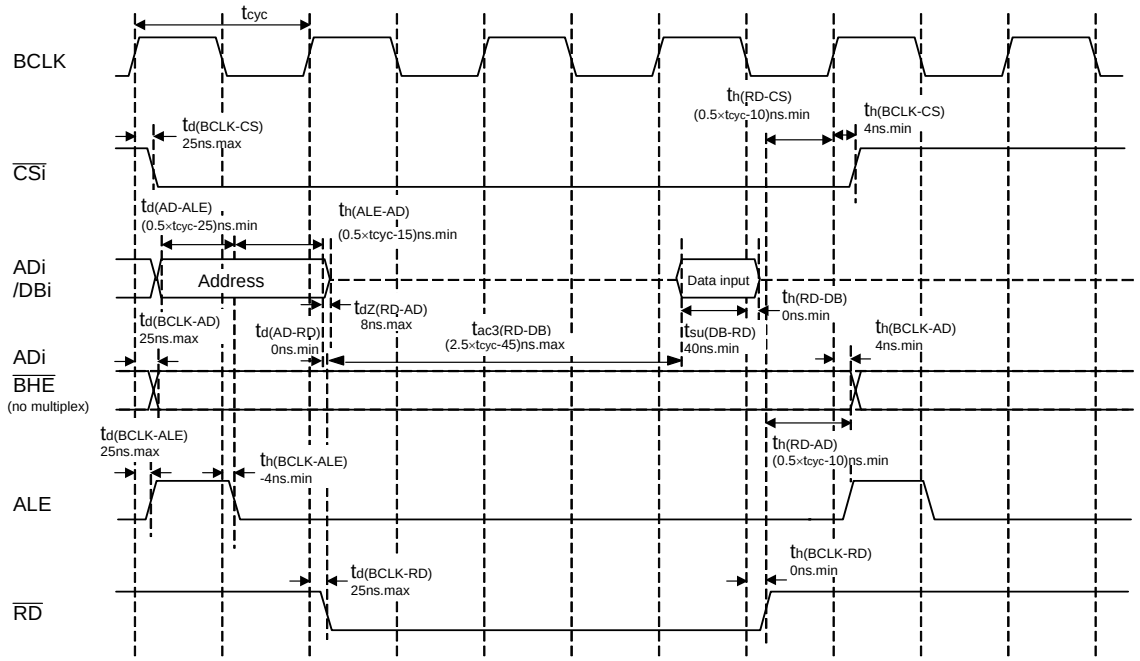
Measuring conditions
· $V_{CC1}=V_{CC2}=5V$
· Input timing voltage : $V_{IL}=0.8V$, $V_{IH}=2.0V$
· Output timing voltage : $V_{OL}=0.4V$, $V_{OH}=2.4V$

Figure 5.9 Timing Diagram (7)

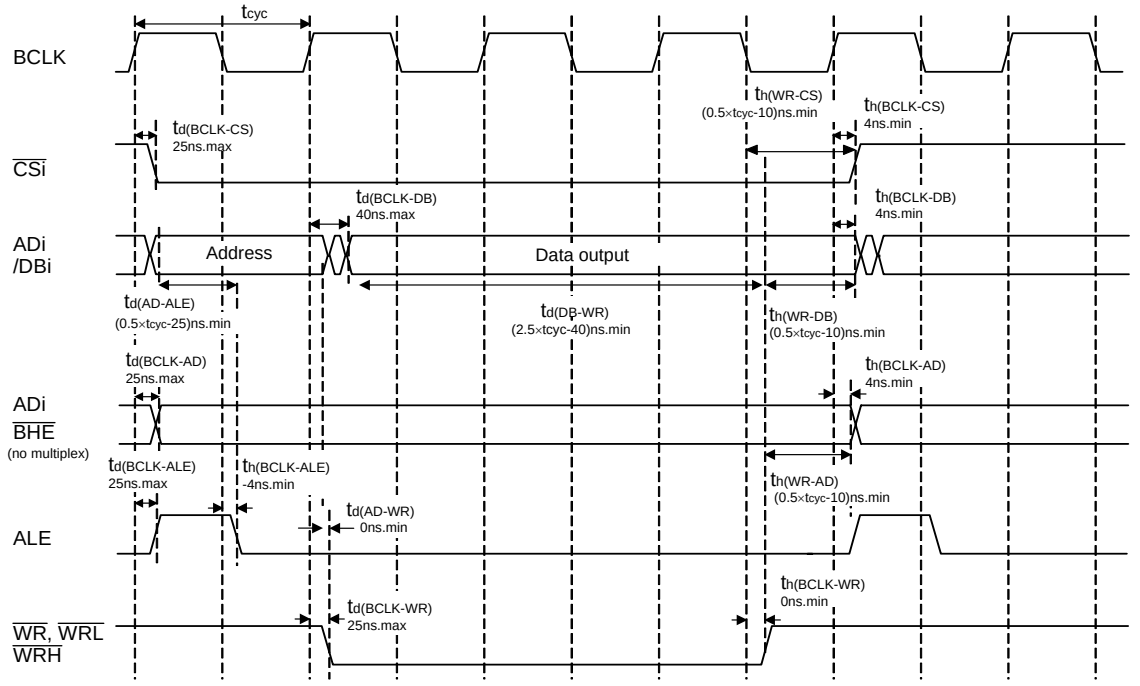
$V_{CC1}=V_{CC2}=5V$

Memory Expansion Mode, Microprocessor Mode
(For 3-wait setting, external area access and multiplex bus selection**)**

Read timing



Write timing



$$t_{cyc}=\frac{1}{f(BCLK)}$$

Measuring conditions
· $V_{CC1}=V_{CC2}=5V$
· Input timing voltage : $V_{IL}=0.8V$, $V_{IH}=2.0V$
· Output timing voltage : $V_{OL}=0.4V$, $V_{OH}=2.4V$

Figure 5.11 Timing Diagram (9)

$V_{CC1}=V_{CC2}=3V$

Timing Requirements
(V_{CC1} = V_{CC2} = 3V, V_{SS} = 0V, at T_{opr} = –20 to 85°C / –40 to 85°C unless otherwise specified)

Table 5.40 Timer B Input (Counter Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN Input Cycle Time (counted on one edge)	150		ns
$t_{w(TBH)}$	TBiIN Input HIGH Pulse Width (counted on one edge)	60		ns
$t_{w(TBL)}$	TBiIN Input LOW Pulse Width (counted on one edge)	60		ns
$t_{c(TB)}$	TBiIN Input Cycle Time (counted on both edges)	300		ns
$t_{w(TBH)}$	TBiIN Input HIGH Pulse Width (counted on both edges)	120		ns
$t_{w(TBL)}$	TBiIN Input LOW Pulse Width (counted on both edges)	120		ns

Table 5.41 Timer B Input (Pulse Period Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN Input Cycle Time	600		ns
$t_{w(TBH)}$	TBiIN Input HIGH Pulse Width	300		ns
$t_{w(TBL)}$	TBiIN Input LOW Pulse Width	300		ns

Table 5.42 Timer B Input (Pulse Width Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN Input Cycle Time	600		ns
$t_{w(TBH)}$	TBiIN Input HIGH Pulse Width	300		ns
$t_{w(TBL)}$	TBiIN Input LOW Pulse Width	300		ns

Table 5.43 A/D Trigger Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(AD)}$	$\overline{\text{ADTRG}}$ Input Cycle Time	1500		ns
$t_{w(ADL)}$	$\overline{\text{ADTRG}}$ Input LOW Pulse Width	200		ns

Table 5.44 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi Input Cycle Time	300		ns
$t_{w(CKH)}$	CLKi Input HIGH Pulse Width	150		ns
$t_{w(CKL)}$	CLKi Input LOW Pulse Width	150		ns
$t_{d(C-Q)}$	TXDi Output Delay Time		160	ns
$t_{h(C-Q)}$	TXDi Hold Time	0		ns
$t_{su(D-C)}$	RXDi Input Setup Time	100		ns
$t_{h(C-D)}$	RXDi Input Hold Time	90		ns

Table 5.45 External Interrupt $\overline{\text{INTi}}$ Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(INH)}$	$\overline{\text{INTi}}$ Input HIGH Pulse Width	380		ns
$t_{w(INL)}$	$\overline{\text{INTi}}$ Input LOW Pulse Width	380		ns

Table 5.56 Power Supply Circuit Timing Characteristics

Symbol	Parameter	Measuring Condition	Standard			Unit
			Min.	Typ.	Max.	
$t_{d(P-R)}$	Time for Internal Power Supply Stabilization During Powering-On	V_{CC1}=4.0V to 5.5V			2	ms
$t_{d(R-S)}$	STOP Release Time				150	µs
$t_{d(W-S)}$	Low Power Dissipation Mode Wait Mode Release Time				150	µs

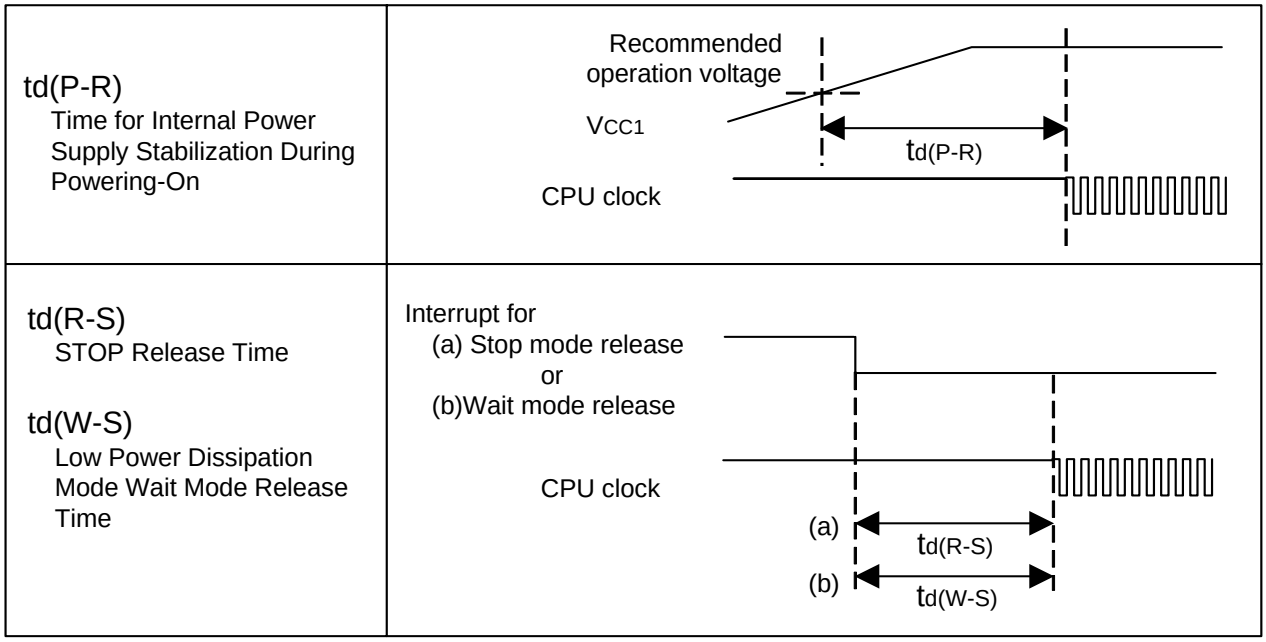


Figure 5.22 Power Supply Circuit Timing Diagram

$V_{CC1}=V_{CC2}=5V$

Timing Requirements
(V_{CC1} = V_{CC2} = 5V, V_{SS} = 0V, at T_{opr} = –40 to 85°C (T version) / –40 to 125°C (V version) unless otherwise specified)

Table 5.59 External Clock Input (XIN input)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
t_c	External Clock Input Cycle Time	62.5		ns
$t_{w(H)}$	External Clock Input HIGH Pulse Width	25		ns
$t_{w(L)}$	External Clock Input LOW Pulse Width	25		ns
t_r	External Clock Rise Time		15	ns
t_f	External Clock Fall Time		15	ns

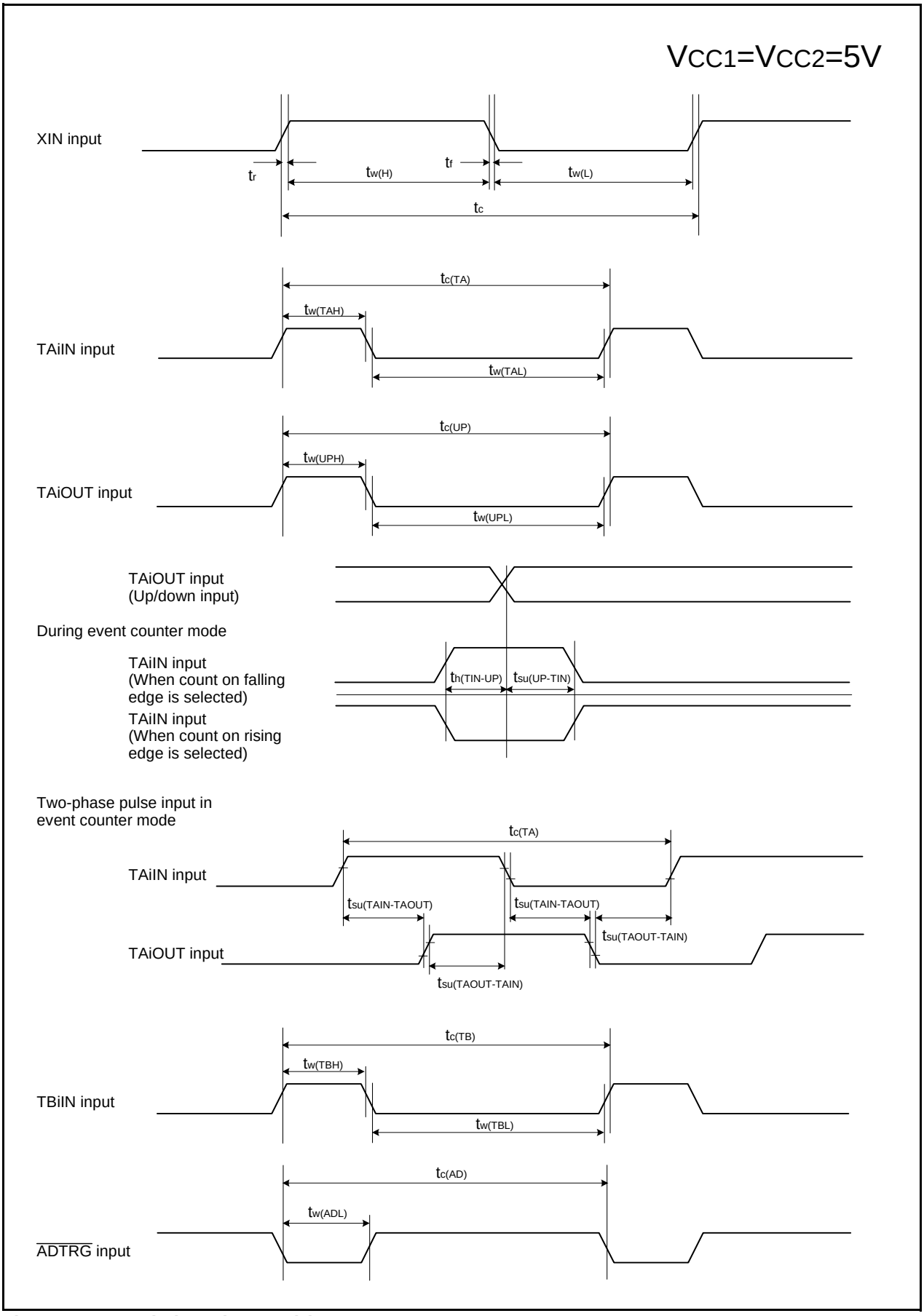
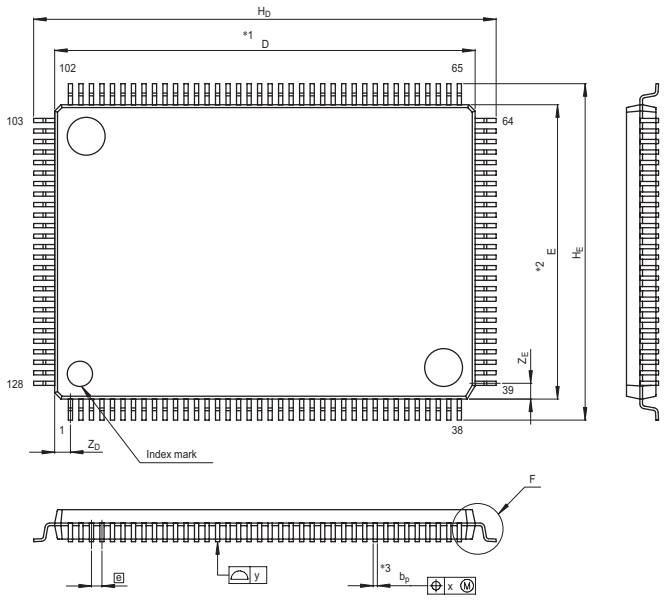
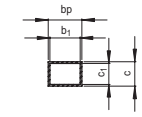


Figure 5.24 Timing Diagram (1)

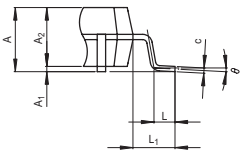
Appendix 1.Package Dimensions

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP128-14x20-0.50	PLQP0128KB-A	128P6Q-A	0.9g





Terminal cross section

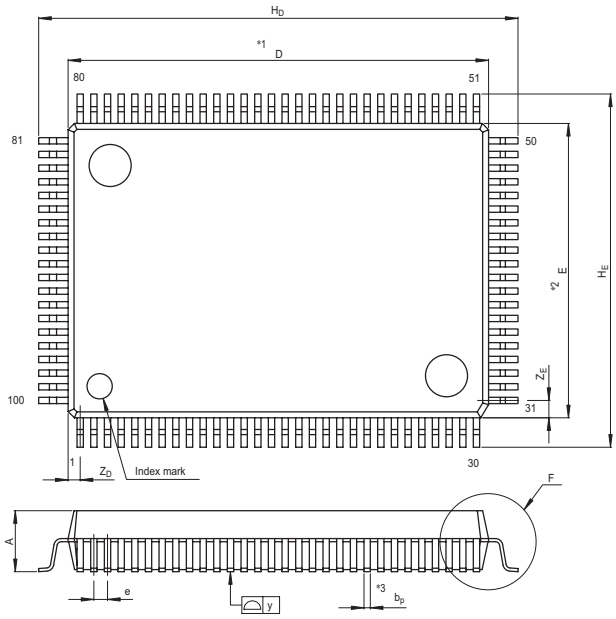


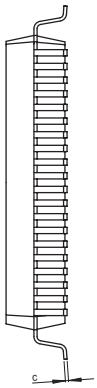
DetailF

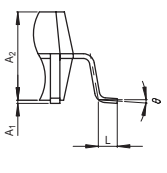
NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	19.9	20.0	20.1
E	13.9	14.0	14.1
A_2	—	1.4	—
H_D	21.8	22.0	22.2
H_E	15.8	16.0	16.2
A	—	—	1.7
A_1	0.05	0.125	0.2
b_p	0.17	0.22	0.27
b_1	—	0.20	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.5	—
x	—	—	0.10
y	—	—	0.10
Z_D	—	0.75	—
Z_E	—	0.75	—
L	0.35	0.5	0.65
L_1	—	1.0	—

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-QFP100-14x20-0.65	PRQP0100JB-A	100P6S-A	1.6g







Detail F

NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	19.8	20.0	20.2
E	13.8	14.0	14.2
A_2	—	2.8	—
H_D	22.5	22.8	23.1
H_E	16.5	16.8	17.1
A	—	—	3.05
A_1	0	0.1	0.2
b_p	0.25	0.3	0.4
c	0.13	0.15	0.2
θ	0°	—	10°
e	0.5	0.65	0.8
y	—	—	0.10
Z_D	—	0.575	—
Z_E	—	0.825	—
L	0.4	0.6	0.8

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