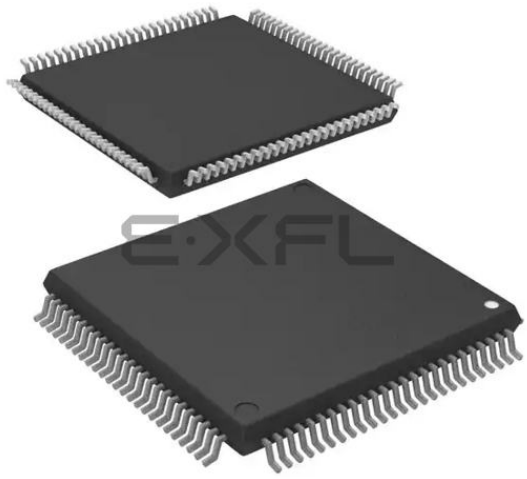
# Renesas Electronics America Inc - M30626FHPGP#U5C Datasheet



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## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Not For New Designs |
| Core Processor | M16C/60 |
| Core Size | 16-Bit |
| Speed | 24MHz |
| Connectivity | I²C, IEBus, UART/USART |
| Peripherals | DMA, WDT |
| Number of I/O | 85 |
| Program Memory Size | 384KB (384K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | 4K x 8 |
| RAM Size | 31K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.7V ~ 5.5V |
| Data Converters | A/D 26x10b; D/A 2x8b |
| Oscillator Type | Internal |
| Operating Temperature | -20°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 100-LQFP |
| Supplier Device Package | 100-LFQFP (14x14) |
| Purchase URL | https://www.e-xfl.com/product-detail/renesas-electronics-america/m30626fhpgp-u5c |

# 1. Overview

The M16C/62P Group (M16C/62P, M16C/62PT) of single-chip microcomputers are built using the high performance silicon gate CMOS process using a M16C/60 Series CPU core and are packaged in a 80-pin, 100-pin and 128-pin plastic molded QFP. These single-chip microcomputers operate using sophisticated instructions featuring a high level of instruction efficiency. With 1M bytes of address space, they are capable of executing instructions at high speed. In addition, this microcomputer contains a multiplier and DMAC which combined with fast instruction processing capability, makes it suitable for control of various OA, communication, and industrial equipment which requires high-speed arithmetic/logic operations.

## 1.1 Applications

Audio, cameras, television, home appliance, office/communications/portable/industrial equipment, automobile, etc.

Specifications written in this manual are believed to be accurate, but are not guaranteed to be entirely free of error. Specifications in this manual may be changed for functional or performance improvements. Please make sure your manual is the latest edition.

**Table 1.11 Pin Characteristics for 128-Pin Package (2)**

| Pin No. | Control Pin | Port | Interrupt Pin | Timer Pin | UART Pin | Analog Pin | Bus Control Pin |
|---|---|---|---|---|---|---|---|
| 51 | | P5_6 | | | | | ALE |
| 52 | | P5_5 | | | | | $\overline{\text{HOLD}}$ |
| 53 | | P5_4 | | | | | $\overline{\text{HLDA}}$ |
| 54 | | P13_3 | | | | | |
| 55 | | P13_2 | | | | | |
| 56 | | P13_1 | | | | | |
| 57 | | P13_0 | | | | | |
| 58 | | P5_3 | | | | | BCLK |
| 59 | | P5_2 | | | | | $\overline{\text{RD}}$ |
| 60 | | P5_1 | | | | | $\overline{\text{WRH}}$/$\overline{\text{BHE}}$ |
| 61 | | P5_0 | | | | | $\overline{\text{WRL}}$/$\overline{\text{WR}}$ |
| 62 | | P12_7 | | | | | |
| 63 | | P12_6 | | | | | |
| 64 | | P12_5 | | | | | |
| 65 | | P4_7 | | | | | $\overline{\text{CS3}}$ |
| 66 | | P4_6 | | | | | $\overline{\text{CS2}}$ |
| 67 | | P4_5 | | | | | $\overline{\text{CS1}}$ |
| 68 | | P4_4 | | | | | $\overline{\text{CS0}}$ |
| 69 | | P4_3 | | | | | A19 |
| 70 | | P4_2 | | | | | A18 |
| 71 | | P4_1 | | | | | A17 |
| 72 | | P4_0 | | | | | A16 |
| 73 | | P3_7 | | | | | A15 |
| 74 | | P3_6 | | | | | A14 |
| 75 | | P3_5 | | | | | A13 |
| 76 | | P3_4 | | | | | A12 |
| 77 | | P3_3 | | | | | A11 |
| 78 | | P3_2 | | | | | A10 |
| 79 | | P3_1 | | | | | A9 |
| 80 | | P12_4 | | | | | |
| 81 | | P12_3 | | | | | |
| 82 | | P12_2 | | | | | |
| 83 | | P12_1 | | | | | |
| 84 | | P12_0 | | | | | |
| 85 | VCC2 | | | | | | |
| 86 | | P3_0 | | | | | A8(/-/D7) |
| 87 | VSS | | | | | | |
| 88 | | P2_7 | | | | AN2_7 | A7(/D7/D6) |
| 89 | | P2_6 | | | | AN2_6 | A6(/D6/D5) |
| 90 | | P2_5 | | | | AN2_5 | A5(/D5/D4) |
| 91 | | P2_4 | | | | AN2_4 | A4(/D4/D3) |
| 92 | | P2_3 | | | | AN2_3 | A3(/D3/D2) |
| 93 | | P2_2 | | | | AN2_2 | A2(/D2/D1) |
| 94 | | P2_1 | | | | AN2_1 | A1(/D1/D0) |
| 95 | | P2_0 | | | | AN2_0 | A0(/D0/-) |
| 96 | | P1_7 | $\overline{\text{INT5}}$ | | | | D15 |
| 97 | | P1_6 | $\overline{\text{INT4}}$ | | | | D14 |
| 98 | | P1_5 | $\overline{\text{INT3}}$ | | | | D13 |
| 99 | | P1_4 | | | | | D12 |
| 100 | | P1_3 | | | | | D11 |

**Table 1.14 Pin Characteristics for 100-Pin Package (2)**

| Pin No. | | Control Pin | Port | Interrupt Pin | Timer Pin | UART Pin | Analog Pin | Bus Control Pin |
|---|---|---|---|---|---|---|---|---|
| FP | GP | | | | | | | |
| 51 | 49 | | P4_3 | | | | | A19 |
| 52 | 50 | | P4_2 | | | | | A18 |
| 53 | 51 | | P4_1 | | | | | A17 |
| 54 | 52 | | P4_0 | | | | | A16 |
| 55 | 53 | | P3_7 | | | | | A15 |
| 56 | 54 | | P3_6 | | | | | A14 |
| 57 | 55 | | P3_5 | | | | | A13 |
| 58 | 56 | | P3_4 | | | | | A12 |
| 59 | 57 | | P3_3 | | | | | A11 |
| 60 | 58 | | P3_2 | | | | | A10 |
| 61 | 59 | | P3_1 | | | | | A9 |
| 62 | 60 | VCC2 | | | | | | |
| 63 | 61 | | P3_0 | | | | | A8(/-/D7) |
| 64 | 62 | VSS | | | | | | |
| 65 | 63 | | P2_7 | | | | AN2_7 | A7(/D7/D6) |
| 66 | 64 | | P2_6 | | | | AN2_6 | A6(/D6/D5) |
| 67 | 65 | | P2_5 | | | | AN2_5 | A5(/D5/D4) |
| 68 | 66 | | P2_4 | | | | AN2_4 | A4(/D4/D3) |
| 69 | 67 | | P2_3 | | | | AN2_3 | A3(/D3/D2) |
| 70 | 68 | | P2_2 | | | | AN2_2 | A2(/D2/D1) |
| 71 | 69 | | P2_1 | | | | AN2_1 | A1(/D1/D0) |
| 72 | 70 | | P2_0 | | | | AN2_0 | A0(/D0/-) |
| 73 | 71 | | P1_7 | $\overline{\text{INT5}}$ | | | | D15 |
| 74 | 72 | | P1_6 | $\overline{\text{INT4}}$ | | | | D14 |
| 75 | 73 | | P1_5 | $\overline{\text{INT3}}$ | | | | D13 |
| 76 | 74 | | P1_4 | | | | | D12 |
| 77 | 75 | | P1_3 | | | | | D11 |
| 78 | 76 | | P1_2 | | | | | D10 |
| 79 | 77 | | P1_1 | | | | | D9 |
| 80 | 78 | | P1_0 | | | | | D8 |
| 81 | 79 | | P0_7 | | | | AN0_7 | D7 |
| 82 | 80 | | P0_6 | | | | AN0_6 | D6 |
| 83 | 81 | | P0_5 | | | | AN0_5 | D5 |
| 84 | 82 | | P0_4 | | | | AN0_4 | D4 |
| 85 | 83 | | P0_3 | | | | AN0_3 | D3 |
| 86 | 84 | | P0_2 | | | | AN0_2 | D2 |
| 87 | 85 | | P0_1 | | | | AN0_1 | D1 |
| 88 | 86 | | P0_0 | | | | AN0_0 | D0 |
| 89 | 87 | | P10_7 | $\overline{\text{KI3}}$ | | | AN7 | |
| 90 | 88 | | P10_6 | $\overline{\text{KI2}}$ | | | AN6 | |
| 91 | 89 | | P10_5 | $\overline{\text{KI1}}$ | | | AN5 | |
| 92 | 90 | | P10_4 | $\overline{\text{KI0}}$ | | | AN4 | |
| 93 | 91 | | P10_3 | | | | AN3 | |
| 94 | 92 | | P10_2 | | | | AN2 | |
| 95 | 93 | | P10_1 | | | | AN1 | |
| 96 | 94 | AVSS | | | | | | |
| 97 | 95 | | P10_0 | | | | AN0 | |
| 98 | 96 | VREF | | | | | | |
| 99 | 97 | AVCC | | | | | | |
| 100 | 98 | | P9_7 | | | SIN4 | $\overline{\text{ADTRG}}$ | |

**Table 1.15 Pin Characteristics for 80-Pin Package (1)**

| Pin No. | Control Pin | Port | Interrupt Pin | Timer Pin | UART Pin | Analog Pin | Bus Control Pin |
|---|---|---|---|---|---|---|---|
| 1 | | P9_5 | | | CLK4 | ANEX0 | |
| 2 | | P9_4 | | TB4IN | | DA1 | |
| 3 | | P9_3 | | TB3IN | | DA0 | |
| 4 | | P9_2 | | TB2IN | SOUT3 | | |
| 5 | | P9_0 | | TB0IN | CLK3 | | |
| 6 | CNVSS (BYTE) | | | | | | |
| 7 | XCIN | P8_7 | | | | | |
| 8 | XCOUT | P8_6 | | | | | |
| 9 | $\overline{\text{RESET}}$ | | | | | | |
| 10 | XOUT | | | | | | |
| 11 | VSS | | | | | | |
| 12 | XIN | | | | | | |
| 13 | VCC1 | | | | | | |
| 14 | | P8_5 | $\overline{\text{NMI}}$ | | | | |
| 15 | | P8_4 | $\overline{\text{INT2}}$ | ZP | | | |
| 16 | | P8_3 | $\overline{\text{INT1}}$ | | | | |
| 17 | | P8_2 | $\overline{\text{INT0}}$ | | | | |
| 18 | | P8_1 | | TA4IN | | | |
| 19 | | P8_0 | | TA4OUT | | | |
| 20 | | P7_7 | | TA3IN | | | |
| 21 | | P7_6 | | TA3OUT | | | |
| 22 | | P7_1 | | TA0IN/TB5IN | RXD2/SCL2 | | |
| 23 | | P7_0 | | TA0OUT | TXD2/SDA2 | | |
| 24 | | P6_7 | | | TXD1/SDA1 | | |
| 25 | | P6_6 | | | RXD1/SCL1 | | |
| 26 | | P6_5 | | | CLK1 | | |
| 27 | | P6_4 | | | $\overline{\text{CTS1}}$/$\overline{\text{RTS1}}$/$\overline{\text{CTS0}}$/CLKS1 | | |
| 28 | | P6_3 | | | TXD0/SDA0 | | |
| 29 | | P6_2 | | | RXD0/SCL0 | | |
| 30 | | P6_1 | | | CLK0 | | |
| 31 | | P6_0 | | | $\overline{\text{CTS0}}$/$\overline{\text{RTS0}}$ | | |
| 32 | | P5_7 | | | | | CLKOUT |
| 33 | | P5_6 | | | | | |
| 34 | | P5_5 | | | | | |
| 35 | | P5_4 | | | | | |
| 36 | | P5_3 | | | | | |
| 37 | | P5_2 | | | | | |
| 38 | | P5_1 | | | | | |
| 39 | | P5_0 | | | | | |
| 40 | | P4_3 | | | | | |
| 41 | | P4_2 | | | | | |
| 42 | | P4_1 | | | | | |
| 43 | | P4_0 | | | | | |
| 44 | | P3_7 | | | | | |
| 45 | | P3_6 | | | | | |
| 46 | | P3_5 | | | | | |
| 47 | | P3_4 | | | | | |
| 48 | | P3_3 | | | | | |
| 49 | | P3_2 | | | | | |
| 50 | | P3_1 | | | | | |

**Table 1.18 Pin Description (100-pin and 128-pin Version) (2)**

| Signal Name | Pin Name | I/O Type | Power Supply(1) | Description |
|---|---|---|---|---|
| Main clock input | XIN | I | VCC1 | I/O pins for the main clock generation circuit. Connect a ceramic resonator or crystal oscillator between XIN and XOUT (3). To use the external clock, input the clock from XIN and leave XOUT open. |
| Main clock output | XOUT | O | VCC1 | |
| Sub clock input | XCIN | I | VCC1 | I/O pins for a sub clock oscillation circuit. Connect a crystal oscillator between XCIN and XCOUT (3). To use the external clock, input the clock from XCIN and leave XCOUT open. |
| Sub clock output | XCOUT | O | VCC1 | |
| BCLK output (2) | BCLK | O | VCC2 | Outputs the BCLK signal. |
| Clock output | CLKOUT | O | VCC2 | The clock of the same cycle as fC, f8, or f32 is outputted. |
| $\overline{\text{INT}}$ interrupt input | $\overline{\text{INT0}}$ to $\overline{\text{INT2}}$ | I | VCC1 | Input pins for the $\overline{\text{INT}}$ interrupt. |
| | $\overline{\text{NT3}}$ to $\overline{\text{INT5}}$ | I | VCC2 | |
| $\overline{\text{NMI}}$ interrupt input | $\overline{\text{NMI}}$ | I | VCC1 | Input pin for the $\overline{\text{NMI}}$ interrupt. Pin states can be read by the P8_5 bit in the P8 register. |
| Key input interrupt input | $\overline{\text{KI0}}$ to $\overline{\text{KI3}}$ | I | VCC1 | Input pins for the key input interrupt. |
| Timer A | TA0OUT to TA4OUT | I/O | VCC1 | These are timer A0 to timer A4 I/O pins. (however, output of TA0OUT for the N-channel open drain output.) |
| | TA0IN to TA4IN | I | VCC1 | These are timer A0 to timer A4 input pins. |
| | ZP | I | VCC1 | Input pin for the Z-phase. |
| Timer B | TB0IN to TB5IN | I | VCC1 | These are timer B0 to timer B5 input pins. |
| Three-phase motor control output | U, $\overline{\text{U}}$, V, $\overline{\text{V}}$, W, $\overline{\text{W}}$ | O | VCC1 | These are Three-phase motor control output pins. |
| Serial interface | $\overline{\text{CTS0}}$ to $\overline{\text{CTS2}}$ | I | VCC1 | These are send control input pins. |
| | $\overline{\text{RTS0}}$ to $\overline{\text{RTS2}}$ | O | VCC1 | These are receive control output pins. |
| | CLK0 to CLK4 | I/O | VCC1 | These are transfer clock I/O pins. |
| | RXD0 to RXD2 | I | VCC1 | These are serial data input pins. |
| | SIN3, SIN4 | I | VCC1 | These are serial data input pins. |
| | TXD0 to TXD2 | O | VCC1 | These are serial data output pins. (however, output of TXD2 for the N-channel open drain output.) |
| | SOUT3, SOUT4 | O | VCC1 | These are serial data output pins. |
| | CLKS1 | O | VCC1 | This is output pin for transfer clock output from multiple pins function. |
| $I^2C$ mode | SDA0 to SDA2 | I/O | VCC1 | These are serial data I/O pins. (however, output of SDA2 for the N-channel open drain output.) |
| | SCL0 to SCL2 | I/O | VCC1 | These are transfer clock I/O pins. (however, output of SCL2 for the N-channel open drain output.) |

I : Input O : Output I/O : Input and output

NOTES:
1. When use VCC1 > VCC2, contacts due to some points or restrictions to be checked.
2. This pin function in M16C/62PT cannot be used.
3. Ask the oscillator maker the oscillation characteristic.

# 3. Memory

Figure 3.1 is a Memory Map of the M16C/62P group. The address space extends the 1M bytes from address 00000h to FFFFFh.
The internal ROM is allocated in a lower address direction beginning with address FFFFFh. For example, a 64-Kbyte internal ROM is allocated to the addresses from F0000h to FFFFFh.
As for the flash memory version, 4-Kbyte space (block A) exists in 0F000h to 0FFFFh. 4-Kbyte space is mainly for storing data. In addition to storing data, 4-Kbyte space also can store programs.
The fixed interrupt vector table is allocated to the addresses from FFFDCh to FFFFFh. Therefore, store the start address of each interrupt routine here.
The internal RAM is allocated in an upper address direction beginning with address 00400h. For example, a 10-Kbyte internal RAM is allocated to the addresses from 00400h to 02BFFh. In addition to storing data, the internal RAM also stores the stack used when calling subroutines and when interrupts are generated.
The SRF is allocated to the addresses from 00000h to 003FFh. Peripheral function control registers are located here. Of the SFR, any area which has no functions allocated is reserved for future use and cannot be used by users.
The special page vector table is allocated to the addresses from FFE00h to FFFDBh. This vector is used by the JMPS or JSRS instruction. For details, refer to the **M16C/60 and M16C/20 Series Software Manual**.
In memory expansion and microprocessor modes, some areas are reserved for future use and cannot be used by users. Use M16C/62P (80-pin version) and M16C/62PT in single-chip mode. The memory expansion and microprocessor modes cannot be used
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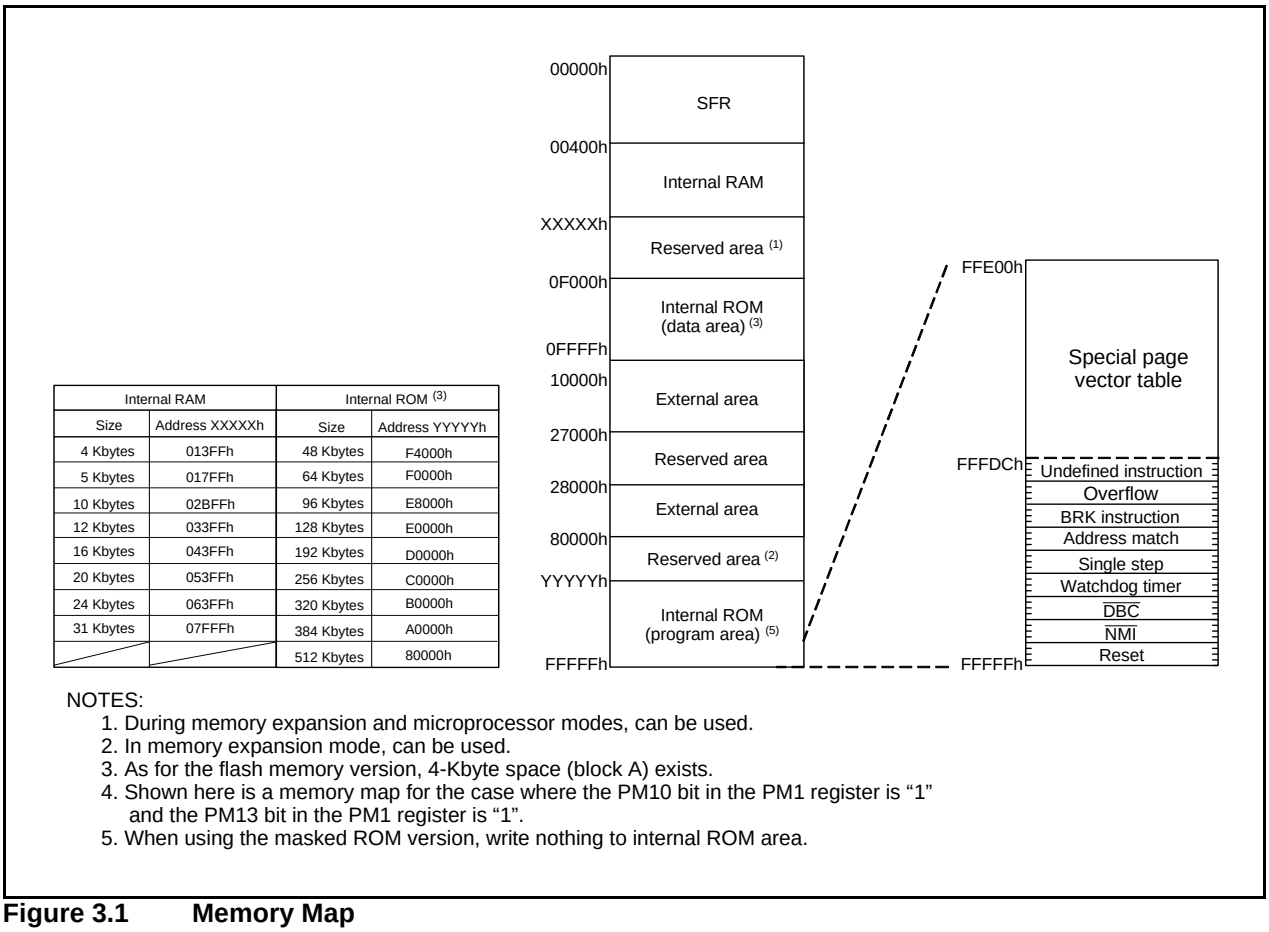



| Internal RAM | | Internal ROM (3) | |
|---|---|---|---|
| Size | Address XXXXXh | Size | Address YYYYYh |
| 4 Kbytes | 013FFh | 48 Kbytes | F4000h |
| 5 Kbytes | 017FFh | 64 Kbytes | F0000h |
| 10 Kbytes | 02BFFh | 96 Kbytes | E8000h |
| 12 Kbytes | 033FFh | 128 Kbytes | E0000h |
| 16 Kbytes | 043FFh | 192 Kbytes | D0000h |
| 20 Kbytes | 053FFh | 256 Kbytes | C0000h |
| 24 Kbytes | 063FFh | 320 Kbytes | B0000h |
| 31 Kbytes | 07FFFh | 384 Kbytes | A0000h |
| | | 512 Kbytes | 80000h |

NOTES:
1. During memory expansion and microprocessor modes, can be used.
2. In memory expansion mode, can be used.
3. As for the flash memory version, 4-Kbyte space (block A) exists.
4. Shown here is a memory map for the case where the PM10 bit in the PM1 register is “1” and the PM13 bit in the PM1 register is “1”.
5. When using the masked ROM version, write nothing to internal ROM area.

**Figure 3.1 Memory Map**

**Table 4.2 SFR Information (2)** (1)

| Address | Register | Symbol | After Reset |
|---|---|---|---|
| 0040h | | | |
| 0041h | | | |
| 0042h | | | |
| 0043h | | | |
| 0044h | INT3 Interrupt Control Register | INT3IC | XX00X000b |
| 0045h | Timer B5 Interrupt Control Register | TB5IC | XXXXX000b |
| 0046h | Timer B4 Interrupt Control Register, UART1 BUS Collision Detection Interrupt Control Register | TB4IC, U1BCNIC | XXXXX000b |
| 0047h | Timer B3 Interrupt Control Register, UART0 BUS Collision Detection Interrupt Control Register | TB3IC, U0BCNIC | XXXXX000b |
| 0048h | SI/O4 Interrupt Control Register, INT5 Interrupt Control Register | S4IC, INT5IC | XX00X000b |
| 0049h | SI/O3 Interrupt Control Register, INT4 Interrupt Control Register | S3IC, INT4IC | XX00X000b |
| 004Ah | UART2 Bus Collision Detection Interrupt Control Register | BCNIC | XXXXX000b |
| 004Bh | DMA0 Interrupt Control Register | DM0IC | XXXXX000b |
| 004Ch | DMA1 Interrupt Control Register | DM1IC | XXXXX000b |
| 004Dh | Key Input Interrupt Control Register | KUPIC | XXXXX000b |
| 004Eh | A/D Conversion Interrupt Control Register | ADIC | XXXXX000b |
| 004Fh | UART2 Transmit Interrupt Control Register | S2TIC | XXXXX000b |
| 0050h | UART2 Receive Interrupt Control Register | S2RIC | XXXXX000b |
| 0051h | UART0 Transmit Interrupt Control Register | S0TIC | XXXXX000b |
| 0052h | UART0 Receive Interrupt Control Register | S0RIC | XXXXX000b |
| 0053h | UART1 Transmit Interrupt Control Register | S1TIC | XXXXX000b |
| 0054h | UART1 Receive Interrupt Control Register | S1RIC | XXXXX000b |
| 0055h | Timer A0 Interrupt Control Register | TA0IC | XXXXX000b |
| 0056h | Timer A1 Interrupt Control Register | TA1IC | XXXXX000b |
| 0057h | Timer A2 Interrupt Control Register | TA2IC | XXXXX000b |
| 0058h | Timer A3 Interrupt Control Register | TA3IC | XXXXX000b |
| 0059h | Timer A4 Interrupt Control Register | TA4IC | XXXXX000b |
| 005Ah | Timer B0 Interrupt Control Register | TB0IC | XXXXX000b |
| 005Bh | Timer B1 Interrupt Control Register | TB1IC | XXXXX000b |
| 005Ch | Timer B2 Interrupt Control Register | TB2IC | XXXXX000b |
| 005Dh | INT0 Interrupt Control Register | INT0IC | XX00X000b |
| 005Eh | INT1 Interrupt Control Register | INT1IC | XX00X000b |
| 005Fh | INT2 Interrupt Control Register | INT2IC | XX00X000b |
| 0060h | | | |
| 0061h | | | |
| 0062h | | | |
| 0063h | | | |
| 0064h | | | |
| 0065h | | | |
| 0066h | | | |
| 0067h | | | |
| 0068h | | | |
| 0069h | | | |
| 006Ah | | | |
| 006Bh | | | |
| 006Ch | | | |
| 006Dh | | | |
| 006Eh | | | |
| 006Fh | | | |
| 0070h | | | |
| 0071h | | | |
| 0072h | | | |
| 0073h | | | |
| 0074h | | | |
| 0075h | | | |
| 0076h | | | |
| 0077h | | | |
| 0078h | | | |
| 0079h | | | |
| 007Ah | | | |
| 007Bh | | | |
| 007Ch | | | |
| 007Dh | | | |
| 007Eh | | | |
| 007Fh | | | |

NOTES:
1. The blank areas are reserved and cannot be accessed by users.

X : Nothing is mapped to this bit

**Table 5.6 Flash Memory Version Electrical Characteristics (1) for 100 cycle products (D3, D5, U3, U5)**

| Symbol | Parameter | | Standard | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| – | Program and Erase Endurance (3) | | 100 | | | cycle |
| – | Word Program Time ($V_{CC1}$=5.0V) | | | 25 | 200 | µs |
| – | Lock Bit Program Time | | | 25 | 200 | µs |
| – | Block Erase Time ($V_{CC1}$=5.0V) | 4-Kbyte block | | 0.3 | 4 | s |
| – | | 8-Kbyte block | | 0.3 | 4 | s |
| – | | 32-Kbyte block | | 0.5 | 4 | s |
| – | | 64-Kbyte block | | 0.8 | 4 | s |
| – | Erase All Unlocked Blocks Time (2) | | | | 4×n | s |
| $t_{PS}$ | Flash Memory Circuit Stabilization Wait Time | | | | 15 | µs |
| – | Data Hold Time (5) | | 10 | | | year |

**Table 5.7 Flash Memory Version Electrical Characteristics (6) for 10,000 cycle products (D7, D9, U7, U9) (Block A and Block 1 (7))**

| Symbol | Parameter | | Standard | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| – | Program and Erase Endurance (3, 8, 9) | | 10,000 (4) | | | cycle |
| – | Word Program Time ($V_{CC1}$=5.0V) | | | 25 | | µs |
| – | Lock Bit Program Time | | | 25 | | µs |
| – | Block Erase Time ($V_{CC1}$=5.0V) | 4-Kbyte block | | 0.3 | | s |
| $t_{PS}$ | Flash Memory Circuit Stabilization Wait Time | | | | 15 | µs |
| – | Data Hold Time (5) | | 10 | | | year |

NOTES:
1. Referenced to $V_{CC1}$=4.5 to 5.5V, 3.0 to 3.6V at Topr = 0 to 60 °C (D3, D5, U3, U5) unless otherwise specified.
2. n denotes the number of block erases.
3. Program and Erase Endurance refers to the number of times a block erase can be performed.
   If the program and erase endurance is n (n=100, 1,000, or 10,000), each block can be erased n times.
   For example, if a 4 Kbytes block A is erased after writing 1 word data 2,048 times, each to a different address, this counts as one program and erase endurance. Data cannot be written to the same address more than once without erasing the block. (Rewrite prohibited)
4. Maximum number of E/W cycles for which operation is guaranteed.
5. Topr = -40 to 85 °C (D3, D7, U3, U7) / -20 to 85 °C (D5, D9, U5, U9).
6. Referenced to $V_{CC1}$ = 4.5 to 5.5V, 3.0 to 3.6V at $T_{opr}$ = -40 to 85 °C (D7, U7) / -20 to 85 °C (D9, U9) unless otherwise specified.
7. Table 5.7 applies for block A or block 1 program and erase endurance > 1,000. Otherwise, use Table 5.6.
8. To reduce the number of program and erase endurance when working with systems requiring numerous rewrites, write to unused word addresses within the block instead of rewrite. Erase block only after all possible addresses are used. For example, an 8-word program can be written 256 times maximum before erase becomes necessary.
   Maintaining an equal number of erasure between block A and block 1 will also improve efficiency. It is important to track the total number of times erasure is used.
9. Should erase error occur during block erase, attempt to execute clear status register command, then block erase command at least three times until erase error disappears.
10. Set the PM17 bit in the PM1 register to “1” (wait state) when executing more than 100 times rewrites (D7, D9, U7 and U9).
11. Customers desiring E/W failure rate information should contact their Renesas technical support representative.

**Table 5.8 Flash Memory Version Program / Erase Voltage and Read Operation Voltage Characteristics (at $T_{opr}$ = 0 to 60 °C(D3, D5, U3, U5), $T_{opr}$ = -40 to 85 °C(D7, U7) / $T_{opr}$ = -20 to 85 °C(D9, U9))**

| Flash Program, Erase Voltage | Flash Read Operation Voltage |
|---|---|
| $V_{CC1}$ = 3.3 V ± 0.3 V or 5.0 V ± 0.5 V | $V_{CC1}$=2.7 to 5.5 V |

## $V_{CC1}=V_{CC2}=5V$

### Switching Characteristics

**($V_{CC1}$ = $V_{CC2}$ = 5V, $V_{SS}$ = 0V, at $T_{opr}$ = –20 to 85°C / –40 to 85°C unless otherwise specified)**

**Table 5.29 Memory Expansion and Microprocessor Modes (for 2- to 3-wait setting, external area access and multiplex bus selection)**

| Symbol | Parameter | | Standard | | Unit |
|---|---|---|---|---|---|
| | | | Min. | Max. | |
| td(BCLK-AD) | Address Output Delay Time | See **Figure 5.2** | | 25 | ns |
| th(BCLK-AD) | Address Output Hold Time (in relation to BCLK) | | 4 | | ns |
| th(RD-AD) | Address Output Hold Time (in relation to RD) | | (NOTE 1) | | ns |
| th(WR-AD) | Address Output Hold Time (in relation to WR) | | (NOTE 1) | | ns |
| td(BCLK-CS) | Chip Select Output Delay Time | | | 25 | ns |
| th(BCLK-CS) | Chip Select Output Hold Time (in relation to BCLK) | | 4 | | ns |
| th(RD-CS) | Chip Select Output Hold Time (in relation to RD) | | (NOTE 1) | | ns |
| th(WR-CS) | Chip Select Output Hold Time (in relation to WR) | | (NOTE 1) | | ns |
| td(BCLK-RD) | RD Signal Output Delay Time | | | 25 | ns |
| th(BCLK-RD) | RD Signal Output Hold Time | | 0 | | ns |
| td(BCLK-WR) | WR Signal Output Delay Time | | | 25 | ns |
| th(BCLK-WR) | WR Signal Output Hold Time | | 0 | | ns |
| td(BCLK-DB) | Data Output Delay Time (in relation to BCLK) | | | 40 | ns |
| th(BCLK-DB) | Data Output Hold Time (in relation to BCLK) | | 4 | | ns |
| td(DB-WR) | Data Output Delay Time (in relation to WR) | | (NOTE 2) | | ns |
| th(WR-DB) | Data Output Hold Time (in relation to WR) | | (NOTE 1) | | ns |
| td(BCLK-HLDA) | HLDA Output Delay Time | | | 40 | ns |
| td(BCLK-ALE) | ALE Signal Output Delay Time (in relation to BCLK) | | | 15 | ns |
| th(BCLK-ALE) | ALE Signal Output Hold Time (in relation to BCLK) | | –4 | | ns |
| td(AD-ALE) | ALE Signal Output Delay Time (in relation to Address) | | (NOTE 3) | | ns |
| th(AD-ALE) | ALE Signal Output Hold Time (in relation to Address) | | (NOTE 4) | | ns |
| td(AD-RD) | RD Signal Output Delay From the End of Address | | 0 | | ns |
| td(AD-WR) | WR Signal Output Delay From the End of Address | | 0 | | ns |
| tdz(RD-AD) | Address Output Floating Start Time | | | 8 | ns |

NOTES:

1. Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f(BCLK)} - 10[ns]$$

2. Calculated according to the BCLK frequency as follows:

$$\frac{(n-0.5) \times 10^9}{f(BCLK)} - 40[ns]$$

n is “2” for 2-wait setting, “3” for 3-wait setting.

3. Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f(BCLK)} - 25[ns]$$

4. Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f(BCLK)} - 15[ns]$$

## $V_{CC1}=V_{CC2}=3V$

**Table 5.30 Electrical Characteristics (1)** (1)

| Symbol | Parameter | | Measuring Condition | Standard | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | Max. | |
| $V_{OH}$ | HIGH Output Voltage (3) | P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P14_0, P14_1 | $I_{OH}$=–1mA | $V_{CC1}$–0.5 | | $V_{CC1}$ | V |
| | | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P12_0 to P12_7, P13_0 to P13_7 | $I_{OH}$=–1mA (2) | $V_{CC2}$–0.5 | | $V_{CC2}$ | |
| $V_{OH}$ | HIGH Output Voltage XOUT | HIGHPOWER | $I_{OH}$=–0.1mA | $V_{CC1}$–0.5 | | $V_{CC1}$ | V |
| | | LOWPOWER | $I_{OH}$=–50µA | $V_{CC1}$–0.5 | | $V_{CC1}$ | |
| | HIGH Output Voltage XCOUT | HIGHPOWER | With no load applied | | 2.5 | | V |
| | | LOWPOWER | With no load applied | | 1.6 | | |
| $V_{OL}$ | LOW Output Voltage (3) | P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P14_0, P14_1 | $I_{OL}$=1mA | | | 0.5 | V |
| | | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P12_0 to P12_7, P13_0 to P13_7 | $I_{OL}$=1mA (2) | | | 0.5 | |
| $V_{OL}$ | LOW Output Voltage XOUT | HIGHPOWER | $I_{OL}$=0.1mA | | | 0.5 | V |
| | | LOWPOWER | $I_{OL}$=50µA | | | 0.5 | |
| | LOW Output Voltage XCOUT | HIGHPOWER | With no load applied | | 0 | | V |
| | | LOWPOWER | With no load applied | | 0 | | |
| $V_{T+}$-$V_{T-}$ | Hysteresis | $\overline{HOLD}$, $\overline{RDY}$, TA0IN to TA4IN, $\overline{TB0IN}$ to $\overline{TB5IN}$, $\overline{INT0}$ to $\overline{INT5}$, $\overline{NMI}$, $\overline{ADTRG}$, $\overline{CTS0}$ to $\overline{CTS2}$, CLK0 to CLK4, TA0OUT to TA4OUT, $\overline{KI0}$ to $\overline{KI3}$, RXD0 to RXD2, SCL0 to SCL2, SDA0 to SDA2, SIN3, SIN4 | | 0.2 | | 0.8 | V |
| $V_{T+}$-$V_{T-}$ | Hysteresis | $\overline{RESET}$ | | 0.2 | (0.7) | 1.8 | V |
| $I_{IH}$ | HIGH Input Current (3) | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1, XIN, $\overline{RESET}$, CNVSS, BYTE | $V_I$=3V | | | 4.0 | µA |
| $I_{IL}$ | LOW Input Current (3) | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1, XIN, $\overline{RESET}$, CNVSS, BYTE | $V_I$=0V | | | –4.0 | µA |
| $R_{PULLUP}$ | Pull-Up Resistance (3) | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7,P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1 | $V_I$=0V | 50 | 100 | 500 | kΩ |
| $R_{fXIN}$ | Feedback Resistance XIN | | | | 3.0 | | MΩ |
| $R_{fXCIN}$ | Feedback Resistance XCIN | | | | 25 | | MΩ |
| $V_{RAM}$ | RAM Retention Voltage | | At stop mode | 2.0 | | | V |

NOTES:
1. Referenced to $V_{CC1}$ = $V_{CC2}$ = 2.7 to 3.3V, $V_{SS}$ = 0V at Topr = –20 to 85°C / –40 to 85°C, f(XIN)=10MHz no wait unless otherwise specified.
2. $V_{CC1}$ for the port P6 to P11 and P14, and $V_{CC2}$ for the port P0 to P5 and P12 to P13
3. There is no external connections for port P1_0 to P1_7, P4_4 to P4_7, P7_2 to P7_5 and P9_1 in 80-pin version.

# $V_{CC1}=V_{CC2}=3V$

**Timing Requirements**
**($V_{CC1}$ = $V_{CC2}$ = 3V, $V_{SS}$ = 0V, at $T_{opr}$ = –20 to 85°C / –40 to 85°C unless otherwise specified)**

**Table 5.40 Timer B Input (Counter Input in Event Counter Mode)**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(TB)}$ | TBiIN Input Cycle Time (counted on one edge) | 150 | | ns |
| $t_{w(TBH)}$ | TBiIN Input HIGH Pulse Width (counted on one edge) | 60 | | ns |
| $t_{w(TBL)}$ | TBiIN Input LOW Pulse Width (counted on one edge) | 60 | | ns |
| $t_{c(TB)}$ | TBiIN Input Cycle Time (counted on both edges) | 300 | | ns |
| $t_{w(TBH)}$ | TBiIN Input HIGH Pulse Width (counted on both edges) | 120 | | ns |
| $t_{w(TBL)}$ | TBiIN Input LOW Pulse Width (counted on both edges) | 120 | | ns |

**Table 5.41 Timer B Input (Pulse Period Measurement Mode)**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(TB)}$ | TBiIN Input Cycle Time | 600 | | ns |
| $t_{w(TBH)}$ | TBiIN Input HIGH Pulse Width | 300 | | ns |
| $t_{w(TBL)}$ | TBiIN Input LOW Pulse Width | 300 | | ns |

**Table 5.42 Timer B Input (Pulse Width Measurement Mode)**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(TB)}$ | TBiIN Input Cycle Time | 600 | | ns |
| $t_{w(TBH)}$ | TBiIN Input HIGH Pulse Width | 300 | | ns |
| $t_{w(TBL)}$ | TBiIN Input LOW Pulse Width | 300 | | ns |

**Table 5.43 A/D Trigger Input**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(AD)}$ | $\overline{\text{ADTRG}}$ Input Cycle Time | 1500 | | ns |
| $t_{w(ADL)}$ | $\overline{\text{ADTRG}}$ Input LOW Pulse Width | 200 | | ns |

**Table 5.44 Serial Interface**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(CK)}$ | CLKi Input Cycle Time | 300 | | ns |
| $t_{w(CKH)}$ | CLKi Input HIGH Pulse Width | 150 | | ns |
| $t_{w(CKL)}$ | CLKi Input LOW Pulse Width | 150 | | ns |
| $t_{d(C-Q)}$ | TXDi Output Delay Time | | 160 | ns |
| $t_{h(C-Q)}$ | TXDi Hold Time | 0 | | ns |
| $t_{su(D-C)}$ | RXDi Input Setup Time | 100 | | ns |
| $t_{h(C-D)}$ | RXDi Input Hold Time | 90 | | ns |

**Table 5.45 External Interrupt $\overline{\text{INTi}}$ Input**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{w(INH)}$ | $\overline{\text{INTi}}$ Input HIGH Pulse Width | 380 | | ns |
| $t_{w(INL)}$ | $\overline{\text{INTi}}$ Input LOW Pulse Width | 380 | | ns |

# $V_{CC1}=V_{CC2}=3V$

## Switching Characteristics

**($V_{CC1}$ = $V_{CC2}$ = 5V, $V_{SS}$ = 0V, at $T_{opr}$ = –20 to 85°C / –40 to 85°C unless otherwise specified)**

**Table 5.47 Memory Expansion and Microprocessor Modes (for 1- to 3-wait setting and external area access)**

| Symbol | Parameter | | Standard | | Unit |
|---|---|---|---|---|---|
| | | | Min. | Max. | |
| $t_{d(BCLK-AD)}$ | Address Output Delay Time | See **Figure 5.12** | | 30 | ns |
| $t_{h(BCLK-AD)}$ | Address Output Hold Time (in relation to BCLK) | | 4 | | ns |
| $t_{h(RD-AD)}$ | Address Output Hold Time (in relation to RD) | | 0 | | ns |
| $t_{h(WR-AD)}$ | Address Output Hold Time (in relation to WR) | | (NOTE 2) | | ns |
| $t_{d(BCLK-CS)}$ | Chip Select Output Delay Time | | | 30 | ns |
| $t_{h(BCLK-CS)}$ | Chip Select Output Hold Time (in relation to BCLK) | | 4 | | ns |
| $t_{d(BCLK-ALE)}$ | ALE Signal Output Delay Time | | | 25 | ns |
| $t_{h(BCLK-ALE)}$ | ALE Signal Output Hold Time | | -4 | | ns |
| $t_{d(BCLK-RD)}$ | RD Signal Output Delay Time | | | 30 | ns |
| $t_{h(BCLK-RD)}$ | RD Signal Output Hold Time | | 0 | | ns |
| $t_{d(BCLK-WR)}$ | WR Signal Output Delay Time | | | 30 | ns |
| $t_{h(BCLK-WR)}$ | WR Signal Output Hold Time | | 0 | | ns |
| $t_{d(BCLK-DB)}$ | Data Output Delay Time (in relation to BCLK) | | | 40 | ns |
| $t_{h(BCLK-DB)}$ | Data Output Hold Time (in relation to BCLK) (3) | | 4 | | ns |
| $t_{d(DB-WR)}$ | Data Output Delay Time (in relation to WR) | | (NOTE 1) | | ns |
| th(WR-DB) | Data Output Hold Time (in relation to WR)(3) | | (NOTE 2) | | ns |
| $t_{d(BCLK-HLDA)}$ | HLDA Output Delay Time | | | 40 | ns |

NOTES:

1. Calculated according to the BCLK frequency as follows:

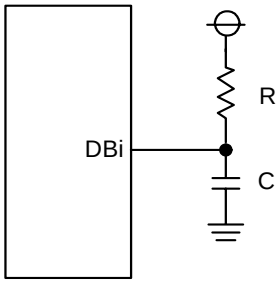
$$\frac{(n-0.5)\times 10^9}{f(BCLK)} - 40[ns]$$

n is “1” for 1-wait setting, “2” for 2-wait setting and “3” for 3-wait setting.
(BCLK) is 12.5MHz or less.

2. Calculated according to the BCLK frequency as follows:

$$\frac{0.5\times 10^9}{f(BCLK)} - 10[ns]$$

3. This standard value shows the timing when the output is off, and does not show hold time of data bus.
Hold time of data bus varies with capacitor volume and pull-up (pull-down) resistance value.
Hold time of data bus is expressed in
$t = -CR \times \ln(1 - V_{OL} / V_{CC2})$
by a circuit of the right figure.
For example, when $V_{OL}$ = 0.2$V_{CC2}$, C = 30pF, R = 1kΩ, hold time of output ”L” level is
$t = -30pF \times 1k\Omega \times \ln(1 - 0.2V_{CC2} / V_{CC2})$
= 6.7ns.



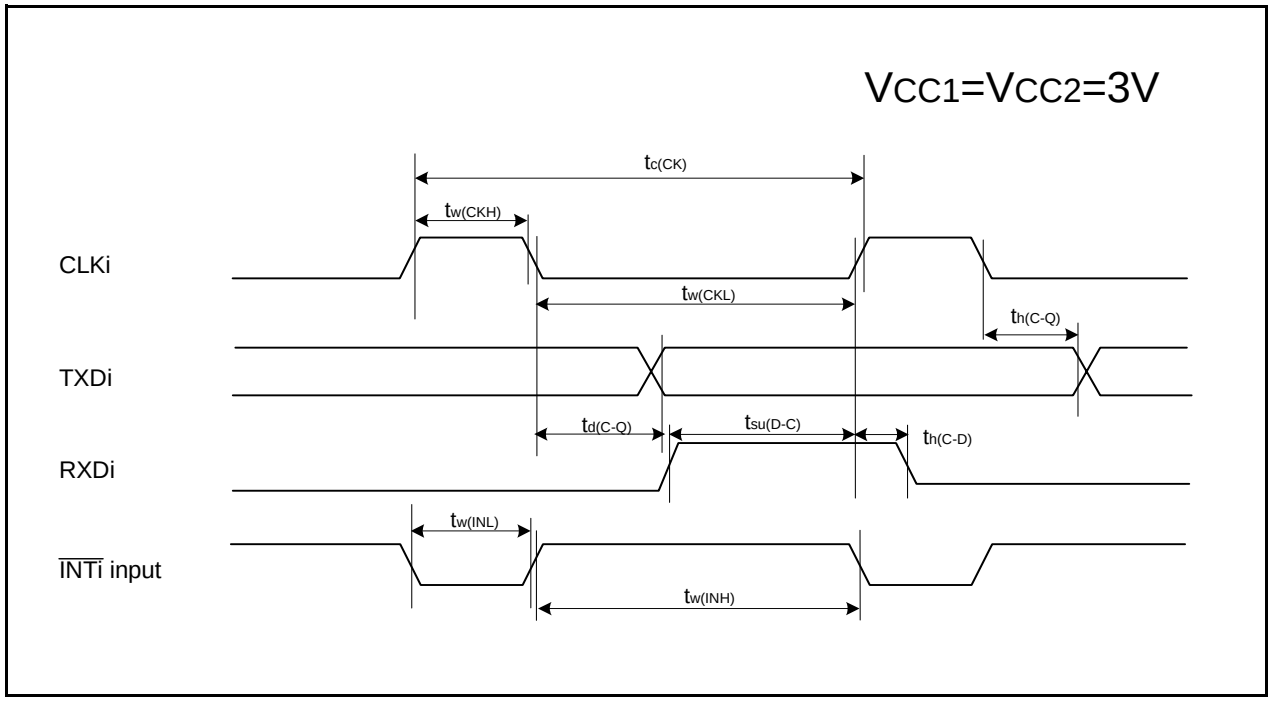
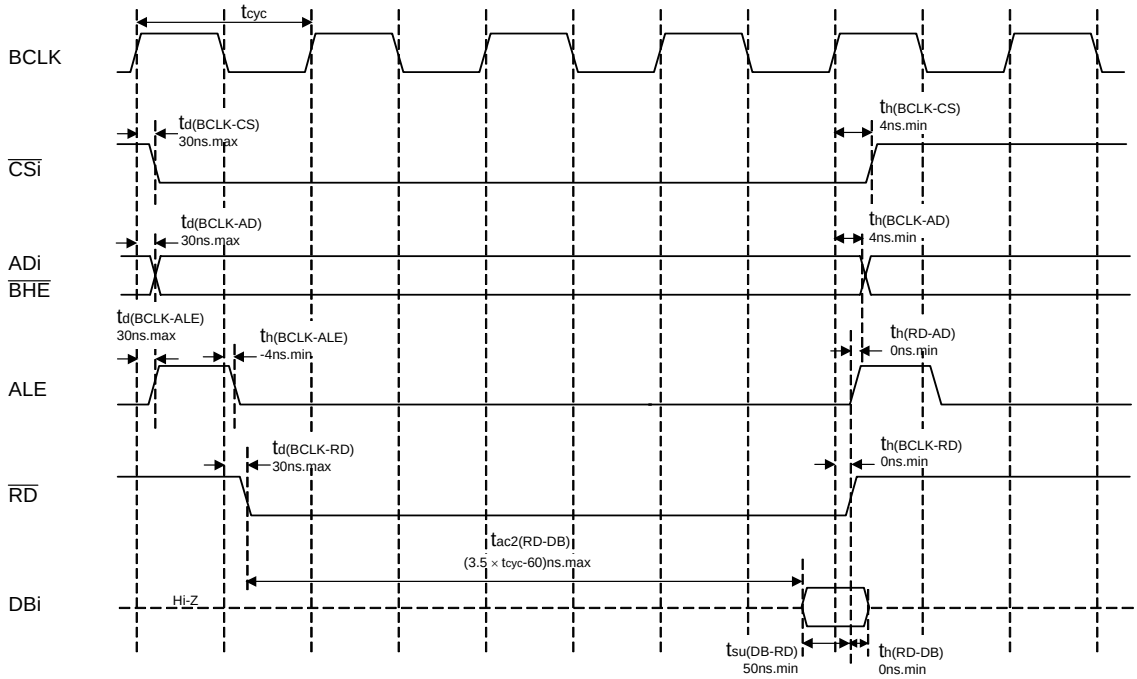



**Figure 5.14 Timing Diagram (2)**

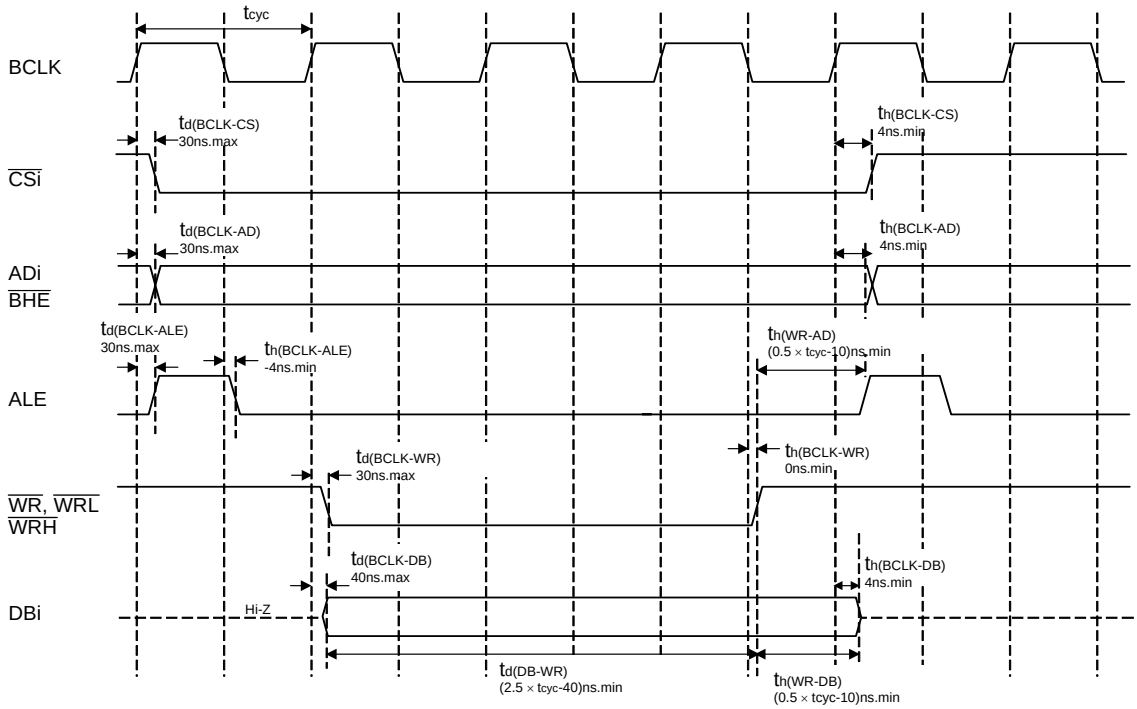
$V_{CC1} = V_{CC2} = 3V$

**Memory Expansion Mode, Microprocessor Mode**
**(**for 3-wait setting and external area access**)**

**Read timing**




**Write timing**




$$t_{cyc} = \frac{1}{f(BCLK)}$$

Measuring conditions
· $V_{CC1}$=$V_{CC2}$=3V
· Input timing voltage : $V_{IL}$=0.6V, $V_{IH}$=2.4V
· Output timing voltage : $V_{OL}$=1.5V, $V_{OH}$=1.5V

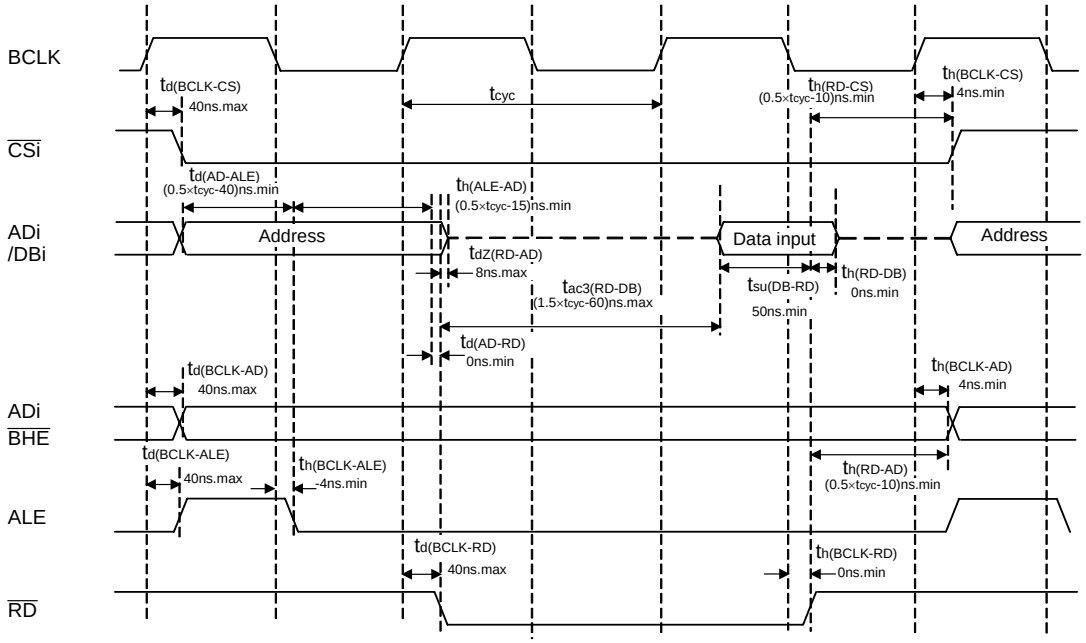
**Figure 5.19 Timing Diagram (7)**

## Memory Expansion Mode, Microprocessor Mode

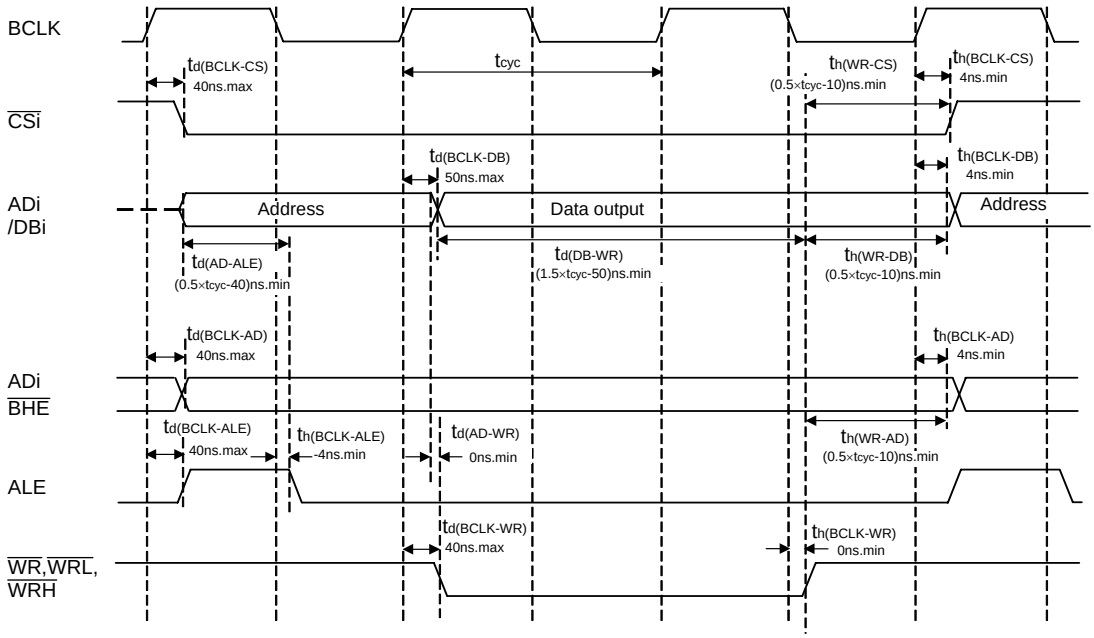
$V_{CC1}=V_{CC2}=3V$

**(**For 2-wait setting, external area access and multiplex bus selection**)**

**Read timing**




**Write timing**




$$t_{cyc}=\frac{1}{f(BCLK)}$$

Measuring conditions
- $V_{CC1}=V_{CC2}=3V$
- Input timing voltage : $V_{IL}=0.6V$, $V_{IH}=2.4V$
- Output timing voltage : $V_{OL}=1.5V$, $V_{OH}=1.5V$

**Figure 5.20 Timing Diagram (8)**

## 5.2 Electrical Characteristics (M16C/62PT)

**Table 5.49 Absolute Maximum Ratings**

| Symbol | Parameter | | Condition | Rated Value | Unit |
|---|---|---|---|---|---|
| $V_{CC1}$, $V_{CC2}$ | Supply Voltage | | $V_{CC1}$=$V_{CC2}$=AVcc | –0.3 to 6.5 | V |
| AVcc | Analog Supply Voltage | | $V_{CC1}$=$V_{CC2}$=AVcc | –0.3 to 6.5 | V |
| $V_I$ | Input Voltage | $\overline{\text{RESET}}$, CNVSS, BYTE, P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P14_0, P14_1, VREF, XIN | | –0.3 to $V_{CC1}$+0.3 (1) | V |
| | | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P12_0 to P12_7, P13_0 to P13_7 | | –0.3 to $V_{CC2}$+0.3 (1) | V |
| | | P7_0, P7_1 | | –0.3 to 6.5 | V |
| $V_O$ | Output Voltage | P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P14_0, P14_1, XOUT | | –0.3 to $V_{CC1}$+0.3 (1) | V |
| | | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P12_0 to P12_7, P13_0 to P13_7 | | –0.3 to $V_{CC2}$+0.3 (1) | V |
| | | P7_0, P7_1 | | –0.3 to 6.5 | V |
| $P_d$ | Power Dissipation | | –40°C<$T_{opr}$≤85°C | 300 | mW |
| | | | 85°C<$T_{opr}$≤125°C | 200 | |
| $T_{opr}$ | Operating Ambient Temperature | When the Microcomputer is Operating | | –40 to 85 / –40 to 125 (2) | °C |
| | | Flash Program Erase | | 0 to 60 | |
| $T_{stg}$ | Storage Temperature | | | –65 to 150 | °C |

NOTES:
1. There is no external connections for port P1_0 to P1_7, P4_4 to P4_7, P7_2 to P7_5 and P9_1 in 80-pin version.
2. T version = –40 to 85 °C, V version= –40 to 125 °C.

# $V_{CC1}=V_{CC2}=5V$

**Timing Requirements**
**($V_{CC1}$ = $V_{CC2}$ = 5V, $V_{SS}$ = 0V, at $T_{opr}$ = –40 to 85°C (T version) / –40 to 125°C (V version) unless otherwise specified)**

**Table 5.59 External Clock Input (XIN input)**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_c$ | External Clock Input Cycle Time | 62.5 | | ns |
| $t_{w(H)}$ | External Clock Input HIGH Pulse Width | 25 | | ns |
| $t_{w(L)}$ | External Clock Input LOW Pulse Width | 25 | | ns |
| $t_r$ | External Clock Rise Time | | 15 | ns |
| $t_f$ | External Clock Fall Time | | 15 | ns |

# $V_{CC1}$=$V_{CC2}$=5V

**Timing Requirements**
**($V_{CC1}$ = $V_{CC2}$ = 5V, $V_{SS}$ = 0V, at $T_{opr}$ = –40 to 85°C (T version) / –40 to 125°C (V version) unless otherwise specified)**

**Table 5.60 Timer A Input (Counter Input in Event Counter Mode)**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(TA)}$ | TAiIN Input Cycle Time | 100 | | ns |
| $t_{w(TAH)}$ | TAiIN Input HIGH Pulse Width | 40 | | ns |
| $t_{w(TAL)}$ | TAiIN Input LOW Pulse Width | 40 | | ns |

**Table 5.61 Timer A Input (Gating Input in Timer Mode)**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(TA)}$ | TAiIN Input Cycle Time | 400 | | ns |
| $t_{w(TAH)}$ | TAiIN Input HIGH Pulse Width | 200 | | ns |
| $t_{w(TAL)}$ | TAiIN Input LOW Pulse Width | 200 | | ns |

**Table 5.62 Timer A Input (External Trigger Input in One-shot Timer Mode)**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(TA)}$ | TAiIN Input Cycle Time | 200 | | ns |
| $t_{w(TAH)}$ | TAiIN Input HIGH Pulse Width | 100 | | ns |
| $t_{w(TAL)}$ | TAiIN Input LOW Pulse Width | 100 | | ns |

**Table 5.63 Timer A Input (External Trigger Input in Pulse Width Modulation Mode)**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{w(TAH)}$ | TAiIN Input HIGH Pulse Width | 100 | | ns |
| $t_{w(TAL)}$ | TAiIN Input LOW Pulse Width | 100 | | ns |

**Table 5.64 Timer A Input (Counter Increment/Decrement Input in Event Counter Mode)**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(UP)}$ | TAiOUT Input Cycle Time | 2000 | | ns |
| $t_{w(UPH)}$ | TAiOUT Input HIGH Pulse Width | 1000 | | ns |
| $t_{w(UPL)}$ | TAiOUT Input LOW Pulse Width | 1000 | | ns |
| $t_{su(UP-TIN)}$ | TAiOUT Input Setup Time | 400 | | ns |
| $t_{h(TIN-UP)}$ | TAiOUT Input Hold Time | 400 | | ns |

**Table 5.65 Timer A Input (Two-phase Pulse Input in Event Counter Mode)**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(TA)}$ | TAiIN Input Cycle Time | 800 | | ns |
| $t_{su(TAIN-TAOUT)}$ | TAiOUT Input Setup Time | 200 | | ns |
| $t_{su(TAOUT-TAIN)}$ | TAiIN Input Setup Time | 200 | | ns |

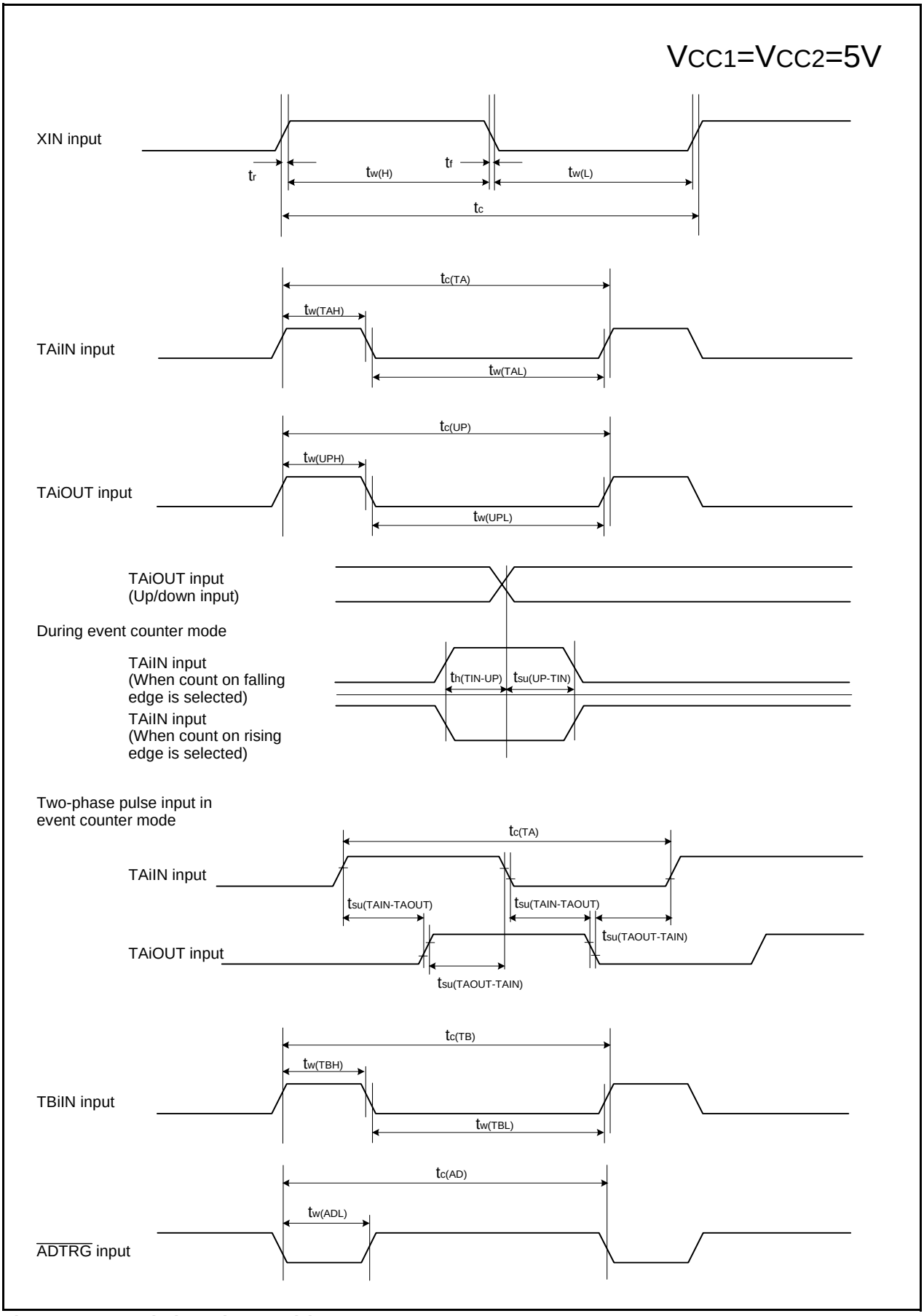



**Figure 5.24 Timing Diagram (1)**

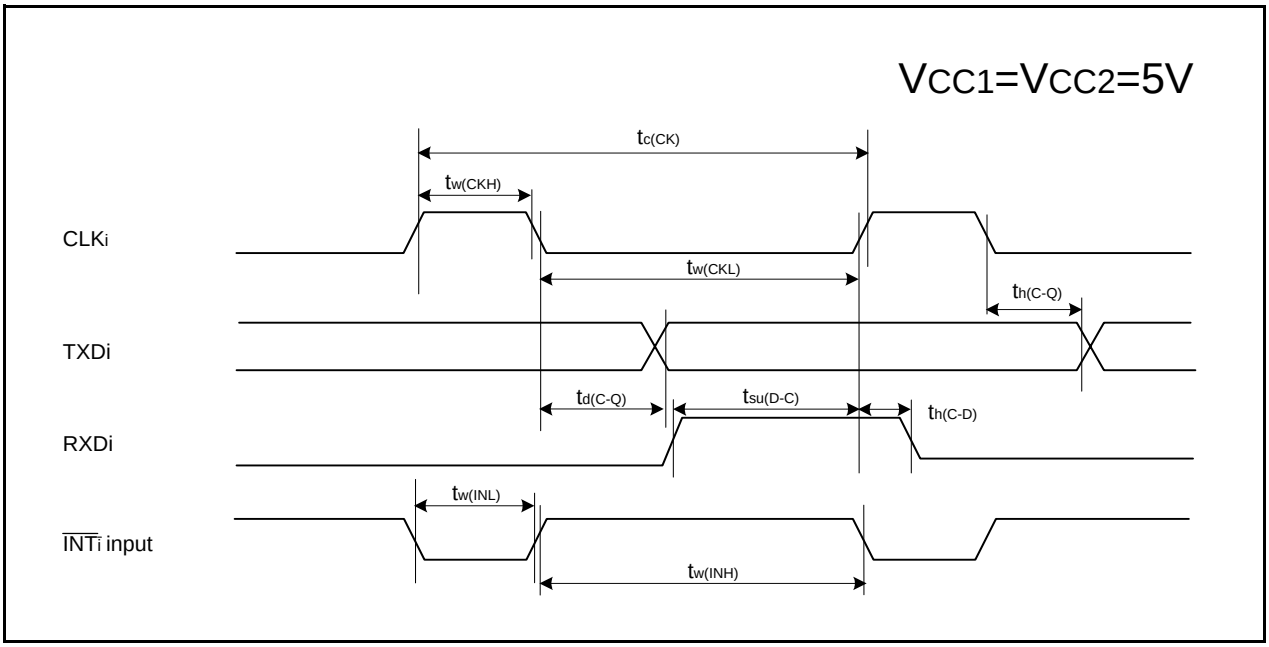



**Figure 5.25 Timing Diagram (2)**