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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Not For New Designs
Core Processor	M16C/60
Core Size	16-Bit
Speed	24MHz
Connectivity	I ² C, IEBus, UART/USART
Peripherals	DMA, WDT
Number of I/O	85
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	31K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 26x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-BQFP
Supplier Device Package	100-QFP (14x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/m30626fjfp-u3c

1.2 Performance Outline

Table 1.1 to 1.3 list Performance Outline of M16C/62P Group (M16C/62P, M16C/62PT)(128-pin version).

Table 1.1 Performance Outline of M16C/62P Group (M16C/62P, M16C/62PT)(128-pin version)

	Item	Performance
		M16C/62P
CPU	Number of Basic Instructions	91 instructions
	Minimum Instruction Execution Time	41.7ns(f(BCLK)=24MHz, VCC1=3.3 to 5.5V) 100ns(f(BCLK)=10MHz, VCC1=2.7 to 5.5V)
	Operating Mode	Single-chip, memory expansion and microprocessor mode
	Address Space	1 Mbyte (Available to 4 Mbytes by memory space expansion function)
	Memory Capacity	See Table 1.4 to 1.5 Product List
Peripheral Function	Port	Input/Output : 113 pins, Input : 1 pin
	Multifunction Timer	Timer A : 16 bits x 5 channels, Timer B : 16 bits x 6 channels, Three phase motor control circuit
	Serial Interface	3 channels Clock synchronous, UART, I ² C bus ⁽¹⁾ , IEBus ⁽²⁾ 2 channels Clock synchronous
	A/D Converter	10-bit A/D converter: 1 circuit, 26 channels
	D/A Converter	8 bits x 2 channels
	DMAC	2 channels
	CRC Calculation Circuit	CCITT-CRC
	Watchdog Timer	15 bits x 1 channel (with prescaler)
	Interrupt	Internal: 29 sources, External: 8 sources, Software: 4 sources, Priority level: 7 levels
	Clock Generation Circuit	4 circuits Main clock generation circuit (*), Subclock generation circuit (*), On-chip oscillator, PLL synthesizer (*)Equipped with a built-in feedback resistor.
	Oscillation Stop Detection Function	Stop detection of main clock oscillation, re-oscillation detection function
	Voltage Detection Circuit	Available (option ⁽⁴⁾)
Electric Characteristics	Supply Voltage	VCC1=3.0 to 5.5 V, VCC2=2.7V to VCC1 (f(BCLK)=24MHz) VCC1=2.7 to 5.5 V, VCC2=2.7V to VCC1 (f(BCLK)=10MHz)
	Power Consumption	14 mA (VCC1=VCC2=5V, f(BCLK)=24MHz) 8 mA (VCC1=VCC2=3V, f(BCLK)=10MHz) 1.8μA (VCC1=VCC2=3V, f(XCIN)=32kHz, wait mode) 0.7μA (VCC1=VCC2=3V, stop mode)
Flash memory version	Program/Erase Supply Voltage	3.3±0.3 V or 5.0±0.5 V
	Program and Erase Endurance	100 times (all area) or 1,000 times (user ROM area without block A and block 1) / 10,000 times (block A, block 1) ⁽³⁾
Operating Ambient Temperature		-20 to 85°C, -40 to 85°C ⁽³⁾
Package		128-pin plastic mold LQFP

NOTES:

1. I²C bus is a registered trademark of Koninklijke Philips Electronics N. V.
2. IEBus is a registered trademark of NEC Electronics Corporation.
3. See **Table 1.8 Product Code** for the program and erase endurance, and operating ambient temperature. In addition 1,000 times/10,000 times are under development as of Jul., 2005. Please inquire about a release schedule.
4. All options are on request basis.

1.4 Product List

Table 1.4 to 1.7 list the product list, Figure 1.3 shows the Type No., Memory Size, and Package, Table 1.8 lists the Product Code of Flash Memory version and ROMless version for M16C/62P, and Table 1.9 lists the Product Code of Flash Memory version for M16C/62PT. Figure 1.4 shows the Marking Diagram of Flash Memory version and ROM-less version for M16C/62P (Top View), and Figure 1.5 shows the Marking Diagram of Flash Memory version for M16C/62PT (Top View) at the time of ROM order.

Table 1.4 Product List (1) (M16C/62P)

As of Dec. 2005

Type No.	ROM Capacity	RAM Capacity	Package Type ⁽¹⁾	Remarks
M30622M6P-XXXFP	48 Kbytes	4 Kbytes	PRQP0100JB-A	Mask ROM version
M30622M6P-XXXGP			PLQP0100KB-A	
M30622M8P-XXXFP	64 Kbytes	4 Kbytes	PRQP0100JB-A	
M30622M8P-XXXGP			PLQP0100KB-A	
M30623M8P-XXXGP			PRQP0080JA-A	
M30622MAP-XXXFP	96 Kbytes	5 Kbytes	PRQP0100JB-A	
M30622MAP-XXXGP			PLQP0100KB-A	
M30623MAP-XXXGP			PRQP0080JA-A	
M30620MCP-XXXFP	128 Kbytes	10 Kbytes	PRQP0100JB-A	
M30620MCP-XXXGP			PLQP0100KB-A	
M30621MCP-XXXGP			PRQP0080JA-A	
M30622MEP-XXXFP	192 Kbytes	12 Kbytes	PRQP0100JB-A	
M30622MEP-XXXGP			PLQP0100KB-A	
M30623MEP-XXXGP			PLQP0128KB-A	
M30622MGP-XXXFP	256 Kbytes	12 Kbytes	PRQP0100JB-A	
M30622MGP-XXXGP			PLQP0100KB-A	
M30623MGP-XXXGP			PLQP0128KB-A	
M30624MGP-XXXFP		20 Kbytes	PRQP0100JB-A	
M30624MGP-XXXGP			PLQP0100KB-A	
M30625MGP-XXXGP			PLQP0128KB-A	
M30622MWP-XXXFP			PRQP0100JB-A	
M30622MWP-XXXGP	320 Kbytes	16 Kbytes	PLQP0100KB-A	
M30623MWP-XXXGP			PLQP0128KB-A	
M30624MWP-XXXFP		24 Kbytes	PRQP0100JB-A	
M30624MWP-XXXGP			PLQP0100KB-A	
M30625MWP-XXXGP			PLQP0128KB-A	
M30626MWP-XXXFP		31 Kbytes	PRQP0100JB-A	
M30626MWP-XXXGP			PLQP0100KB-A	
M30627MWP-XXXGP			PLQP0128KB-A	

(D): Under development

NOTES:

- The old package type numbers of each package type are as follows.

PLQP0128KB-A : 128P6Q-A,
 PRQP0100JB-A : 100P6S-A,
 PLQP0100KB-A : 100P6Q-A,
 PRQP0080JA-A : 80P6S-A

Table 1.5 Product List (2) (M16C/62P)

As of Dec. 2005

Type No.	ROM Capacity	RAM Capacity	Package Type ⁽¹⁾	Remarks
M30622MHP-XXXFP	384 Kbytes	16 Kbytes	PRQP0100JB-A	Mask ROM version
M30622MHP-XXXGP			PLQP0100KB-A	
M30623MHP-XXXGP			PLQP0128KB-A	
M30624MHP-XXXFP		24 Kbytes	PRQP0100JB-A	
M30624MHP-XXXGP			PLQP0100KB-A	
M30625MHP-XXXGP			PLQP0128KB-A	
M30626MHP-XXXFP		31 Kbytes	PRQP0100JB-A	
M30626MHP-XXXGP			PLQP0100KB-A	
M30627MHP-XXXGP			PLQP0128KB-A	
M30626MJP-XXXFP (D)	512 Kbytes	31 Kbytes	PRQP0100JB-A	Flash memory version ⁽²⁾
M30626MJP-XXXGP (D)			PLQP0100KB-A	
M30627MJP-XXXGP (D)			PLQP0128KB-A	
M30622F8PFP	64K+4 Kbytes	4 Kbytes	PRQP0100JB-A	
M30622F8PGP			PLQP0100KB-A	
M30623F8PGP			PRQP0080JA-A	
M30620FCPFP	128K+4 Kbytes	10 Kbytes	PRQP0100JB-A	
M30620FCPGP			PLQP0100KB-A	
M30621FCPGP			PRQP0080JA-A	
M3062LFGPFP ⁽³⁾ (D)	256K+4 Kbytes	20 Kbytes	PRQP0100JB-A	
M3062LFGPGP ⁽³⁾ (D)			PLQP0100KB-A	
M30625FGPGP			PLQP0128KB-A	
M30626FHPFP	384K+4 Kbytes	31 Kbytes	PRQP0100JB-A	ROM-less version
M30626FHPPGP			PLQP0100KB-A	
M30627FHPPGP			PLQP0128KB-A	
M30626FJPFP	512K+4 Kbytes	31 Kbytes	PRQP0100JB-A	
M30626FJPPGP			PLQP0100KB-A	
M30627FJPPGP			PLQP0128KB-A	
M30622SPFP	–	4 Kbytes	PRQP0100JB-A	
M30622SPGP			PLQP0100KB-A	
M30620SPFP		10 Kbytes	PRQP0100JB-A	
M30620SPGP			PLQP0100KB-A	
M30624SPFP (D)	–	20 Kbytes	PRQP0100JB-A	
M30624SPGP (D)			PLQP0100KB-A	
M30626SPFP (D)		31 Kbytes	PRQP0100JB-A	
M30626SPGP (D)			PLQP0100KB-A	

(D): Under development

NOTES:

- The old package type numbers of each package type are as follows.
 PLQP0128KB-A : 128P6Q-A,
 PRQP0100JB-A : 100P6S-A,
 PLQP0100KB-A : 100P6Q-A,
 PRQP0080JA-A : 80P6S-A
- In the flash memory version, there is 4K bytes area (block A).
- Please use M3062LFGPFP and M3062LFGPGP for your new system instead of M30624FGPFP and M30624FGPGP. The M16C/62P Group (M16C/62P, M16C/62PT) hardware manual is still good for M30624FGPFP and M30624FGPGP.

M30624FGPFP	256K+4 Kbytes	20 Kbytes	PRQP0100JB-A	Flash memory version
M30624FGPGP			PLQP0100KB-A	

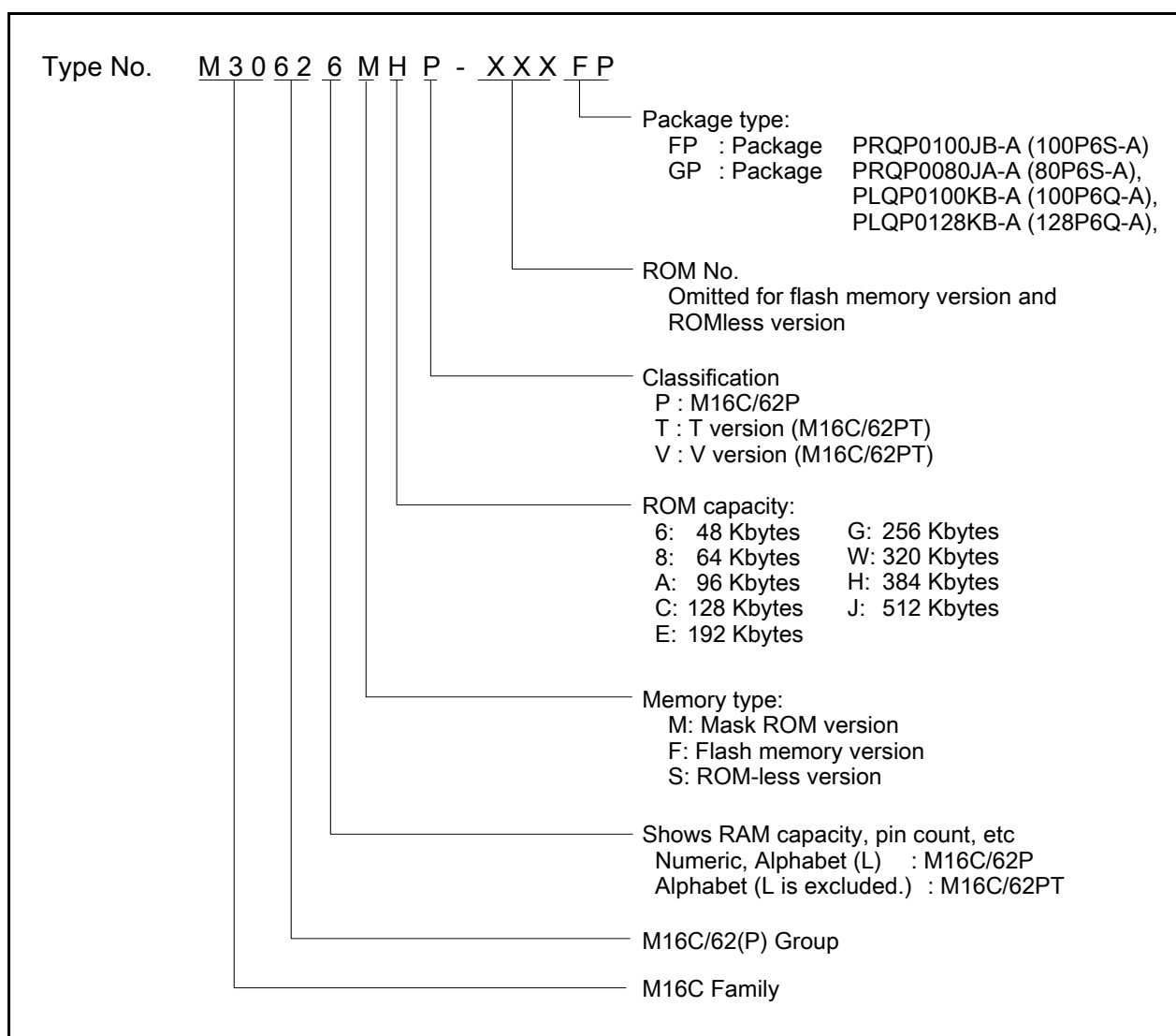
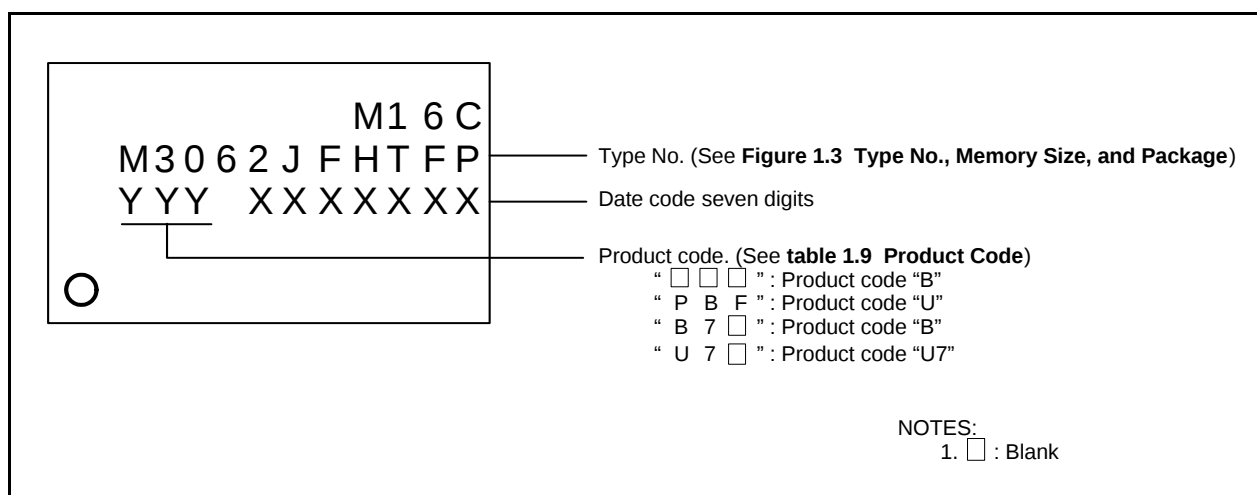


Figure 1.3 Type No., Memory Size, and Package

Table 1.9 Product Code of Flash Memory version for M16C/62PT

		Product Code	Package	Internal ROM (User ROM Area Without Block A, Block 1)		Internal ROM (Block A, Block 1)		Operating Ambient Temperature
				Program and Erase Endurance	Temperature Range	Program and Erase Endurance	Temperature Range	
Flash memory Version	T Version	B	Lead- included	100	0°C to 60°C	100	0°C to 60°C	-40°C to 85°C
	V Version							-40°C to 125°C
	T Version	B7		1,000		10,000	-40°C to 85°C	-40°C to 85°C
	V Version						-40°C to 125°C	-40°C to 125°C
	T Version	U	Lead-free	100		100	0°C to 60°C	-40°C to 85°C
	V Version							-40°C to 125°C
	T Version	U7		1,000		10,000	-40°C to 85°C	-40°C to 85°C
	V Version						-40°C to 125°C	-40°C to 125°C

**Figure 1.5 Marking Diagram of Flash Memory version for M16C/62PT (Top View)**

2.8.8 Stack Pointer Select Flag (U Flag)

ISP is selected when the U flag is “0”; USP is selected when the U flag is “1”.

The U flag is cleared to “0” when a hardware interrupt request is accepted or an INT instruction for software interrupt Nos. 0 to 31 is executed.

2.8.9 Processor Interrupt Priority Level (IPL)

IPL is configured with three bits, for specification of up to eight processor interrupt priority levels from level 0 to level 7.

If a requested interrupt has priority greater than IPL, the interrupt is enabled.

2.8.10 Reserved Area

When write to this bit, write “0”. When read, its content is indeterminate.

Table 4.2 SFR Information (2) ⁽¹⁾

Address	Register	Symbol	After Reset
0040h			
0041h			
0042h			
0043h			
0044h	INT3 Interrupt Control Register	INT3IC	XX00X000b
0045h	Timer B5 Interrupt Control Register	TB5IC	XXXXX000b
0046h	Timer B4 Interrupt Control Register, UART1 BUS Collision Detection Interrupt Control Register	TB4IC, U1BCNIC	XXXXX000b
0047h	Timer B3 Interrupt Control Register, UART0 BUS Collision Detection Interrupt Control Register	TB3IC, U0BCNIC	XXXXX000b
0048h	SI/O4 Interrupt Control Register, INT5 Interrupt Control Register	S4IC, INT5IC	XX00X000b
0049h	SI/O3 Interrupt Control Register, INT4 Interrupt Control Register	S3IC, INT4IC	XX00X000b
004Ah	UART2 Bus Collision Detection Interrupt Control Register	BCNIC	XXXXX000b
004Bh	DMA0 Interrupt Control Register	DM0IC	XXXXX000b
004Ch	DMA1 Interrupt Control Register	DM1IC	XXXXX000b
004Dh	Key Input Interrupt Control Register	KUPIC	XXXXX000b
004Eh	A/D Conversion Interrupt Control Register	ADIC	XXXXX000b
004Fh	UART2 Transmit Interrupt Control Register	S2TIC	XXXXX000b
0050h	UART2 Receive Interrupt Control Register	S2RIC	XXXXX000b
0051h	UART0 Transmit Interrupt Control Register	S0TIC	XXXXX000b
0052h	UART0 Receive Interrupt Control Register	S0RIC	XXXXX000b
0053h	UART1 Transmit Interrupt Control Register	S1TIC	XXXXX000b
0054h	UART1 Receive Interrupt Control Register	S1RIC	XXXXX000b
0055h	Timer A0 Interrupt Control Register	TA0IC	XXXXX000b
0056h	Timer A1 Interrupt Control Register	TA1IC	XXXXX000b
0057h	Timer A2 Interrupt Control Register	TA2IC	XXXXX000b
0058h	Timer A3 Interrupt Control Register	TA3IC	XXXXX000b
0059h	Timer A4 Interrupt Control Register	TA4IC	XXXXX000b
005Ah	Timer B0 Interrupt Control Register	TB0IC	XXXXX000b
005Bh	Timer B1 Interrupt Control Register	TB1IC	XXXXX000b
005Ch	Timer B2 Interrupt Control Register	TB2IC	XXXXX000b
005Dh	INT0 Interrupt Control Register	INT0IC	XX00X000b
005Eh	INT1 Interrupt Control Register	INT1IC	XX00X000b
005Fh	INT2 Interrupt Control Register	INT2IC	XX00X000b
0060h			
0061h			
0062h			
0063h			
0064h			
0065h			
0066h			
0067h			
0068h			
0069h			
006Ah			
006Bh			
006Ch			
006Dh			
006Eh			
006Fh			
0070h			
0071h			
0072h			
0073h			
0074h			
0075h			
0076h			
0077h			
0078h			
0079h			
007Ah			
007Bh			
007Ch			
007Dh			
007Eh			
007Fh			

NOTES:

1. The blank areas are reserved and cannot be accessed by users.

X : Nothing is mapped to this bit

Table 4.6 SFR Information (6) ⁽¹⁾

Address	Register	Symbol	After Reset
03C0h 03C1h	A/D Register 0	AD0	XXh XXh
03C2h 03C3h	A/D Register 1	AD1	XXh XXh
03C4h 03C5h	A/D Register 2	AD2	XXh XXh
03C6h 03C7h	A/D Register 3	AD3	XXh XXh
03C8h 03C9h	A/D Register 4	AD4	XXh XXh
03CAh 03CBh	A/D Register 5	AD5	XXh XXh
03CCh 03CDh	A/D Register 6	AD6	XXh XXh
03CEh 03CFh	A/D Register 7	AD7	XXh XXh
03D0h			
03D1h			
03D2h			
03D3h			
03D4h 03D5h	A/D Control Register 2	ADCON2	00h
03D6h	A/D Control Register 0	ADCON0	00000XXXb
03D7h	A/D Control Register 1	ADCON1	00h
03D8h 03D9h	D/A Register 0	DA0	00h
03DAh	D/A Register 1	DA1	00h
03DBh			
03DCh 03DDh	D/A Control Register	DACON	00h
03DEh	Port P14 Control Register ⁽³⁾	PC14	XX00XXXXb
03DFh	Pull-Up Control Register 3 ⁽³⁾	PUR3	00h
03E0h	Port P0 Register	P0	XXh
03E1h	Port P1 Register	P1	XXh
03E2h	Port P0 Direction Register	PD0	00h
03E3h	Port P1 Direction Register	PD1	00h
03E4h	Port P2 Register	P2	XXh
03E5h	Port P3 Register	P3	XXh
03E6h	Port P2 Direction Register	PD2	00h
03E7h	Port P3 Direction Register	PD3	00h
03E8h	Port P4 Register	P4	XXh
03E9h	Port P5 Register	P5	XXh
03EAh	Port P4 Direction Register	PD4	00h
03EBh	Port P5 Direction Register	PD5	00h
03ECh	Port P6 Register	P6	XXh
03EDh	Port P7 Register	P7	XXh
03EEh	Port P6 Direction Register	PD6	00h
03EFh	Port P7 Direction Register	PD7	00h
03F0h	Port P8 Register	P8	XXh
03F1h	Port P9 Register	P9	XXh
03F2h	Port P8 Direction Register	PD8	00X00000b
03F3h	Port P9 Direction Register	PD9	00h
03F4h	Port P10 Register	P10	XXh
03F5h	Port P11 Register ⁽³⁾	P11	XXh
03F6h	Port P10 Direction Register	PD10	00h
03F7h	Port P11 Direction Register ⁽³⁾	PD11	00h
03F8h	Port P12 Register ⁽³⁾	P12	XXh
03F9h	Port P13 Register ⁽³⁾	P13	XXh
03FAh	Port P12 Direction Register ⁽³⁾	PD12	00h
03FBh	Port P13 Direction Register ⁽³⁾	PD13	00h
03FCh	Pull-Up Control Register 0	PUR0	00h
03FDh	Pull-Up Control Register 1	PUR1	00000000b ⁽²⁾ 00000010b ⁽²⁾
03FEh	Pull-Up Control Register 2	PUR2	00h
03FFh	Port Control Register	PCR	00h

NOTES:

- The blank areas are reserved and cannot be accessed by users.
- At hardware reset 1 or hardware reset 2, the register is as follows:
 - "00000000b" where "L" is inputted to the CNVSS pin
 - "00000010b" where "H" is inputted to the CNVSS pin
 At software reset, watchdog timer reset and oscillation stop detection reset, the register is as follows:
 - "00000000b" where the PM01 to PM00 bits in the PM0 register are "00b" (single-chip mode).
 - "00000010b" where the PM01 to PM00 bits in the PM0 register are "01b" (memory expansion mode) or "11b" (microprocessor mode).
- These registers do not exist in M16C/62P (80-pin version), and M16C/62PT (80-pin version).

X : Nothing is mapped to this bit

Table 5.4 A/D Conversion Characteristics (1)

Symbol	Parameter		Measuring Condition		Standard			Unit
					Min.	Typ.	Max.	
–	Resolution		VREF=VCC1				10	Bits
INL	Integral Non-Linearity Error	10bit	VREF=VCC1=5V	AN0 to AN7 input, AN0_0 to AN0_7 input, AN2_0 to AN2_7 input, ANEX0, ANEX1 input			±3	LSB
				External operation amp connection mode			±7	LSB
			VREF=VCC1=3.3V	AN0 to AN7 input, AN0_0 to AN0_7 input, AN2_0 to AN2_7 input, ANEX0, ANEX1 input			±5	LSB
				External operation amp connection mode			±7	LSB
		8bit	VREF=VCC1=5V, 3.3V				±2	LSB
		–	Absolute Accuracy	10bit	VREF=VCC1=5V	AN0 to AN7 input, AN0_0 to AN0_7 input, AN2_0 to AN2_7 input, ANEX0, ANEX1 input		
External operation amp connection mode						±7	LSB	
VREF=VCC1=3.3V	AN0 to AN7 input, AN0_0 to AN0_7 input, AN2_0 to AN2_7 input, ANEX0, ANEX1 input					±5	LSB	
	External operation amp connection mode					±7	LSB	
8bit	VREF=VCC1=5V, 3.3V					±2	LSB	
–	Tolerance Level Impedance						3	
DNL	Differential Non-Linearity Error						±1	LSB
–	Offset Error						±3	LSB
–	Gain Error						±3	LSB
RLADDER	Ladder Resistance		VREF=VCC1		10		40	kΩ
tCONV	10-bit Conversion Time, Sample & Hold Available		VREF=VCC1=5V, φAD=12MHz		2.75			μs
tCONV	8-bit Conversion Time, Sample & Hold Available		VREF=VCC1=5V, φAD=12MHz		2.33			μs
tsAMP	Sampling Time				0.25			μs
VREF	Reference Voltage				2.0		VCC1	V
VIA	Analog Input Voltage				0		VREF	V

NOTES:

1. Referenced to VCC1=AVCC=VREF=3.3 to 5.5V, VSS=AVSS=0V at T_{opr} = –20 to 85°C / –40 to 85°C unless otherwise specified.
2. If VCC1 > VCC2, do not use AN0_0 to AN0_7 and AN2_0 to AN2_7 as analog input pins.
3. φAD frequency must be 12 MHz or less. And divide the fAD if VCC1 is less than 4.0V, and φAD frequency into 10 MHz or less.
4. When sample & hold is disabled, φAD frequency must be 250 kHz or more, in addition to the limitation in Note 3.
When sample & hold is enabled, φAD frequency must be 1MHz or more, in addition to the limitation in Note 3.

$$V_{CC1}=V_{CC2}=5V$$

Timing Requirements

($V_{CC1} = V_{CC2} = 5V$, $V_{SS} = 0V$, at $T_{opr} = -20$ to $85^{\circ}C$ / -40 to $85^{\circ}C$ unless otherwise specified)

Table 5.13 External Clock Input (XIN input) ⁽¹⁾

Symbol	Parameter	Standard		Unit
		Min.	Max.	
t_c	External Clock Input Cycle Time	62.5		ns
$t_{w(H)}$	External Clock Input HIGH Pulse Width	25		ns
$t_{w(L)}$	External Clock Input LOW Pulse Width	25		ns
t_r	External Clock Rise Time		15	ns
t_f	External Clock Fall Time		15	ns

NOTES:

1. The condition is $V_{CC1}=V_{CC2}=3.0$ to $5.0V$.

Table 5.14 Memory Expansion Mode and Microprocessor Mode

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{ac1(RD-DB)}$	Data Input Access Time (for setting with no wait)		(NOTE 1)	ns
$t_{ac2(RD-DB)}$	Data Input Access Time (for setting with wait)		(NOTE 2)	ns
$t_{ac3(RD-DB)}$	Data Input Access Time (when accessing multiplex bus area)		(NOTE 3)	ns
$t_{su(DB-RD)}$	Data Input Setup Time	40		ns
$t_{su(RDY-BCLK)}$	RDY Input Setup Time	30		ns
$t_{su(HOLD-BCLK)}$	HOLD Input Setup Time	40		ns
$t_h(RD-DB)$	Data Input Hold Time	0		ns
$t_h(BCLK-RDY)$	RDY Input Hold Time	0		ns
$t_h(BCLK-HOLD)$	HOLD Input Hold Time	0		ns

NOTES:

1. Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f(BCLK)} - 45 [ns]$$

2. Calculated according to the BCLK frequency as follows:

$$\frac{(n-0.5) \times 10^9}{f(BCLK)} - 45 [ns] \quad n \text{ is "2" for 1-wait setting, "3" for 2-wait setting and "4" for 3-wait setting.}$$

3. Calculated according to the BCLK frequency as follows:

$$\frac{(n-0.5) \times 10^9}{f(BCLK)} - 45 [ns] \quad n \text{ is "2" for 2-wait setting, "3" for 3-wait setting.}$$

$$V_{CC1}=V_{CC2}=5V$$

Timing Requirements(V_{CC1} = V_{CC2} = 5V, V_{SS} = 0V, at T_{opr} = –20 to 85°C / –40 to 85°C unless otherwise specified)**Table 5.15 Timer A Input (Counter Input in Event Counter Mode)**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
t _c (TA)	TAiIN Input Cycle Time	100		ns
t _w (TAH)	TAiIN Input HIGH Pulse Width	40		ns
t _w (TAL)	TAiIN Input LOW Pulse Width	40		ns

Table 5.16 Timer A Input (Gating Input in Timer Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
t _c (TA)	TAiIN Input Cycle Time	400		ns
t _w (TAH)	TAiIN Input HIGH Pulse Width	200		ns
t _w (TAL)	TAiIN Input LOW Pulse Width	200		ns

Table 5.17 Timer A Input (External Trigger Input in One-shot Timer Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
t _c (TA)	TAiIN Input Cycle Time	200		ns
t _w (TAH)	TAiIN Input HIGH Pulse Width	100		ns
t _w (TAL)	TAiIN Input LOW Pulse Width	100		ns

Table 5.18 Timer A Input (External Trigger Input in Pulse Width Modulation Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
t _w (TAH)	TAiIN Input HIGH Pulse Width	100		ns
t _w (TAL)	TAiIN Input LOW Pulse Width	100		ns

Table 5.19 Timer A Input (Counter Increment/Decrement Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
t _c (UP)	TAiOUT Input Cycle Time	2000		ns
t _w (UPH)	TAiOUT Input HIGH Pulse Width	1000		ns
t _w (UPL)	TAiOUT Input LOW Pulse Width	1000		ns
t _{su} (UP-TIN)	TAiOUT Input Setup Time	400		ns
t _h (TIN-UP)	TAiOUT Input Hold Time	400		ns

Table 5.20 Timer A Input (Two-phase Pulse Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
t _c (TA)	TAiIN Input Cycle Time	800		ns
t _{su} (TAIN-TAOUT)	TAiOUT Input Setup Time	200		ns
t _{su} (TAOUT-TAIN)	TAiIN Input Setup Time	200		ns

$$V_{CC1}=V_{CC2}=5V$$

Switching Characteristics

($V_{CC1} = V_{CC2} = 5V$, $V_{SS} = 0V$, at $T_{opr} = -20$ to $85^{\circ}C$ / -40 to $85^{\circ}C$ unless otherwise specified)

Table 5.28 Memory Expansion and Microprocessor Modes (for 1- to 3-wait setting and external area access)

Symbol	Parameter		Standard		Unit
			Min.	Max.	
$t_d(BCLK-AD)$	Address Output Delay Time	See Figure 5.2		25	ns
$t_h(BCLK-AD)$	Address Output Hold Time (in relation to BCLK)		4		ns
$t_h(RD-AD)$	Address Output Hold Time (in relation to RD)		0		ns
$t_h(WR-AD)$	Address Output Hold Time (in relation to WR)		(NOTE 2)		ns
$t_d(BCLK-CS)$	Chip Select Output Delay Time			25	ns
$t_h(BCLK-CS)$	Chip Select Output Hold Time (in relation to BCLK)		4		ns
$t_d(BCLK-ALE)$	ALE Signal Output Delay Time			15	ns
$t_h(BCLK-ALE)$	ALE Signal Output Hold Time		-4		ns
$t_d(BCLK-RD)$	RD Signal Output Delay Time			25	ns
$t_h(BCLK-RD)$	RD Signal Output Hold Time		0		ns
$t_d(BCLK-WR)$	WR Signal Output Delay Time			25	ns
$t_h(BCLK-WR)$	WR Signal Output Hold Time		0		ns
$t_d(BCLK-DB)$	Data Output Delay Time (in relation to BCLK)			40	ns
$t_h(BCLK-DB)$	Data Output Hold Time (in relation to BCLK) ⁽³⁾		4		ns
$t_d(DB-WR)$	Data Output Delay Time (in relation to WR)		(NOTE 1)		ns
$t_h(WR-DB)$	Data Output Hold Time (in relation to WR) ⁽³⁾		(NOTE 2)		ns
$t_d(BCLK-HLDA)$	HLDA Output Delay Time			40	ns

NOTES:

1. Calculated according to the BCLK frequency as follows:

$$\frac{(n-0.5) \times 10^9}{f(BCLK)} - 40[ns]$$

n is "1" for 1-wait setting, "2" for 2-wait setting and "3" for 3-wait setting.
(BCLK) is 12.5MHz or less.

2. Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f(BCLK)} - 10[ns]$$

3. This standard value shows the timing when the output is off, and does not show hold time of data bus.
Hold time of data bus varies with capacitor volume and pull-up (pull-down) resistance value.

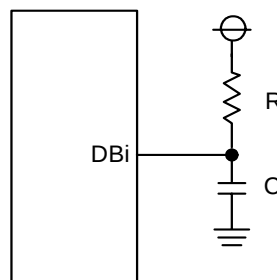
Hold time of data bus is expressed in

$$t = -CR \times \ln(1 - V_{OL} / V_{CC2})$$

by a circuit of the right figure.

For example, when $V_{OL} = 0.2V_{CC2}$, $C = 30pF$, $R = 1k\Omega$, hold time of output "L" level is

$$t = -30pF \times 1k\Omega \times \ln(1 - 0.2V_{CC2} / V_{CC2}) \\ = 6.7ns.$$



$$V_{CC1}=V_{CC2}=5V$$

Switching Characteristics(V_{CC1} = V_{CC2} = 5V, V_{SS} = 0V, at T_{opr} = –20 to 85°C / –40 to 85°C unless otherwise specified)**Table 5.29 Memory Expansion and Microprocessor Modes (for 2- to 3-wait setting, external area access and multiplex bus selection)**

Symbol	Parameter		Standard		Unit
			Min.	Max.	
t _d (BCLK-AD)	Address Output Delay Time	See Figure 5.2		25	ns
t _h (BCLK-AD)	Address Output Hold Time (in relation to BCLK)		4		ns
t _h (RD-AD)	Address Output Hold Time (in relation to RD)		(NOTE 1)		ns
t _h (WR-AD)	Address Output Hold Time (in relation to WR)		(NOTE 1)		ns
t _d (BCLK-CS)	Chip Select Output Delay Time			25	ns
t _h (BCLK-CS)	Chip Select Output Hold Time (in relation to BCLK)		4		ns
t _h (RD-CS)	Chip Select Output Hold Time (in relation to RD)		(NOTE 1)		ns
t _h (WR-CS)	Chip Select Output Hold Time (in relation to WR)		(NOTE 1)		ns
t _d (BCLK-RD)	RD Signal Output Delay Time			25	ns
t _h (BCLK-RD)	RD Signal Output Hold Time		0		ns
t _d (BCLK-WR)	WR Signal Output Delay Time			25	ns
t _h (BCLK-WR)	WR Signal Output Hold Time		0		ns
t _d (BCLK-DB)	Data Output Delay Time (in relation to BCLK)			40	ns
t _h (BCLK-DB)	Data Output Hold Time (in relation to BCLK)		4		ns
t _d (DB-WR)	Data Output Delay Time (in relation to WR)		(NOTE 2)		ns
t _h (WR-DB)	Data Output Hold Time (in relation to WR)		(NOTE 1)		ns
t _d (BCLK-HLDA)	HLDA Output Delay Time			40	ns
t _d (BCLK-ALE)	ALE Signal Output Delay Time (in relation to BCLK)			15	ns
t _h (BCLK-ALE)	ALE Signal Output Hold Time (in relation to BCLK)		–4		ns
t _d (AD-ALE)	ALE Signal Output Delay Time (in relation to Address)		(NOTE 3)		ns
t _h (AD-ALE)	ALE Signal Output Hold Time (in relation to Address)		(NOTE 4)		ns
t _d (AD-RD)	RD Signal Output Delay From the End of Address		0		ns
t _d (AD-WR)	WR Signal Output Delay From the End of Address		0		ns
t _{dz} (RD-AD)	Address Output Floating Start Time			8	ns

NOTES:

1. Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f(\text{BCLK})} - 10 [\text{ns}]$$

2. Calculated according to the BCLK frequency as follows:

$$\frac{(n - 0.5) \times 10^9}{f(\text{BCLK})} - 40 [\text{ns}] \quad n \text{ is "2" for 2-wait setting, "3" for 3-wait setting.}$$

3. Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f(\text{BCLK})} - 25 [\text{ns}]$$

4. Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f(\text{BCLK})} - 15 [\text{ns}]$$

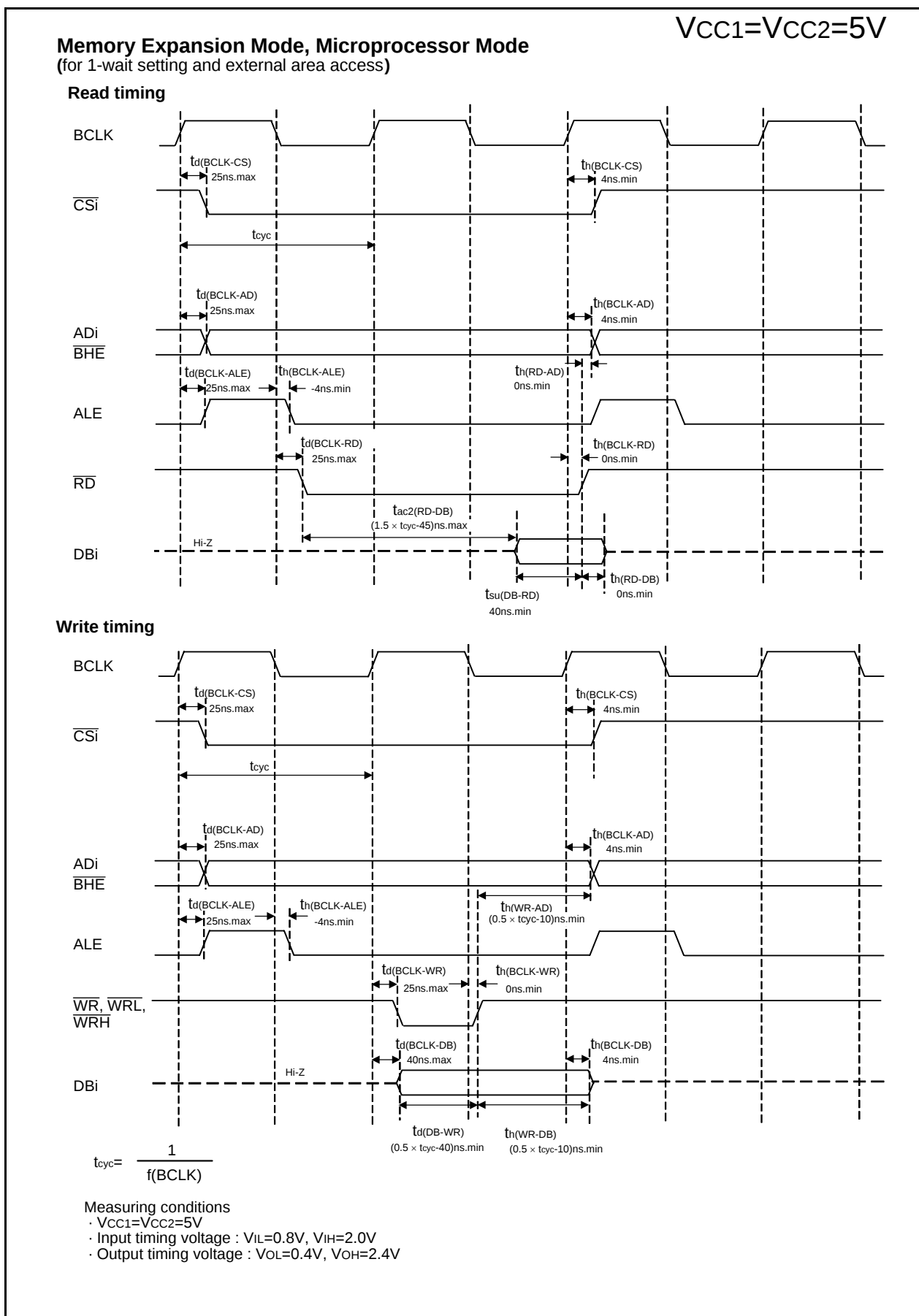


Figure 5.7 Timing Diagram (5)

$$V_{CC1}=V_{CC2}=3V$$

Table 5.30 Electrical Characteristics (1) (1)

Symbol	Parameter		Measuring Condition	Standard			Unit
				Min.	Typ.	Max.	
VOH	HIGH Output Voltage (3)	P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P14_0, P14_1	IOH=−1mA	VCC1−0.5		VCC1	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P12_0 to P12_7, P13_0 to P13_7	IOH=−1mA (2)	VCC2−0.5		VCC2	
VOH	HIGH Output Voltage XOUT	HIGHPOWER	IOH=−0.1mA	VCC1−0.5		VCC1	V
		LOWPOWER	IOH=−50μA	VCC1−0.5		VCC1	
	HIGH Output Voltage XCOUT	HIGHPOWER	With no load applied		2.5		V
		LOWPOWER	With no load applied		1.6		
VOL	LOW Output Voltage (3)	P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P14_0, P14_1	IOL=1mA			0.5	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P12_0 to P12_7, P13_0 to P13_7	IOL=1mA (2)			0.5	
VOL	LOW Output Voltage XOUT	HIGHPOWER	IOL=0.1mA			0.5	V
		LOWPOWER	IOL=50μA			0.5	
	LOW Output Voltage XCOUT	HIGHPOWER	With no load applied		0		V
		LOWPOWER	With no load applied		0		
VT+−VT−	Hysteresis	HOLD, RDY, TA0IN to TA4IN, TBOIN to TB5IN, INT0 to INT5, NMI, ADTRG, CTS0 to CTS2, CLK0 to CLK4, TA0OUT to TA4OUT, KI0 to KI3, RXD0 to RXD2, SCL0 to SCL2, SDA0 to SDA2, SIN3, SIN4		0.2		0.8	V
VT+−VT−	Hysteresis	RESET		0.2	(0.7)	1.8	V
IiH	HIGH Input Current (3)	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1, XIN, RESET, CNVSS, BYTE	VI=3V			4.0	μA
IiL	LOW Input Current (3)	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1, XIN, RESET, CNVSS, BYTE	VI=0V			−4.0	μA
RPULLUP	Pull-Up Resistance (3)	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1	VI=0V	50	100	500	kΩ
RfXIN	Feedback Resistance XIN				3.0		MΩ
RfXCIN	Feedback Resistance XCIN				25		MΩ
VRAM	RAM Retention Voltage		At stop mode	2.0			V

NOTES:

1. Referenced to VCC1 = VCC2 = 2.7 to 3.3V, VSS = 0V at Topr = −20 to 85°C / −40 to 85°C, f(XIN)=10MHz no wait unless otherwise specified.
2. VCC1 for the port P6 to P11 and P14, and VCC2 for the port P0 to P5 and P12 to P13
3. There is no external connections for port P1_0 to P1_7, P4_4 to P4_7, P7_2 to P7_5 and P9_1 in 80-pin version.

Table 5.51 A/D Conversion Characteristics (1)

Symbol	Parameter		Measuring Condition	Standard			Unit
				Min.	Typ.	Max.	
–	Resolution		$V_{REF}=V_{CC1}$			10	Bits
INL	Integral Non-Linearity Error	10bit	$V_{REF}=V_{CC1}=5V$ AN0 to AN7 input, AN0_0 to AN0_7 input, AN2_0 to AN2_7 input, ANEX0, ANEX1 input			± 3	LSB
			External operation amp connection mode			± 7	LSB
		8bit	$V_{REF}=V_{CC1}=5V$			± 2	LSB
–	Absolute Accuracy	10bit	$V_{REF}=V_{CC1}=5V$ AN0 to AN7 input, AN0_0 to AN0_7 input, AN2_0 to AN2_7 input, ANEX0, ANEX1 input			± 3	LSB
			External operation amp connection mode			± 7	LSB
		8bit	$V_{REF}=V_{CC1}=5V$			± 2	LSB
–	Tolerance Level Impedance				3		$k\Omega$
DNL	Differential Non-Linearity Error					± 1	LSB
–	Offset Error					± 3	LSB
–	Gain Error					± 3	LSB
RLADDER	Ladder Resistance		$V_{REF}=V_{CC1}$	10		40	$k\Omega$
tCONV	10-bit Conversion Time, Sample & Hold Function Available		$V_{REF}=V_{CC1}=5V$, $\phi_{AD}=12MHz$	2.75			μs
tCONV	8-bit Conversion Time, Sample & Hold Function Available		$V_{REF}=V_{CC1}=5V$, $\phi_{AD}=12MHz$	2.33			μs
tSAMP	Sampling Time			0.25			μs
VREF	Reference Voltage			2.0		V_{CC1}	V
Via	Analog Input Voltage			0		V_{REF}	V

NOTES:

1. Referenced to $V_{CC1}=AV_{CC}=V_{REF}=4.0$ to $5.5V$, $V_{SS}=AV_{SS}=0V$ at $T_{opr} = -40$ to $85^{\circ}C$ / -40 to $125^{\circ}C$ unless otherwise specified.
T version = -40 to $85^{\circ}C$, V version = -40 to $125^{\circ}C$
2. ϕ_{AD} frequency must be 12 MHz or less.
3. When sample & hold is disabled, ϕ_{AD} frequency must be 250 kHz or more, in addition to the limitation in Note 2.
When sample & hold is enabled, ϕ_{AD} frequency must be 1MHz or more, in addition to the limitation in Note 2.

Table 5.52 D/A Conversion Characteristics (1)

Symbol	Parameter	Measuring Condition	Standard			Unit
			Min.	Typ.	Max.	
–	Resolution				8	Bits
–	Absolute Accuracy				1.0	%
tSU	Setup Time				3	μs
R _O	Output Resistance		4	10	20	$k\Omega$
I _{VREF}	Reference Power Supply Input Current	(NOTE 2)			1.5	mA

NOTES:

1. Referenced to $V_{CC1}=V_{REF}=4.0$ to $5.5V$, $V_{SS}=AV_{SS}=0V$ at $T_{opr} = -40$ to $85^{\circ}C$ / -40 to $125^{\circ}C$ unless otherwise specified. T version = -40 to $85^{\circ}C$, V version = -40 to $125^{\circ}C$
2. This applies when using one D/A converter, with the D/A register for the unused D/A converter set to "00h". The resistor ladder of the A/D converter is not included. Also, when D/A register contents are not "00h", the I_{VREF} will flow even if V_{ref} is disconnected by the A/D control register.

$$V_{CC1}=V_{CC2}=5V$$

Switching Characteristics

($V_{CC1} = V_{CC2} = 5V$, $V_{SS} = 0V$, at $T_{opr} = -40$ to $85^{\circ}C$ (T version) / -40 to $125^{\circ}C$ (V version) unless otherwise specified)

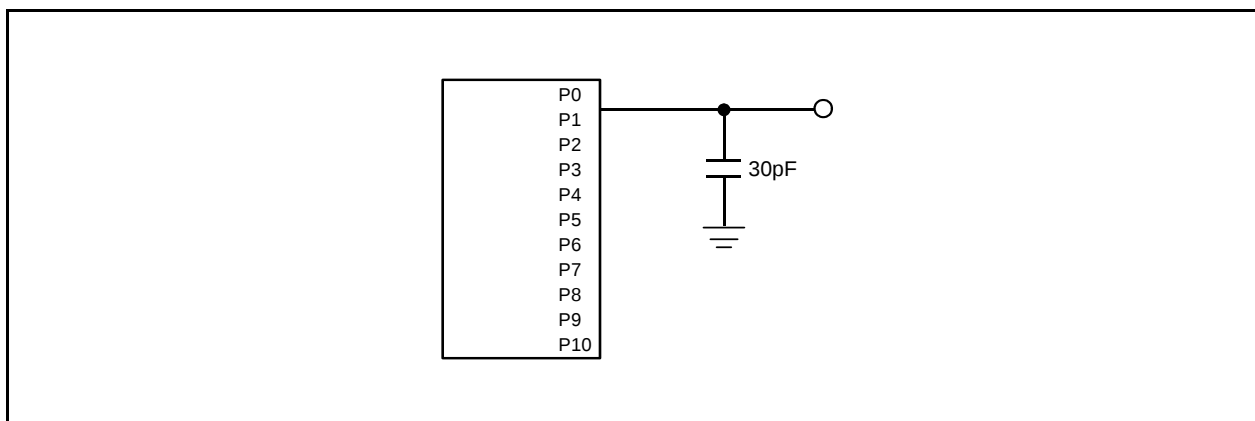


Figure 5.23 Ports P0 to P10 Measurement Circuit

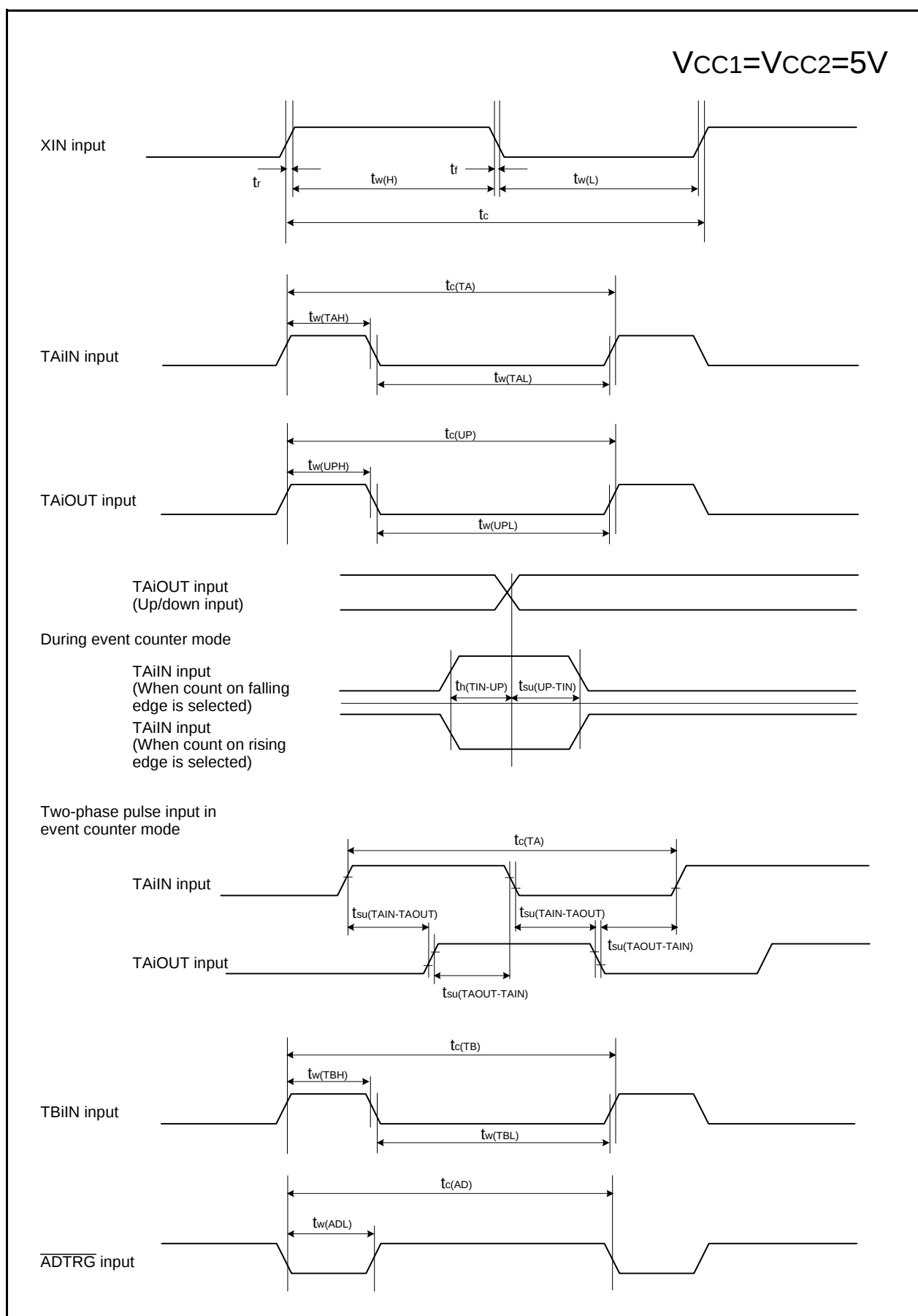


Figure 5.24 Timing Diagram (1)

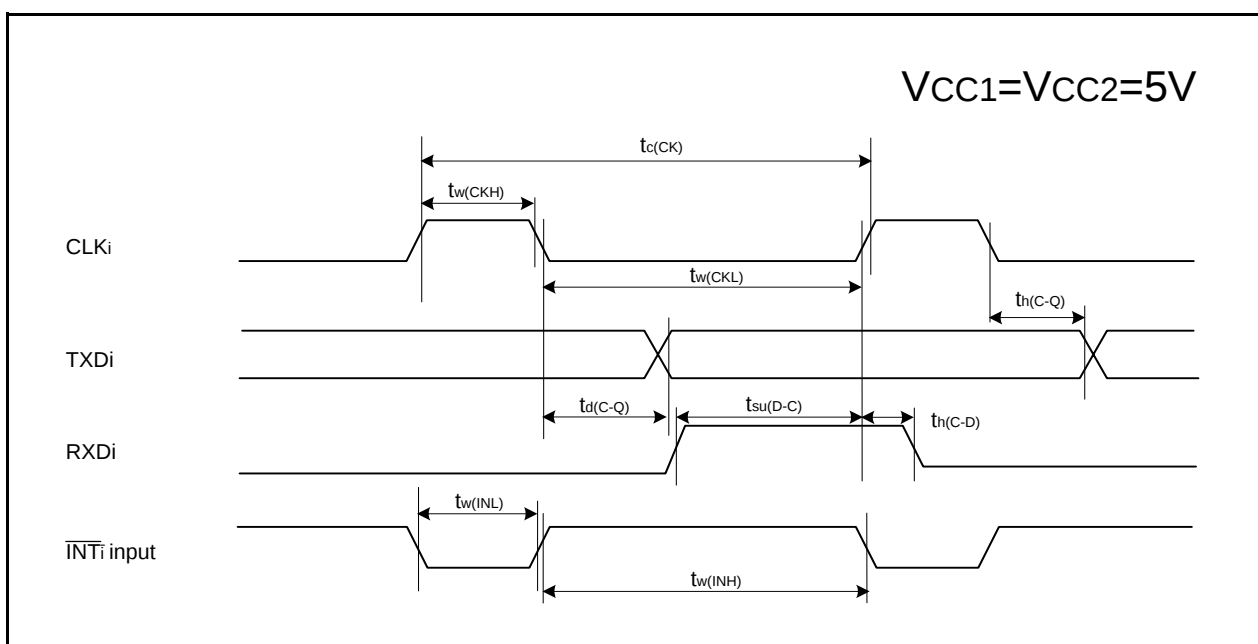


Figure 5.25 Timing Diagram (2)

Appendix 1. Package Dimensions

