



Welcome to [E-XFL.COM](#)

What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	M16C/60
Core Size	16-Bit
Speed	24MHz
Connectivity	I ² C, IEBus, UART/USART
Peripherals	DMA, WDT
Number of I/O	85
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	31K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 26x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-BQFP
Supplier Device Package	100-QFP (14x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/m30626fjfp-u7c

1.4 Product List

Table 1.4 to 1.7 list the product list, Figure 1.3 shows the Type No., Memory Size, and Package, Table 1.8 lists the Product Code of Flash Memory version and ROMless version for M16C/62P, and Table 1.9 lists the Product Code of Flash Memory version for M16C/62PT. Figure 1.4 shows the Marking Diagram of Flash Memory version and ROM-less version for M16C/62P (Top View), and Figure 1.5 shows the Marking Diagram of Flash Memory version for M16C/62PT (Top View) at the time of ROM order.

Table 1.4 Product List (1) (M16C/62P)

As of Dec. 2005

Type No.	ROM Capacity	RAM Capacity	Package Type ⁽¹⁾	Remarks
M30622M6P-XXXFP	48 Kbytes	4 Kbytes	PRQP0100JB-A	Mask ROM version
M30622M6P-XXXGP			PLQP0100KB-A	
M30622M8P-XXXFP	64 Kbytes	4 Kbytes	PRQP0100JB-A	
M30622M8P-XXXGP			PLQP0100KB-A	
M30623M8P-XXXGP			PRQP0080JA-A	
M30622MAP-XXXFP	96 Kbytes	5 Kbytes	PRQP0100JB-A	
M30622MAP-XXXGP			PLQP0100KB-A	
M30623MAP-XXXGP			PRQP0080JA-A	
M30620MCP-XXXFP	128 Kbytes	10 Kbytes	PRQP0100JB-A	
M30620MCP-XXXGP			PLQP0100KB-A	
M30621MCP-XXXGP			PRQP0080JA-A	
M30622MEP-XXXFP	192 Kbytes	12 Kbytes	PRQP0100JB-A	
M30622MEP-XXXGP			PLQP0100KB-A	
M30623MEP-XXXGP			PLQP0128KB-A	
M30622MGP-XXXFP	256 Kbytes	12 Kbytes	PRQP0100JB-A	
M30622MGP-XXXGP			PLQP0100KB-A	
M30623MGP-XXXGP			PLQP0128KB-A	
M30624MGP-XXXFP		20 Kbytes	PRQP0100JB-A	
M30624MGP-XXXGP			PLQP0100KB-A	
M30625MGP-XXXGP			PLQP0128KB-A	
M30622MWP-XXXFP		320 Kbytes	16 Kbytes	
M30622MWP-XXXGP	PLQP0100KB-A			
M30623MWP-XXXGP	PLQP0128KB-A			
M30624MWP-XXXFP	24 Kbytes		PRQP0100JB-A	
M30624MWP-XXXGP			PLQP0100KB-A	
M30625MWP-XXXGP			PLQP0128KB-A	
M30626MWP-XXXFP	31 Kbytes		PRQP0100JB-A	
M30626MWP-XXXGP			PLQP0100KB-A	
M30627MWP-XXXGP			PLQP0128KB-A	

(D): Under development

NOTES:

- The old package type numbers of each package type are as follows.

PLQP0128KB-A : 128P6Q-A,
 PRQP0100JB-A : 100P6S-A,
 PLQP0100KB-A : 100P6Q-A,
 PRQP0080JA-A : 80P6S-A

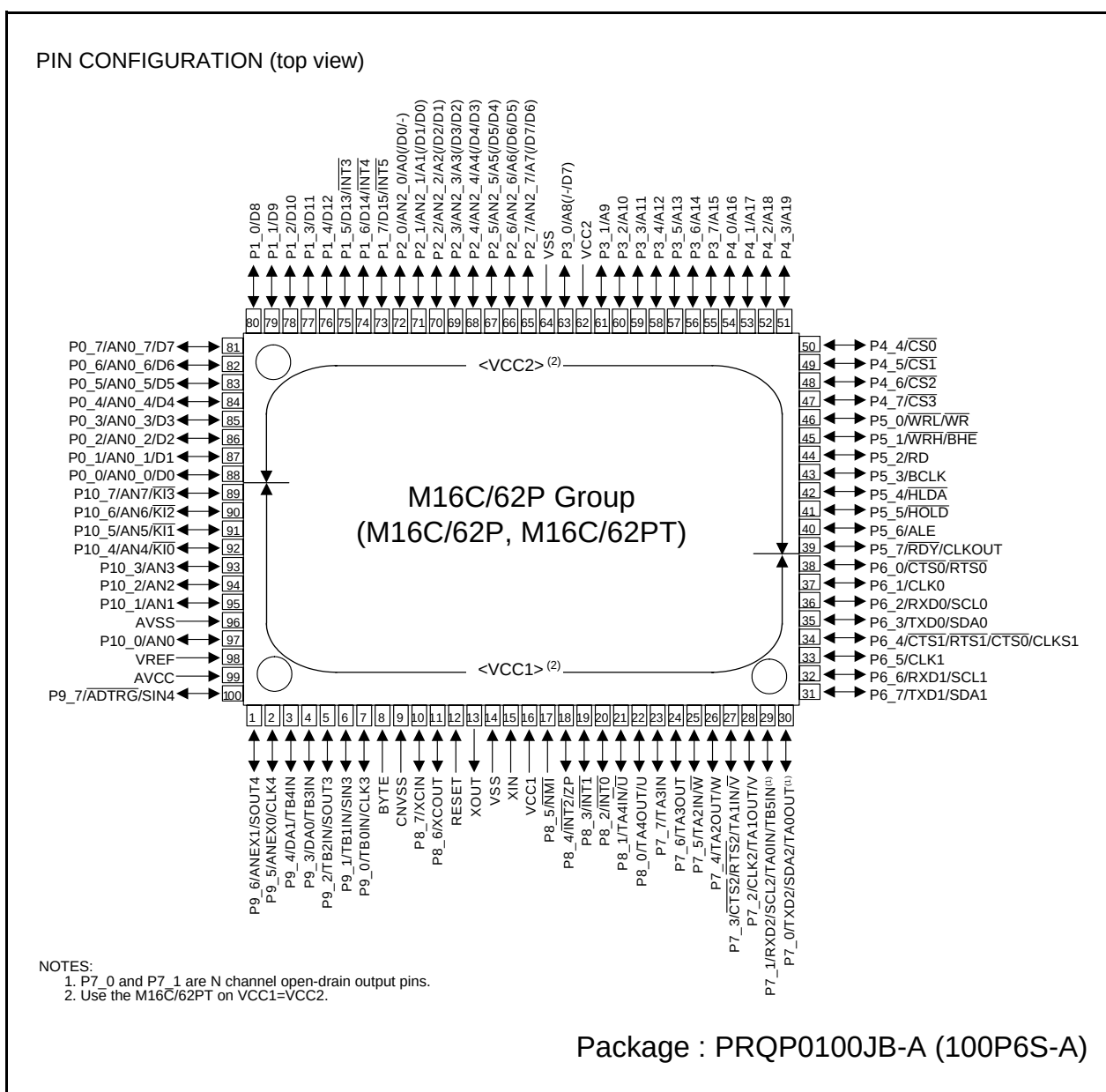


Figure 1.7 Pin Configuration (Top View)

Table 1.15 Pin Characteristics for 80-Pin Package (1)

Pin No.	Control Pin	Port	Interrupt Pin	Timer Pin	UART Pin	Analog Pin	Bus Control Pin
1		P9_5			CLK4	ANEX0	
2		P9_4		TB4IN		DA1	
3		P9_3		TB3IN		DA0	
4		P9_2		TB2IN	SOUT3		
5		P9_0		TB0IN	CLK3		
6	CNVSS (BYTE)						
7	XCIN	P8_7					
8	XCOUT	P8_6					
9	RESET						
10	XOUT						
11	VSS						
12	XIN						
13	VCC1						
14		P8_5	NMI				
15		P8_4	INT2	ZP			
16		P8_3	INT1				
17		P8_2	INT0				
18		P8_1		TA4IN			
19		P8_0		TA4OUT			
20		P7_7		TA3IN			
21		P7_6		TA3OUT			
22		P7_1		TA0IN/TB5IN	RXD2/SCL2		
23		P7_0		TA0OUT	TXD2/SDA2		
24		P6_7			TXD1/SDA1		
25		P6_6			RXD1/SCL1		
26		P6_5			CLK1		
27		P6_4			CTS1/RTS1/CTS0/CLKS1		
28		P6_3			TXD0/SDA0		
29		P6_2			RXD0/SCL0		
30		P6_1			CLK0		
31		P6_0			CTS0/RTS0		
32		P5_7					CLKOUT
33		P5_6					
34		P5_5					
35		P5_4					
36		P5_3					
37		P5_2					
38		P5_1					
39		P5_0					
40		P4_3					
41		P4_2					
42		P4_1					
43		P4_0					
44		P3_7					
45		P3_6					
46		P3_5					
47		P3_4					
48		P3_3					
49		P3_2					
50		P3_1					

Table 1.18 Pin Description (100-pin and 128-pin Version) (2)

Signal Name	Pin Name	I/O Type	Power Supply ⁽¹⁾	Description
Main clock input	XIN	I	VCC1	I/O pins for the main clock generation circuit. Connect a ceramic resonator or crystal oscillator between XIN and XOUT ⁽³⁾ . To use the external clock, input the clock from XIN and leave XOUT open.
Main clock output	XOUT	O	VCC1	
Sub clock input	XCIN	I	VCC1	I/O pins for a sub clock oscillation circuit. Connect a crystal oscillator between XCIN and XCOU ^T ⁽³⁾ . To use the external clock, input the clock from XCIN and leave XCOU ^T open.
Sub clock output	XCOU ^T	O	VCC1	
BCLK output ⁽²⁾	BCLK	O	VCC2	Outputs the BCLK signal.
Clock output	CLKOUT	O	VCC2	The clock of the same cycle as f _C , f ₈ , or f ₃₂ is outputted.
INT interrupt input	INT0 to INT2	I	VCC1	Input pins for the INT interrupt.
	INT3 to INT5	I	VCC2	
NMI interrupt input	NMI	I	VCC1	Input pin for the NMI interrupt. Pin states can be read by the P8_5 bit in the P8 register.
Key input interrupt input	KI0 to KI3	I	VCC1	Input pins for the key input interrupt.
Timer A	TA0OUT to TA4OUT	I/O	VCC1	These are timer A0 to timer A4 I/O pins. (however, output of TA0OUT for the N-channel open drain output.)
	TA0IN to TA4IN	I	VCC1	These are timer A0 to timer A4 input pins.
	ZP	I	VCC1	Input pin for the Z-phase.
Timer B	TB0IN to TB5IN	I	VCC1	These are timer B0 to timer B5 input pins.
Three-phase motor control output	U, $\bar{U}$, V, $\bar{V}$, W, $\bar{W}$	O	VCC1	These are Three-phase motor control output pins.
Serial interface	CTS0 to CTS2	I	VCC1	These are send control input pins.
	RTS0 to RTS2	O	VCC1	These are receive control output pins.
	CLK0 to CLK4	I/O	VCC1	These are transfer clock I/O pins.
	RXD0 to RXD2	I	VCC1	These are serial data input pins.
	SIN3, SIN4	I	VCC1	These are serial data input pins.
	TXD0 to TXD2	O	VCC1	These are serial data output pins. (however, output of TXD2 for the N-channel open drain output.)
	SOUT3, SOUT4	O	VCC1	These are serial data output pins.
	CLKS1	O	VCC1	This is output pin for transfer clock output from multiple pins function.
I ² C mode	SDA0 to SDA2	I/O	VCC1	These are serial data I/O pins. (however, output of SDA2 for the N-channel open drain output.)
	SCL0 to SCL2	I/O	VCC1	These are transfer clock I/O pins. (however, output of SCL2 for the N-channel open drain output.)

I : Input O : Output I/O : Input and output

NOTES:

1. When use VCC1 > VCC2, contacts due to some points or restrictions to be checked.
2. This pin function in M16C/62PT cannot be used.
3. Ask the oscillator maker the oscillation characteristic.

Table 4.6 SFR Information (6) ⁽¹⁾

Address	Register	Symbol	After Reset
03C0h 03C1h	A/D Register 0	AD0	XXh XXh
03C2h 03C3h	A/D Register 1	AD1	XXh XXh
03C4h 03C5h	A/D Register 2	AD2	XXh XXh
03C6h 03C7h	A/D Register 3	AD3	XXh XXh
03C8h 03C9h	A/D Register 4	AD4	XXh XXh
03CAh 03CBh	A/D Register 5	AD5	XXh XXh
03CCh 03CDh	A/D Register 6	AD6	XXh XXh
03CEh 03CFh	A/D Register 7	AD7	XXh XXh
03D0h			
03D1h			
03D2h			
03D3h			
03D4h 03D5h	A/D Control Register 2	ADCON2	00h
03D6h	A/D Control Register 0	ADCON0	00000XXXb
03D7h	A/D Control Register 1	ADCON1	00h
03D8h 03D9h	D/A Register 0	DA0	00h
03DAh	D/A Register 1	DA1	00h
03DBh			
03DCh 03DDh	D/A Control Register	DACON	00h
03DEh	Port P14 Control Register ⁽³⁾	PC14	XX00XXXXb
03DFh	Pull-Up Control Register 3 ⁽³⁾	PUR3	00h
03E0h	Port P0 Register	P0	XXh
03E1h	Port P1 Register	P1	XXh
03E2h	Port P0 Direction Register	PD0	00h
03E3h	Port P1 Direction Register	PD1	00h
03E4h	Port P2 Register	P2	XXh
03E5h	Port P3 Register	P3	XXh
03E6h	Port P2 Direction Register	PD2	00h
03E7h	Port P3 Direction Register	PD3	00h
03E8h	Port P4 Register	P4	XXh
03E9h	Port P5 Register	P5	XXh
03EAh	Port P4 Direction Register	PD4	00h
03EBh	Port P5 Direction Register	PD5	00h
03ECh	Port P6 Register	P6	XXh
03EDh	Port P7 Register	P7	XXh
03EEh	Port P6 Direction Register	PD6	00h
03EFh	Port P7 Direction Register	PD7	00h
03F0h	Port P8 Register	P8	XXh
03F1h	Port P9 Register	P9	XXh
03F2h	Port P8 Direction Register	PD8	00X00000b
03F3h	Port P9 Direction Register	PD9	00h
03F4h	Port P10 Register	P10	XXh
03F5h	Port P11 Register ⁽³⁾	P11	XXh
03F6h	Port P10 Direction Register	PD10	00h
03F7h	Port P11 Direction Register ⁽³⁾	PD11	00h
03F8h	Port P12 Register ⁽³⁾	P12	XXh
03F9h	Port P13 Register ⁽³⁾	P13	XXh
03FAh	Port P12 Direction Register ⁽³⁾	PD12	00h
03FBh	Port P13 Direction Register ⁽³⁾	PD13	00h
03FCh	Pull-Up Control Register 0	PUR0	00h
03FDh	Pull-Up Control Register 1	PUR1	00000000b ⁽²⁾ 00000010b ⁽²⁾
03FEh	Pull-Up Control Register 2	PUR2	00h
03FFh	Port Control Register	PCR	00h

NOTES:

- The blank areas are reserved and cannot be accessed by users.
- At hardware reset 1 or hardware reset 2, the register is as follows:
 - "00000000b" where "L" is inputted to the CNVSS pin
 - "00000010b" where "H" is inputted to the CNVSS pin
 At software reset, watchdog timer reset and oscillation stop detection reset, the register is as follows:
 - "00000000b" where the PM01 to PM00 bits in the PM0 register are "00b" (single-chip mode).
 - "00000010b" where the PM01 to PM00 bits in the PM0 register are "01b" (memory expansion mode) or "11b" (microprocessor mode).
- These registers do not exist in M16C/62P (80-pin version), and M16C/62PT (80-pin version).

X : Nothing is mapped to this bit

Table 5.6 Flash Memory Version Electrical Characteristics ⁽¹⁾ for 100 cycle products (D3, D5, U3, U5)

Symbol	Parameter		Standard			Unit
			Min.	Typ.	Max.	
–	Program and Erase Endurance ⁽³⁾		100			cycle
–	Word Program Time (Vcc1=5.0V)			25	200	μs
–	Lock Bit Program Time			25	200	μs
–	Block Erase Time (Vcc1=5.0V)	4-Kbyte block		0.3	4	s
–		8-Kbyte block		0.3	4	s
–		32-Kbyte block		0.5	4	s
–		64-Kbyte block		0.8	4	s
–	Erase All Unlocked Blocks Time ⁽²⁾				4×n	s
t _{ps}	Flash Memory Circuit Stabilization Wait Time				15	μs
–	Data Hold Time ⁽⁵⁾		10			year

Table 5.7 Flash Memory Version Electrical Characteristics ⁽⁶⁾ for 10,000 cycle products (D7, D9, U7, U9) (Block A and Block 1 ⁽⁷⁾)

Symbol	Parameter	Standard			Unit
		Min.	Typ.	Max.	
—	Program and Erase Endurance ^(3, 8, 9)	10,000 ⁽⁴⁾			cycle
—	Word Program Time (V _{CC1} =5.0V)		25		μs
—	Lock Bit Program Time		25		μs
—	Block Erase Time (V _{CC1} =5.0V)	4-Kbyte block		0.3	s
t _{PS}	Flash Memory Circuit Stabilization Wait Time			15	μs
—	Data Hold Time ⁽⁵⁾	10			year

NOTES:

1. Referenced to V_{CC1}=4.5 to 5.5V, 3.0 to 3.6V at T_{opr} = 0 to 60 °C (D3, D5, U3, U5) unless otherwise specified.
2. n denotes the number of block erases.
3. Program and Erase Endurance refers to the number of times a block erase can be performed.
If the program and erase endurance is n (n=100, 1,000, or 10,000), each block can be erased n times.
For example, if a 4 Kbytes block A is erased after writing 1 word data 2,048 times, each to a different address, this counts as one program and erase endurance. Data cannot be written to the same address more than once without erasing the block. (Rewrite prohibited)
4. Maximum number of E/W cycles for which operation is guaranteed.
5. T_{opr} = -40 to 85 °C (D3, D7, U3, U7) / -20 to 85 °C (D5, D9, U5, U9).
6. Referenced to V_{CC1} = 4.5 to 5.5V, 3.0 to 3.6V at T_{opr} = -40 to 85 °C (D7, U7) / -20 to 85 °C (D9, U9) unless otherwise specified.
7. Table 5.7 applies for block A or block 1 program and erase endurance > 1,000. Otherwise, use Table 5.6.
8. To reduce the number of program and erase endurance when working with systems requiring numerous rewrites, write to unused word addresses within the block instead of rewrite. Erase block only after all possible addresses are used. For example, an 8-word program can be written 256 times maximum before erase becomes necessary. Maintaining an equal number of erasure between block A and block 1 will also improve efficiency. It is important to track the total number of times erasure is used.
9. Should erase error occur during block erase, attempt to execute clear status register command, then block erase command at least three times until erase error disappears.
10. Set the PM17 bit in the PM1 register to "1" (wait state) when executing more than 100 times rewrites (D7, D9, U7 and U9).
11. Customers desiring E/W failure rate information should contact their Renesas technical support representative.

Table 5.8 Flash Memory Version Program / Erase Voltage and Read Operation Voltage Characteristics (at T_{opr} = 0 to 60 °C(D3, D5, U3, U5), T_{opr} = -40 to 85 °C(D7, U7) / T_{opr} = -20 to 85 °C(D9, U9))

Flash Program, Erase Voltage	Flash Read Operation Voltage
V _{CC1} = 3.3 V ± 0.3 V or 5.0 V ± 0.5 V	V _{CC1} =2.7 to 5.5 V

Table 5.9 Low Voltage Detection Circuit Electrical Characteristics

Symbol	Parameter	Measuring Condition	Standard			Unit
			Min.	Typ.	Max.	
V _{det4}	Low Voltage Detection Voltage ⁽¹⁾	V _{CC1} =0.8V to 5.5V	3.3	3.8	4.4	V
V _{det3}	Reset Level Detection Voltage ^(1, 2)		2.2	2.8	3.6	V
V _{det4} -V _{det3}	Electric potential difference of Low Voltage Detection and Reset Level Detection		0.3			V
V _{det3s}	Low Voltage Reset Retention Voltage				0.8	V
V _{det3r}	Low Voltage Reset Release Voltage ⁽³⁾		2.2	2.9	4.0	V

NOTES:

1. V_{det4} > V_{det3}.
2. Where reset level detection voltage is less than 2.7 V, if the supply power voltage is greater than the reset level detection voltage, the microcomputer operates with f(BCLK) ≤ 10MHz.
3. V_{det3r} > V_{det3} is not guaranteed.
4. The voltage detection circuit is designed to use when V_{CC1} is set to 5V.

Table 5.10 Power Supply Circuit Timing Characteristics

Symbol	Parameter	Measuring Condition	Standard			Unit
			Min.	Typ.	Max.	
t _d (P-R)	Time for Internal Power Supply Stabilization During Powering-On	V _{CC1} =2.7V to 5.5V			2	ms
t _d (R-S)	STOP Release Time				150	μs
t _d (W-S)	Low Power Dissipation Mode Wait Mode Release Time				150	μs
t _d (S-R)	Brown-out Detection Reset (Hardware Reset 2) Release Wait Time	V _{CC1} =V _{det3r} to 5.5V		6 ⁽¹⁾	20	ms
t _d (E-A)	Low Voltage Detection Circuit Operation Start Time	V _{CC1} =2.7V to 5.5V			20	μs

NOTES:

1. When V_{CC1} = 5V.

$$V_{CC1}=V_{CC2}=5V$$

Timing Requirements

($V_{CC1} = V_{CC2} = 5V$, $V_{SS} = 0V$, at $T_{opr} = -20$ to $85^{\circ}C$ / -40 to $85^{\circ}C$ unless otherwise specified)

Table 5.21 Timer B Input (Counter Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN Input Cycle Time (counted on one edge)	100		ns
$t_{w(TBH)}$	TBiIN Input HIGH Pulse Width (counted on one edge)	40		ns
$t_{w(TBL)}$	TBiIN Input LOW Pulse Width (counted on one edge)	40		ns
$t_{c(TB)}$	TBiIN Input Cycle Time (counted on both edges)	200		ns
$t_{w(TBH)}$	TBiIN Input HIGH Pulse Width (counted on both edges)	80		ns
$t_{w(TBL)}$	TBiIN Input LOW Pulse Width (counted on both edges)	80		ns

Table 5.22 Timer B Input (Pulse Period Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN Input Cycle Time	400		ns
$t_{w(TBH)}$	TBiIN Input HIGH Pulse Width	200		ns
$t_{w(TBL)}$	TBiIN Input LOW Pulse Width	200		ns

Table 5.23 Timer B Input (Pulse Width Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN Input Cycle Time	400		ns
$t_{w(TBH)}$	TBiIN Input HIGH Pulse Width	200		ns
$t_{w(TBL)}$	TBiIN Input LOW Pulse Width	200		ns

Table 5.24 A/D Trigger Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(AD)}$	$\overline{ADTRG}$ Input Cycle Time	1000		ns
$t_{w(ADL)}$	$\overline{ADTRG}$ input LOW Pulse Width	125		ns

Table 5.25 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi Input Cycle Time	200		ns
$t_{w(CKH)}$	CLKi Input HIGH Pulse Width	100		ns
$t_{w(CKL)}$	CLKi Input LOW Pulse Width	100		ns
$t_{d(C-Q)}$	TXDi Output Delay Time		80	ns
$t_{h(C-Q)}$	TXDi Hold Time	0		ns
$t_{su(D-C)}$	RXDi Input Setup Time	70		ns
$t_{h(C-D)}$	RXDi Input Hold Time	90		ns

Table 5.26 External Interrupt $\overline{INTi}$ Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(INH)}$	$\overline{INTi}$ Input HIGH Pulse Width	250		ns
$t_{w(INL)}$	$\overline{INTi}$ Input LOW Pulse Width	250		ns

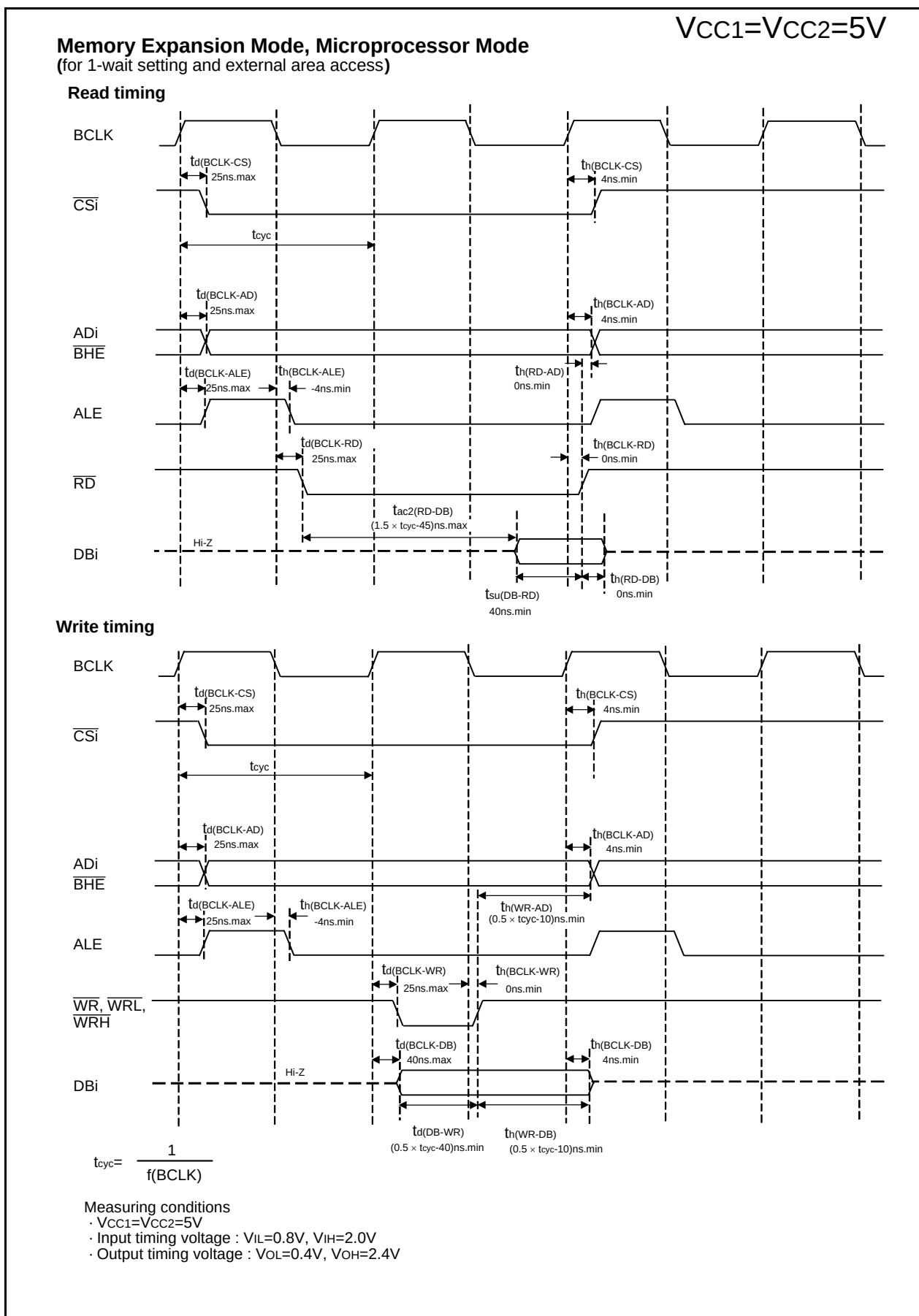


Figure 5.7 Timing Diagram (5)

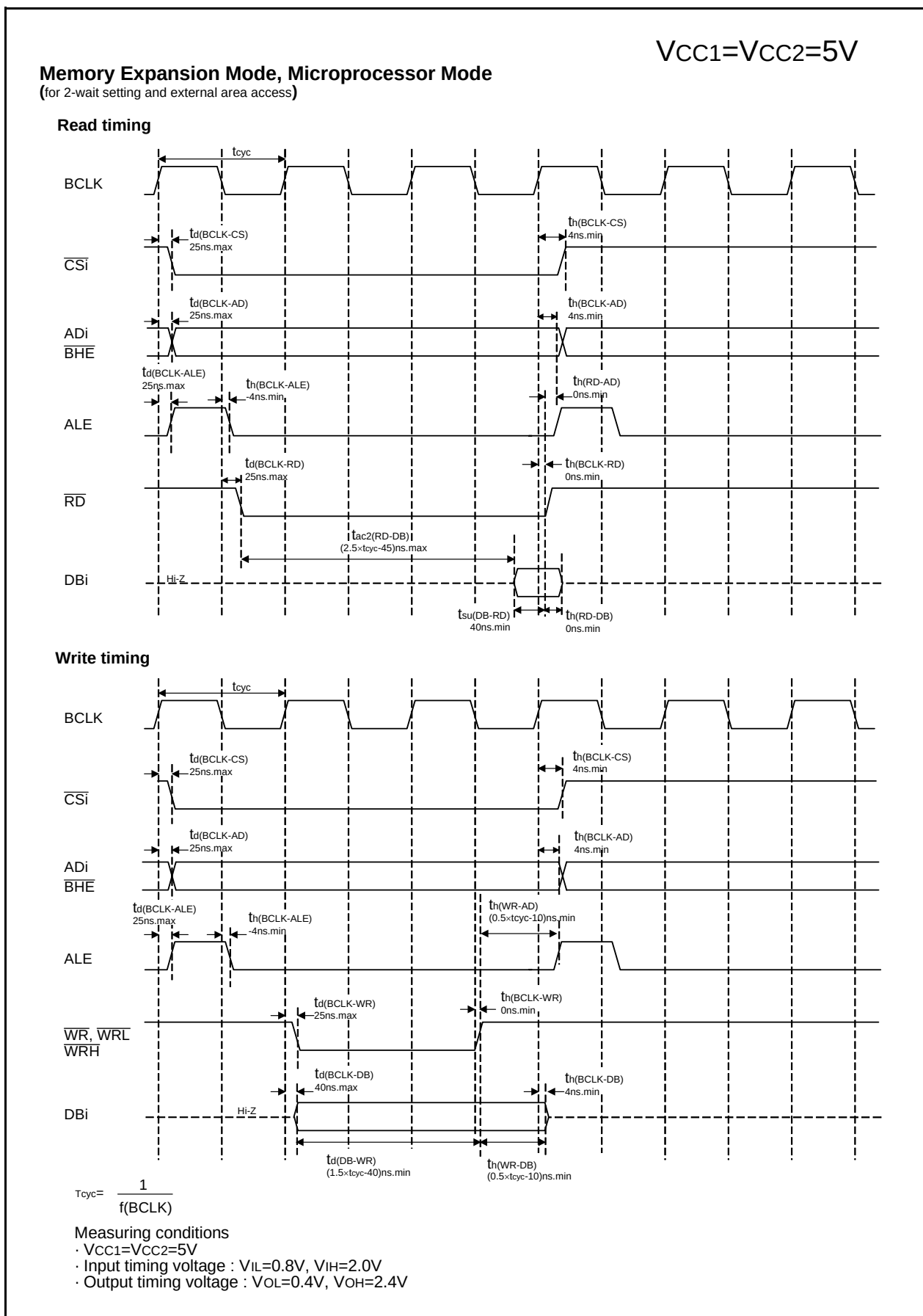


Figure 5.8 Timing Diagram (6)

$$V_{CC1}=V_{CC2}=3V$$

Timing Requirements

($V_{CC1} = V_{CC2} = 3V$, $V_{SS} = 0V$, at $T_{opr} = -20$ to $85^{\circ}C$ / -40 to $85^{\circ}C$ unless otherwise specified)

Table 5.32 External Clock Input (XIN input)⁽¹⁾

Symbol	Parameter	Standard		Unit
		Min.	Max.	
t_c	External Clock Input Cycle Time	(NOTE 2)		ns
$t_{w(H)}$	External Clock Input HIGH Pulse Width	(NOTE 3)		ns
$t_{w(L)}$	External Clock Input LOW Pulse Width	(NOTE 3)		ns
t_r	External Clock Rise Time		(NOTE 4)	ns
t_f	External Clock Fall Time		(NOTE 4)	ns

NOTES:

1. The condition is $V_{CC1}=V_{CC2}=2.7$ to $3.0V$.
2. Calculated according to the V_{CC1} voltage as follows:

$$\frac{10^{-6}}{20 \times V_{CC2} - 44} \text{ [ns]}$$

3. Calculated according to the V_{CC1} voltage as follows:

$$\frac{10^{-6}}{20 \times V_{CC1} - 44} \times 0.4 \text{ [ns]}$$

4. Calculated according to the V_{CC1} voltage as follows:

$$-10 \times V_{CC1} + 45 \text{ [ns]}$$

Table 5.33 Memory Expansion Mode and Microprocessor Mode

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{ac1(RD-DB)}$	Data Input Access Time (for setting with no wait)		(NOTE 1)	ns
$t_{ac2(RD-DB)}$	Data Input Access Time (for setting with wait)		(NOTE 2)	ns
$t_{ac3(RD-DB)}$	Data Input Access Time (when accessing multiplex bus area)		(NOTE 3)	ns
$t_{su(DB-RD)}$	Data Input Setup Time	50		ns
$t_{su(RDY-BCLK)}$	RDY Input Setup Time	40		ns
$t_{su(HOLD-BCLK)}$	HOLD Input Setup Time	50		ns
$t_h(RD-DB)$	Data Input Hold Time	0		ns
$t_h(BCLK-RDY)$	RDY Input Hold Time	0		ns
$t_h(BCLK-HOLD)$	HOLD Input Hold Time	0		ns

NOTES:

1. Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f(BCLK)} - 60 \text{ [ns]}$$

2. Calculated according to the BCLK frequency as follows:

$$\frac{(n-0.5) \times 10^9}{f(BCLK)} - 60 \text{ [ns]} \quad n \text{ is "2" for 1-wait setting, "3" for 2-wait setting and "4" for 3-wait setting.}$$

3. Calculated according to the BCLK frequency as follows:

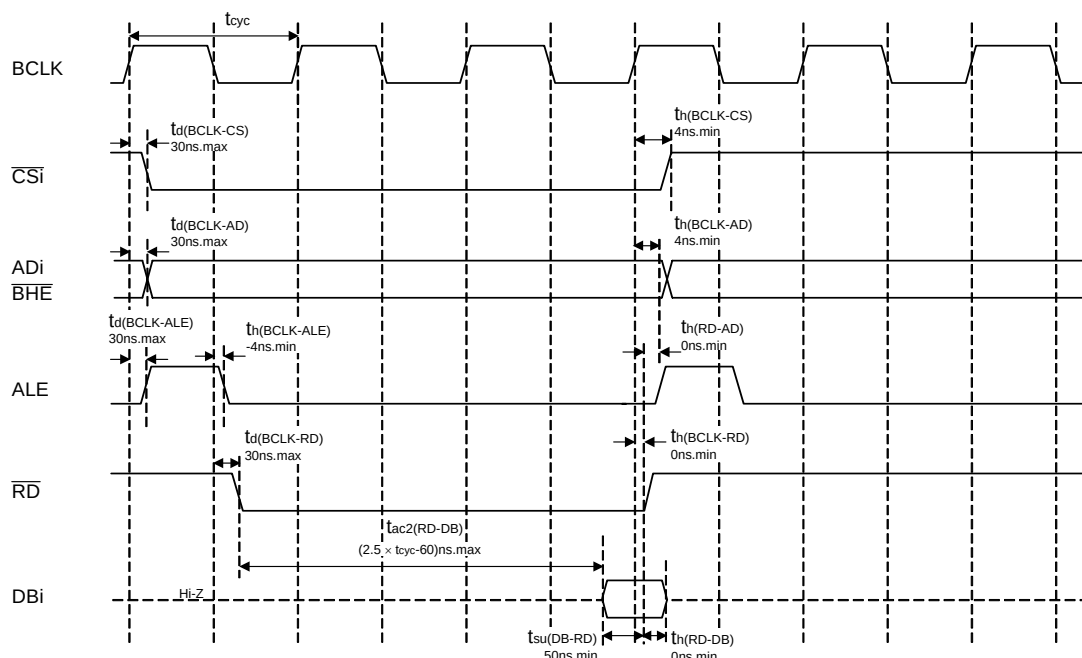
$$\frac{(n-0.5) \times 10^9}{f(BCLK)} - 60 \text{ [ns]} \quad n \text{ is "2" for 2-wait setting, "3" for 3-wait setting.}$$

Memory Expansion Mode, Microprocessor Mode

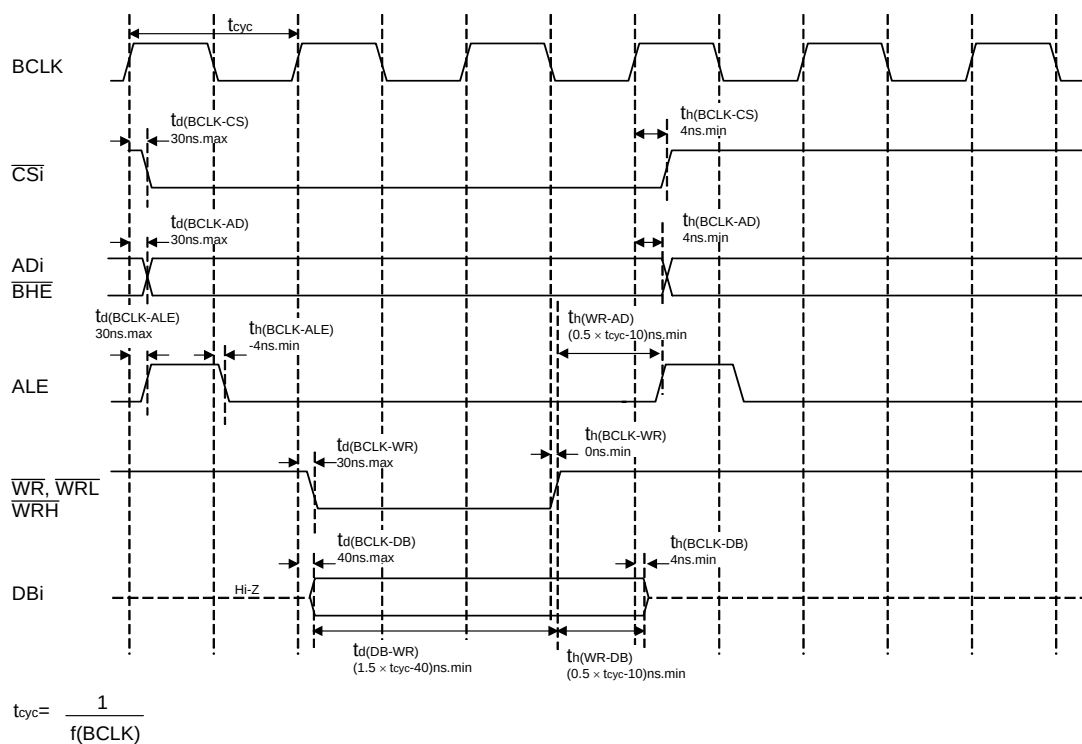
(for 2-wait setting and external area access)

 $V_{CC1}=V_{CC2}=3V$

Read timing



Write timing



Measuring conditions

- $V_{CC1}=V_{CC2}=3V$
- Input timing voltage : $V_{IL}=0.6V$, $V_{IH}=2.4V$
- Output timing voltage : $V_{OL}=1.5V$, $V_{OH}=1.5V$

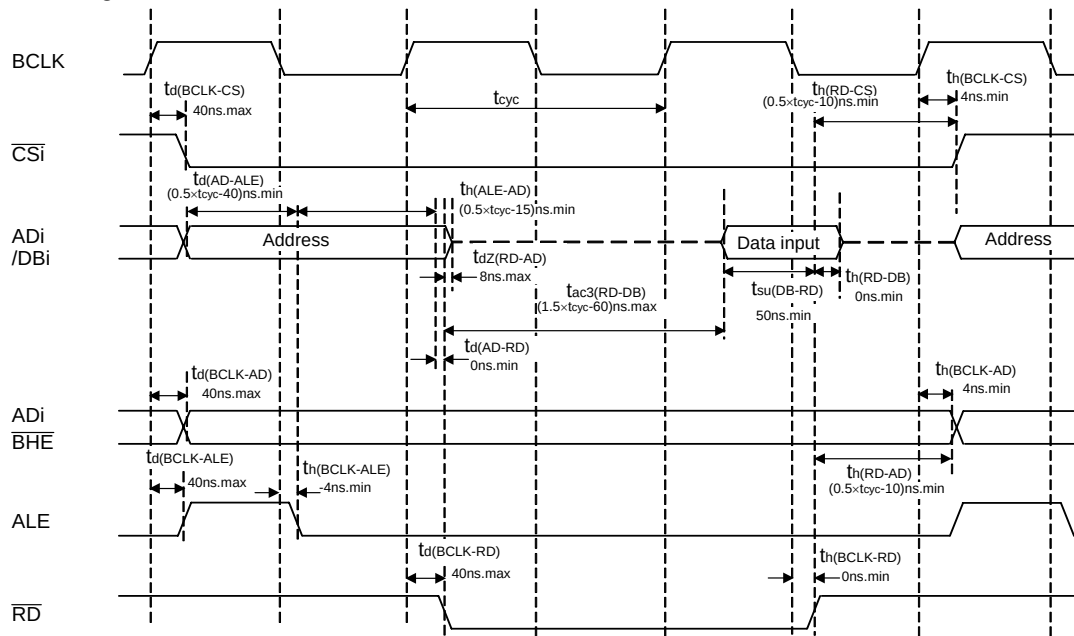
Figure 5.18 Timing Diagram (6)

Memory Expansion Mode, Microprocessor Mode

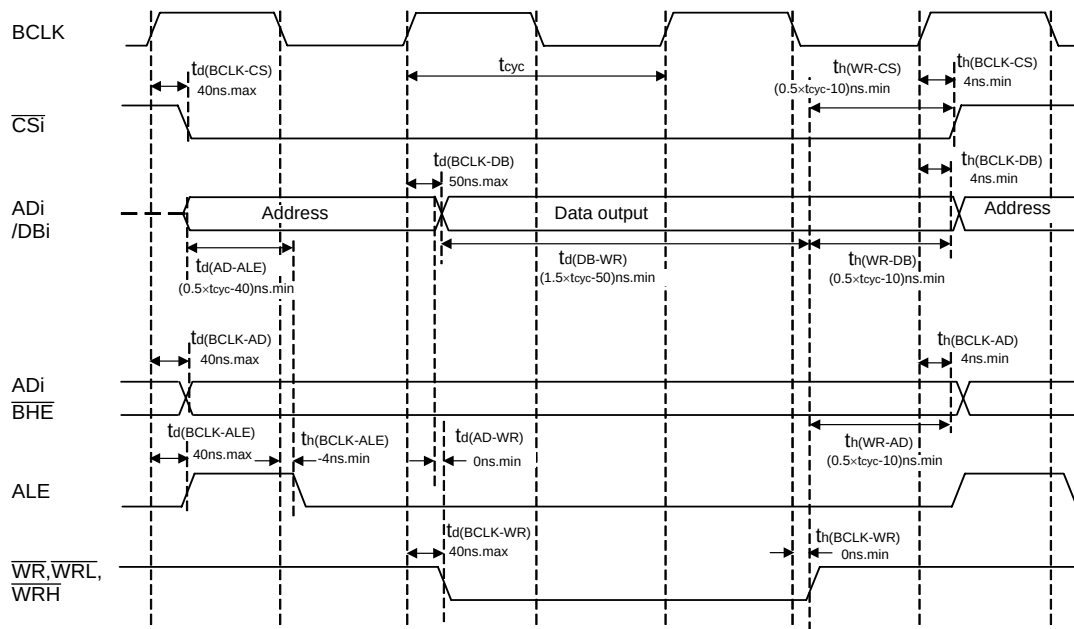
(For 2-wait setting, external area access and multiplex bus selection)

 $V_{CC1}=V_{CC2}=3V$

Read timing



Write timing



$$t_{\text{cyc}} = \frac{1}{f(\text{BCLK})}$$

Measuring conditions

- $V_{CC1}=V_{CC2}=3V$
- Input timing voltage : $V_{IL}=0.6V$, $V_{IH}=2.4V$
- Output timing voltage : $V_{OL}=1.5V$, $V_{OH}=1.5V$

Figure 5.20 Timing Diagram (8)

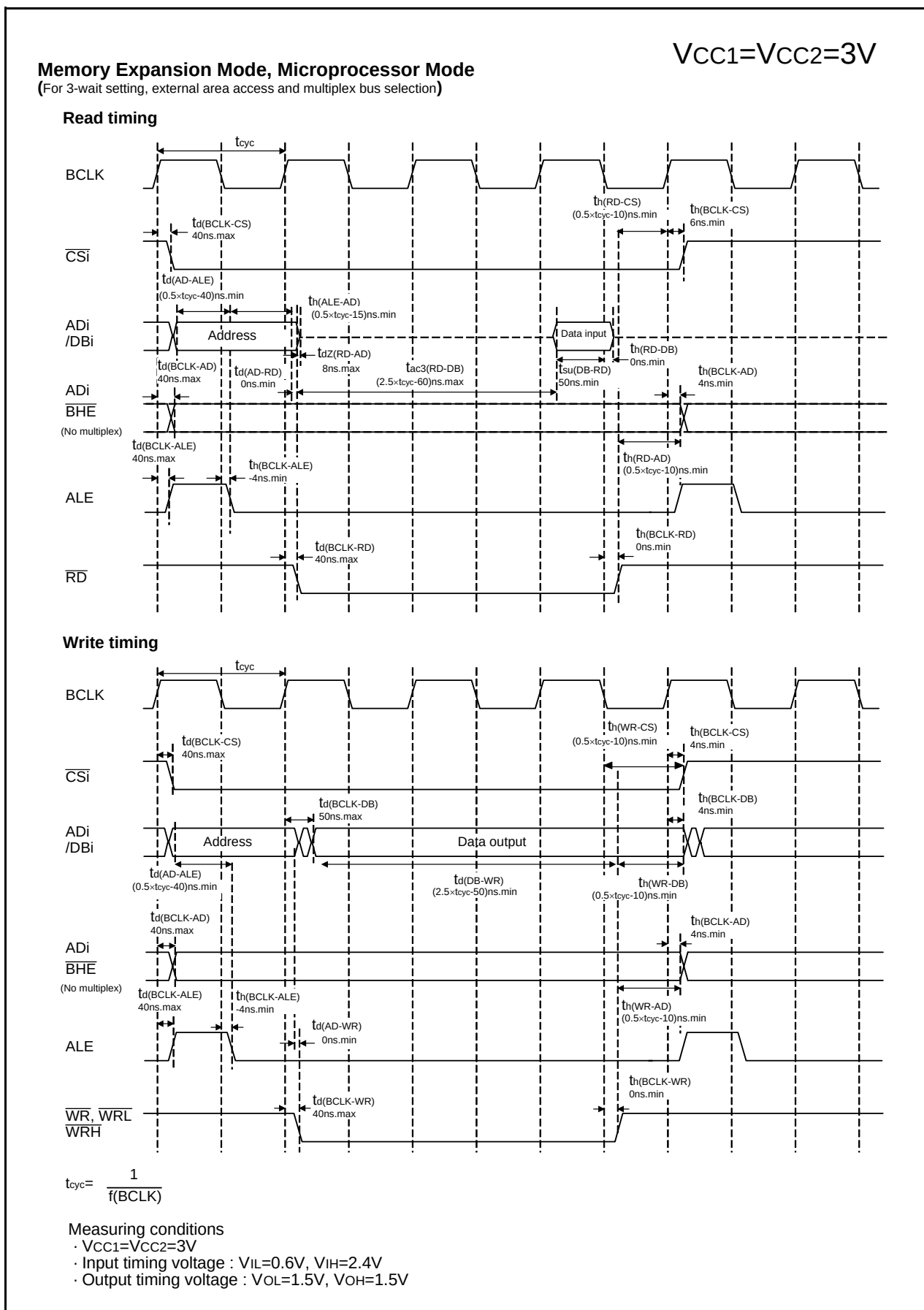


Figure 5.21 Timing Diagram (9)

Table 5.51 A/D Conversion Characteristics (1)

Symbol	Parameter		Measuring Condition	Standard			Unit
				Min.	Typ.	Max.	
–	Resolution		$V_{REF}=V_{CC1}$			10	Bits
INL	Integral Non-Linearity Error	10bit	$V_{REF}=V_{CC1}=5V$ AN0 to AN7 input, AN0_0 to AN0_7 input, AN2_0 to AN2_7 input, ANEX0, ANEX1 input			± 3	LSB
			External operation amp connection mode			± 7	LSB
		8bit	$V_{REF}=V_{CC1}=5V$			± 2	LSB
–	Absolute Accuracy	10bit	$V_{REF}=V_{CC1}=5V$ AN0 to AN7 input, AN0_0 to AN0_7 input, AN2_0 to AN2_7 input, ANEX0, ANEX1 input			± 3	LSB
			External operation amp connection mode			± 7	LSB
		8bit	$V_{REF}=V_{CC1}=5V$			± 2	LSB
–	Tolerance Level Impedance				3		$k\Omega$
DNL	Differential Non-Linearity Error					± 1	LSB
–	Offset Error					± 3	LSB
–	Gain Error					± 3	LSB
RLADDER	Ladder Resistance		$V_{REF}=V_{CC1}$	10		40	$k\Omega$
tCONV	10-bit Conversion Time, Sample & Hold Function Available		$V_{REF}=V_{CC1}=5V$, $\phi_{AD}=12MHz$	2.75			μs
tCONV	8-bit Conversion Time, Sample & Hold Function Available		$V_{REF}=V_{CC1}=5V$, $\phi_{AD}=12MHz$	2.33			μs
tSAMP	Sampling Time			0.25			μs
VREF	Reference Voltage			2.0		V_{CC1}	V
Via	Analog Input Voltage			0		V_{REF}	V

NOTES:

1. Referenced to $V_{CC1}=AV_{CC}=V_{REF}=4.0$ to $5.5V$, $V_{SS}=AV_{SS}=0V$ at $T_{opr} = -40$ to $85^{\circ}C$ / -40 to $125^{\circ}C$ unless otherwise specified.
T version = -40 to $85^{\circ}C$, V version = -40 to $125^{\circ}C$
2. ϕ_{AD} frequency must be 12 MHz or less.
3. When sample & hold is disabled, ϕ_{AD} frequency must be 250 kHz or more, in addition to the limitation in Note 2.
When sample & hold is enabled, ϕ_{AD} frequency must be 1MHz or more, in addition to the limitation in Note 2.

Table 5.52 D/A Conversion Characteristics (1)

Symbol	Parameter	Measuring Condition	Standard			Unit
			Min.	Typ.	Max.	
–	Resolution				8	Bits
–	Absolute Accuracy				1.0	%
tSU	Setup Time				3	μs
R _O	Output Resistance		4	10	20	$k\Omega$
I _{VREF}	Reference Power Supply Input Current	(NOTE 2)			1.5	mA

NOTES:

1. Referenced to $V_{CC1}=V_{REF}=4.0$ to $5.5V$, $V_{SS}=AV_{SS}=0V$ at $T_{opr} = -40$ to $85^{\circ}C$ / -40 to $125^{\circ}C$ unless otherwise specified. T version = -40 to $85^{\circ}C$, V version = -40 to $125^{\circ}C$
2. This applies when using one D/A converter, with the D/A register for the unused D/A converter set to "00h". The resistor ladder of the A/D converter is not included. Also, when D/A register contents are not "00h", the I_{VREF} will flow even if V_{ref} id disconnected by the A/D control register.

$$V_{CC1}=V_{CC2}=5V$$

Table 5.57 Electrical Characteristics (1) ⁽¹⁾

Symbol	Parameter		Measuring Condition	Standard			Unit
				Min.	Typ.	Max.	
VOH	HIGH Output Voltage ⁽²⁾	P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P14_0, P14_1	IOH=-5mA	VCC1-2.0		VCC1	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P12_0 to P12_7, P13_0 to P13_7	IOH=-5mA	VCC2-2.0		VCC2	
VOH	HIGH Output Voltage ⁽²⁾	P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P14_0, P14_1	OH=-200μA	VCC1-0.3		VCC1	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P12_0 to P12_7, P13_0 to P13_7	IOH=-200μA	VCC2-0.3		VCC2	
VOH	HIGH Output Voltage XOUT	HIGHPOWER	IOH=-1mA	VCC1-2.0		VCC1	V
		LOWPOWER	IOH=-0.5mA	VCC1-2.0		VCC1	V
	HIGH Output Voltage XCOUT	HIGHPOWER	With no load applied		2.5		V
		LOWPOWER	With no load applied		1.6		V
VOL	LOW Output Voltage ⁽²⁾	P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P14_0, P14_1	IOL=5mA			2.0	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P12_0 to P12_7, P13_0 to P13_7	IOL=5mA			2.0	
VOL	LOW Output Voltage ⁽²⁾	P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P14_0, P14_1	IOL=200μA			0.45	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P12_0 to P12_7, P13_0 to P13_7	IOL=200μA			0.45	
VOL	LOW Output Voltage XOUT	HIGHPOWER	IOL=1mA			2.0	V
		LOWPOWER	IOL=0.5mA			2.0	
	LOW Output Voltage XCOUT	HIGHPOWER	With no load applied		0		V
		LOWPOWER	With no load applied		0		
VT+-VT-	Hysteresis	HOLD, RDY, TA0IN to TA4IN, TB0IN to TB5IN, INT0 to INT5, NMI, ADTRG, CTS0 to CTS2, CLK0 to CLK4, TA0OUT to TA4OUT, KI0 to KI3, RXD0 to RXD2, SCL0 to SCL2, SDA0 to SDA2, SIN3, SIN4		0.2		1.0	V
VT+-VT-	Hysteresis	RESET		0.2		2.5	V
I _{IH}	HIGH Input Current ⁽²⁾	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1, XIN, RESET, CNVSS, BYTE	Vi=5V			5.0	μA
I _{IL}	LOW Input Current ⁽²⁾	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1, XIN, RESET, CNVSS, BYTE	Vi=0V			-5.0	μA
RPULLUP	Pull-Up Resistance ⁽²⁾	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1	Vi=0V	30	50	170	kΩ
R _{FXIN}	Feedback Resistance XIN				1.5		MΩ
R _{FXCIN}	Feedback Resistance XCIN				15		MΩ
V _{RAM}	RAM Retention Voltage		At stop mode	2.0			V

NOTES:

1. Referenced to VCC1=VCC2=4.0 to 5.5V, VSS = 0V at T_{opr} = -40 to 85°C / -40 to 125°C, f(BCLK)=24MHz unless otherwise specified. T version = -40 to 85°C, V version = -40 to 125°C.
2. There is no external connections for port P1_0 to P1_7, P4_4 to P4_7, P7_2 to P7_5 and P9_1 in 80-pin version.

Table 5.58 Electrical Characteristics (2) ⁽¹⁾

Symbol	Parameter		Measuring Condition		Standard			Unit
					Min.	Typ.	Max.	
I _{cc}	Power Supply Current (V _{CC1} =V _{CC2} =4.0V to 5.5V)	In single-chip mode, the output pins are open and other pins are V _{SS}	Mask ROM	f(BCLK)=24MHz No division, PLL operation		14	20	mA
				No division, On-chip oscillation		1		mA
			Flash Memory	f(BCLK)=24MHz, No division, PLL operation		18	27	mA
				No division, On-chip oscillation		1.8		mA
			Flash Memory Program	f(BCLK)=10MHz, V _{CC1} =5.0V		15		mA
			Flash Memory Erase	f(BCLK)=10MHz, V _{CC1} =5.0V		25		mA
			Mask ROM	f(XCIN)=32kHz Low power dissipation mode, ROM ⁽³⁾		25		μA
			Flash Memory	f(BCLK)=32kHz Low power dissipation mode, RAM ⁽³⁾		25		μA
				f(BCLK)=32kHz Low power dissipation mode, Flash Memory ⁽³⁾		420		μA
				On-chip oscillation, Wait mode		50		μA
			Mask ROM Flash Memory	f(BCLK)=32kHz Wait mode ⁽²⁾ , Oscillation capability High		7.5		μA
				f(BCLK)=32kHz Wait mode ⁽²⁾ , Oscillation capability Low		2.0		μA
				Stop mode T _{opr} =25°C		2.0	6.0	μA
				Stop mode T _{opr} =85°C			20	μA
				Stop mode T _{opr} =125°C			TBD	μA

NOTES:

1. Referenced to V_{CC1}=V_{CC2}=4.0 to 5.5V, V_{SS} = 0V at T_{opr} = -40 to 85°C / -40 to 125°C, f(BCLK)=24MHz unless otherwise specified. T version = -40 to 85°C, V version = -40 to 125°C.
2. With one timer operated using fC32.
3. This indicates the memory in which the program to be executed exists.

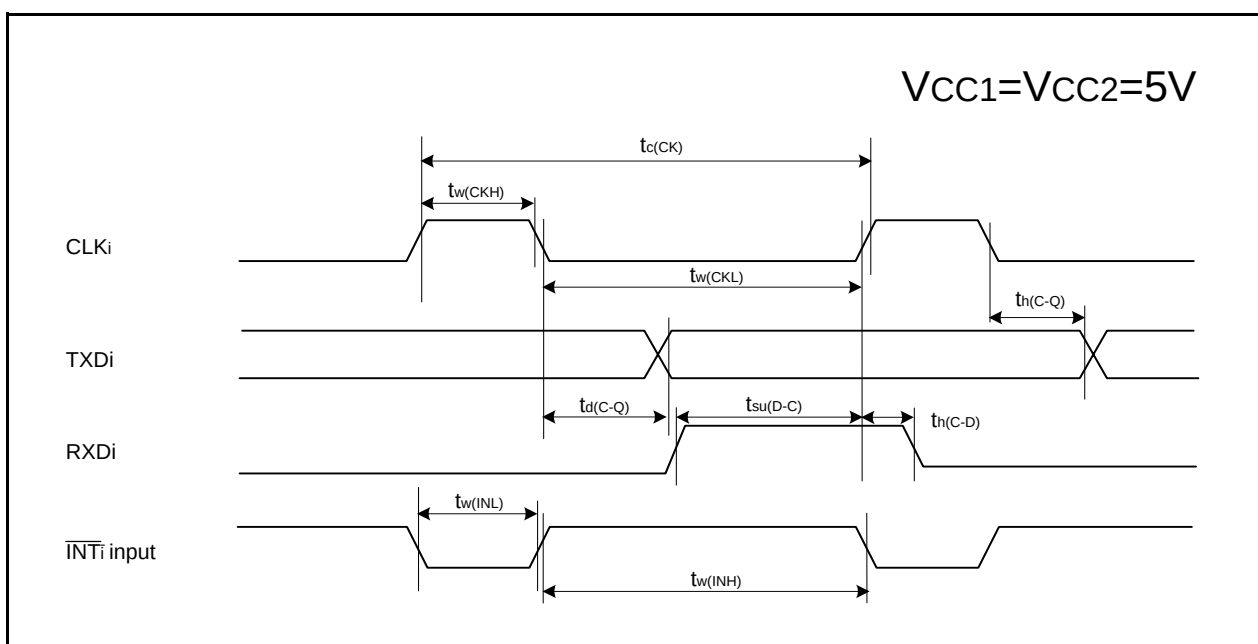


Figure 5.25 Timing Diagram (2)

REVISION HISTORY		M16C/62P Group (M16C/62P, M16C/62PT) Hardware Manual	
Rev.	Date	Description	
		Page	Summary
		47	Figure 5.1 Power Supply Circuit Timing Diagram is partly revised.
		48	Table 5.11 Electrical Characteristics (1) is partly deleted.
		49	Table 5.12 Electrical Characteristics (2) is partly revised.
		50	Note 1 of Table 5.13 External Clock Input (XIN input) is added.
		67	Notes 1 to 4 of Table 5.32 External Clock Input (XIN input) are added.
		85	Table 5.53 Flash Memory Version Electrical Characteristics for 100 cycle products is partly revised. Standard (Min.) is partly revised. Table 5.54 Flash Memory Version Electrical Characteristics for 10,000 cycle products is partly revised. Standard (Min.) is partly revised. Note 5 is revised. Table 23.55 Flash Memory Version Program / Erase Voltage and Read Operation Voltage Characteristics is partly revised.
		87	Table 5.57 Electrical Characteristics (1) is partly deleted.
		88	Table 5.58 Electrical Characteristics is partly revised.

Renesas Technology Corp. Sales Strategic Planning Div. Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan

Keep safety first in your circuit designs!

1. Renesas Technology Corp. puts the maximum effort into making semiconductor products better and more reliable, but there is always the possibility that trouble may occur with them. Trouble with semiconductors may lead to personal injury, fire or property damage. Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of nonflammable material or (iii) prevention against any malfunction or mishap.

Notes regarding these materials

1. These materials are intended as a reference to assist our customers in the selection of the Renesas Technology Corp. product best suited to the customer's application; they do not convey any license under any intellectual property rights, or any other rights, belonging to Renesas Technology Corp. or a third party.
2. Renesas Technology Corp. assumes no responsibility for any damage, or infringement of any third-party's rights, originating in the use of any product data, diagrams, charts, programs, algorithms, or circuit application examples contained in these materials.
3. All information contained in these materials, including product data, diagrams, charts, programs and algorithms represents information on products at the time of publication of these materials, and are subject to change by Renesas Technology Corp. without notice due to product improvements or other reasons. It is therefore recommended that customers contact Renesas Technology Corp. or an authorized Renesas Technology Corp. product distributor for the latest product information before purchasing a product listed herein.
The information described here may contain technical inaccuracies or typographical errors.
Renesas Technology Corp. assumes no responsibility for any damage, liability, or other loss rising from these inaccuracies or errors.
Please also pay attention to information published by Renesas Technology Corp. by various means, including the Renesas Technology Corp. Semiconductor home page (<http://www.renesas.com>).
4. When using any or all of the information contained in these materials, including product data, diagrams, charts, programs, and algorithms, please be sure to evaluate all information as a total system before making a final decision on the applicability of the information and products. Renesas Technology Corp. assumes no responsibility for any damage, liability or other loss resulting from the information contained herein.
5. Renesas Technology Corp. semiconductors are not designed or manufactured for use in a device or system that is used under circumstances in which human life is potentially at stake. Please contact Renesas Technology Corp. or an authorized Renesas Technology Corp. product distributor when considering the use of a product contained herein for any specific purposes, such as apparatus or systems for transportation, vehicular, medical, aerospace, nuclear, or undersea repeater use.
6. The prior written approval of Renesas Technology Corp. is necessary to reprint or reproduce in whole or in part these materials.
7. If these products or technologies are subject to the Japanese export control restrictions, they must be exported under a license from the Japanese government and cannot be imported into a country other than the approved destination.
Any diversion or reexport contrary to the export control laws and regulations of Japan and/or the country of destination is prohibited.
8. Please contact Renesas Technology Corp. for further details on these materials or the products contained therein.



RENESAS SALES OFFICES

<http://www.renesas.com>

Refer to "<http://www.renesas.com/en/network>" for the latest and detailed information.

Renesas Technology America, Inc.

450 Holger Way, San Jose, CA 95134-1368, U.S.A
Tel: <1> (408) 382-7500, Fax: <1> (408) 382-7501

Renesas Technology Europe Limited

Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K.
Tel: <44> (1628) 585-100, Fax: <44> (1628) 585-900

Renesas Technology Hong Kong Ltd.

7th Floor, North Tower, World Finance Centre, Harbour City, 1 Canton Road, Tsimshatsui, Kowloon, Hong Kong
Tel: <852> 2265-6688, Fax: <852> 2730-6071

Renesas Technology Taiwan Co., Ltd.

10th Floor, No.99, Fushing North Road, Taipei, Taiwan
Tel: <886> (2) 2715-2888, Fax: <886> (2) 2713-2999

Renesas Technology (Shanghai) Co., Ltd.

Unit2607 Ruijing Building, No.205 Maoming Road (S), Shanghai 200020, China
Tel: <86> (21) 6472-1001, Fax: <86> (21) 6415-2952

Renesas Technology Singapore Pte. Ltd.

1 Harbour Front Avenue, #06-10, Keppel Bay Tower, Singapore 098632
Tel: <65> 6213-0200, Fax: <65> 6278-8001

Renesas Technology Korea Co., Ltd.

Kukje Center Bldg. 18th Fl., 191, 2-ka, Hangang-ro, Yongsan-ku, Seoul 140-702, Korea
Tel: <82> 2-796-3115, Fax: <82> 2-796-2145

Renesas Technology Malaysia Sdn. Bhd.

Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No.18, Jalan Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: <603> 7955-9390, Fax: <603> 7955-9510