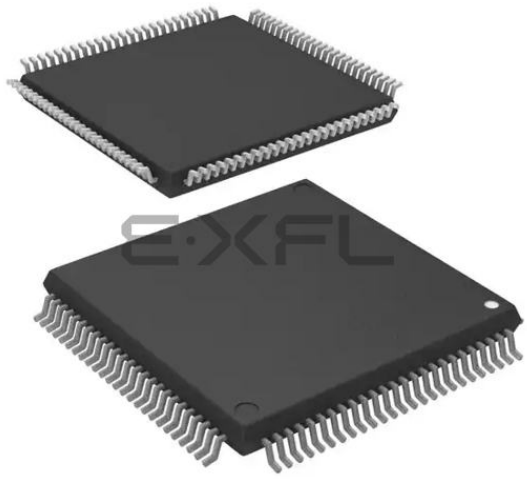
# Renesas Electronics America Inc - M30626FJPGP#U5C Datasheet



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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

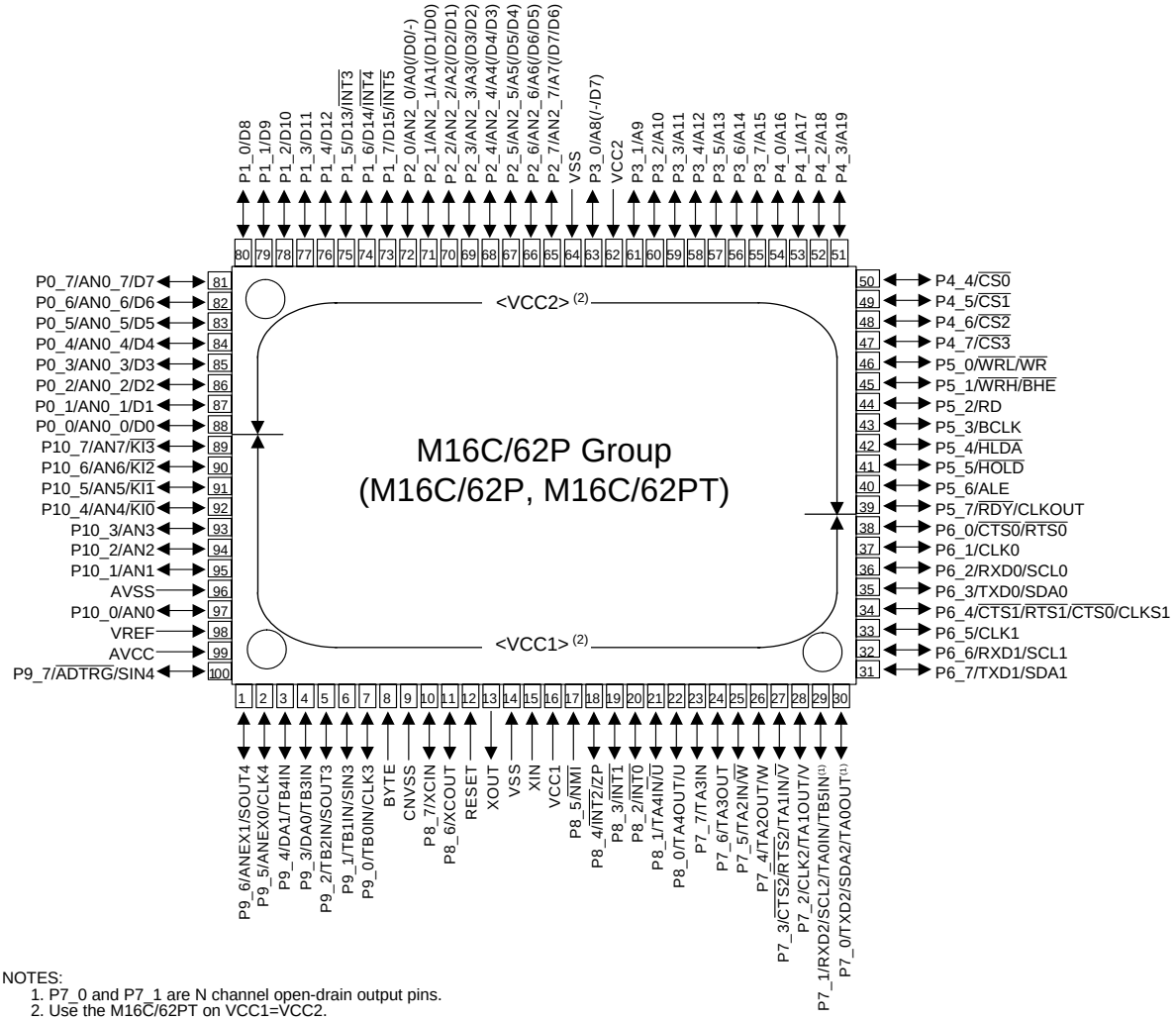
| Details | |
|---|---|
| Product Status | Not For New Designs |
| Core Processor | M16C/60 |
| Core Size | 16-Bit |
| Speed | 24MHz |
| Connectivity | I²C, IEBus, UART/USART |
| Peripherals | DMA, WDT |
| Number of I/O | 85 |
| Program Memory Size | 512KB (512K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | 4K x 8 |
| RAM Size | 31K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.7V ~ 5.5V |
| Data Converters | A/D 26x10b; D/A 2x8b |
| Oscillator Type | Internal |
| Operating Temperature | -20°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 100-LQFP |
| Supplier Device Package | 100-LFQFP (14x14) |
| Purchase URL | https://www.e-xfl.com/product-detail/renesas-electronics-america/m30626fjpgp-u5c |

**Table 1.7 Product List (4) (V version (M16C/62PT)) As of Dec. 2005**

| Type No. | ROM Capacity | RAM Capacity | Package Type(1) | Remarks | |
|---|---|---|---|---|---|
| M3062CM6V-XXXFP (P) | 48 Kbytes | 4 Kbytes | PRQP0100JB-A | Mask ROM version | V Version (High reliability 125°C version) |
| M3062CM6V-XXXGP (P) | | | PLQP0100KB-A | | |
| M3062EM6V-XXXGP (P) | | | PRQP0080JA-A | | |
| M3062CM8V-XXXFP (P) | 64 Kbytes | 4 Kbytes | PRQP0100JB-A | | |
| M3062CM8V-XXXGP (P) | | | PLQP0100KB-A | | |
| M3062EM8V-XXXGP (P) | | | PRQP0080JA-A | | |
| M3062CMAV-XXXFP (P) | 96 Kbytes | 5 Kbytes | PRQP0100JB-A | | |
| M3062CMAV-XXXGP (P) | | | PLQP0100KB-A | | |
| M3062EMAV-XXXGP (P) | | | PRQP0080JA-A | | |
| M3062AMCV-XXXFP (D) | 128 Kbytes | 10 Kbytes | PRQP0100JB-A | | |
| M3062AMCV-XXXGP (D) | | | PLQP0100KB-A | | |
| M3062BMCV-XXXGP (P) | | | PRQP0080JA-A | | |
| M3062AFCVFP (D) | 128K+4 Kbytes | 10 Kbytes | PRQP0100JB-A | Flash memory version (2) | |
| M3062AFCVGP (D) | | | PLQP0100KB-A | | |
| M3062BFCVGP (P) | | | PRQP0080JA-A | | |
| M3062JFHVFP (P) | 384K+4 Kbytes | 31 Kbytes | PRQP0100JB-A | | |
| M3062JFHVGP (P) | | | PLQP0100KB-A | | |

(D): Under development
(P): Under planning
NOTES:
1. The old package type numbers of each package type are as follows.
   PLQP0128KB-A : 128P6Q-A,
   PRQP0100JB-A : 100P6S-A,
   PLQP0100KB-A : 100P6Q-A,
   PRQP0080JA-A : 80P6S-A
2. In the flash memory version, there is 4K bytes area (block A).

PIN CONFIGURATION (top view)

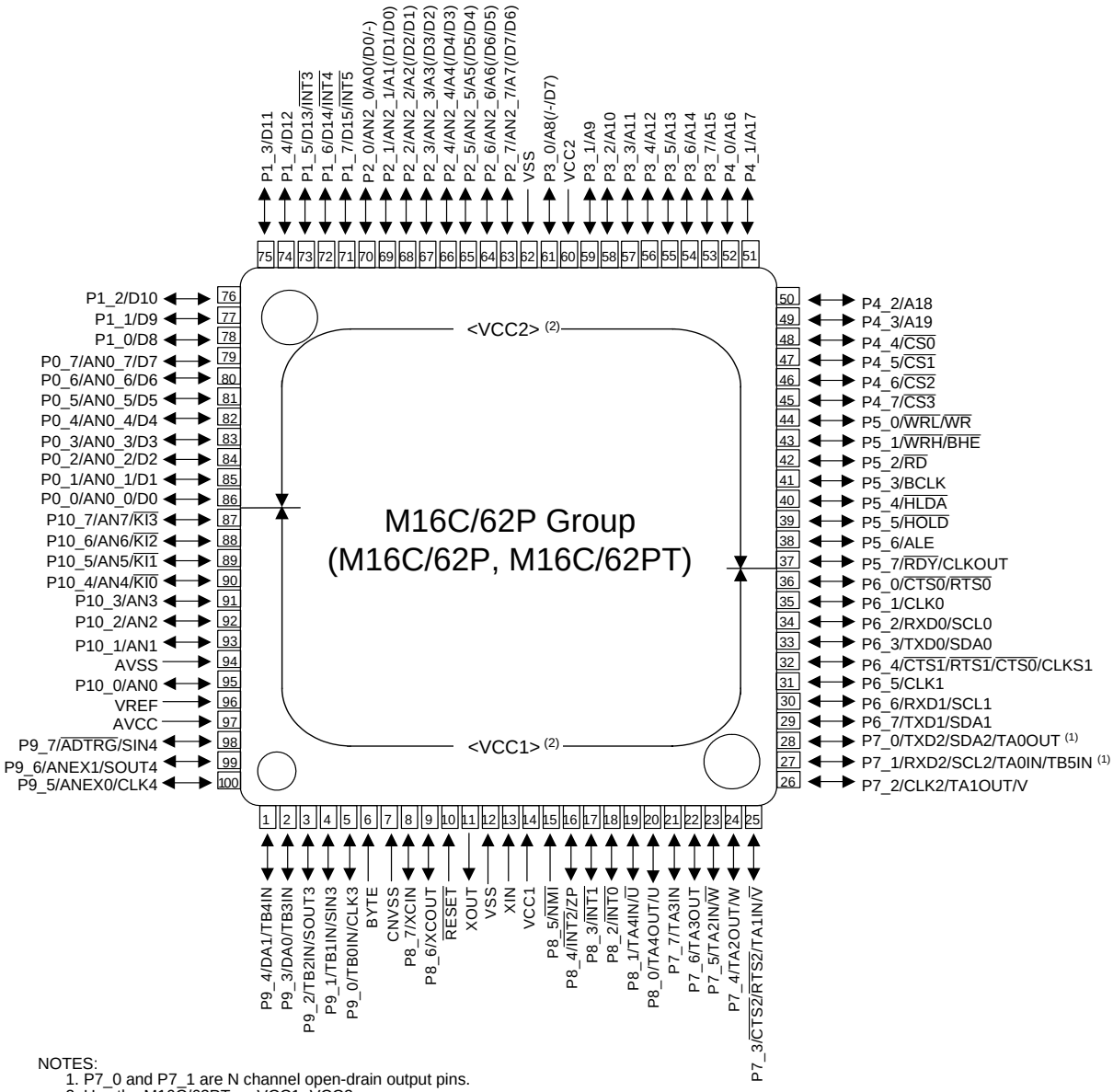



NOTES:
1. P7_0 and P7_1 are N channel open-drain output pins.
2. Use the M16C/62PT on VCC1=VCC2.

Package : PRQP0100JB-A (100P6S-A)

**Figure 1.7 Pin Configuration (Top View)**

PIN CONFIGURATION (top view)



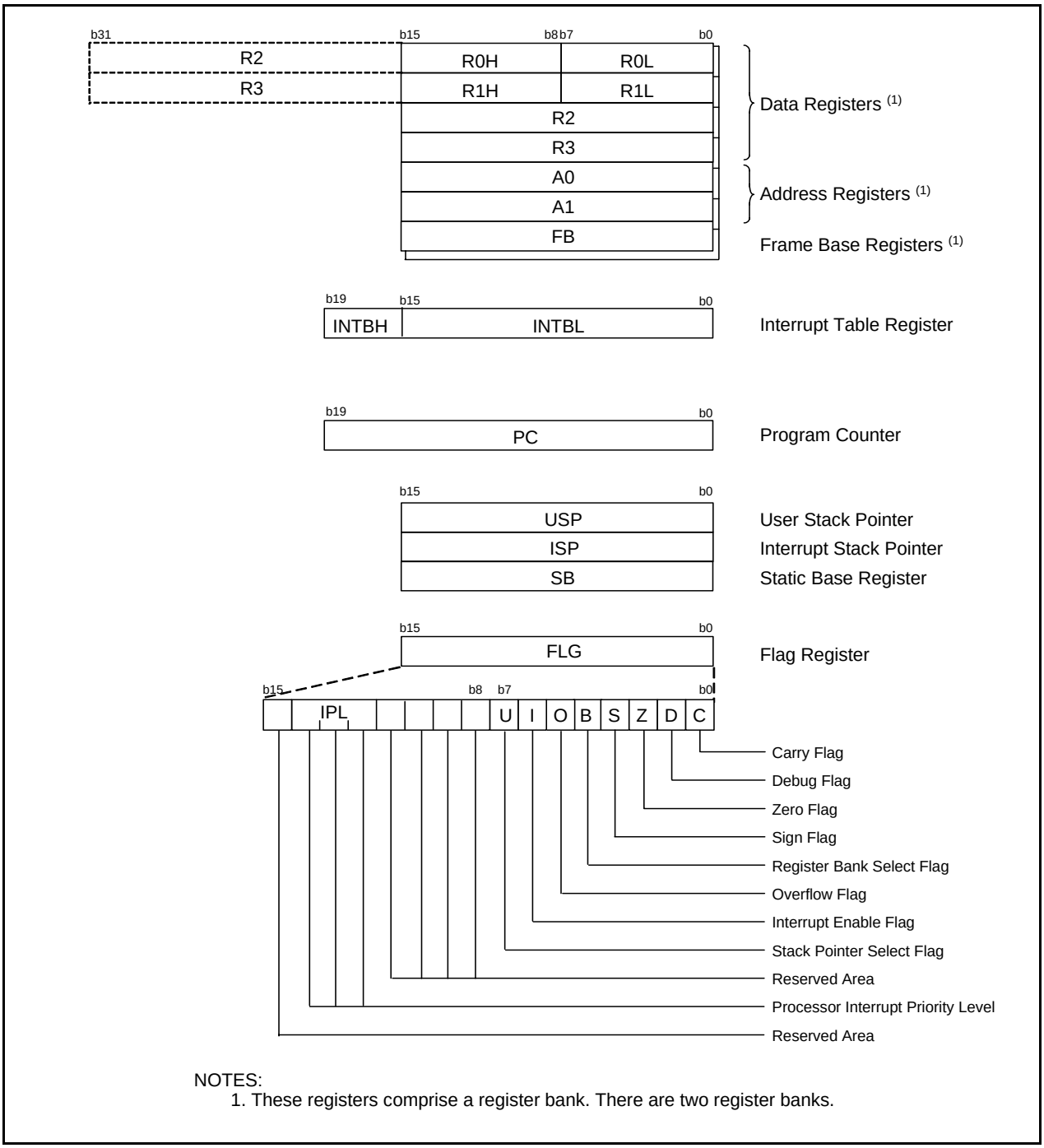

NOTES:
1. P7_0 and P7_1 are N channel open-drain output pins.
2. Use the M16C/62PT on VCC1=VCC2.

Package : PLQP0100KB-A (100P6Q-A)

**Figure 1.8 Pin Configuration (Top View)**

# 2. Central Processing Unit (CPU)

Figure 2.1 shows the CPU registers. The CPU has 13 registers. Of these, R0, R1, R2, R3, A0, A1 and FB comprise a register bank. There are two register banks.




NOTES:
1. These registers comprise a register bank. There are two register banks.

**Figure 2.1 Central Processing Unit Register**

## 2.1 Data Registers (R0, R1, R2 and R3)

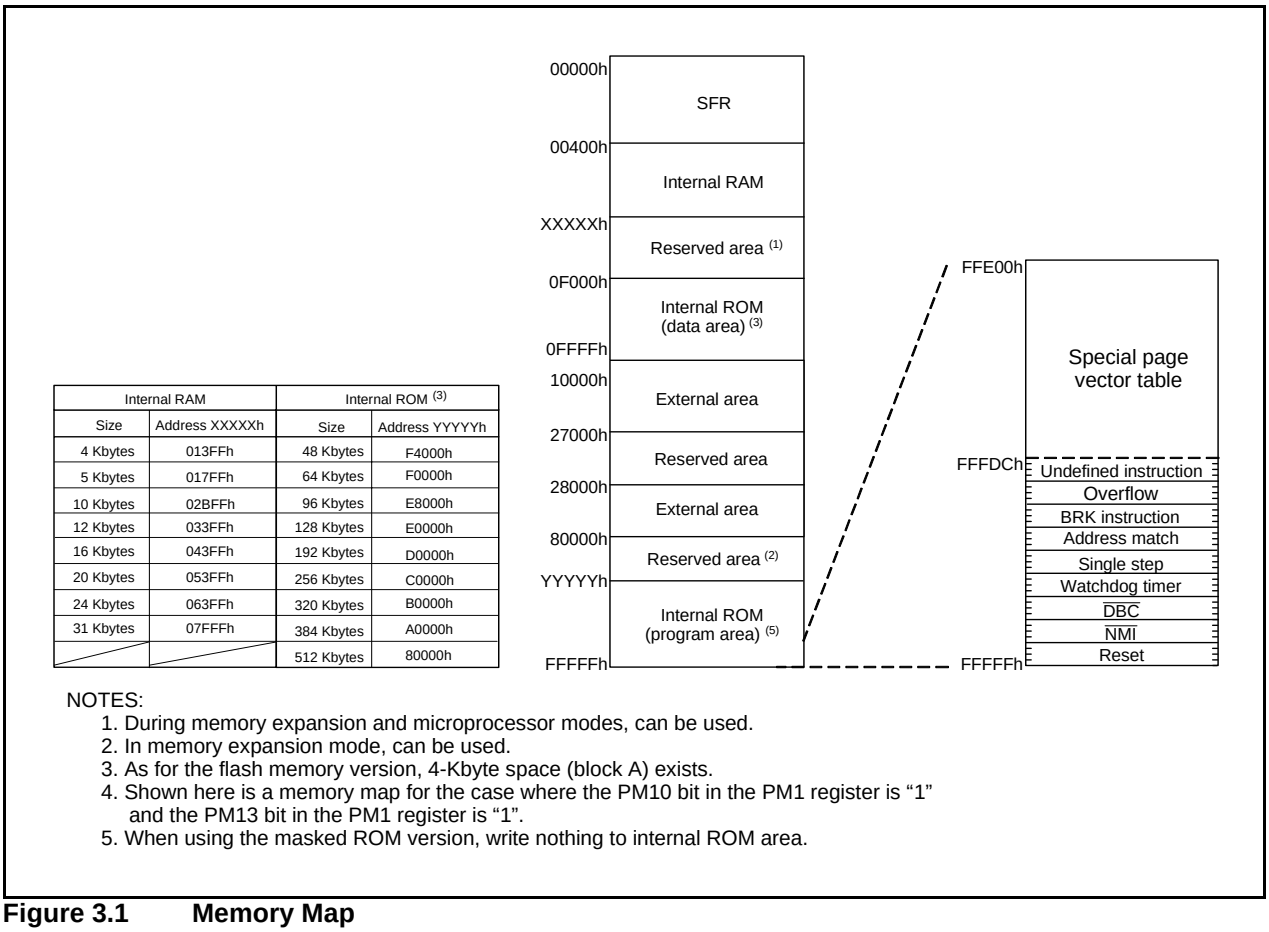
The R0 register consists of 16 bits, and is used mainly for transfers and arithmetic/logic operations. R1 to R3 are the same as R0.

The R0 register can be separated between high (R0H) and low (R0L) for use as two 8-bit data registers.

R1H and R1L are the same as R0H and R0L. Conversely, R2 and R0 can be combined for use as a 32-bit data register (R2R0). R3R1 is the same as R2R0.

# 3. Memory

Figure 3.1 is a Memory Map of the M16C/62P group. The address space extends the 1M bytes from address 00000h to FFFFFh.
The internal ROM is allocated in a lower address direction beginning with address FFFFFh. For example, a 64-Kbyte internal ROM is allocated to the addresses from F0000h to FFFFFh.
As for the flash memory version, 4-Kbyte space (block A) exists in 0F000h to 0FFFFh. 4-Kbyte space is mainly for storing data. In addition to storing data, 4-Kbyte space also can store programs.
The fixed interrupt vector table is allocated to the addresses from FFFDCh to FFFFFh. Therefore, store the start address of each interrupt routine here.
The internal RAM is allocated in an upper address direction beginning with address 00400h. For example, a 10-Kbyte internal RAM is allocated to the addresses from 00400h to 02BFFh. In addition to storing data, the internal RAM also stores the stack used when calling subroutines and when interrupts are generated.
The SRF is allocated to the addresses from 00000h to 003FFh. Peripheral function control registers are located here. Of the SFR, any area which has no functions allocated is reserved for future use and cannot be used by users.
The special page vector table is allocated to the addresses from FFE00h to FFFDBh. This vector is used by the JMPS or JSRS instruction. For details, refer to the **M16C/60 and M16C/20 Series Software Manual**.
In memory expansion and microprocessor modes, some areas are reserved for future use and cannot be used by users. Use M16C/62P (80-pin version) and M16C/62PT in single-chip mode. The memory expansion and microprocessor modes cannot be used
.




| Internal RAM | | Internal ROM (3) | |
|---|---|---|---|
| Size | Address XXXXXh | Size | Address YYYYYh |
| 4 Kbytes | 013FFh | 48 Kbytes | F4000h |
| 5 Kbytes | 017FFh | 64 Kbytes | F0000h |
| 10 Kbytes | 02BFFh | 96 Kbytes | E8000h |
| 12 Kbytes | 033FFh | 128 Kbytes | E0000h |
| 16 Kbytes | 043FFh | 192 Kbytes | D0000h |
| 20 Kbytes | 053FFh | 256 Kbytes | C0000h |
| 24 Kbytes | 063FFh | 320 Kbytes | B0000h |
| 31 Kbytes | 07FFFh | 384 Kbytes | A0000h |
| | | 512 Kbytes | 80000h |

NOTES:
1. During memory expansion and microprocessor modes, can be used.
2. In memory expansion mode, can be used.
3. As for the flash memory version, 4-Kbyte space (block A) exists.
4. Shown here is a memory map for the case where the PM10 bit in the PM1 register is “1” and the PM13 bit in the PM1 register is “1”.
5. When using the masked ROM version, write nothing to internal ROM area.

**Figure 3.1 Memory Map**

**Table 4.2 SFR Information (2)** (1)

| Address | Register | Symbol | After Reset |
|---|---|---|---|
| 0040h | | | |
| 0041h | | | |
| 0042h | | | |
| 0043h | | | |
| 0044h | INT3 Interrupt Control Register | INT3IC | XX00X000b |
| 0045h | Timer B5 Interrupt Control Register | TB5IC | XXXXX000b |
| 0046h | Timer B4 Interrupt Control Register, UART1 BUS Collision Detection Interrupt Control Register | TB4IC, U1BCNIC | XXXXX000b |
| 0047h | Timer B3 Interrupt Control Register, UART0 BUS Collision Detection Interrupt Control Register | TB3IC, U0BCNIC | XXXXX000b |
| 0048h | SI/O4 Interrupt Control Register, INT5 Interrupt Control Register | S4IC, INT5IC | XX00X000b |
| 0049h | SI/O3 Interrupt Control Register, INT4 Interrupt Control Register | S3IC, INT4IC | XX00X000b |
| 004Ah | UART2 Bus Collision Detection Interrupt Control Register | BCNIC | XXXXX000b |
| 004Bh | DMA0 Interrupt Control Register | DM0IC | XXXXX000b |
| 004Ch | DMA1 Interrupt Control Register | DM1IC | XXXXX000b |
| 004Dh | Key Input Interrupt Control Register | KUPIC | XXXXX000b |
| 004Eh | A/D Conversion Interrupt Control Register | ADIC | XXXXX000b |
| 004Fh | UART2 Transmit Interrupt Control Register | S2TIC | XXXXX000b |
| 0050h | UART2 Receive Interrupt Control Register | S2RIC | XXXXX000b |
| 0051h | UART0 Transmit Interrupt Control Register | S0TIC | XXXXX000b |
| 0052h | UART0 Receive Interrupt Control Register | S0RIC | XXXXX000b |
| 0053h | UART1 Transmit Interrupt Control Register | S1TIC | XXXXX000b |
| 0054h | UART1 Receive Interrupt Control Register | S1RIC | XXXXX000b |
| 0055h | Timer A0 Interrupt Control Register | TA0IC | XXXXX000b |
| 0056h | Timer A1 Interrupt Control Register | TA1IC | XXXXX000b |
| 0057h | Timer A2 Interrupt Control Register | TA2IC | XXXXX000b |
| 0058h | Timer A3 Interrupt Control Register | TA3IC | XXXXX000b |
| 0059h | Timer A4 Interrupt Control Register | TA4IC | XXXXX000b |
| 005Ah | Timer B0 Interrupt Control Register | TB0IC | XXXXX000b |
| 005Bh | Timer B1 Interrupt Control Register | TB1IC | XXXXX000b |
| 005Ch | Timer B2 Interrupt Control Register | TB2IC | XXXXX000b |
| 005Dh | INT0 Interrupt Control Register | INT0IC | XX00X000b |
| 005Eh | INT1 Interrupt Control Register | INT1IC | XX00X000b |
| 005Fh | INT2 Interrupt Control Register | INT2IC | XX00X000b |
| 0060h | | | |
| 0061h | | | |
| 0062h | | | |
| 0063h | | | |
| 0064h | | | |
| 0065h | | | |
| 0066h | | | |
| 0067h | | | |
| 0068h | | | |
| 0069h | | | |
| 006Ah | | | |
| 006Bh | | | |
| 006Ch | | | |
| 006Dh | | | |
| 006Eh | | | |
| 006Fh | | | |
| 0070h | | | |
| 0071h | | | |
| 0072h | | | |
| 0073h | | | |
| 0074h | | | |
| 0075h | | | |
| 0076h | | | |
| 0077h | | | |
| 0078h | | | |
| 0079h | | | |
| 007Ah | | | |
| 007Bh | | | |
| 007Ch | | | |
| 007Dh | | | |
| 007Eh | | | |
| 007Fh | | | |

NOTES:
1. The blank areas are reserved and cannot be accessed by users.

X : Nothing is mapped to this bit

**Table 5.2 Recommended Operating Conditions (1)** (1)

| Symbol | Parameter | | Standard | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| $V_{CC1}$, $V_{CC2}$ | Supply Voltage ($V_{CC1} \geq V_{CC2}$) | | 2.7 | 5.0 | 5.5 | V |
| AVcc | Analog Supply Voltage | | | $V_{CC1}$ | | V |
| Vss | Supply Voltage | | | 0 | | V |
| AVss | Analog Supply Voltage | | | 0 | | V |
| $V_{IH}$ | HIGH Input Voltage | P3_1 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P12_0 to P12_7, P13_0 to P13_7 | 0.8$V_{CC2}$ | | $V_{CC2}$ | V |
| | | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 (during single-chip mode) | 0.8$V_{CC2}$ | | $V_{CC2}$ | V |
| | | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 (data input during memory expansion and microprocessor mode) | 0.5$V_{CC2}$ | | $V_{CC2}$ | V |
| | | P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P14_0, P14_1, XIN, $\overline{RESET}$, CNVSS, BYTE | 0.8$V_{CC1}$ | | $V_{CC1}$ | V |
| | | P7_0, P7_1 | 0.8$V_{CC1}$ | | 6.5 | V |
| $V_{IL}$ | LOW Input Voltage | P3_1 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P12_0 to P12_7, P13_0 to P13_7 | 0 | | 0.2$V_{CC2}$ | V |
| | | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 (during single-chip mode) | 0 | | 0.2$V_{CC2}$ | V |
| | | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 (data input during memory expansion and microprocessor mode) | 0 | | 0.16$V_{CC2}$ | V |
| | | P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P14_0, P14_1, XIN, $\overline{RESET}$, CNVSS, BYTE | 0 | | 0.2$V_{CC}$ | V |
| $I_{OH(peak)}$ | HIGH Peak Output Current | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1 | | | –10.0 | mA |
| $I_{OH(avg)}$ | HIGH Average Output Current | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1 | | | –5.0 | mA |
| $I_{OL(peak)}$ | LOW Peak Output Current | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1 | | | 10.0 | mA |
| $I_{OL(avg)}$ | LOW Average Output Current | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1 | | | 5.0 | mA |

NOTES:

1. Referenced to $V_{CC1}$ = $V_{CC2}$ = 2.7 to 5.5V at $T_{opr}$ = –20 to 85°C / –40 to 85°C unless otherwise specified.
2. The Average Output Current is the mean value within 100ms.
3. The total $I_{OL(peak)}$ for ports P0, P1, P2, P8_6, P8_7, P9, P10, P11, P14_0, and P14_1 must be 80mA max. The total $I_{OL(peak)}$ for ports P3, P4, P5, P6, P7, P8_0 to P8_4, P12, and P13 must be 80mA max. The total $I_{OH(peak)}$ for ports P0, P1, and P2 must be –40mA max. The total $I_{OH(peak)}$ for ports P3, P4, P5, P12, and P13 must be –40mA max. The total $I_{OH(peak)}$ for ports P6, P7, and P8_0 to P8_4 must be –40mA max. The total $I_{OH(peak)}$ for ports P8_6, P8_7, P9, P10, P14_0, and P14_1 must be –40mA max. Set Average Output Current to 1/2 of peak. The total $I_{OH(peak)}$ for ports P8_6, P8_7, P9 , P10, P11, P14_0, and P14_1 must be –40mA max.
   As for 80-pin version, the total $I_{OL(peak)}$ for all ports and $I_{OH(peak)}$ must be 80mA. max. due to one $V_{CC}$ and one $V_{SS}$.
4. There is no external connections for port P1_0 to P1_7, P4_4 to P4_7, P7_2 to P7_5 and P9_1 in 80-pin version.

**Table 5.9 Low Voltage Detection Circuit Electrical Characteristics**

| Symbol | Parameter | Measuring Condition | Standard | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| $V_{det4}$ | Low Voltage Detection Voltage (1) | $V_{CC1}$=0.8V to 5.5V | 3.3 | 3.8 | 4.4 | V |
| $V_{det3}$ | Reset Level Detection Voltage (1, 2) | | 2.2 | 2.8 | 3.6 | V |
| $V_{det4}$-$V_{det3}$ | Electric potential difference of Low Voltage Detection and Reset Level Detection | | 0.3 | | | V |
| $V_{det3s}$ | Low Voltage Reset Retention Voltage | | | | 0.8 | V |
| $V_{det3r}$ | Low Voltage Reset Release Voltage (3) | | 2.2 | 2.9 | 4.0 | V |

NOTES:
1. $V_{det4} > V_{det3}$.
2. Where reset level detection voltage is less than 2.7 V, if the supply power voltage is greater than the reset level detection voltage, the microcomputer operates with f(BCLK) ≤ 10MHz.
3. $V_{det3r} > V_{det3}$ is not guaranteed.
4. The voltage detection circuit is designed to use when VCC1 is set to 5V.

**Table 5.10 Power Supply Circuit Timing Characteristics**

| Symbol | Parameter | Measuring Condition | Standard | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| $t_{d(P-R)}$ | Time for Internal Power Supply Stabilization During Powering-On | $V_{CC1}$=2.7V to 5.5V | | | 2 | ms |
| $t_{d(R-S)}$ | STOP Release Time | | | | 150 | µs |
| $t_{d(W-S)}$ | Low Power Dissipation Mode Wait Mode Release Time | | | | 150 | µs |
| $t_{d(S-R)}$ | Brown-out Detection Reset (Hardware Reset 2) Release Wait Time | $V_{CC1}$=$V_{det3r}$ to 5.5V | | 6 (1) | 20 | ms |
| $t_{d(E-A)}$ | Low Voltage Detection Circuit Operation Start Time | $V_{CC1}$=2.7V to 5.5V | | | 20 | µs |

NOTES:
1. When $V_{CC1}$ = 5V.

# $V_{CC1}=V_{CC2}=5V$

**Timing Requirements**
**($V_{CC1}$ = $V_{CC2}$ = 5V, $V_{SS}$ = 0V, at $T_{opr}$ = –20 to 85°C / –40 to 85°C unless otherwise specified)**

**Table 5.13 External Clock Input (XIN input) (1)**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_c$ | External Clock Input Cycle Time | 62.5 | | ns |
| $t_{w(H)}$ | External Clock Input HIGH Pulse Width | 25 | | ns |
| $t_{w(L)}$ | External Clock Input LOW Pulse Width | 25 | | ns |
| $t_r$ | External Clock Rise Time | | 15 | ns |
| $t_f$ | External Clock Fall Time | | 15 | ns |

NOTES:
1. The condition is $V_{CC1}$=$V_{CC2}$=3.0 to 5.0V.

**Table 5.14 Memory Expansion Mode and Microprocessor Mode**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{ac1(RD-DB)}$ | Data Input Access Time (for setting with no wait) | | (NOTE 1) | ns |
| $t_{ac2(RD-DB)}$ | Data Input Access Time (for setting with wait) | | (NOTE 2) | ns |
| $t_{ac3(RD-DB)}$ | Data Input Access Time (when accessing multiplex bus area) | | (NOTE 3) | ns |
| $t_{su(DB-RD)}$ | Data Input Setup Time | 40 | | ns |
| $t_{su(RDY-BCLK)}$ | $\overline{RDY}$ Input Setup Time | 30 | | ns |
| $t_{su(HOLD-BCLK)}$ | $\overline{HOLD}$ Input Setup Time | 40 | | ns |
| $t_{h(RD-DB)}$ | Data Input Hold Time | 0 | | ns |
| $t_{h(BCLK-RDY)}$ | $\overline{RDY}$ Input Hold Time | 0 | | ns |
| $t_{h(BCLK-HOLD)}$ | $\overline{HOLD}$ Input Hold Time | 0 | | ns |

NOTES:
1. Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f(BCLK)} - 45[ns]$$

2. Calculated according to the BCLK frequency as follows:

$$\frac{(n-0.5) \times 10^9}{f(BCLK)} - 45[ns]$$ n is ”2” for 1-wait setting, “3” for 2-wait setting and “4” for 3-wait setting.

3. Calculated according to the BCLK frequency as follows:

$$\frac{(n-0.5) \times 10^9}{f(BCLK)} - 45[ns]$$ n is “2” for 2-wait setting, “3” for 3-wait setting.

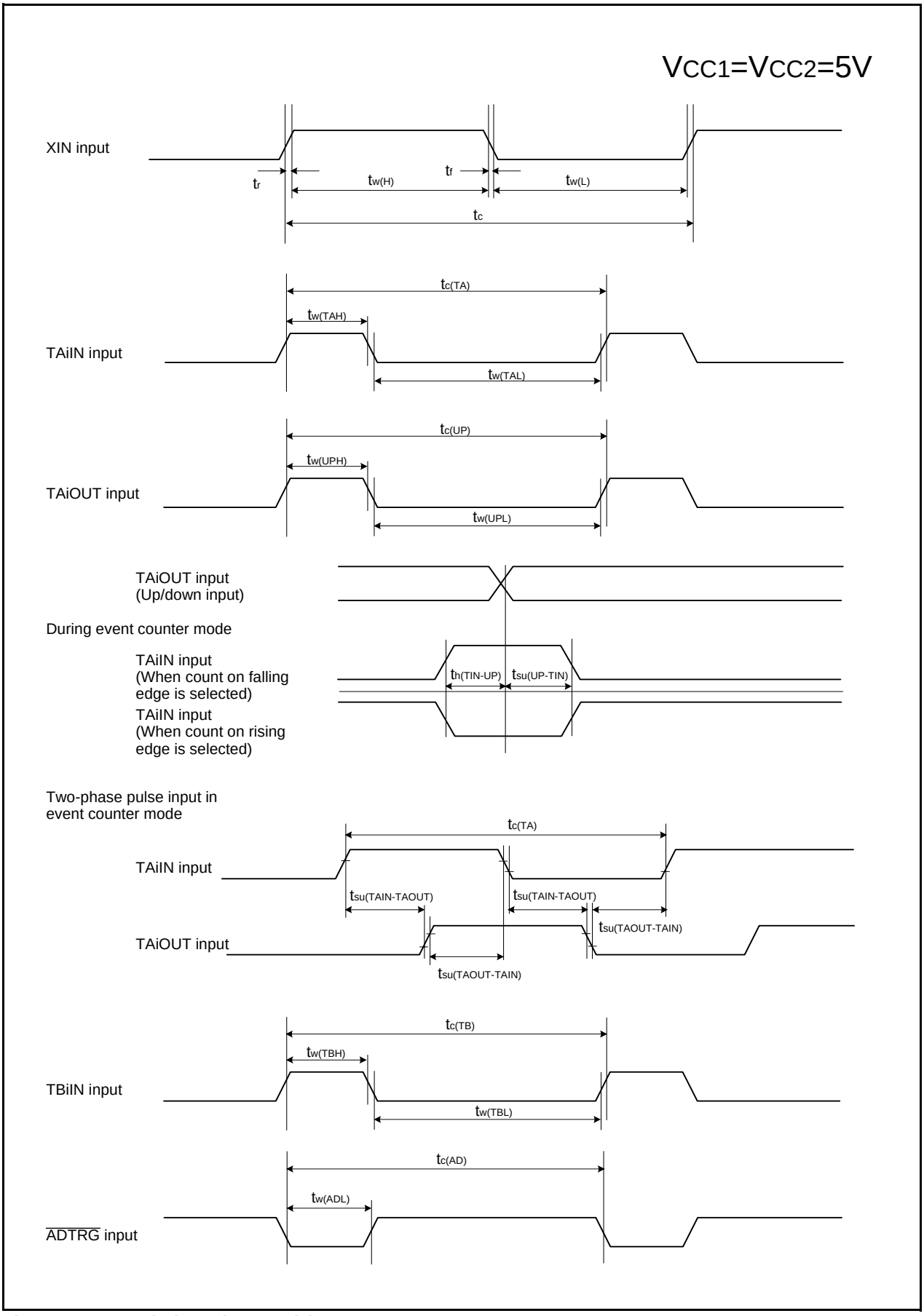



**Figure 5.3 Timing Diagram (1)**

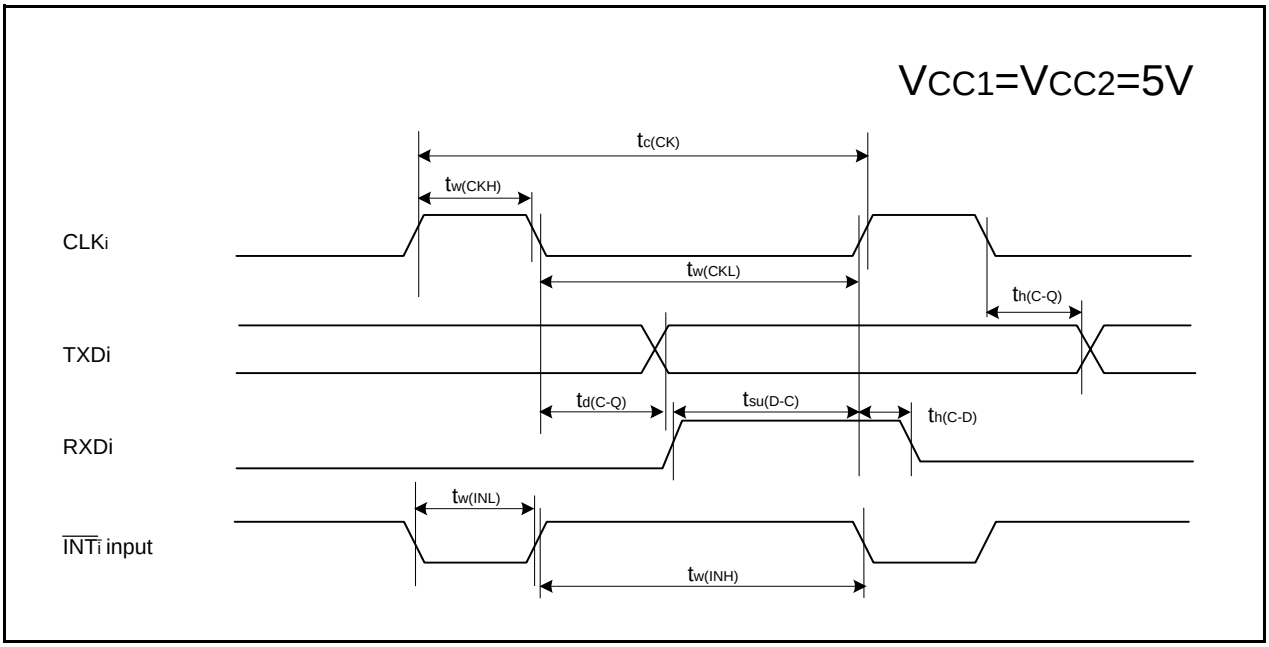
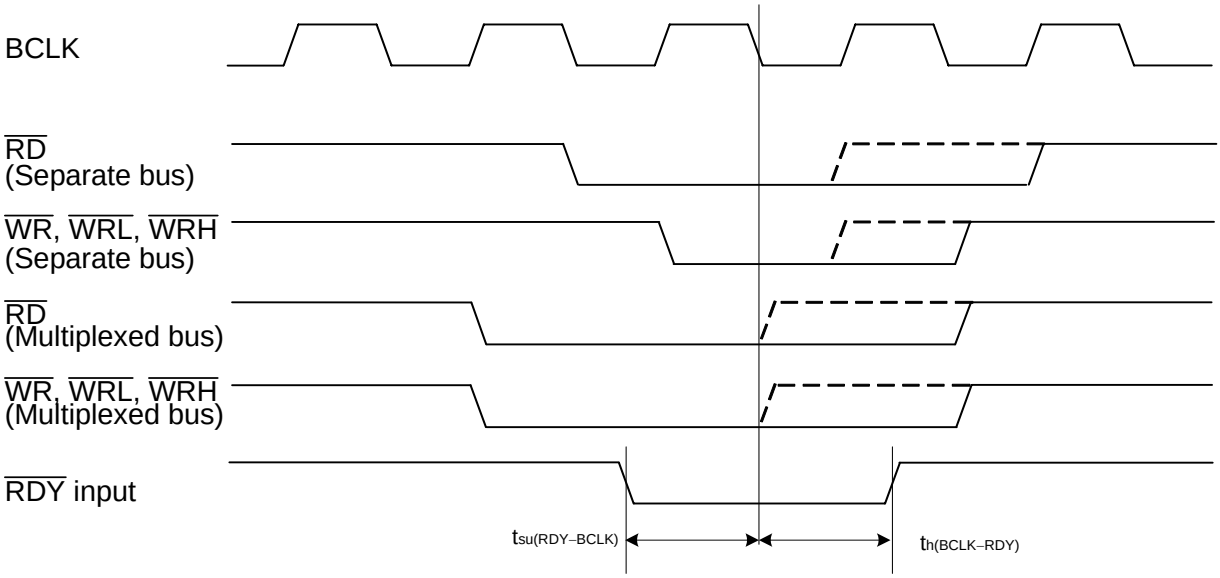



**Figure 5.4 Timing Diagram (2)**

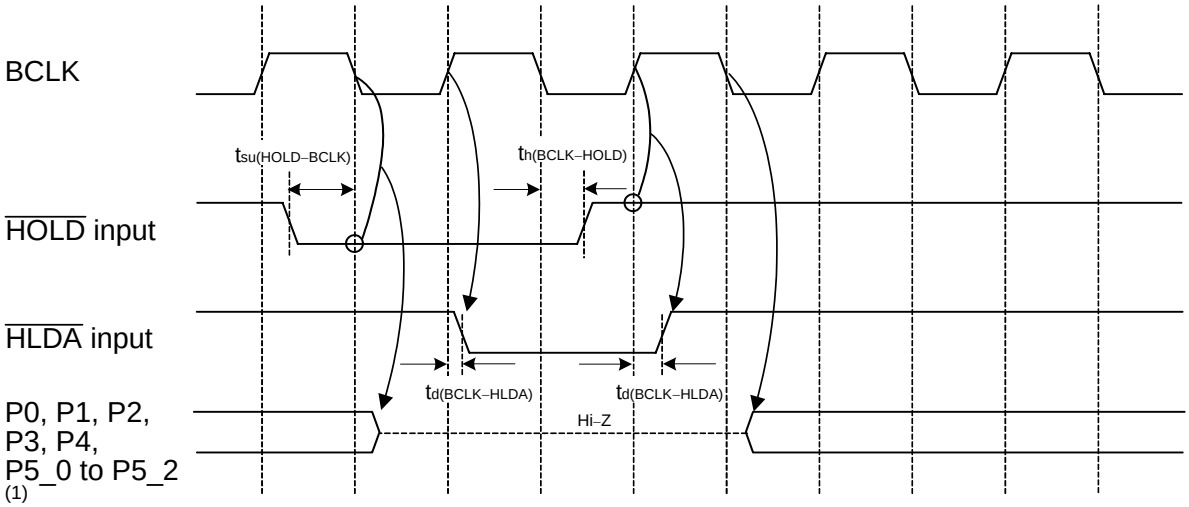
$V_{CC1}=V_{CC2}=5V$

**Memory Expansion Mode, Microprocessor Mode**

**(**Effective for setting with wait**)**




**(**Common to setting with wait and setting without wait**)**




NOTES:

1. These pins are set to high-impedance regardless of the input level of the BYTE pin, PM06 bit in PM0 register and PM11 bit in PM1 register.

· Measuring conditions :
· $V_{CC1}=V_{CC2}=5V$
· Input timing voltage : Determined with $V_{IL}=1.0V$, $V_{IH}=4.0V$
· Output timing voltage : Determined with $V_{OL}=2.5V$, $V_{OH}=2.5V$

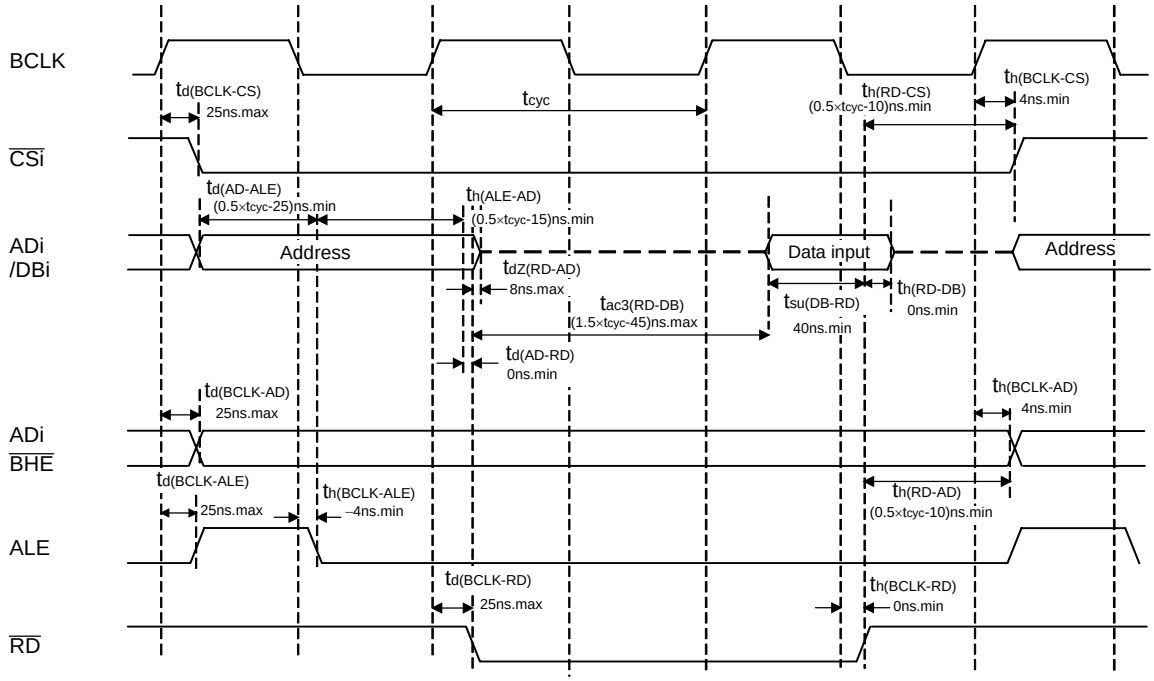
**Figure 5.5 Timing Diagram (3)**

$V_{CC1}=V_{CC2}=5V$

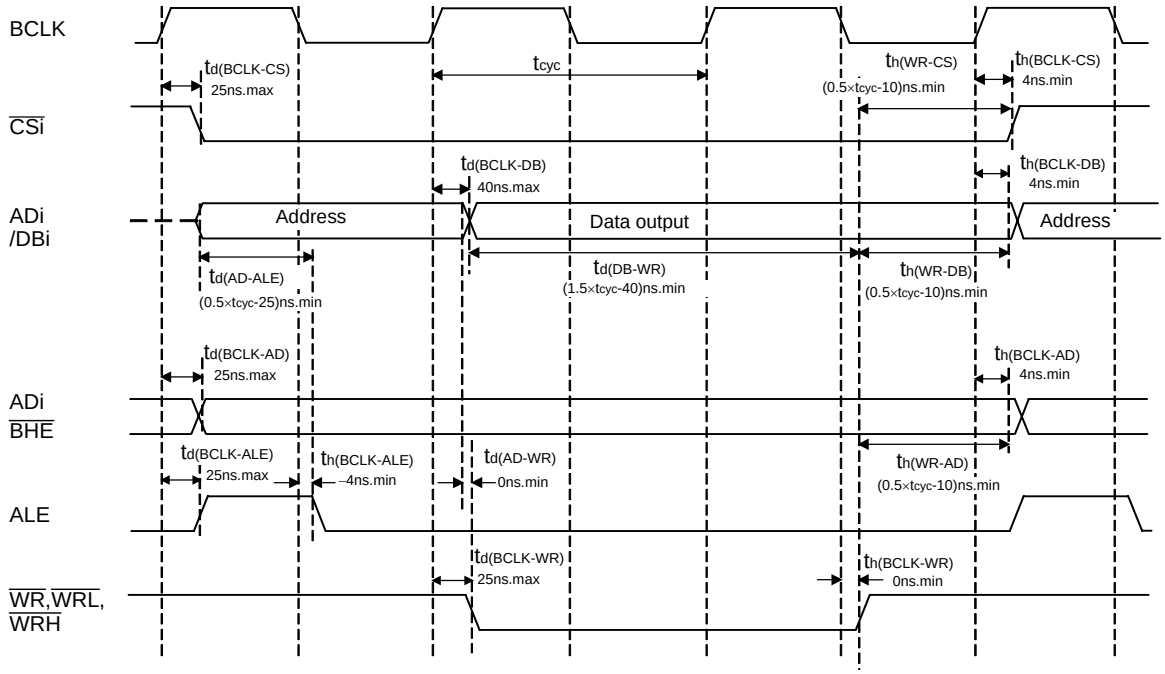
## Memory Expansion Mode, Microprocessor Mode

**(**For 1- or 2-wait setting, external area access and multiplex bus selection**)**

### Read timing




### Write timing




Measuring conditions
· $V_{CC1}=V_{CC2}=5V$
· Input timing voltage : $V_{IL}=0.8V$, $V_{IH}=2.0V$
· Output timing voltage : $V_{OL}=0.4V$, $V_{OH}=2.4V$

**Figure 5.10 Timing Diagram (8)**

**Table 5.31 Electrical Characteristics (2)** (1)

| Symbol | Parameter | | Measuring Condition | | Standard | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min. | Typ. | Max. | |
| $I_{CC}$ | Power Supply Current ($V_{CC1}$=$V_{CC2}$=2.7V to 3.6V) | In single-chip mode, the output pins are open and other pins are $V_{SS}$ | Mask ROM | f(BCLK)=10MHz<br>No division | | 8 | 11 | mA |
| | | | | No division,<br>On-chip oscillation | | 1 | | mA |
| | | | Flash Memory | f(BCLK)=10MHz,<br>No division | | 8 | 13 | mA |
| | | | | No division,<br>On-chip oscillation | | 1.8 | | mA |
| | | | Flash Memory Program | f(BCLK)=10MHz,<br>VCC1=3.0V | | 12 | | mA |
| | | | Flash Memory Erase | f(BCLK)=10MHz,<br>VCC1=3.0V | | 22 | | mA |
| | | | Mask ROM | f(XCIN)=32kHz<br>Low power dissipation mode, ROM (3) | | 25 | | µA |
| | | | Flash Memory | f(BCLK)=32kHz<br>Low power dissipation mode, RAM (3) | | 25 | | µA |
| | | | | f(BCLK)=32kHz<br>Low power dissipation mode, Flash Memory (3) | | 420 | | µA |
| | | | | On-chip oscillation,<br>Wait mode | | 45 | | µA |
| | | | Mask ROM<br>Flash Memory | f(BCLK)=32kHz<br>Wait mode (2),<br>Oscillation capability High | | 6.0 | | µA |
| | | | | f(BCLK)=32kHz<br>Wait mode (2),<br>Oscillation capability Low | | 1.8 | | µA |
| | | | | Stop mode<br>Topr =25°C | | 0.7 | 3.0 | µA |
| $I_{det4}$ | Low Voltage Detection Dissipation Current (4) | | | | | 0.6 | 4 | µA |
| $I_{det3}$ | Reset Area Detection Dissipation Current (4) | | | | | 0.4 | 2 | µA |

NOTES:
1. Referenced to $V_{CC1}$=$V_{CC2}$=2.7 to 3.3V, $V_{SS}$ = 0V at $T_{opr}$ = –20 to 85°C / –40 to 85°C, f(BCLK)=10MHz unless otherwise specified.
2. With one timer operated using fC32.
3. This indicates the memory in which the program to be executed exists.
4. $I_{det}$ is dissipation current when the following bit is set to “1” (detection circuit enabled).

   $I_{det4}$: VC27 bit in the VCR2 register

   $I_{det3}$: VC26 bit in the VCR2 register

# $V_{CC1}=V_{CC2}=3V$

## Switching Characteristics

**($V_{CC1}$ = $V_{CC2}$ = 3V, $V_{SS}$ = 0V, at $T_{opr}$ = –20 to 85°C / –40 to 85°C unless otherwise specified)**

**Table 5.46 Memory Expansion and Microprocessor Modes (for setting with no wait)**

| Symbol | Parameter | | Standard | | Unit |
|---|---|---|---|---|---|
| | | | Min. | Max. | |
| td(BCLK-AD) | Address Output Delay Time | See **Figure 5.12** | | 30 | ns |
| th(BCLK-AD) | Address Output Hold Time (in relation to BCLK) | | 4 | | ns |
| th(RD-AD) | Address Output Hold Time (in relation to RD) | | 0 | | ns |
| th(WR-AD) | Address Output Hold Time (in relation to WR) | | (NOTE 2) | | ns |
| td(BCLK-CS) | Chip Select Output Delay Time | | | 30 | ns |
| th(BCLK-CS) | Chip Select Output Hold Time (in relation to BCLK) | | 4 | | ns |
| td(BCLK-ALE) | ALE Signal Output Delay Time | | | 25 | ns |
| th(BCLK-ALE) | ALE Signal Output Hold Time | | –4 | | ns |
| td(BCLK-RD) | RD Signal Output Delay Time | | | 30 | ns |
| th(BCLK-RD) | RD Signal Output Hold Time | | 0 | | ns |
| td(BCLK-WR) | WR Signal Output Delay Time | | | 30 | ns |
| th(BCLK-WR) | WR Signal Output Hold Time | | 0 | | ns |
| td(BCLK-DB) | Data Output Delay Time (in relation to BCLK) | | | 40 | ns |
| th(BCLK-DB) | Data Output Hold Time (in relation to BCLK) (3) | | 4 | | ns |
| td(DB-WR) | Data Output Delay Time (in relation to WR) | | (NOTE 1) | | ns |
| th(WR-DB) | Data Output Hold Time (in relation to WR) (3) | | (NOTE 2) | | ns |
| td(BCLK-HLDA) | HLDA Output Delay Time | | | 40 | ns |

NOTES:

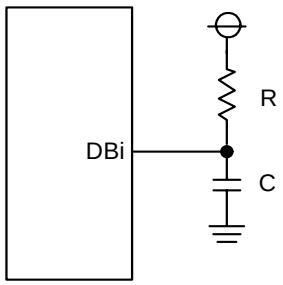
1. Calculated according to the BCLK frequency as follows:

$$\frac{0.5\times10^{9}}{f(BCLK)} - 40[ns]$$ f(BCLK) is 12.5MHz or less.

2. Calculated according to the BCLK frequency as follows:

$$\frac{0.5\times10^{9}}{f(BCLK)} - 10[ns]$$

3. This standard value shows the timing when the output is off, and does not show hold time of data bus.
   Hold time of data bus varies with capacitor volume and pull-up (pull-down) resistance value.
   Hold time of data bus is expressed in
   $t = -CR \times \ln(1 - V_{OL} / V_{CC2})$
   by a circuit of the right figure.
   For example, when $V_{OL} = 0.2V_{CC2}$, C = 30pF, R = 1kΩ, hold time of output "L" level is
   $t = -30pF \times 1k\Omega \times \ln(1 - 0.2V_{CC2} / V_{CC2})$
   = 6.7ns.



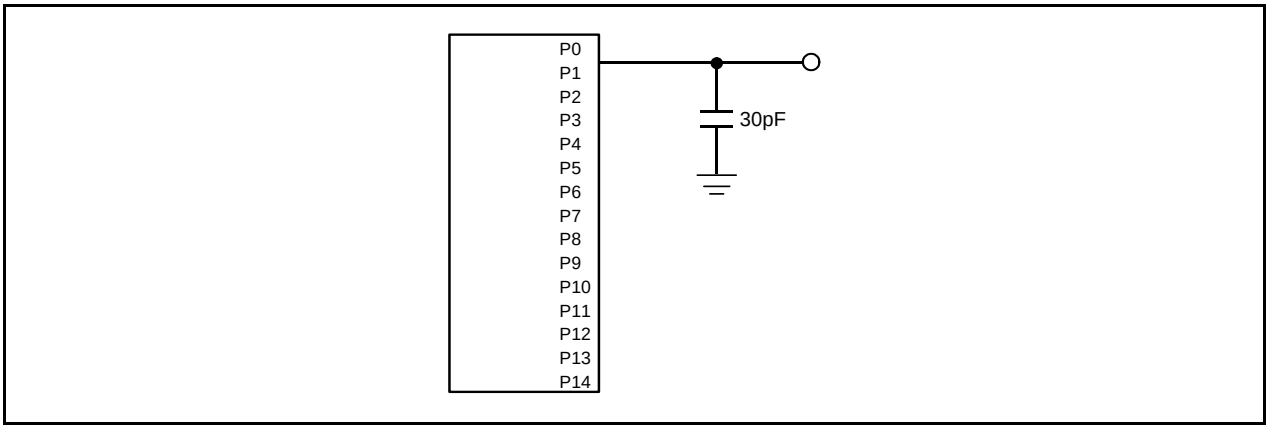




**Figure 5.12 Ports P0 to P14 Measurement Circuit**

# $V_{CC1}=V_{CC2}=3V$

## Switching Characteristics

**($V_{CC1}$ = $V_{CC2}$ = 5V, $V_{SS}$ = 0V, at $T_{opr}$ = –20 to 85°C / –40 to 85°C unless otherwise specified)**

**Table 5.47 Memory Expansion and Microprocessor Modes (for 1- to 3-wait setting and external area access)**

| Symbol | Parameter | | Standard | | Unit |
|---|---|---|---|---|---|
| | | | Min. | Max. | |
| $t_{d(BCLK-AD)}$ | Address Output Delay Time | See **Figure 5.12** | | 30 | ns |
| $t_{h(BCLK-AD)}$ | Address Output Hold Time (in relation to BCLK) | | 4 | | ns |
| $t_{h(RD-AD)}$ | Address Output Hold Time (in relation to RD) | | 0 | | ns |
| $t_{h(WR-AD)}$ | Address Output Hold Time (in relation to WR) | | (NOTE 2) | | ns |
| $t_{d(BCLK-CS)}$ | Chip Select Output Delay Time | | | 30 | ns |
| $t_{h(BCLK-CS)}$ | Chip Select Output Hold Time (in relation to BCLK) | | 4 | | ns |
| $t_{d(BCLK-ALE)}$ | ALE Signal Output Delay Time | | | 25 | ns |
| $t_{h(BCLK-ALE)}$ | ALE Signal Output Hold Time | | -4 | | ns |
| $t_{d(BCLK-RD)}$ | RD Signal Output Delay Time | | | 30 | ns |
| $t_{h(BCLK-RD)}$ | RD Signal Output Hold Time | | 0 | | ns |
| $t_{d(BCLK-WR)}$ | WR Signal Output Delay Time | | | 30 | ns |
| $t_{h(BCLK-WR)}$ | WR Signal Output Hold Time | | 0 | | ns |
| $t_{d(BCLK-DB)}$ | Data Output Delay Time (in relation to BCLK) | | | 40 | ns |
| $t_{h(BCLK-DB)}$ | Data Output Hold Time (in relation to BCLK) (3) | | 4 | | ns |
| $t_{d(DB-WR)}$ | Data Output Delay Time (in relation to WR) | | (NOTE 1) | | ns |
| th(WR-DB) | Data Output Hold Time (in relation to WR)(3) | | (NOTE 2) | | ns |
| $t_{d(BCLK-HLDA)}$ | HLDA Output Delay Time | | | 40 | ns |

NOTES:

1. Calculated according to the BCLK frequency as follows:

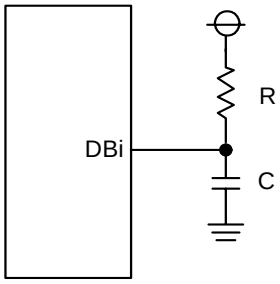
$$\frac{(n-0.5)\times 10^9}{f(BCLK)} - 40[ns]$$

n is “1” for 1-wait setting, “2” for 2-wait setting and “3” for 3-wait setting.
(BCLK) is 12.5MHz or less.

2. Calculated according to the BCLK frequency as follows:

$$\frac{0.5\times 10^9}{f(BCLK)} - 10[ns]$$

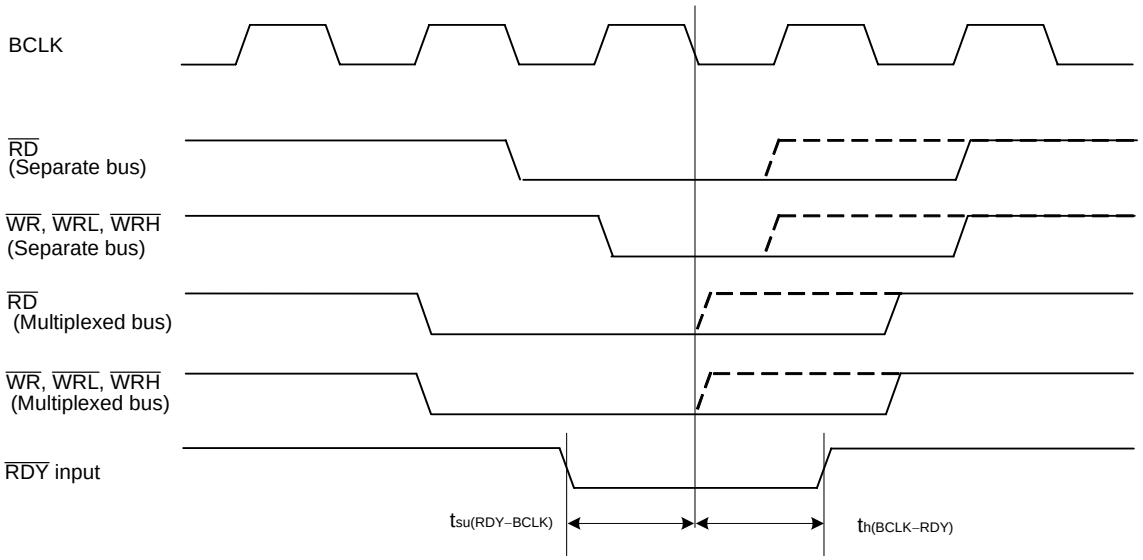
3. This standard value shows the timing when the output is off, and does not show hold time of data bus.
Hold time of data bus varies with capacitor volume and pull-up (pull-down) resistance value.
Hold time of data bus is expressed in
$t = -CR \times \ln(1 - V_{OL} / V_{CC2})$
by a circuit of the right figure.
For example, when $V_{OL}$ = 0.2$V_{CC2}$, C = 30pF, R = 1kΩ, hold time of output ”L” level is
$t = -30pF \times 1k\Omega \times \ln(1 - 0.2V_{CC2} / V_{CC2})$
= 6.7ns.



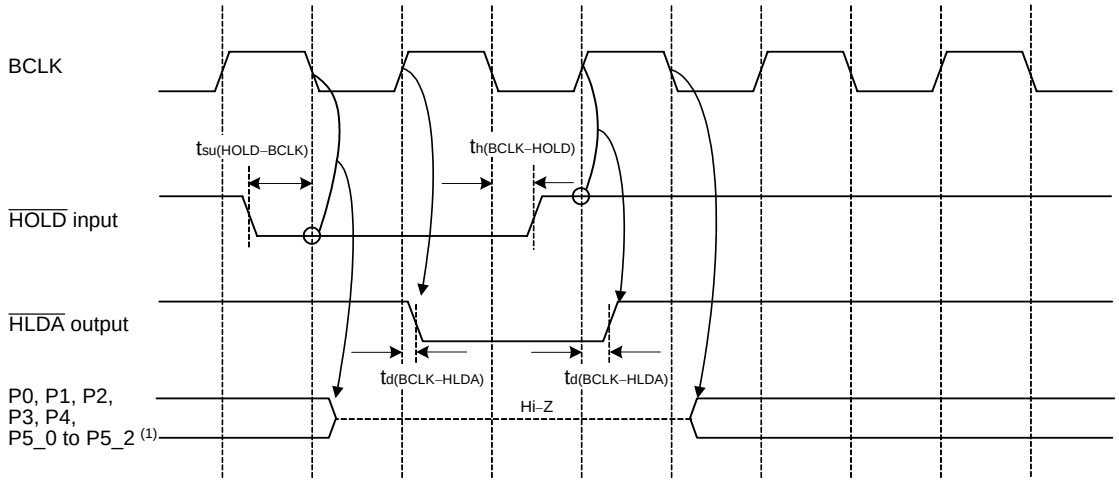
**Memory Expansion Mode, Microprocessor Mode**

$V_{CC1}=V_{CC2}=3V$

(Effective for setting with wait)




(Common to setting with wait and setting without wait)




NOTES:
1. These pins are set to high-impedance regardless of the input level of the BYTE pin, PM06 bit in PM0 register and PM11 bit in PM1 register.

Measuring conditions :
· $V_{CC1}=V_{CC2}=3V$
· Input timing voltage : Determined with $V_{IL}=0.6V$, $V_{IH}=2.4V$
· Output timing voltage : Determined with $V_{OL}=1.5V$, $V_{OH}=1.5V$

**Figure 5.15 Timing Diagram (3)**

**Table 5.56 Power Supply Circuit Timing Characteristics**

| Symbol | Parameter | Measuring Condition | Standard | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| $t_{d(P-R)}$ | Time for Internal Power Supply Stabilization During Powering-On | $V_{CC1}$=4.0V to 5.5V | | | 2 | ms |
| $t_{d(R-S)}$ | STOP Release Time | | | | 150 | µs |
| $t_{d(W-S)}$ | Low Power Dissipation Mode Wait Mode Release Time | | | | 150 | µs |

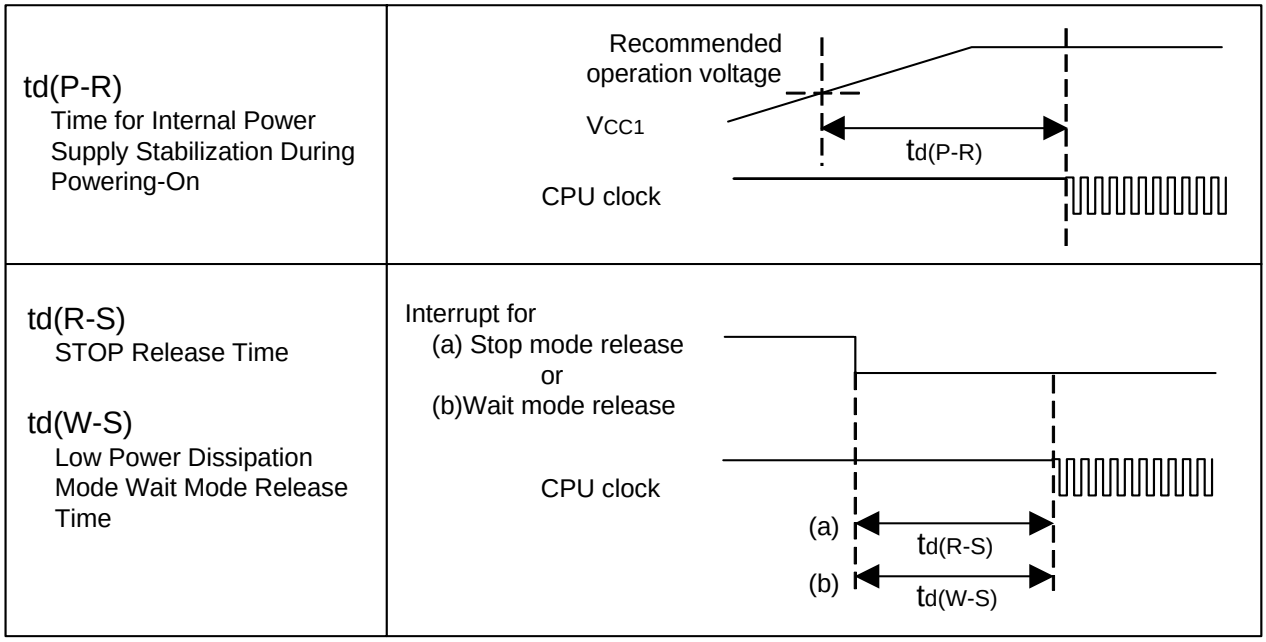



**Figure 5.22 Power Supply Circuit Timing Diagram**

# $V_{CC1}=V_{CC2}=5V$

**Table 5.57 Electrical Characteristics (1)** (1)

| Symbol | Parameter | | Measuring Condition | Standard | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | Max. | |
| $V_{OH}$ | HIGH Output Voltage (2) | P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P14_0, P14_1 | $I_{OH}$=–5mA | $V_{CC1}$–2.0 | | $V_{CC1}$ | V |
| | | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P12_0 to P12_7, P13_0 to P13_7 | $I_{OH}$=–5mA | $V_{CC2}$–2.0 | | $V_{CC2}$ | |
| $V_{OH}$ | HIGH Output Voltage (2) | P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P14_0, P14_1 | $I_{OH}$=–200μA | $V_{CC1}$–0.3 | | $V_{CC1}$ | V |
| | | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P12_0 to P12_7, P13_0 to P13_7 | $I_{OH}$=–200μA | $V_{CC2}$–0.3 | | $V_{CC2}$ | |
| $V_{OH}$ | HIGH Output Voltage XOUT | HIGHPOWER | $I_{OH}$=–1mA | $V_{CC1}$–2.0 | | $V_{CC1}$ | V |
| | | LOWPOWER | $I_{OH}$=–0.5mA | $V_{CC1}$–2.0 | | $V_{CC1}$ | |
| | HIGH Output Voltage XCOUT | HIGHPOWER | With no load applied | | 2.5 | | V |
| | | LOWPOWER | With no load applied | | 1.6 | | |
| $V_{OL}$ | LOW Output Voltage (2) | P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P14_0, P14_1 | $I_{OL}$=5mA | | | 2.0 | V |
| | | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P12_0 to P12_7, P13_0 to P13_7 | $I_{OL}$=5mA | | | 2.0 | |
| $V_{OL}$ | LOW Output Voltage (2) | P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P14_0, P14_1 | $I_{OL}$=200μA | | | 0.45 | V |
| | | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P12_0 to P12_7, P13_0 to P13_7 | $I_{OL}$=200μA | | | 0.45 | |
| $V_{OL}$ | LOW Output Voltage XOUT | HIGHPOWER | $I_{OL}$=1mA | | | 2.0 | V |
| | | LOWPOWER | $I_{OL}$=0.5mA | | | 2.0 | |
| | LOW Output Voltage XCOUT | HIGHPOWER | With no load applied | | 0 | | V |
| | | LOWPOWER | With no load applied | | 0 | | |
| $V_{T+}$-$V_{T-}$ | Hysteresis | HOLD, RDY, TA0IN to TA4IN, TB0IN to TB5IN, INT0 to INT5, NMI, ADTRG, CTS0 to CTS2, CLK0 to CLK4, TA0OUT to TA4OUT, KI0 to KI3, RXD0 to RXD2, SCL0 to SCL2, SDA0 to SDA2, SIN3, SIN4 | | 0.2 | | 1.0 | V |
| $V_{T+}$-$V_{T-}$ | Hysteresis | RESET | | 0.2 | | 2.5 | V |
| $I_{IH}$ | HIGH Input Current (2) | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1, XIN, RESET, CNVSS, BYTE | $V_I$=5V | | | 5.0 | μA |
| $I_{IL}$ | LOW Input Current (2) | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7,P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1, XIN, RESET, CNVSS, BYTE | $V_I$=0V | | | –5.0 | μA |
| $R_{PULLUP}$ | Pull-Up Resistance (2) | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7,P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1 | $V_I$=0V | 30 | 50 | 170 | kΩ |
| $R_{fXIN}$ | Feedback Resistance XIN | | | | 1.5 | | MΩ |
| $R_{fXCIN}$ | Feedback Resistance XCIN | | | | 15 | | MΩ |
| $V_{RAM}$ | RAM Retention Voltage | | At stop mode | 2.0 | | | V |

NOTES:
1. Referenced to $V_{CC1}=V_{CC2}$=4.0 to 5.5V, $V_{SS}$ = 0V at $T_{opr}$ = –40 to 85°C / –40 to 125°C, f(BCLK)=24MHz unless otherwise specified. T version = –40 to 85°C, V version =–40 to 125°C.
2. There is no external connections for port P1_0 to P1_7, P4_4 to P4_7, P7_2 to P7_5 and P9_1 in 80-pin version.

| Rev. | Date | Description | |
|---|---|---|---|
| | | Page | Summary |
| | | 33 | Table 5.4 A-D Conversion Characteristics is revised. |
| | | | Table 5.5 D-A Conversion Characteristics revised. |
| | | 34,74 | Table 5.6 to 5.7 and table 5.54 to 5.55 are revised. |
| | | 36 | Table 5.11 is revised. |
| | | 38,55 | Table 5.14 and 5.33 HLDA output deley time is deleted. |
| | | 41 | Figure 5.1 is partly revised. |
| | | 41-43, 58-60 | Table 5.27 to 5.29 and table 5.46 to 48 HLDA output deley time is added. |
| | | 44 | Figure 5.2 Timing Diagram (1) XIN input is added. |
| | | 47-48 | Figure 5.5 to 5.6 Read timing DB → DBi |
| | | 49-50 | Figure 5.7 to 5.8 Write timing DB → DBi |
| | | 52 | Figure 5.10 DB → DBi |
| | | 53 | Table 5.30 is revised. |
| | | 58 | Figure 5.11 is partly revised. |
| | | 61 | Figure 5.12 Timing Diagram (1) XIN input is added. |
| | | 64-65 | Figure 5.15 to 5.16 Read timing DB → DBi |
| | | 66-67 | Figure 5.17 to 5.18 Write timing DB → DBi |
| | | 69 | Figure 5.20 DB → DBi |
| | | 70-85 | Electrical Characteristics (M16C/62PT) is added. |
| 2.10 | Nov 07, 2003 | 8-9 | Table 1.5 to 1.7 Product List is partly revised. Note 1 is deleted. |
| | | 23 | Table 3.1 is revised. |
| | | 71 | Table 5.50 is revised. |
| | | 72 | Table 5.51 is deleted. |
| 2.11 | Jan 06, 2004 | 16 | Table 1.9 NOTE 3 VCC1 VCC2 → VCC1 > VCC2 |
| | | 17-18 | Table 1.10 to 1.11 NOTE 1 VCC1 VCC2 → VCC1 > VCC2 |
| | | 31 | Table 5.2 Power Supply Ripple Allowable Frequency Unit MHz → kHz |
| 2.30 | Sep 01, 2004 | 12 | Table 1.9 and Figure 1.5 are added. |
| | | 18, 20 | Table 1.11 to 1.13 are revised. |
| | | 19,21 | Table 1.12 to 1.14 are revised. |
| | | 24 | Figure 3.1 is partly revised. |
| | | | Note 3 is added. |
| | | 25 | Note 6 is added. |
| | | 33 | Table 5.3 is revised. |
| | | | Note 2 in Table 5.4 is added. |
| | | 34 | Table 5.5 to 5.6 is partly revised. |
| | | 35 | Table 5.8 is revised. |
| | | | Table 5.9 is revised. |
| | | 37 | Table 5.11 is revised. |