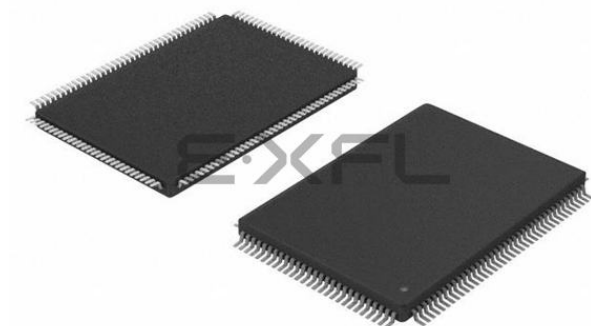


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Details

Product Status	Not For New Designs
Core Processor	M16C/60
Core Size	16-Bit
Speed	24MHz
Connectivity	I ² C, IEBus, UART/USART
Peripherals	DMA, WDT
Number of I/O	111
Program Memory Size	384KB (384K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	31K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 26x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	128-LQFP
Supplier Device Package	128-LFQFP (14x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/m30627fhpgp-u7c

Table 1.3 Performance Outline of M16C/62P Group (M16C/62P, M16C/62PT)(80-pin version)

	Item	Performance	
		M16C/62P	M16C/62PT ⁽⁴⁾
CPU	Number of Basic Instructions	91 instructions	
	Minimum Instruction Execution Time	41.7ns(f(BCLK)=24MHz, VCC1=3.3 to 5.5V) 100ns(f(BCLK)=10MHz, VCC1=2.7 to 5.5V)	41.7ns(f(BCLK)=24MHz, VCC1=4.0 to 5.5V)
	Operating Mode	Single-chip mode	
	Address Space	1 Mbyte	
	Memory Capacity	See Table 1.4 to 1.7 Product List	
Peripheral Function	Port	Input/Output : 70 pins, Input : 1 pin	
	Multifunction Timer	Timer A : 16 bits x 5 channels (Timer A1 and A2 are internal timer), Timer B : 16 bits x 6 channels (Timer B1 is internal timer)	
	Serial Interface	2 channels Clock synchronous, UART, I ² C bus ⁽¹⁾ , IEBus ⁽²⁾ 1 channel Clock synchronous, I ² C bus ⁽¹⁾ , IEBus ⁽²⁾ 2 channels Clock synchronous (1 channel is only transmission)	
	A/D Converter	10-bit A/D converter: 1 circuit, 26 channels	
	D/A Converter	8 bits x 2 channels	
	DMAC	2 channels	
	CRC Calculation Circuit	CCITT-CRC	
	Watchdog Timer	15 bits x 1 channel (with prescaler)	
	Interrupt	Internal: 29 sources, External: 5 sources, Software: 4 sources, Priority level: 7 levels	
	Clock Generation Circuit	4 circuits Main clock generation circuit (*), Subclock generation circuit (*), On-chip oscillator, PLL synthesizer (*)Equipped with a built-in feedback resistor.	
	Oscillation Stop Detection Function	Stop detection of main clock oscillation, re-oscillation detection function	
	Voltage Detection Circuit	Available (option ⁽⁴⁾)	Absent
Electric Characteristics	Supply Voltage	VCC1=3.0 to 5.5 V, (f(BCLK)=24MHz) VCC1=2.7 to 5.5 V, (f(BCLK)=10MHz)	VCC1=4.0 to 5.5V, (f(BCLK)=24MHz)
	Power Consumption	14 mA (VCC1=5V, f(BCLK)=24MHz) 8 mA (VCC1=3V, f(BCLK)=10MHz) 1.8μA (VCC1=3V, f(XCIN)=32kHz, wait mode) 0.7μA (VCC1=3V, stop mode)	14 mA (VCC1=5V, f(BCLK)=24MHz) 2.0μA (VCC1=5V, f(XCIN)=32kHz, wait mode) 0.8μA (VCC1=5V, stop mode)
Flash memory version	Program/Erase Supply Voltage	3.3 ± 0.3V or 5.0 ± 0.5V	5.0 ± 0.5V
	Program and Erase Endurance	100 times (all area) or 1,000 times (user ROM area without block A and block 1) / 10,000 times (block A, block 1) ⁽³⁾	
Operating Ambient Temperature		-20 to 85°C, -40 to 85°C ⁽³⁾	T version : -40 to 85°C V version : -40 to 125°C
Package		80-pin plastic mold QFP	

NOTES:

- I²C bus is a registered trademark of Koninklijke Philips Electronics N. V.
- IEBus is a registered trademark of NEC Electronics Corporation.
- See **Table 1.8 and 1.9 Product Code** for the program and erase endurance, and operating ambient temperature.
In addition 1,000 times/10,000 times are under development as of Jul., 2005. Please inquire about a release schedule.
- All options are on request basis.

1.4 Product List

Table 1.4 to 1.7 list the product list, Figure 1.3 shows the Type No., Memory Size, and Package, Table 1.8 lists the Product Code of Flash Memory version and ROMless version for M16C/62P, and Table 1.9 lists the Product Code of Flash Memory version for M16C/62PT. Figure 1.4 shows the Marking Diagram of Flash Memory version and ROM-less version for M16C/62P (Top View), and Figure 1.5 shows the Marking Diagram of Flash Memory version for M16C/62PT (Top View) at the time of ROM order.

Table 1.4 Product List (1) (M16C/62P)

As of Dec. 2005

Type No.	ROM Capacity	RAM Capacity	Package Type ⁽¹⁾	Remarks
M30622M6P-XXXFP	48 Kbytes	4 Kbytes	PRQP0100JB-A	Mask ROM version
M30622M6P-XXXGP			PLQP0100KB-A	
M30622M8P-XXXFP	64 Kbytes	4 Kbytes	PRQP0100JB-A	
M30622M8P-XXXGP			PLQP0100KB-A	
M30623M8P-XXXGP			PRQP0080JA-A	
M30622MAP-XXXFP	96 Kbytes	5 Kbytes	PRQP0100JB-A	
M30622MAP-XXXGP			PLQP0100KB-A	
M30623MAP-XXXGP			PRQP0080JA-A	
M30620MCP-XXXFP	128 Kbytes	10 Kbytes	PRQP0100JB-A	
M30620MCP-XXXGP			PLQP0100KB-A	
M30621MCP-XXXGP			PRQP0080JA-A	
M30622MEP-XXXFP	192 Kbytes	12 Kbytes	PRQP0100JB-A	
M30622MEP-XXXGP			PLQP0100KB-A	
M30623MEP-XXXGP			PLQP0128KB-A	
M30622MGP-XXXFP	256 Kbytes	12 Kbytes	PRQP0100JB-A	
M30622MGP-XXXGP			PLQP0100KB-A	
M30623MGP-XXXGP			PLQP0128KB-A	
M30624MGP-XXXFP		20 Kbytes	PRQP0100JB-A	
M30624MGP-XXXGP			PLQP0100KB-A	
M30625MGP-XXXGP			PLQP0128KB-A	
M30622MWP-XXXFP			PRQP0100JB-A	
M30622MWP-XXXGP	320 Kbytes	16 Kbytes	PLQP0100KB-A	
M30623MWP-XXXGP			PLQP0128KB-A	
M30624MWP-XXXFP		24 Kbytes	PRQP0100JB-A	
M30624MWP-XXXGP			PLQP0100KB-A	
M30625MWP-XXXGP			PLQP0128KB-A	
M30626MWP-XXXFP		31 Kbytes	PRQP0100JB-A	
M30626MWP-XXXGP			PLQP0100KB-A	
M30627MWP-XXXGP			PLQP0128KB-A	

(D): Under development

NOTES:

- The old package type numbers of each package type are as follows.

PLQP0128KB-A : 128P6Q-A,
 PRQP0100JB-A : 100P6S-A,
 PLQP0100KB-A : 100P6Q-A,
 PRQP0080JA-A : 80P6S-A

Table 1.8 Product Code of Flash Memory version and ROMless version for M16C/62P

	Product Code	Package	Internal ROM (User ROM Area Without Block A, Block 1)		Internal ROM (Block A, Block 1)		Operating Ambient Temperature
			Program and Erase Endurance	Temperature Range	Program and Erase Endurance	Temperature Range	
Flash memory Version	D3	Lead-included	100	0°C to 60°C	100	0°C to 60°C	-40°C to 85°C
	D5						-20°C to 85°C
	D7		1,000		10,000	-40°C to 85°C	-40°C to 85°C
	D9					-20°C to 85°C	-20°C to 85°C
	U3	Lead-free	100		100	0°C to 60°C	-40°C to 85°C
	U5					-20°C to 85°C	
	U7		1,000		10,000	-40°C to 85°C	-40°C to 85°C
	U9					-20°C to 85°C	-20°C to 85°C
ROM-less version	D3	Lead-included	—	—	—	—	-40°C to 85°C
	D5		—	—	—	—	-20°C to 85°C
	U3	Lead-free	—	—	—	—	-40°C to 85°C
	U5		—	—	—	—	-20°C to 85°C

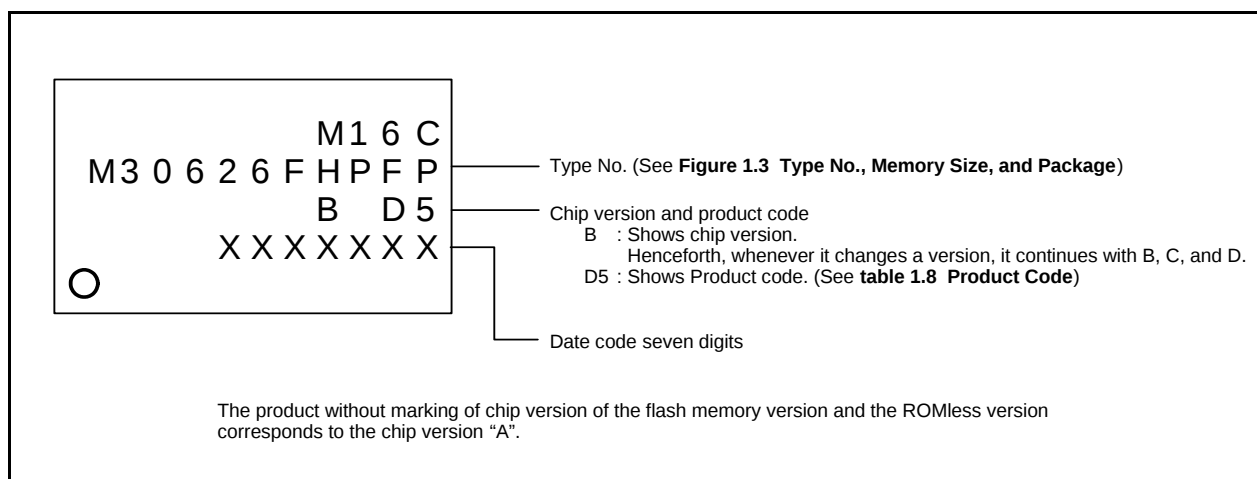
**Figure 1.4 Marking Diagram of Flash Memory version and ROM-less version for M16C/62P (Top View)**

Table 1.19 Pin Description (100-pin and 128-pin Version) (3)

Signal Name	Pin Name	I/O Type	Power Supply ⁽¹⁾	Description
Reference voltage input	VREF	I	VCC1	Applies the reference voltage for the A/D converter and D/A converter.
A/D converter	AN0 to AN7, AN0_0 to AN0_7, AN2_0 to AN2_7	I	VCC1	Analog input pins for the A/D converter.
	ADTRG	I	VCC1	This is an A/D trigger input pin.
	ANEX0	I/O	VCC1	This is the extended analog input pin for the A/D converter, and is the output in external op-amp connection mode.
	ANEX1	I	VCC1	This is the extended analog input pin for the A/D converter.
D/A converter	DA0, DA1	O	VCC1	This is the output pin for the D/A converter.
I/O port	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P12_0 to P12_7 (2), P13_0 to P13_7 (2)	I/O	VCC2	8-bit I/O ports in CMOS, having a direction register to select an input or output. Each pin is set as an input port or output port. An input port can be set for a pull-up or for no pull-up in 4-bit unit by program.
	P6_0 to P6_7, P7_0 to P7_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7 (2)	I/O	VCC1	8-bit I/O ports having equivalent functions to P0. (however, output of P7_0 and P7_1 for the N-channel open drain output.)
	P8_0 to P8_4, P8_6, P8_7, P14_0, P14_1(2)	I/O	VCC1	I/O ports having equivalent functions to P0.
Input port	P8_5	I	VCC1	Input pin for the $\overline{\text{NMI}}$ interrupt. Pin states can be read by the P8_5 bit in the P8 register.

I : Input O : Output I/O : Input and output

NOTES:

1. When use VCC1 > VCC2, contacts due to some points or restrictions to be checked.
2. Ports P11 to P14 in M16C/62P (100-pin version) and M16C/62PT (100-pin version) cannot be used.

5. Electrical Characteristics

5.1 Electrical Characteristics (M16C/62P)

Table 5.1 Absolute Maximum Ratings

Symbol	Parameter		Condition	Rated Value	Unit
V _{CC1} , V _{CC2}	Supply Voltage		V _{CC1} =AV _{CC}	−0.3 to 6.5	V
V _{CC2}	Supply Voltage		V _{CC2}	−0.3 to V _{CC1} +0.1	V
AV _{CC}	Analog Supply Voltage		V _{CC1} =AV _{CC}	−0.3 to 6.5	V
V _I	Input Voltage	RESET, CNVSS, BYTE, P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P14_0, P14_1, VREF, XIN		−0.3 to V _{CC1} +0.3 ⁽¹⁾	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P12_0 to P12_7, P13_0 to P13_7		−0.3 to V _{CC2} +0.3 ⁽¹⁾	V
		P7_0, P7_1		−0.3 to 6.5	V
V _O	Output Voltage	P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P14_0, P14_1, XOUT		−0.3 to V _{CC1} +0.3 ⁽¹⁾	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P12_0 to P12_7, P13_0 to P13_7		−0.3 to V _{CC2} +0.3 ⁽¹⁾	V
		P7_0, P7_1		−0.3 to 6.5	V
P _d	Power Dissipation		−40°C<T _{opr} ≤85°C	300	mW
T _{opr}	Operating Ambient Temperature	When the Microcomputer is Operating		−20 to 85 / −40 to 85	°C
		Flash Program Erase		0 to 60	
T _{stg}	Storage Temperature			−65 to 150	°C

NOTES:

1. There is no external connections for port P1_0 to P1_7, P4_4 to P4_7, P7_2 to P7_5 and P9_1 in 80-pin version.

Table 5.2 Recommended Operating Conditions (1) (1)

Symbol	Parameter		Standard			Unit
			Min.	Typ.	Max.	
V _{CC1} , V _{CC2}	Supply Voltage (V _{CC1} ≥ V _{CC2})		2.7	5.0	5.5	V
AV _{CC}	Analog Supply Voltage			V _{CC1}		V
V _{SS}	Supply Voltage			0		V
AV _{SS}	Analog Supply Voltage			0		V
V _{IH}	HIGH Input Voltage	P3_1 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P12_0 to P12_7, P13_0 to P13_7	0.8V _{CC2}		V _{CC2}	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 (during single-chip mode)	0.8V _{CC2}		V _{CC2}	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 (data input during memory expansion and microprocessor mode)	0.5V _{CC2}		V _{CC2}	V
		P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P14_0, P14_1, XIN, RESET, CNVSS, BYTE	0.8V _{CC1}		V _{CC1}	V
		P7_0, P7_1	0.8V _{CC1}		6.5	V
V _{IL}	LOW Input Voltage	P3_1 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P12_0 to P12_7, P13_0 to P13_7	0		0.2V _{CC2}	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 (during single-chip mode)	0		0.2V _{CC2}	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 (data input during memory expansion and microprocessor mode)	0		0.16V _{CC2}	V
		P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P14_0, P14_1, XIN, RESET, CNVSS, BYTE	0		0.2V _{CC}	V
I _{OH(peak)}	HIGH Peak Output Current	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1			-10.0	mA
I _{OH(avg)}	HIGH Average Output Current	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1			-5.0	mA
I _{OL(peak)}	LOW Peak Output Current	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1			10.0	mA
I _{OL(avg)}	LOW Average Output Current	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1			5.0	mA

NOTES:

1. Referenced to V_{CC1} = V_{CC2} = 2.7 to 5.5V at T_{opr} = -20 to 85°C / -40 to 85°C unless otherwise specified.
2. The Average Output Current is the mean value within 100ms.
3. The total I_{OL(peak)} for ports P0, P1, P2, P8_6, P8_7, P9, P10, P11, P14_0, and P14_1 must be 80mA max. The total I_{OL(peak)} for ports P3, P4, P5, P6, P7, P8_0 to P8_4, P12, and P13 must be 80mA max. The total I_{OH(peak)} for ports P0, P1, and P2 must be -40mA max. The total I_{OH(peak)} for ports P3, P4, P5, P12, and P13 must be -40mA max. The total I_{OH(peak)} for ports P6, P7, and P8_0 to P8_4 must be -40mA max. The total I_{OH(peak)} for ports P8_6, P8_7, P9, P10, P14_0, and P14_1 must be -40mA max. Set Average Output Current to 1/2 of peak. The total I_{OH(peak)} for ports P8_6, P8_7, P9, P10, P11, P14_0, and P14_1 must be -40mA max.
As for 80-pin version, the total I_{OL(peak)} for all ports and I_{OH(peak)} must be 80mA. max. due to one V_{CC} and one V_{SS}.
4. There is no external connections for port P1_0 to P1_7, P4_4 to P4_7, P7_2 to P7_5 and P9_1 in 80-pin version.

Table 5.5 D/A Conversion Characteristics ⁽¹⁾

Symbol	Parameter	Measuring Condition	Standard			Unit
			Min.	Typ.	Max.	
–	Resolution				8	Bits
–	Absolute Accuracy				1.0	%
t _{su}	Setup Time				3	μs
R _o	Output Resistance		4	10	20	kΩ
I _{VREF}	Reference Power Supply Input Current	(NOTE 2)			1.5	mA

NOTES:

1. Referenced to V_{CC1}=V_{REF}=3.3 to 5.5V, V_{SS}=AV_{SS}=0V at T_{opr} = –20 to 85°C / –40 to 85°C unless otherwise specified.
2. This applies when using one D/A converter, with the D/A register for the unused D/A converter set to “00h”. The resistor ladder of the A/D converter is not included. Also, when D/A register contents are not “00h”, the I_{VREF} will flow even if V_{ref} is disconnected by the A/D control register.

$$V_{CC1}=V_{CC2}=5V$$

Switching Characteristics(V_{CC1} = V_{CC2} = 5V, V_{SS} = 0V, at T_{opr} = –20 to 85°C / –40 to 85°C unless otherwise specified)**Table 5.27 Memory Expansion and Microprocessor Modes (for setting with no wait)**

Symbol	Parameter		Standard		Unit
			Min.	Max.	
t _d (BCLK-AD)	Address Output Delay Time	See Figure 5.2		25	ns
t _h (BCLK-AD)	Address Output Hold Time (in relation to BCLK)		4		ns
t _h (RD-AD)	Address Output Hold Time (in relation to RD)		0		ns
t _h (WR-AD)	Address Output Hold Time (in relation to WR)		(NOTE 2)		ns
t _d (BCLK-CS)	Chip Select Output Delay Time			25	ns
t _h (BCLK-CS)	Chip Select Output Hold Time (in relation to BCLK)		4		ns
t _d (BCLK-ALE)	ALE Signal Output Delay Time			15	ns
t _h (BCLK-ALE)	ALE Signal Output Hold Time		–4		ns
t _d (BCLK-RD)	RD Signal Output Delay Time			25	ns
t _h (BCLK-RD)	RD Signal Output Hold Time		0		ns
t _d (BCLK-WR)	WR Signal Output Delay Time			25	ns
t _h (BCLK-WR)	WR Signal Output Hold Time		0		ns
t _d (BCLK-DB)	Data Output Delay Time (in relation to BCLK)			40	ns
t _h (BCLK-DB)	Data Output Hold Time (in relation to BCLK) ⁽³⁾		4		ns
t _d (DB-WR)	Data Output Delay Time (in relation to WR)		(NOTE 1)		ns
t _h (WR-DB)	Data Output Hold Time (in relation to WR) ⁽³⁾		(NOTE 2)		ns
t _d (BCLK-HLDA)	HLDA Output Delay Time			40	ns

NOTES:

1. Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f(\text{BCLK})} - 40 [\text{ns}] \quad f(\text{BCLK}) \text{ is } 12.5\text{MHz or less.}$$

2. Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f(\text{BCLK})} - 10 [\text{ns}]$$

3. This standard value shows the timing when the output is off, and does not show hold time of data bus.

Hold time of data bus varies with capacitor volume and pull-up (pull-down) resistance value.

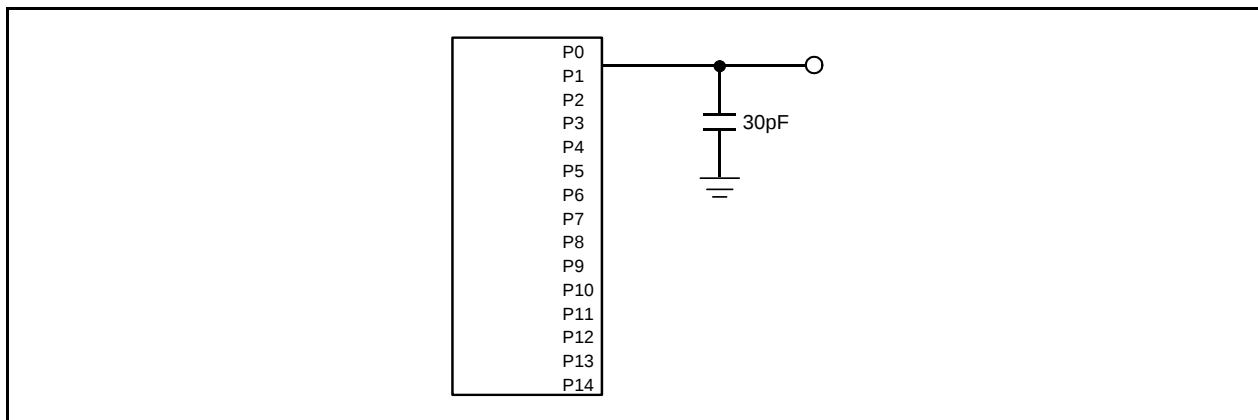
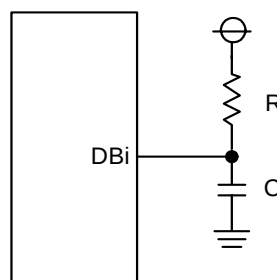
Hold time of data bus is expressed in

$$t = -CR \times \ln(1 - V_{OL} / V_{CC2})$$

by a circuit of the right figure.

For example, when V_{OL} = 0.2V_{CC2}, C = 30pF, R = 1kΩ, hold time of output "L" level is

$$t = -30\text{pF} \times 1\text{k}\Omega \times \ln(1 - 0.2V_{CC2} / V_{CC2}) = 6.7\text{ns.}$$

**Figure 5.2 Ports P0 to P14 Measurement Circuit**

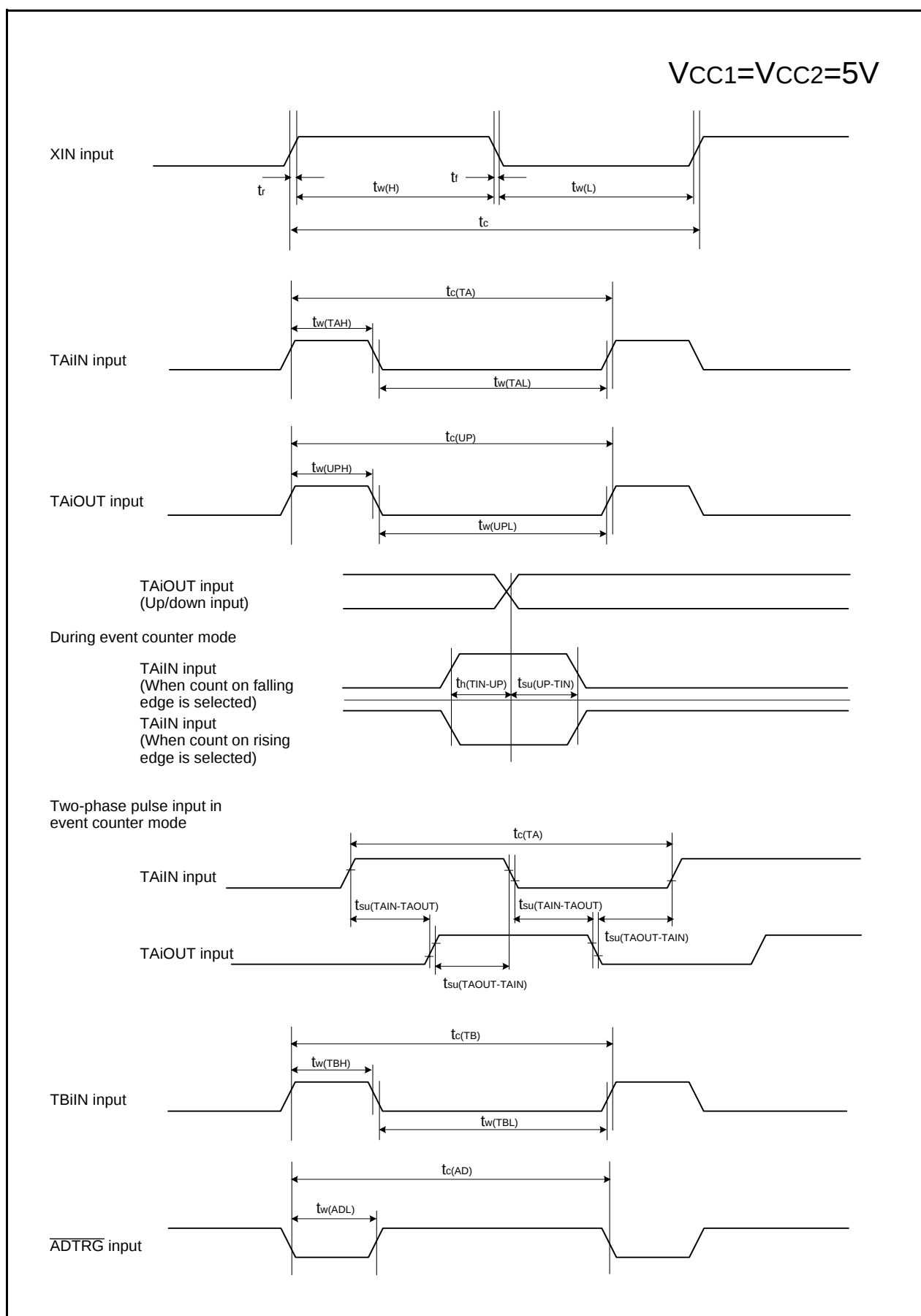


Figure 5.3 Timing Diagram (1)

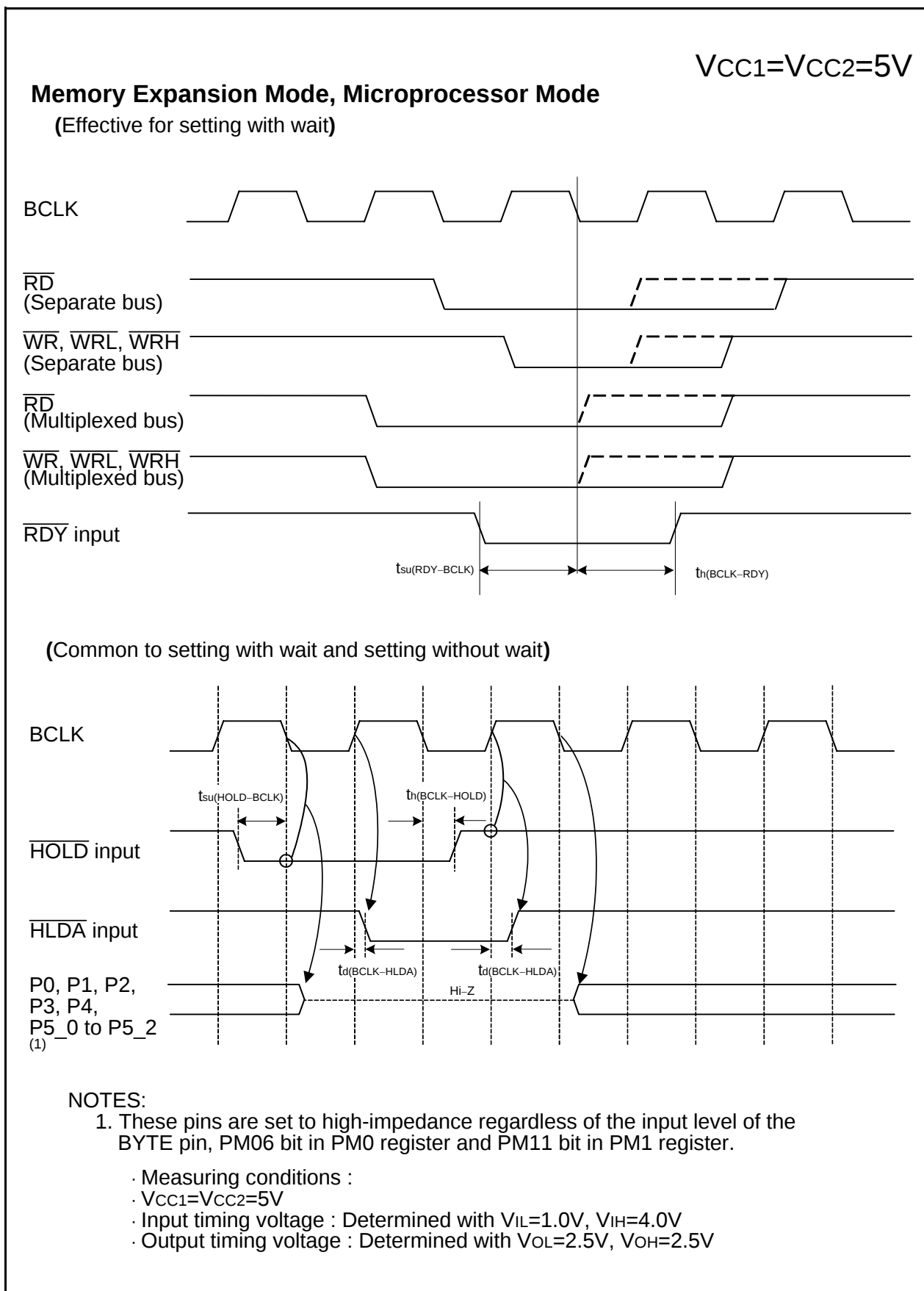


Figure 5.5 Timing Diagram (3)

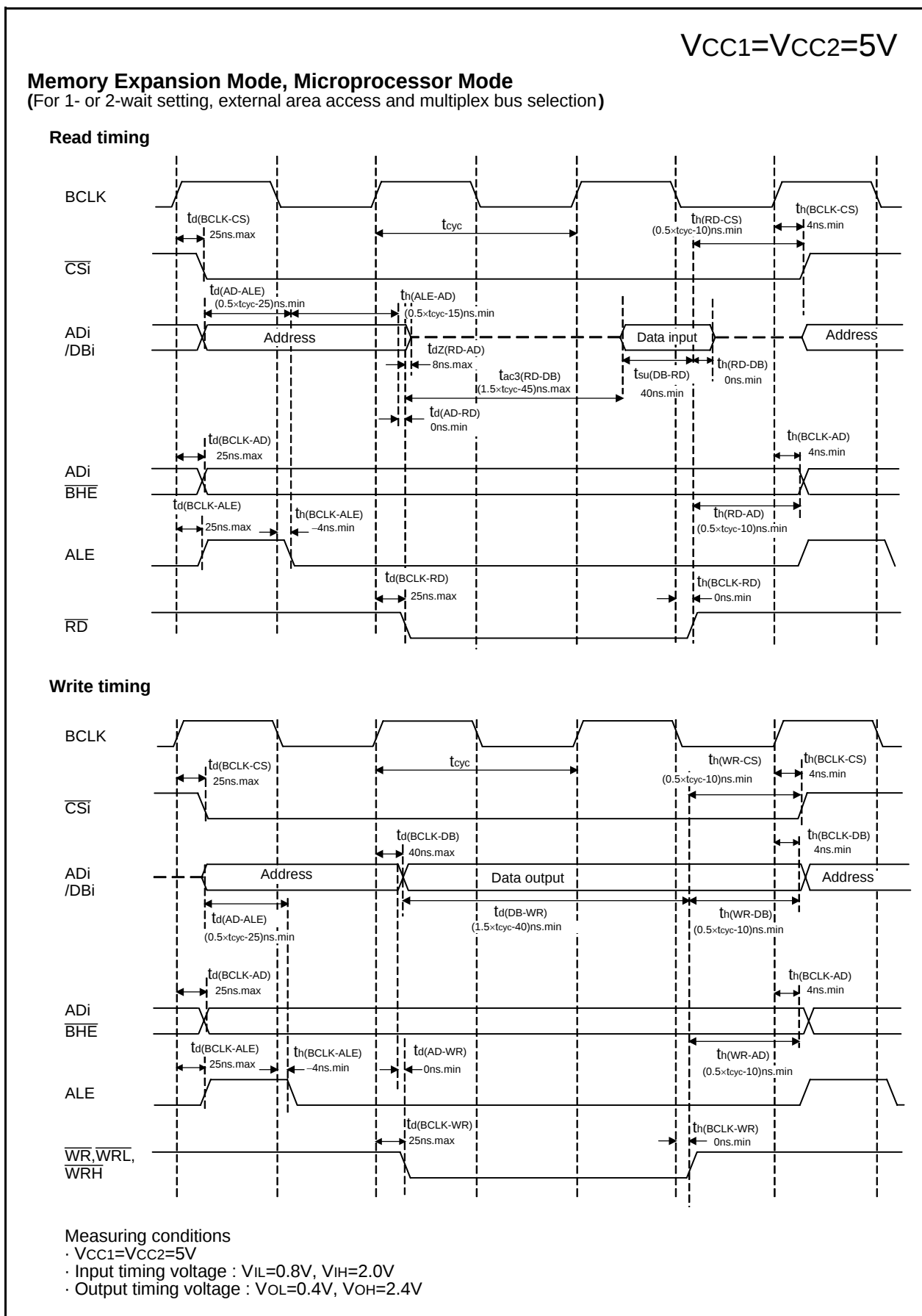


Figure 5.10 Timing Diagram (8)

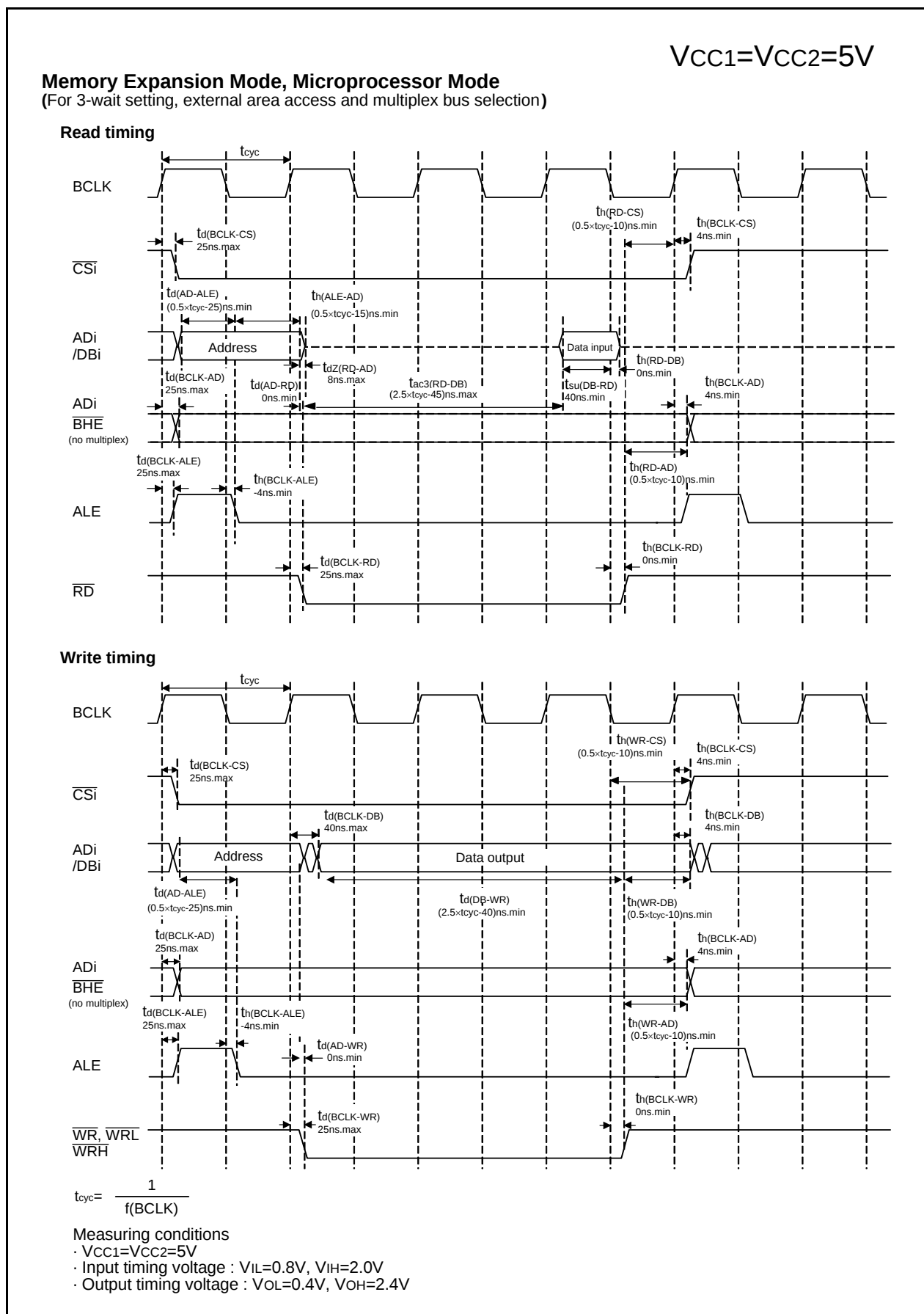


Figure 5.11 Timing Diagram (9)

Table 5.31 Electrical Characteristics (2) ⁽¹⁾

Symbol	Parameter		Measuring Condition		Standard			Unit
					Min.	Typ.	Max.	
Icc	Power Supply Current (Vcc1=Vcc2=2.7V to 3.6V)	In single-chip mode, the output pins are open and other pins are Vss	Mask ROM	f(BCLK)=10MHz No division		8	11	mA
				No division, On-chip oscillation		1		mA
			Flash Memory	f(BCLK)=10MHz, No division		8	13	mA
				No division, On-chip oscillation		1.8		mA
			Flash Memory Program	f(BCLK)=10MHz, VCC1=3.0V		12		mA
			Flash Memory Erase	f(BCLK)=10MHz, VCC1=3.0V		22		mA
			Mask ROM	f(XCIN)=32kHz Low power dissipation mode, ROM ⁽³⁾		25		μA
			Flash Memory	f(BCLK)=32kHz Low power dissipation mode, RAM ⁽³⁾		25		μA
				f(BCLK)=32kHz Low power dissipation mode, Flash Memory ⁽³⁾		420		μA
				On-chip oscillation, Wait mode		45		μA
				Mask ROM Flash Memory	f(BCLK)=32kHz Wait mode ⁽²⁾ , Oscillation capability High		6.0	
			f(BCLK)=32kHz Wait mode ⁽²⁾ , Oscillation capability Low			1.8		μA
			Stop mode Topr =25°C			0.7	3.0	μA
Idet4	Low Voltage Detection Dissipation Current ⁽⁴⁾					0.6	4	μA
Idet3	Reset Area Detection Dissipation Current ⁽⁴⁾					0.4	2	μA

NOTES:

1. Referenced to V_{CC1}=V_{CC2}=2.7 to 3.3V, V_{SS} = 0V at T_{opr} = -20 to 85°C / -40 to 85°C, f(BCLK)=10MHz unless otherwise specified.
2. With one timer operated using fC32.
3. This indicates the memory in which the program to be executed exists.
4. I_{det} is dissipation current when the following bit is set to "1" (detection circuit enabled).
I_{det4}: VC27 bit in the VCR2 register
I_{det3}: VC26 bit in the VCR2 register

$$V_{CC1}=V_{CC2}=3V$$

Timing Requirements(V_{CC1} = V_{CC2} = 3V, V_{SS} = 0V, at T_{opr} = –20 to 85°C / –40 to 85°C unless otherwise specified)**Table 5.40 Timer B Input (Counter Input in Event Counter Mode)**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
t _c (TB)	TBiIN Input Cycle Time (counted on one edge)	150		ns
t _w (TBH)	TBiIN Input HIGH Pulse Width (counted on one edge)	60		ns
t _w (TBL)	TBiIN Input LOW Pulse Width (counted on one edge)	60		ns
t _c (TB)	TBiIN Input Cycle Time (counted on both edges)	300		ns
t _w (TBH)	TBiIN Input HIGH Pulse Width (counted on both edges)	120		ns
t _w (TBL)	TBiIN Input LOW Pulse Width (counted on both edges)	120		ns

Table 5.41 Timer B Input (Pulse Period Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
t _c (TB)	TBiIN Input Cycle Time	600		ns
t _w (TBH)	TBiIN Input HIGH Pulse Width	300		ns
t _w (TBL)	TBiIN Input LOW Pulse Width	300		ns

Table 5.42 Timer B Input (Pulse Width Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
t _c (TB)	TBiIN Input Cycle Time	600		ns
t _w (TBH)	TBiIN Input HIGH Pulse Width	300		ns
t _w (TBL)	TBiIN Input LOW Pulse Width	300		ns

Table 5.43 A/D Trigger Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
t _c (AD)	ADTRG $\overline{\text{Input}}$ Cycle Time	1500		ns
t _w (ADL)	ADTRG $\overline{\text{Input}}$ LOW Pulse Width	200		ns

Table 5.44 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
t _c (CK)	CLKi Input Cycle Time	300		ns
t _w (CKH)	CLKi Input HIGH Pulse Width	150		ns
t _w (CKL)	CLKi Input LOW Pulse Width	150		ns
t _d (C-Q)	TXDi Output Delay Time		160	ns
t _h (C-Q)	TXDi Hold Time	0		ns
t _{su} (D-C)	RXDi Input Setup Time	100		ns
t _h (C-D)	RXDi Input Hold Time	90		ns

Table 5.45 External Interrupt INTi Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
t _w (INH)	INTi Input HIGH Pulse Width	380		ns
t _w (INL)	INTi Input LOW Pulse Width	380		ns

$$V_{CC1}=V_{CC2}=3V$$

Switching Characteristics

($V_{CC1} = V_{CC2} = 3V$, $V_{SS} = 0V$, at $T_{opr} = -20$ to $85^{\circ}C$ / -40 to $85^{\circ}C$ unless otherwise specified)

Table 5.46 Memory Expansion and Microprocessor Modes (for setting with no wait)

Symbol	Parameter		Standard		Unit
			Min.	Max.	
$t_d(BCLK-AD)$	Address Output Delay Time	See Figure 5.12		30	ns
$t_h(BCLK-AD)$	Address Output Hold Time (in relation to BCLK)		4		ns
$t_h(RD-AD)$	Address Output Hold Time (in relation to RD)		0		ns
$t_h(WR-AD)$	Address Output Hold Time (in relation to WR)		(NOTE 2)		ns
$t_d(BCLK-CS)$	Chip Select Output Delay Time			30	ns
$t_h(BCLK-CS)$	Chip Select Output Hold Time (in relation to BCLK)		4		ns
$t_d(BCLK-ALE)$	ALE Signal Output Delay Time			25	ns
$t_h(BCLK-ALE)$	ALE Signal Output Hold Time		-4		ns
$t_d(BCLK-RD)$	RD Signal Output Delay Time			30	ns
$t_h(BCLK-RD)$	RD Signal Output Hold Time		0		ns
$t_d(BCLK-WR)$	WR Signal Output Delay Time			30	ns
$t_h(BCLK-WR)$	WR Signal Output Hold Time		0		ns
$t_d(BCLK-DB)$	Data Output Delay Time (in relation to BCLK)			40	ns
$t_h(BCLK-DB)$	Data Output Hold Time (in relation to BCLK) ⁽³⁾		4		ns
$t_d(DB-WR)$	Data Output Delay Time (in relation to WR)		(NOTE 1)		ns
$t_h(WR-DB)$	Data Output Hold Time (in relation to WR) ⁽³⁾		(NOTE 2)		ns
$t_d(BCLK-HLDA)$	HLDA Output Delay Time			40	ns

NOTES:

1. Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f(BCLK)} - 40 [ns] \quad f(BCLK) \text{ is } 12.5MHz \text{ or less.}$$

2. Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f(BCLK)} - 10 [ns]$$

3. This standard value shows the timing when the output is off, and does not show hold time of data bus.

Hold time of data bus varies with capacitor volume and pull-up (pull-down) resistance value.

Hold time of data bus is expressed in

$$t = -CR \times \ln(1 - V_{OL} / V_{CC2})$$

by a circuit of the right figure.

For example, when $V_{OL} = 0.2V_{CC2}$, $C = 30pF$, $R = 1k\Omega$, hold time of output "L" level is

$$t = -30pF \times 1k\Omega \times \ln(1 - 0.2V_{CC2} / V_{CC2}) \\ = 6.7ns.$$

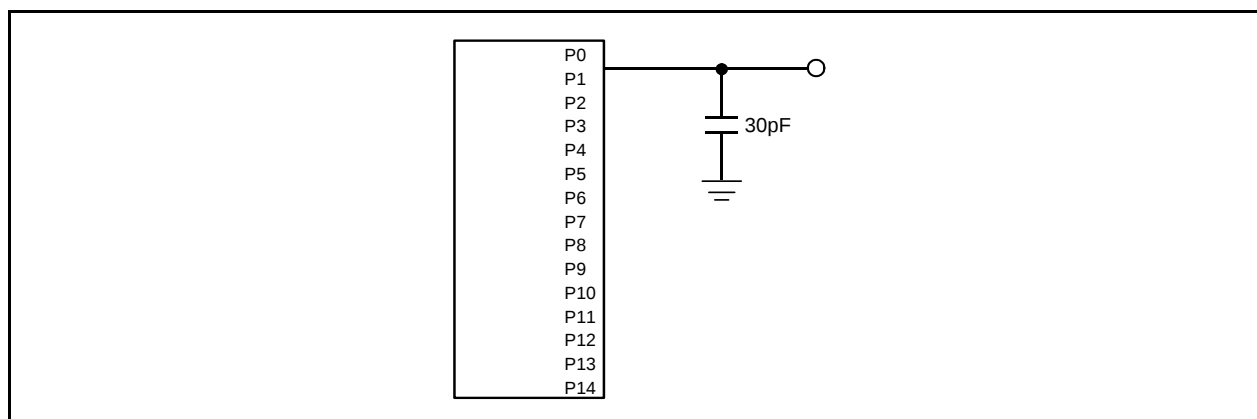
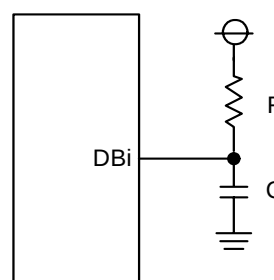
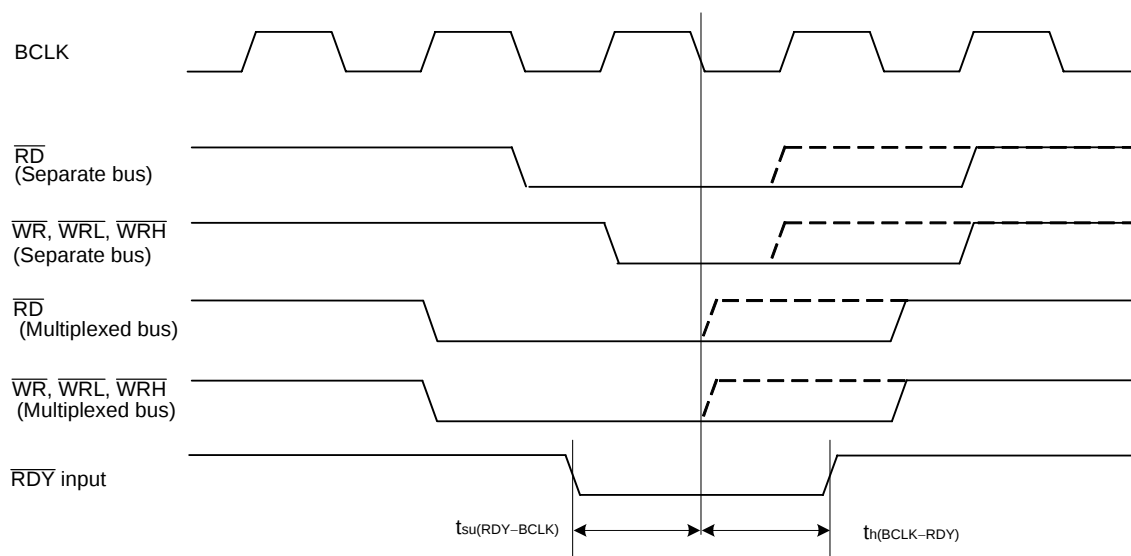


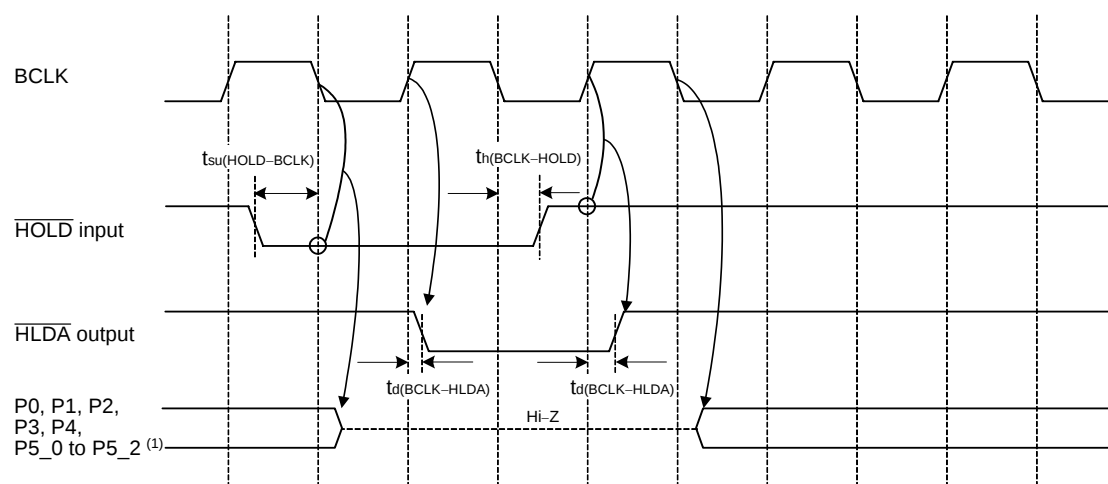
Figure 5.12 Ports P0 to P14 Measurement Circuit

Memory Expansion Mode, Microprocessor Mode

(Effective for setting with wait)

 $V_{CC1}=V_{CC2}=3V$ 

(Common to setting with wait and setting without wait)

**NOTES:**

1. These pins are set to high-impedance regardless of the input level of the BYTE pin, PM06 bit in PM0 register and PM11 bit in PM1 register.

Measuring conditions :

- $V_{CC1}=V_{CC2}=3V$
- Input timing voltage : Determined with $V_{IL}=0.6V$, $V_{IH}=2.4V$
- Output timing voltage : Determined with $V_{OL}=1.5V$, $V_{OH}=1.5V$

Figure 5.15 Timing Diagram (3)

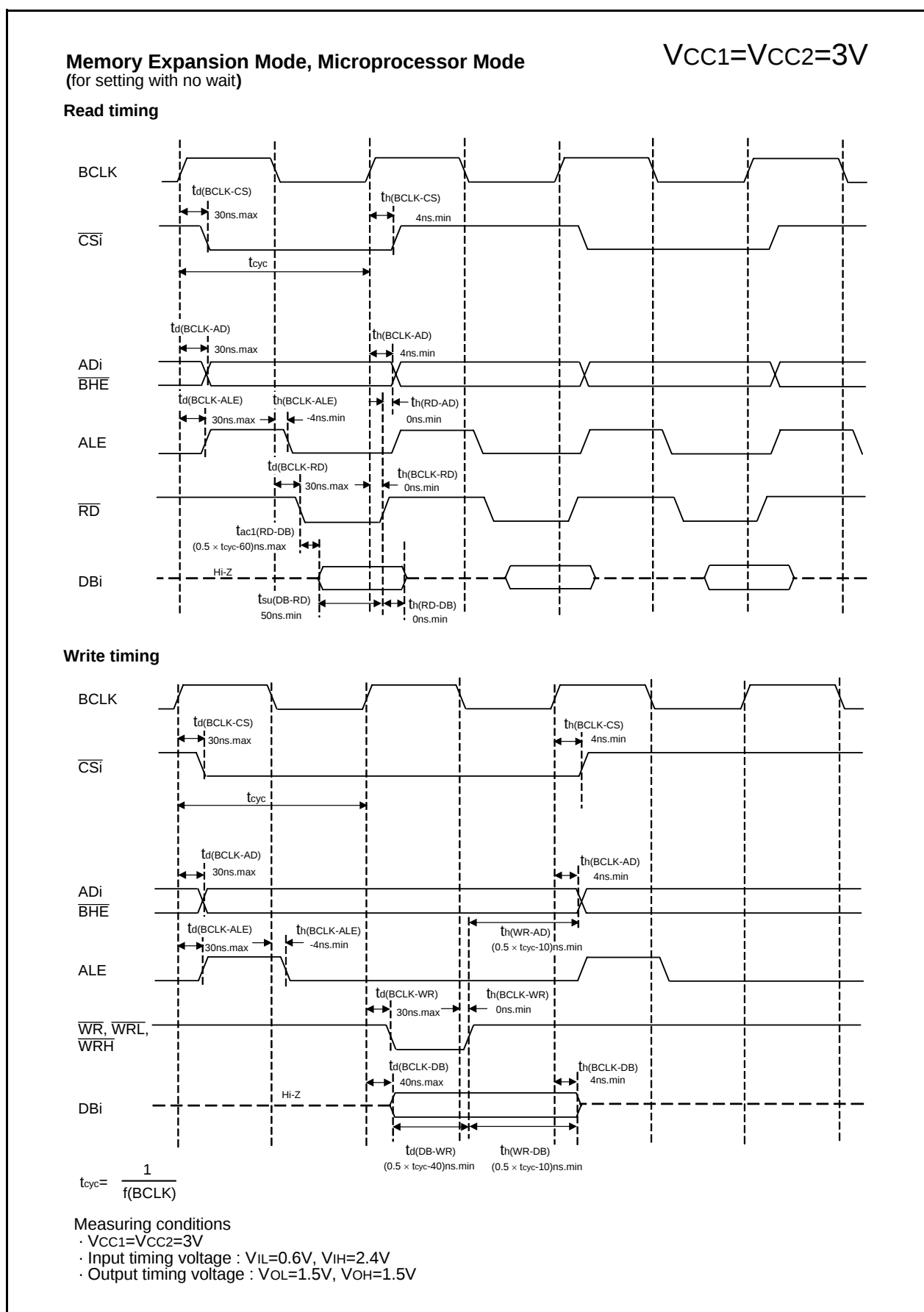


Figure 5.16 Timing Diagram (4)

Table 5.51 A/D Conversion Characteristics (1)

Symbol	Parameter		Measuring Condition	Standard			Unit
				Min.	Typ.	Max.	
–	Resolution		$V_{REF}=V_{CC1}$			10	Bits
INL	Integral Non-Linearity Error	10bit	$V_{REF}=V_{CC1}=5V$ AN0 to AN7 input, AN0_0 to AN0_7 input, AN2_0 to AN2_7 input, ANEX0, ANEX1 input			± 3	LSB
			External operation amp connection mode			± 7	LSB
		8bit	$V_{REF}=V_{CC1}=5V$			± 2	LSB
–	Absolute Accuracy	10bit	$V_{REF}=V_{CC1}=5V$ AN0 to AN7 input, AN0_0 to AN0_7 input, AN2_0 to AN2_7 input, ANEX0, ANEX1 input			± 3	LSB
			External operation amp connection mode			± 7	LSB
		8bit	$V_{REF}=V_{CC1}=5V$			± 2	LSB
–	Tolerance Level Impedance				3		$k\Omega$
DNL	Differential Non-Linearity Error					± 1	LSB
–	Offset Error					± 3	LSB
–	Gain Error					± 3	LSB
RLADDER	Ladder Resistance		$V_{REF}=V_{CC1}$	10		40	$k\Omega$
tCONV	10-bit Conversion Time, Sample & Hold Function Available		$V_{REF}=V_{CC1}=5V$, $\phi_{AD}=12MHz$	2.75			μs
tCONV	8-bit Conversion Time, Sample & Hold Function Available		$V_{REF}=V_{CC1}=5V$, $\phi_{AD}=12MHz$	2.33			μs
tSAMP	Sampling Time			0.25			μs
VREF	Reference Voltage			2.0		V_{CC1}	V
Via	Analog Input Voltage			0		V_{REF}	V

NOTES:

1. Referenced to $V_{CC1}=AV_{CC}=V_{REF}=4.0$ to $5.5V$, $V_{SS}=AV_{SS}=0V$ at $T_{opr} = -40$ to $85^{\circ}C$ / -40 to $125^{\circ}C$ unless otherwise specified.
T version = -40 to $85^{\circ}C$, V version = -40 to $125^{\circ}C$
2. ϕ_{AD} frequency must be 12 MHz or less.
3. When sample & hold is disabled, ϕ_{AD} frequency must be 250 kHz or more, in addition to the limitation in Note 2.
When sample & hold is enabled, ϕ_{AD} frequency must be 1MHz or more, in addition to the limitation in Note 2.

Table 5.52 D/A Conversion Characteristics (1)

Symbol	Parameter	Measuring Condition	Standard			Unit
			Min.	Typ.	Max.	
–	Resolution				8	Bits
–	Absolute Accuracy				1.0	%
tSU	Setup Time				3	μs
R _O	Output Resistance		4	10	20	$k\Omega$
I _{VREF}	Reference Power Supply Input Current	(NOTE 2)			1.5	mA

NOTES:

1. Referenced to $V_{CC1}=V_{REF}=4.0$ to $5.5V$, $V_{SS}=AV_{SS}=0V$ at $T_{opr} = -40$ to $85^{\circ}C$ / -40 to $125^{\circ}C$ unless otherwise specified. T version = -40 to $85^{\circ}C$, V version = -40 to $125^{\circ}C$
2. This applies when using one D/A converter, with the D/A register for the unused D/A converter set to "00h". The resistor ladder of the A/D converter is not included. Also, when D/A register contents are not "00h", the I_{VREF} will flow even if V_{ref} id disconnected by the A/D control register.

$$V_{CC1}=V_{CC2}=5V$$

Switching Characteristics

($V_{CC1} = V_{CC2} = 5V$, $V_{SS} = 0V$, at $T_{opr} = -40$ to $85^{\circ}C$ (T version) / -40 to $125^{\circ}C$ (V version) unless otherwise specified)

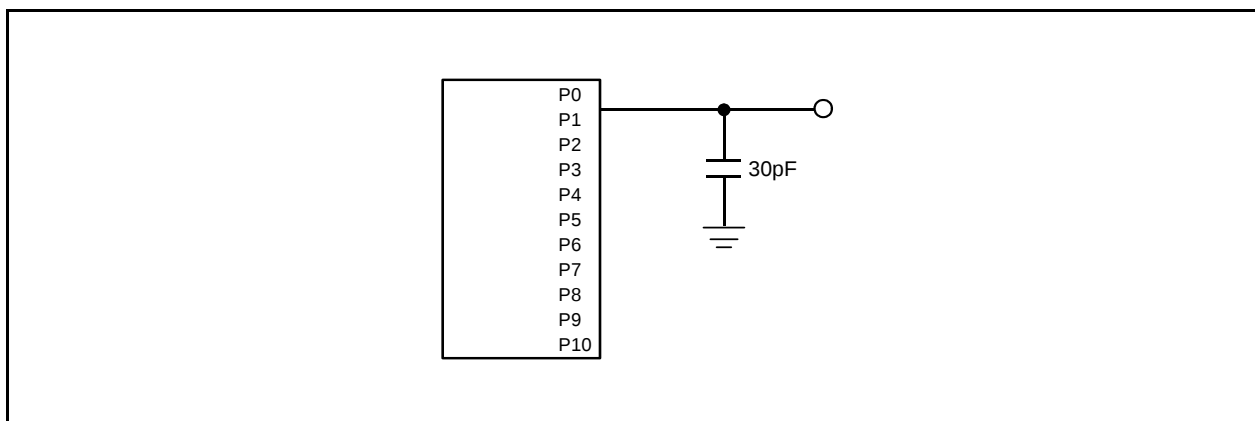


Figure 5.23 Ports P0 to P10 Measurement Circuit

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP100-14x14-0.50	PLQP0100KB-A	100P6Q-A / FP-100U / FP-100UV	0.6g

NOTE)

- DIMENSIONS *1* AND *2* DO NOT INCLUDE MOLD FLASH.
- DIMENSION *3* DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	13.9	14.0	14.1
E	13.9	14.0	14.1
A ₂	—	1.4	—
H _D	15.8	16.0	16.2
H _E	15.8	16.0	16.2
A	—	—	1.7
A ₁	0.05	0.1	0.15
b _p	0.15	0.20	0.25
b ₁	—	0.18	—
c	0.09	0.145	0.20
c ₁	—	0.125	—
θ	0°	—	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
Z _D	—	1.0	—
Z _E	—	1.0	—
L	0.35	0.5	0.65
L ₁	—	1.0	—

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-QFP80-14x14-0.65	PROQ0080JA-A	80P6S-A	1.1g

NOTE)

- DIMENSIONS *1* AND *2* DO NOT INCLUDE MOLD FLASH.
- DIMENSION *3* DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	13.8	14.0	14.2
E	13.8	14.0	14.2
A ₂	—	2.8	—
H _D	16.5	16.8	17.1
H _E	16.5	16.8	17.1
A	—	—	3.05
A ₁	0	0.1	0.2
b _p	0.25	0.3	0.4
c	0.13	0.15	0.2
θ	0°	—	10°
e	—	0.5	0.65
y	—	—	0.10
Z _D	—	0.825	—
Z _E	—	0.825	—
L	0.4	0.6	0.8