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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Not For New Designs
Core Processor	M16C/60
Core Size	16-Bit
Speed	24MHz
Connectivity	I ² C, IEBus, UART/USART
Peripherals	DMA, WDT
Number of I/O	111
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	31K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 26x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	128-LQFP
Supplier Device Package	128-LFQFP (14x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/m30627fjpgp-u3c

Table 1.11 Pin Characteristics for 128-Pin Package (2)

Pin No.	Control Pin	Port	Interrupt Pin	Timer Pin	UART Pin	Analog Pin	Bus Control Pin
51		P5_6					ALE
52		P5_5					$\overline{\text{HOLD}}$
53		P5_4					$\overline{\text{HLDA}}$
54		P13_3					
55		P13_2					
56		P13_1					
57		P13_0					
58		P5_3					BCLK
59		P5_2					$\overline{\text{RD}}$
60		P5_1					$\overline{\text{WRH/BHE}}$
61		P5_0					$\overline{\text{WRL/WR}}$
62		P12_7					
63		P12_6					
64		P12_5					
65		P4_7					$\overline{\text{CS3}}$
66		P4_6					$\overline{\text{CS2}}$
67		P4_5					$\overline{\text{CS1}}$
68		P4_4					$\overline{\text{CS0}}$
69		P4_3					A19
70		P4_2					A18
71		P4_1					A17
72		P4_0					A16
73		P3_7					A15
74		P3_6					A14
75		P3_5					A13
76		P3_4					A12
77		P3_3					A11
78		P3_2					A10
79		P3_1					A9
80		P12_4					
81		P12_3					
82		P12_2					
83		P12_1					
84		P12_0					
85	VCC2						
86		P3_0					A8(/D7)
87	VSS						
88		P2_7				AN2_7	A7(/D7/D6)
89		P2_6				AN2_6	A6(/D6/D5)
90		P2_5				AN2_5	A5(/D5/D4)
91		P2_4				AN2_4	A4(/D4/D3)
92		P2_3				AN2_3	A3(/D3/D2)
93		P2_2				AN2_2	A2(/D2/D1)
94		P2_1				AN2_1	A1(/D1/D0)
95		P2_0				AN2_0	A0(/D0/-)
96		P1_7	$\overline{\text{INT5}}$				D15
97		P1_6	$\overline{\text{INT4}}$				D14
98		P1_5	$\overline{\text{INT3}}$				D13
99		P1_4					D12
100		P1_3					D11

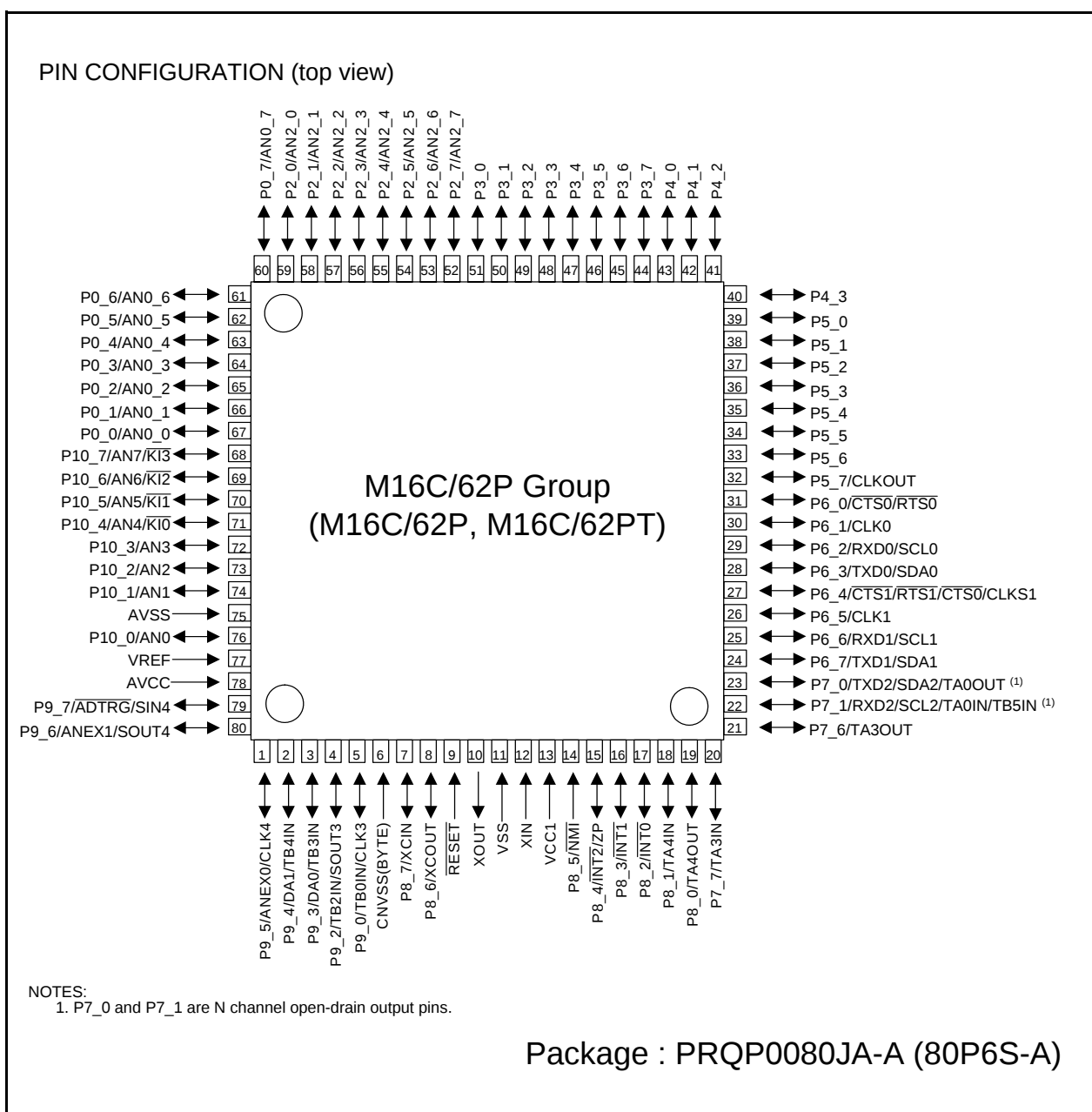


Figure 1.9 Pin Configuration (Top View)

Table 1.15 Pin Characteristics for 80-Pin Package (1)

Pin No.	Control Pin	Port	Interrupt Pin	Timer Pin	UART Pin	Analog Pin	Bus Control Pin
1		P9_5			CLK4	ANEX0	
2		P9_4		TB4IN		DA1	
3		P9_3		TB3IN		DA0	
4		P9_2		TB2IN	SOUT3		
5		P9_0		TB0IN	CLK3		
6	CNVSS (BYTE)						
7	XCIN	P8_7					
8	XCOUT	P8_6					
9	RESET						
10	XOUT						
11	VSS						
12	XIN						
13	VCC1						
14		P8_5	NMI				
15		P8_4	INT2	ZP			
16		P8_3	INT1				
17		P8_2	INT0				
18		P8_1		TA4IN			
19		P8_0		TA4OUT			
20		P7_7		TA3IN			
21		P7_6		TA3OUT			
22		P7_1		TA0IN/TB5IN	RXD2/SCL2		
23		P7_0		TA0OUT	TXD2/SDA2		
24		P6_7			TXD1/SDA1		
25		P6_6			RXD1/SCL1		
26		P6_5			CLK1		
27		P6_4			CTS1/RTS1/CTS0/CLKS1		
28		P6_3			TXD0/SDA0		
29		P6_2			RXD0/SCL0		
30		P6_1			CLK0		
31		P6_0			CTS0/RTS0		
32		P5_7					CLKOUT
33		P5_6					
34		P5_5					
35		P5_4					
36		P5_3					
37		P5_2					
38		P5_1					
39		P5_0					
40		P4_3					
41		P4_2					
42		P4_1					
43		P4_0					
44		P3_7					
45		P3_6					
46		P3_5					
47		P3_4					
48		P3_3					
49		P3_2					
50		P3_1					

Table 1.16 Pin Characteristics for 80-Pin Package (2)

Pin No.	Control Pin	Port	Interrupt Pin	Timer Pin	UART Pin	Analog Pin	Bus Control Pin
51		P3_0					
52		P2_7				AN2_7	
53		P2_6				AN2_6	
54		P2_5				AN2_5	
55		P2_4				AN2_4	
56		P2_3				AN2_3	
57		P2_2				AN2_2	
58		P2_1				AN2_1	
59		P2_0				AN2_0	
60		P0_7				AN0_7	
61		P0_6				AN0_6	
62		P0_5				AN0_5	
63		P0_4				AN0_4	
64		P0_3				AN0_3	
65		P0_2				AN0_2	
66		P0_1				AN0_1	
67		P0_0				AN0_0	
68		P10_7	KI3			AN7	
69		P10_6	KI2			AN6	
70		P10_5	KI1			AN5	
71		P10_4	KI0			AN4	
72		P10_3				AN3	
73		P10_2				AN2	
74		P10_1				AN1	
75	AVSS						
76		P10_0				AN0	
77	VREF						
78	AVCC						
79		P9_7			SIN4	ADTRG	
80		P9_6			SOUT4	ANEX1	

Table 1.19 Pin Description (100-pin and 128-pin Version) (3)

Signal Name	Pin Name	I/O Type	Power Supply ⁽¹⁾	Description
Reference voltage input	VREF	I	VCC1	Applies the reference voltage for the A/D converter and D/A converter.
A/D converter	AN0 to AN7, AN0_0 to AN0_7, AN2_0 to AN2_7	I	VCC1	Analog input pins for the A/D converter.
	ADTRG	I	VCC1	This is an A/D trigger input pin.
	ANEX0	I/O	VCC1	This is the extended analog input pin for the A/D converter, and is the output in external op-amp connection mode.
	ANEX1	I	VCC1	This is the extended analog input pin for the A/D converter.
D/A converter	DA0, DA1	O	VCC1	This is the output pin for the D/A converter.
I/O port	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P12_0 to P12_7 (2), P13_0 to P13_7 (2)	I/O	VCC2	8-bit I/O ports in CMOS, having a direction register to select an input or output. Each pin is set as an input port or output port. An input port can be set for a pull-up or for no pull-up in 4-bit unit by program.
	P6_0 to P6_7, P7_0 to P7_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7 (2)	I/O	VCC1	8-bit I/O ports having equivalent functions to P0. (however, output of P7_0 and P7_1 for the N-channel open drain output.)
	P8_0 to P8_4, P8_6, P8_7, P14_0, P14_1(2)	I/O	VCC1	I/O ports having equivalent functions to P0.
Input port	P8_5	I	VCC1	Input pin for the $\overline{\text{NMI}}$ interrupt. Pin states can be read by the P8_5 bit in the P8 register.

I : Input O : Output I/O : Input and output

NOTES:

1. When use VCC1 > VCC2, contacts due to some points or restrictions to be checked.
2. Ports P11 to P14 in M16C/62P (100-pin version) and M16C/62PT (100-pin version) cannot be used.

2. Central Processing Unit (CPU)

Figure 2.1 shows the CPU registers. The CPU has 13 registers. Of these, R0, R1, R2, R3, A0, A1 and FB comprise a register bank. There are two register banks.

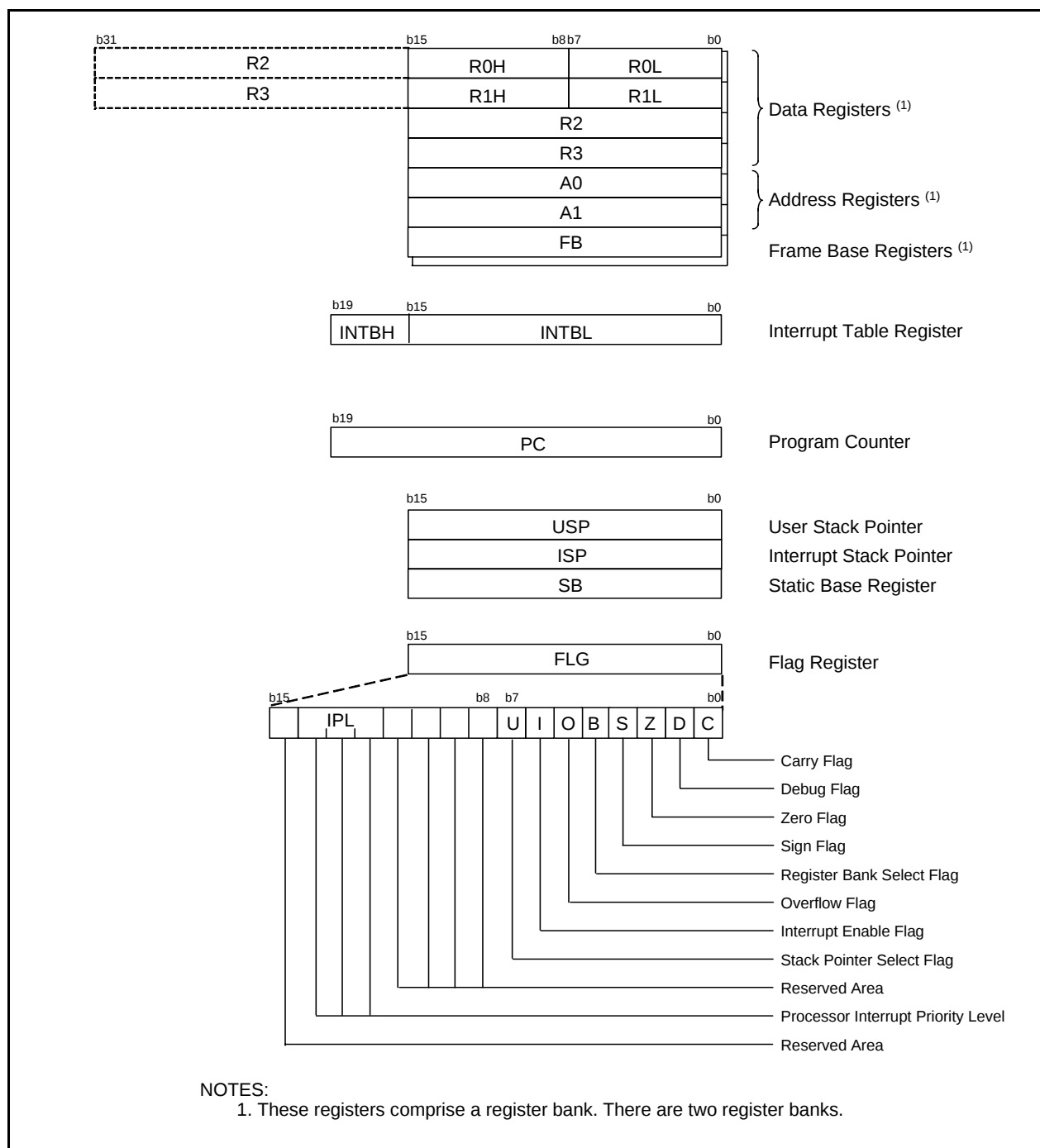


Figure 2.1 Central Processing Unit Register

2.1 Data Registers (R0, R1, R2 and R3)

The R0 register consists of 16 bits, and is used mainly for transfers and arithmetic/logic operations. R1 to R3 are the same as R0.

The R0 register can be separated between high (R0H) and low (R0L) for use as two 8-bit data registers.

R1H and R1L are the same as R0H and R0L. Conversely, R2 and R0 can be combined for use as a 32-bit data register (R2R0). R3R1 is the same as R2R0.

2.8.8 Stack Pointer Select Flag (U Flag)

ISP is selected when the U flag is “0”; USP is selected when the U flag is “1”.

The U flag is cleared to “0” when a hardware interrupt request is accepted or an INT instruction for software interrupt Nos. 0 to 31 is executed.

2.8.9 Processor Interrupt Priority Level (IPL)

IPL is configured with three bits, for specification of up to eight processor interrupt priority levels from level 0 to level 7.

If a requested interrupt has priority greater than IPL, the interrupt is enabled.

2.8.10 Reserved Area

When write to this bit, write “0”. When read, its content is indeterminate.

Table 4.3 SFR Information (3) ⁽¹⁾

Address	Register	Symbol	After Reset
0080h			
0081h			
0082h			
0083h			
0084h			
0085h			
0086h			
0087h to 01AFh			
01B0h			
01B1h			
01B2h			
01B3h			
01B4h	Flash Identification Register ⁽²⁾	FIDR	XXXXXX00b
01B5h	Flash Memory Control Register 1 ⁽²⁾	FMR1	0X00XX0Xb
01B6h			
01B7h	Flash Memory Control Register 0 ⁽²⁾	FMR0	00000001b
01B8h	Address Match Interrupt Register 2	RMAD2	00h
01B9h			00h
01BAh			XXh
01BBh			XXXXXX00b
01BCh	Address Match Interrupt Register 3	RMAD3	00h
01BDh			00h
01BEh			XXh
01C0h to 024Fh			
0250h			
0251h			
0252h			
0253h			
0254h			
0255h			
0256h			
0257h			
0258h			
0259h			
025Ah			
025Bh			
025Ch			
025Dh			
025Eh	Peripheral Clock Select Register	PCLKR	00000011b
025Fh			
0260h to 032Fh			
0330h			
0331h			
0332h			
0333h			
0334h			
0335h			
0336h			
0337h			
0338h			
0339h			
033Ah			
033Bh			
033Ch			
033Dh			
033Eh			
033Fh			

NOTES:

1. The blank areas are reserved and cannot be accessed by users.
2. This register is included in the flash memory version.

X : Nothing is mapped to this bit

Table 4.5 SFR Information (5) ⁽¹⁾

Address	Register	Symbol	After Reset
0380h	Count Start Flag	TABSR	00h
0381h	Clock Prescaler Reset Flag	CPSRF	0XXXXXXb
0382h	One-Shot Start Flag	ONSF	00h
0383h	Trigger Select Register	TRGSR	00h
0384h	Up-Down Flag	UDF	00h ⁽²⁾
0385h			
0386h	Timer A0 Register	TA0	XXh
0387h			XXh
0388h	Timer A1 Register	TA1	XXh
0389h			XXh
038Ah	Timer A2 Register	TA2	XXh
038Bh			XXh
038Ch	Timer A3 Register	TA3	XXh
038Dh			XXh
038Eh	Timer A4 Register	TA4	XXh
038Fh			XXh
0390h	Timer B0 Register	TB0	XXh
0391h			XXh
0392h	Timer B1 Register	TB1	XXh
0393h			XXh
0394h	Timer B2 Register	TB2	XXh
0395h			XXh
0396h	Timer A0 Mode Register	TA0MR	00h
0397h	Timer A1 Mode Register	TA1MR	00h
0398h	Timer A2 Mode Register	TA2MR	00h
0399h	Timer A3 Mode Register	TA3MR	00h
039Ah	Timer A4 Mode Register	TA4MR	00h
039Bh	Timer B0 Mode Register	TB0MR	00XX0000b
039Ch	Timer B1 Mode Register	TB1MR	00XX0000b
039Dh	Timer B2 Mode Register	TB2MR	00XX0000b
039Eh	Timer B2 Special Mode Register	TB2SC	XXXXXX00b
039Fh			
03A0h	UART0 Transmit/Receive Mode Register	U0MR	00h
03A1h	UART0 Bit Rate Generator	U0BRG	XXh
03A2h	UART0 Transmit Buffer Register	U0TB	XXh
03A3h			XXh
03A4h	UART0 Transmit/Receive Control Register 0	U0C0	00001000b
03A5h	UART0 Transmit/Receive Control Register 1	U0C1	00XX0010b
03A6h	UART0 Receive Buffer Register	U0RB	XXh
03A7h			XXh
03A8h	UART1 Transmit/Receive Mode Register	U1MR	00h
03A9h	UART1 Bit Rate Generator	U1BRG	XXh
03AAh	UART1 Transmit Buffer Register	U1TB	XXh
03ABh			XXh
03ACh	UART1 Transmit/Receive Control Register 0	U1C0	00001000b
03ADh	UART1 Transmit/Receive Control Register 1	U1C1	00XX0010b
03AEh	UART1 Receive Buffer Register	U1RB	XXh
03AFh			XXh
03B0h	UART Transmit/Receive Control Register 2	UCON	X0000000b
03B1h			
03B2h			
03B3h			
03B4h			
03B5h			
03B6h			
03B7h			
03B8h	DMA0 Request Factor Select Register	DM0SL	00h
03B9h			
03BAh	DMA1 Request Factor Select Register	DM1SL	00h
03BBh			
03BCh	CRC Data Register	CRCD	XXh
03BDh			XXh
03BEh	CRC Input Register	CRCIN	XXh
03BFh			

NOTES:

1. The blank areas are reserved and cannot be accessed by users.
2. Bit 5 in the Up-down flag is "0" by reset. However, The values in these bits when read are indeterminate.

X : Nothing is mapped to this bit

Table 5.4 A/D Conversion Characteristics (1)

Symbol	Parameter		Measuring Condition		Standard			Unit
					Min.	Typ.	Max.	
–	Resolution		VREF=VCC1				10	Bits
INL	Integral Non-Linearity Error	10bit	VREF=VCC1=5V	AN0 to AN7 input, AN0_0 to AN0_7 input, AN2_0 to AN2_7 input, ANEX0, ANEX1 input			±3	LSB
				External operation amp connection mode			±7	LSB
			VREF=VCC1=3.3V	AN0 to AN7 input, AN0_0 to AN0_7 input, AN2_0 to AN2_7 input, ANEX0, ANEX1 input			±5	LSB
				External operation amp connection mode			±7	LSB
		8bit	VREF=VCC1=5V, 3.3V				±2	LSB
		–	Absolute Accuracy	10bit	VREF=VCC1=5V	AN0 to AN7 input, AN0_0 to AN0_7 input, AN2_0 to AN2_7 input, ANEX0, ANEX1 input		
External operation amp connection mode						±7	LSB	
VREF=VCC1=3.3V	AN0 to AN7 input, AN0_0 to AN0_7 input, AN2_0 to AN2_7 input, ANEX0, ANEX1 input					±5	LSB	
	External operation amp connection mode					±7	LSB	
8bit	VREF=VCC1=5V, 3.3V					±2	LSB	
–	Tolerance Level Impedance						3	
DNL	Differential Non-Linearity Error						±1	LSB
–	Offset Error						±3	LSB
–	Gain Error						±3	LSB
RLADDER	Ladder Resistance		VREF=VCC1		10		40	kΩ
tCONV	10-bit Conversion Time, Sample & Hold Available		VREF=VCC1=5V, φAD=12MHz		2.75			μs
tCONV	8-bit Conversion Time, Sample & Hold Available		VREF=VCC1=5V, φAD=12MHz		2.33			μs
tsAMP	Sampling Time				0.25			μs
VREF	Reference Voltage				2.0		VCC1	V
VIA	Analog Input Voltage				0		VREF	V

NOTES:

1. Referenced to VCC1=AVCC=VREF=3.3 to 5.5V, VSS=AVSS=0V at T_{opr} = –20 to 85°C / –40 to 85°C unless otherwise specified.
2. If VCC1 > VCC2, do not use AN0_0 to AN0_7 and AN2_0 to AN2_7 as analog input pins.
3. φAD frequency must be 12 MHz or less. And divide the fAD if VCC1 is less than 4.0V, and φAD frequency into 10 MHz or less.
4. When sample & hold is disabled, φAD frequency must be 250 kHz or more, in addition to the limitation in Note 3.
When sample & hold is enabled, φAD frequency must be 1MHz or more, in addition to the limitation in Note 3.

Table 5.12 Electrical Characteristics (2) ⁽¹⁾

Symbol	Parameter		Measuring Condition		Standard			Unit	
					Min.	Typ.	Max.		
Icc	Power Supply Current (Vcc1=Vcc2=4.0V to 5.5V)	In single-chip mode, the output pins are open and other pins are Vss	Mask ROM	f(BCLK)=24MHz No division, PLL operation		14	20	mA	
				No division, On-chip oscillation		1		mA	
			Flash Memory	f(BCLK)=24MHz, No division, PLL operation		18	27	mA	
				No division, On-chip oscillation		1.8		mA	
			Flash Memory Program	f(BCLK)=10MHz, VCC1=5.0V		15		mA	
			Flash Memory Erase	f(BCLK)=10MHz, VCC1=5.0V		25		mA	
			Mask ROM	f(XCIN)=32kHz Low power dissipation mode, ROM ⁽³⁾		25		μA	
			Flash Memory	f(BCLK)=32kHz Low power dissipation mode, RAM ⁽³⁾		25		μA	
				f(BCLK)=32kHz Low power dissipation mode, Flash Memory ⁽³⁾		420		μA	
				On-chip oscillation, Wait mode		50		μA	
				Mask ROM Flash Memory	f(BCLK)=32kHz Wait mode ⁽²⁾ , Oscillation capability High		7.5		μA
			f(BCLK)=32kHz Wait mode ⁽²⁾ , Oscillation capability Low			2.0		μA	
			Stop mode Topr =25°C			0.8	3.0	μA	
Idet4	Low Voltage Detection Dissipation Current ⁽⁴⁾					0.7	4	μA	
Idet3	Reset Area Detection Dissipation Current ⁽⁴⁾					1.2	8	μA	

NOTES:

1. Referenced to V_{CC1}=V_{CC2}=4.2 to 5.5V, V_{SS} = 0V at T_{opr} = -20 to 85°C / -40 to 85°C, f(BCLK)=24MHz unless otherwise specified.
2. With one timer operated using fC32.
3. This indicates the memory in which the program to be executed exists.
4. I_{det} is dissipation current when the following bit is set to "1" (detection circuit enabled).
I_{det4}: VC27 bit in the VCR2 register
I_{det3}: VC26 bit in the VCR2 register

$$V_{CC1}=V_{CC2}=5V$$

Switching Characteristics

($V_{CC1} = V_{CC2} = 5V$, $V_{SS} = 0V$, at $T_{opr} = -20$ to $85^{\circ}C$ / -40 to $85^{\circ}C$ unless otherwise specified)

Table 5.27 Memory Expansion and Microprocessor Modes (for setting with no wait)

Symbol	Parameter		Standard		Unit
			Min.	Max.	
$t_d(BCLK-AD)$	Address Output Delay Time	See Figure 5.2		25	ns
$t_h(BCLK-AD)$	Address Output Hold Time (in relation to BCLK)		4		ns
$t_h(RD-AD)$	Address Output Hold Time (in relation to RD)		0		ns
$t_h(WR-AD)$	Address Output Hold Time (in relation to WR)		(NOTE 2)		ns
$t_d(BCLK-CS)$	Chip Select Output Delay Time			25	ns
$t_h(BCLK-CS)$	Chip Select Output Hold Time (in relation to BCLK)		4		ns
$t_d(BCLK-ALE)$	ALE Signal Output Delay Time			15	ns
$t_h(BCLK-ALE)$	ALE Signal Output Hold Time		-4		ns
$t_d(BCLK-RD)$	RD Signal Output Delay Time			25	ns
$t_h(BCLK-RD)$	RD Signal Output Hold Time		0		ns
$t_d(BCLK-WR)$	WR Signal Output Delay Time			25	ns
$t_h(BCLK-WR)$	WR Signal Output Hold Time		0		ns
$t_d(BCLK-DB)$	Data Output Delay Time (in relation to BCLK)			40	ns
$t_h(BCLK-DB)$	Data Output Hold Time (in relation to BCLK) ⁽³⁾		4		ns
$t_d(DB-WR)$	Data Output Delay Time (in relation to WR)		(NOTE 1)		ns
$t_h(WR-DB)$	Data Output Hold Time (in relation to WR) ⁽³⁾		(NOTE 2)		ns
$t_d(BCLK-HLDA)$	HLDA Output Delay Time			40	ns

NOTES:

1. Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f(BCLK)} - 40 [ns] \quad f(BCLK) \text{ is } 12.5MHz \text{ or less.}$$

2. Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f(BCLK)} - 10 [ns]$$

3. This standard value shows the timing when the output is off, and does not show hold time of data bus.

Hold time of data bus varies with capacitor volume and pull-up (pull-down) resistance value.

Hold time of data bus is expressed in

$$t = -CR \times \ln(1 - V_{OL} / V_{CC2})$$

by a circuit of the right figure.

For example, when $V_{OL} = 0.2V_{CC2}$, $C = 30pF$, $R = 1k\Omega$, hold time of output "L" level is

$$t = -30pF \times 1k\Omega \times \ln(1 - 0.2V_{CC2} / V_{CC2}) = 6.7ns.$$

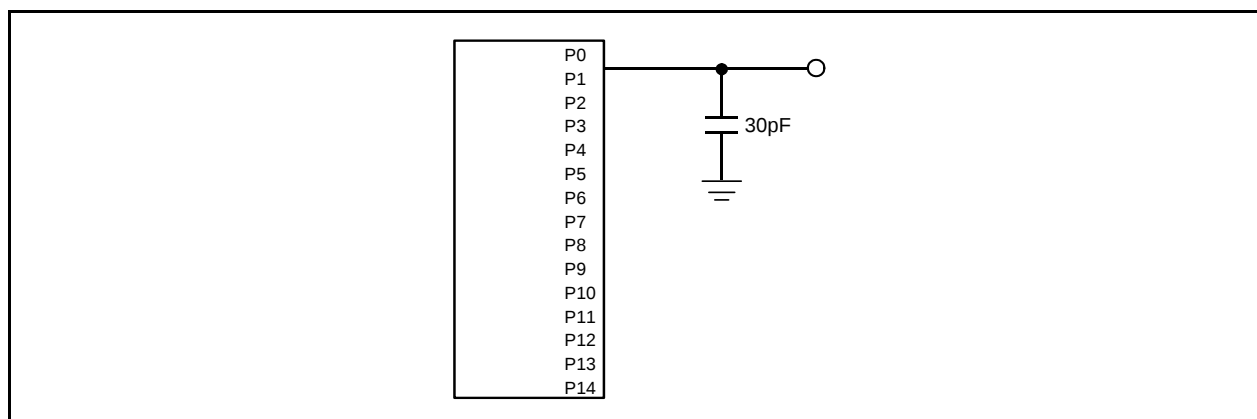
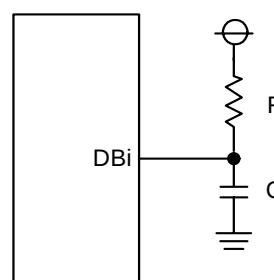


Figure 5.2 Ports P0 to P14 Measurement Circuit

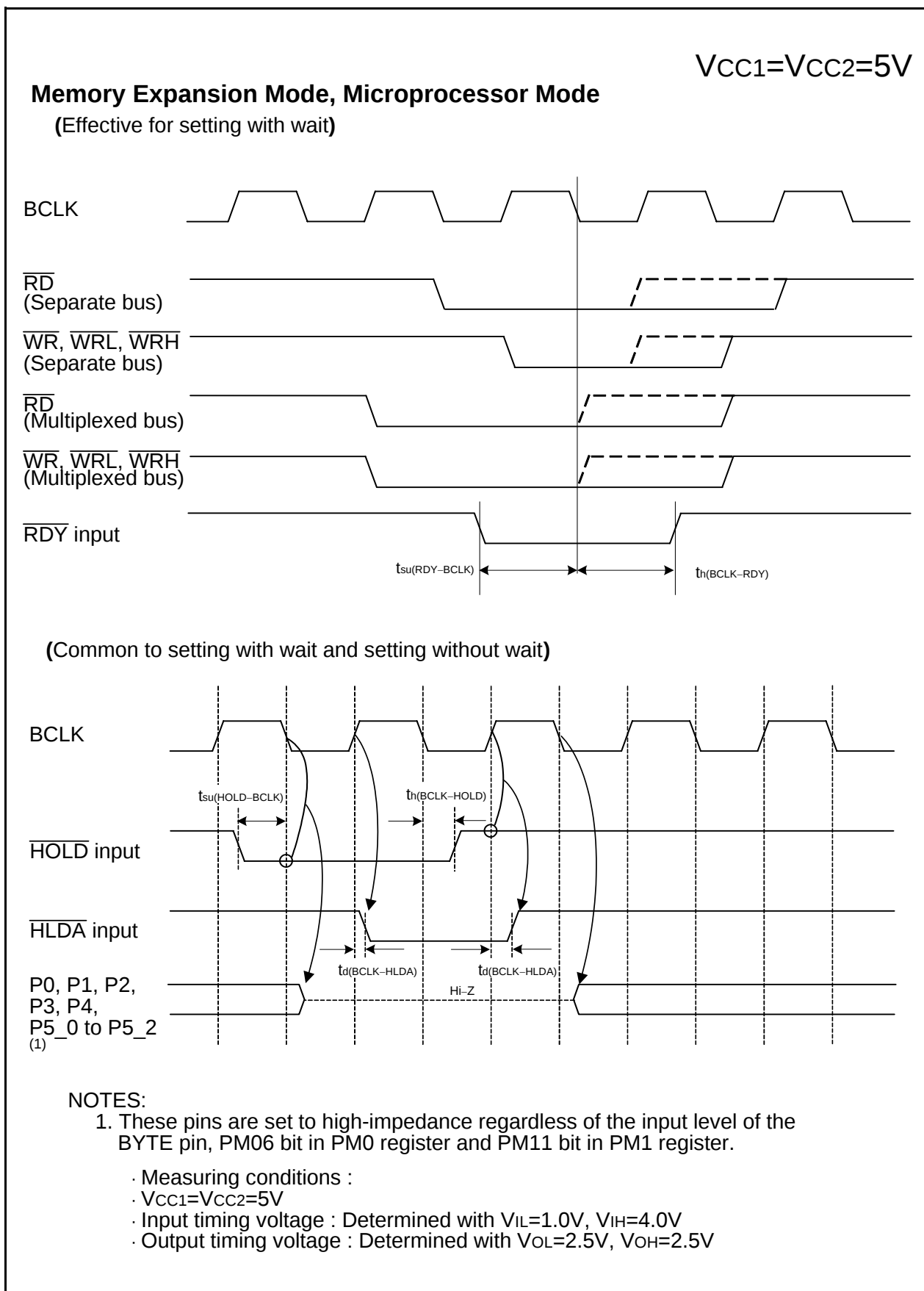


Figure 5.5 Timing Diagram (3)

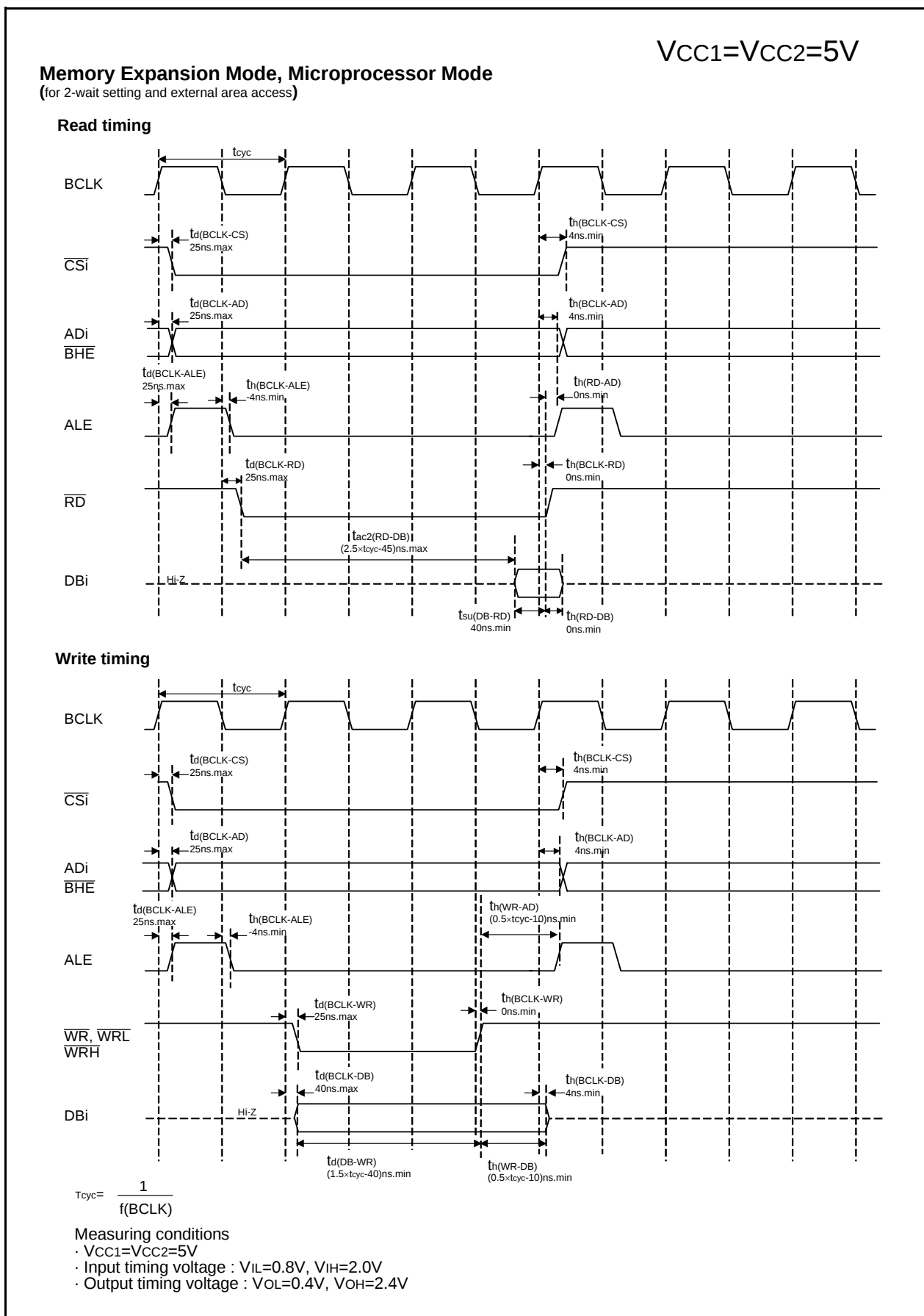


Figure 5.8 Timing Diagram (6)

$$V_{CC1}=V_{CC2}=3V$$

Switching Characteristics(V_{CC1} = V_{CC2} = 5V, V_{SS} = 0V, at T_{opr} = –20 to 85°C / –40 to 85°C unless otherwise specified)**Table 5.48 Memory Expansion and Microprocessor Modes (for 2- to 3-wait setting, external area access and multiplex bus selection)**

Symbol	Parameter		Standard		Unit
			Min.	Max.	
t _d (BCLK-AD)	Address Output Delay Time	See Figure 5.12		50	ns
t _h (BCLK-AD)	Address Output Hold Time (in relation to BCLK)		4		ns
t _h (RD-AD)	Address Output Hold Time (in relation to RD)		(NOTE 1)		ns
t _h (WR-AD)	Address Output Hold Time (in relation to WR)		(NOTE 1)		ns
t _d (BCLK-CS)	Chip Select Output Delay Time			50	ns
t _h (BCLK-CS)	Chip Select Output Hold Time (in relation to BCLK)		4		ns
t _h (RD-CS)	Chip Select Output Hold Time (in relation to RD)		(NOTE 1)		ns
t _h (WR-CS)	Chip Select Output Hold Time (in relation to WR)		(NOTE 1)		ns
t _d (BCLK-RD)	RD Signal Output Delay Time			40	ns
t _h (BCLK-RD)	RD Signal Output Hold Time		0		ns
t _d (BCLK-WR)	WR Signal Output Delay Time			40	ns
t _h (BCLK-WR)	WR Signal Output Hold Time		0		ns
t _d (BCLK-DB)	Data Output Delay Time (in relation to BCLK)			50	ns
t _h (BCLK-DB)	Data Output Hold Time (in relation to BCLK)		4		ns
t _d (DB-WR)	Data Output Delay Time (in relation to WR)		(NOTE 2)		ns
t _h (WR-DB)	Data Output Hold Time (in relation to WR)		(NOTE 1)		ns
t _d (BCLK-HLDA)	HLDA Output Delay Time			40	ns
t _d (BCLK-ALE)	ALE Signal Output Delay Time (in relation to BCLK)			25	ns
t _h (BCLK-ALE)	ALE Signal Output Hold Time (in relation to BCLK)		–4		ns
t _d (AD-ALE)	ALE Signal Output Delay Time (in relation to Address)		(NOTE 3)		ns
t _h (AD-ALE)	ALE Signal Output Hold Time (in relation to Address)		(NOTE 4)		ns
t _d (AD-RD)	RD Signal Output Delay From the End of Address		0		ns
t _d (AD-WR)	WR Signal Output Delay From the End of Address		0		ns
t _{dz} (RD-AD)	Address Output Floating Start Time			8	ns

NOTES:

1. Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f(\text{BCLK})} - 10 [\text{ns}]$$

2. Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f(\text{BCLK})} - 50 [\text{ns}] \quad n \text{ is "2" for 2-wait setting, "3" for 3-wait setting.}$$

3. Calculated according to the BCLK frequency as follows:

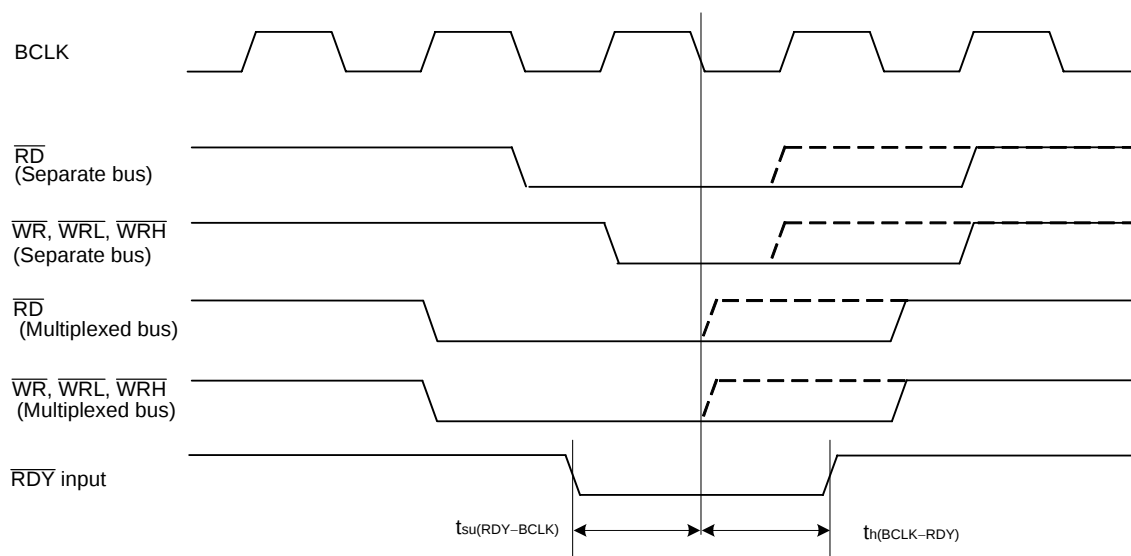
$$\frac{0.5 \times 10^9}{f(\text{BCLK})} - 40 [\text{ns}]$$

4. Calculated according to the BCLK frequency as follows:

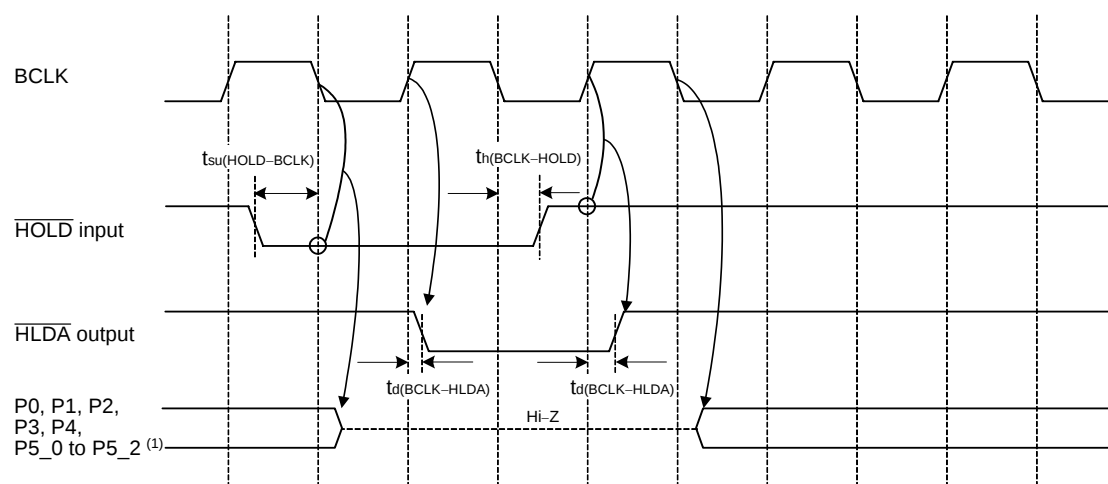
$$\frac{0.5 \times 10^9}{f(\text{BCLK})} - 15 [\text{ns}]$$

Memory Expansion Mode, Microprocessor Mode

(Effective for setting with wait)

 $V_{CC1}=V_{CC2}=3V$ 

(Common to setting with wait and setting without wait)

**NOTES:**

1. These pins are set to high-impedance regardless of the input level of the BYTE pin, PM06 bit in PM0 register and PM11 bit in PM1 register.

Measuring conditions :

- $V_{CC1}=V_{CC2}=3V$
- Input timing voltage : Determined with $V_{IL}=0.6V$, $V_{IH}=2.4V$
- Output timing voltage : Determined with $V_{OL}=1.5V$, $V_{OH}=1.5V$

Figure 5.15 Timing Diagram (3)

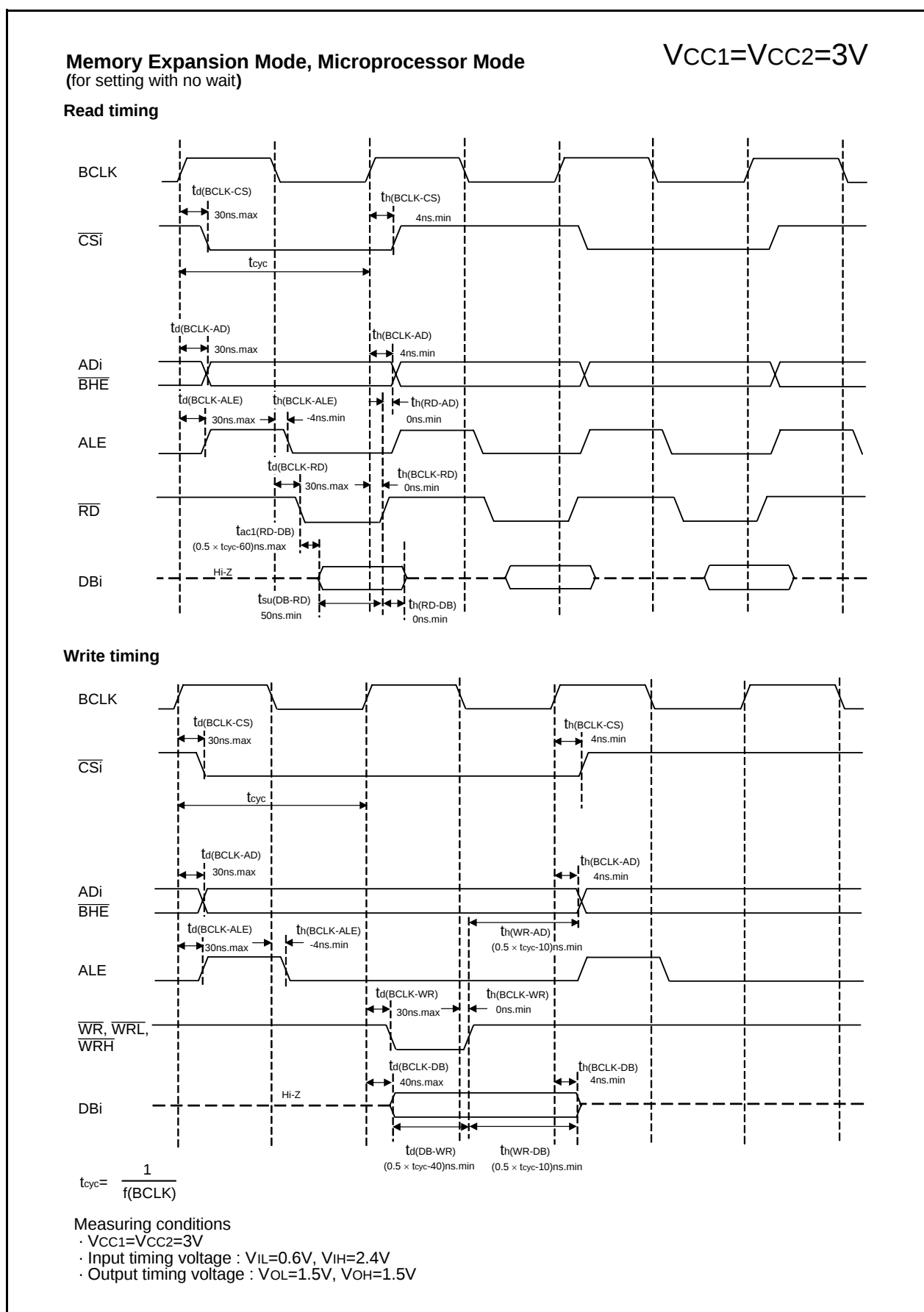
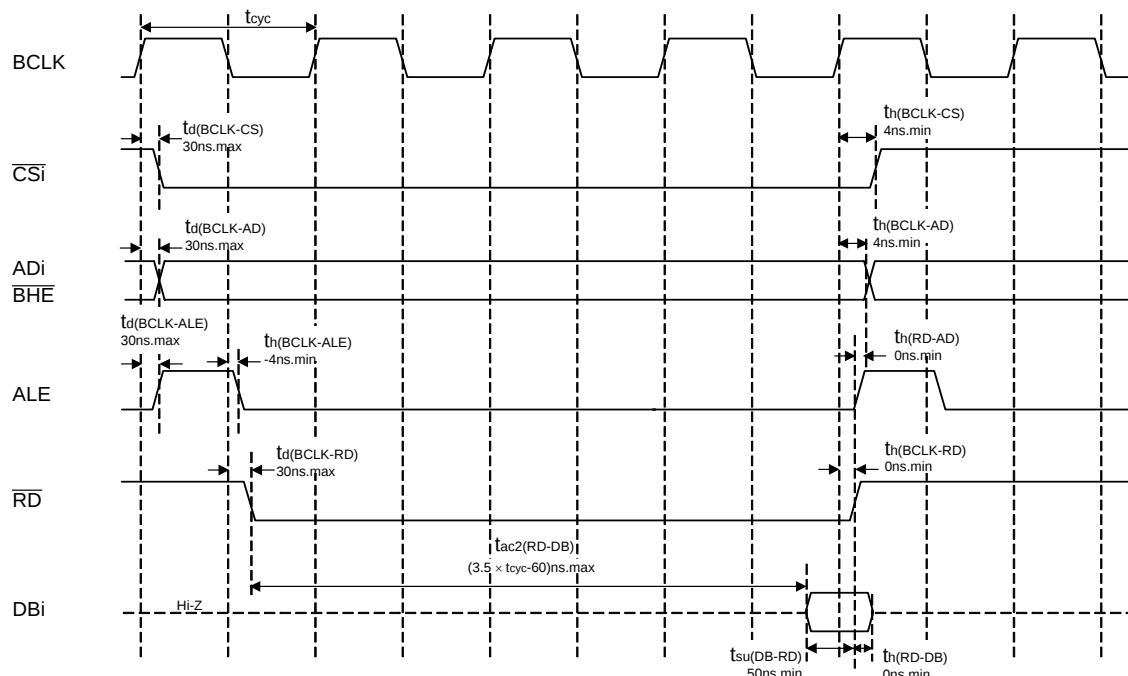
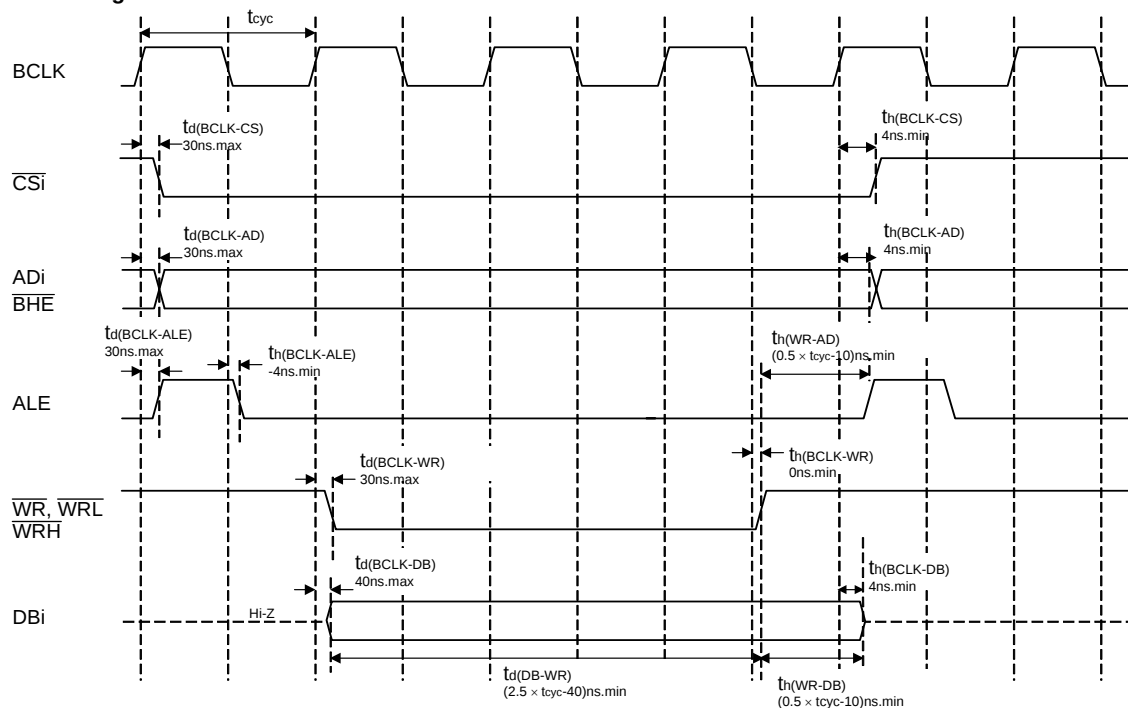


Figure 5.16 Timing Diagram (4)

Memory Expansion Mode, Microprocessor Mode
 (for 3-wait setting and external area access)

$$V_{CC1} = V_{CC2} = 3V$$

Read timing

Write timing


$$t_{cyc} = \frac{1}{f(BCLK)}$$

Measuring conditions

- $V_{CC1}=V_{CC2}=3V$
- Input timing voltage : $V_{IL}=0.6V$, $V_{IH}=2.4V$
- Output timing voltage : $V_{OL}=1.5V$, $V_{OH}=1.5V$

Figure 5.19 Timing Diagram (7)

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP100-14x14-0.50	PLQP0100KB-A	100P6Q-A / FP-100U / FP-100UV	0.6g

NOTE)

- DIMENSIONS *1* AND *2* DO NOT INCLUDE MOLD FLASH.
- DIMENSION *3* DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	13.9	14.0	14.1
E	13.9	14.0	14.1
A ₂	—	1.4	—
H _D	15.8	16.0	16.2
H _E	15.8	16.0	16.2
A	—	—	1.7
A ₁	0.05	0.1	0.15
b _p	0.15	0.20	0.25
b ₁	—	0.18	—
c	0.09	0.145	0.20
c ₁	—	0.125	—
θ	0°	—	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
Z _D	—	1.0	—
Z _E	—	1.0	—
L	0.35	0.5	0.65
L ₁	—	1.0	—

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-QFP80-14x14-0.65	PROP0080JA-A	80P6S-A	1.1g

NOTE)

- DIMENSIONS *1* AND *2* DO NOT INCLUDE MOLD FLASH.
- DIMENSION *3* DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	13.8	14.0	14.2
E	13.8	14.0	14.2
A ₂	—	2.8	—
H _D	16.5	16.8	17.1
H _E	16.5	16.8	17.1
A	—	—	3.05
A ₁	0	0.1	0.2
b _p	0.25	0.3	0.4
c	0.13	0.15	0.2
θ	0°	—	10°
e	—	0.5	0.65
y	—	—	0.10
Z _D	—	0.825	—
Z _E	—	0.825	—
L	0.4	0.6	0.8

REVISION HISTORY		M16C/62P Group (M16C/62P, M16C/62PT) Hardware Manual	
Rev.	Date	Description	
		Page	Summary
		47	Figure 5.1 Power Supply Circuit Timing Diagram is partly revised.
		48	Table 5.11 Electrical Characteristics (1) is partly deleted.
		49	Table 5.12 Electrical Characteristics (2) is partly revised.
		50	Note 1 of Table 5.13 External Clock Input (XIN input) is added.
		67	Notes 1 to 4 of Table 5.32 External Clock Input (XIN input) are added.
		85	Table 5.53 Flash Memory Version Electrical Characteristics for 100 cycle products is partly revised. Standard (Min.) is partly revised. Table 5.54 Flash Memory Version Electrical Characteristics for 10,000 cycle products is partly revised. Standard (Min.) is partly revised. Note 5 is revised. Table 23.55 Flash Memory Version Program / Erase Voltage and Read Operation Voltage Characteristics is partly revised.
		87	Table 5.57 Electrical Characteristics (1) is partly deleted.
		88	Table 5.58 Electrical Characteristics is partly revised.