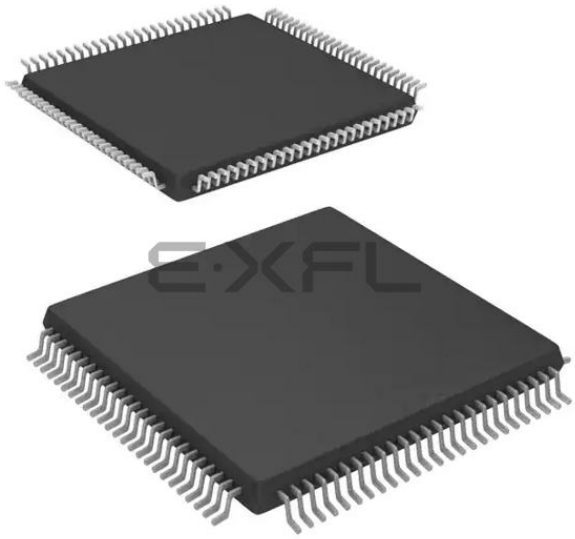

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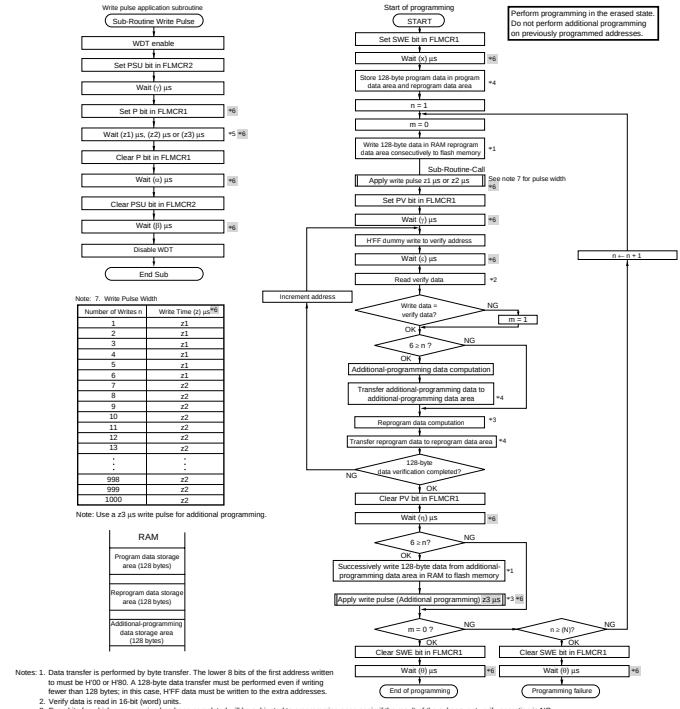
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	H8S/2000
Core Size	16-Bit
Speed	10MHz
Connectivity	Host Interface (LPC), I²C, IrDA, SCI, X-Bus
Peripherals	PWM, WDT
Number of I/O	74
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df2140bvte10v

Item	Page	Revision (See Manual for Details)
23.8.1 Program/ Program-Verify Figure 23.11 Program/Program-Verify Flowchart	625	Figure 23.11 amended  Notes: 1. Data transfer is performed by byte transfer. The lower 8 bits of the first address written to must be H'00 or H'80. A 128-byte data transfer must be performed even if writing fewer than 128 bytes; in this case, H'FF data must be written to the extra addresses. 2. Verify data is read in 16-bit (word) units. 3. Even bits for which programming has been completed will be subjected to programming once again if the result of the subsequent verify operation is NG. 4. A 128-byte area for storing program data, a 128-byte area for storing reprogram data, and a 128-byte area for storing additional data must be provided in RAM. The contents of the reprogram data area and additional data area are modified as programming proceeds. 5. A write pulse of z1 µs or z2 µs is applied according to the progress of the programming operation. See note 7 for details of the pulse widths. When writing of additional-programming data is executed, a z3 µs write pulse should be applied. Reprogram data when the write pulse is applied. 6. The values of x, y, z1, z2, z3, α, β, γ, ε, η, θ, and N are shown in sections 28.1.6 and 28.2.6, Flash Memory Characteristics. Reprogram Data Computation Table Original Data (D) / Verify Data (V) / Reprogram Data (X) / Comments 0 0 1 Programming completed 0 1 0 Programming incomplete; reprogram 1 0 1 — 1 1 1 Still in erased state; no action Additional-Programming Data Computation Table Reprogram Data (X') / Verify Data (V) / Additional-Programming Data (Y) / Comments 0 0 0 Additional programming to be executed 0 1 1 Additional programming not to be executed 1 0 1 — 1 1 1 Additional programming not to be executed
		Section of “Masked ROM” deleted
Section 24 Clock Pulse Generator Figure 24.1 Block Diagram of Clock Pulse Generator	633	Figure 24.1 amended (Before) ϕ2 to f32 → (After) ϕ2 to ϕ32
24.5 Subclock Input Circuit	639	Description of “When Subclock Is Not Needed” and “Note on Subclock Usage” added
25.1.1 Standby Control Register (SBYCR)	643	Table amended … SCK2 to SCK0 must be cleared to B'000.

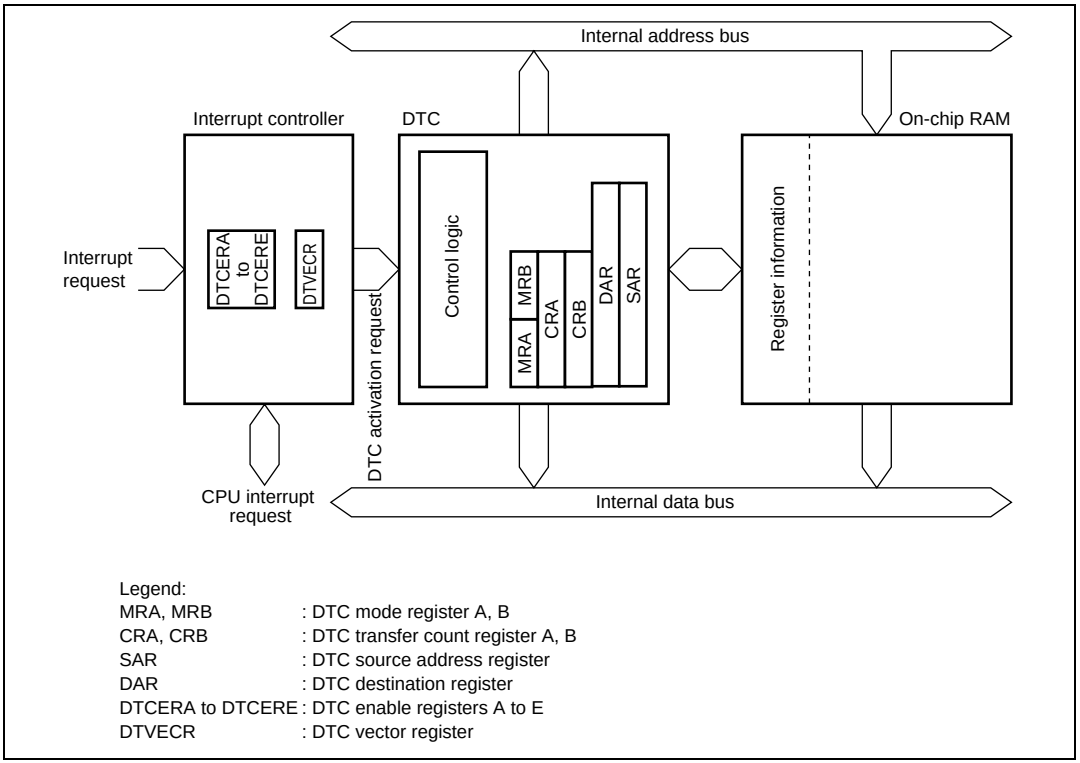


Figure 7.1 Block Diagram of DTC

7.2.8 DTC Vector Register (DTVECR)

DTVECR enables or disables DTC activation by software, and sets a vector number for the software activation interrupt.

DTVECR is initialized to H'00 at a reset and in hardware standby mode.

Bit	Bit Name	Initial Value	R/W	Description
7	SWDTE	0	R/W	DTC Software Activation Enable Setting this bit to 1 activates DTC. Only 1 can always be written to this bit. 0 can be written to after reading 1 from this bit. [Clearing conditions] • When the DISEL bit is 0 and the specified number of transfers have not ended. • When 0 is written to the DISEL bit after a software-activated data transfer end interrupt (SWDTEND) request has been sent to the CPU. [Holding conditions] • When the DISEL bit is 1 and data transfer has ended • When the specified number of transfers have ended. • During data transfer activated by software
6	DTVEC6	0	R/W	DTC Software Activation Vectors 6 to 0 These bits specify a vector number for DTC software activation. The vector address is expressed as H'0400 + (vector number × 2). For example, when DTVEC6 to DTVEC0 = H'10, the vector address is H'0420. When the SWDTE bit is 0, these bits can be written to.
5	DTVEC5	0	R/W	
4	DTVEC4	0	R/W	
3	DTVEC3	0	R/W	
2	DTVEC2	0	R/W	
1	DTVEC1	0	R/W	
0	DTVEC0	0	R/W	

- P66/FTOB/CIN6/$\overline{\text{KIN6}}$/$\overline{\text{IRQ6}}$

  The pin function is switched as shown below according to the combination of the OEB bit in TOCR of the FRT and the P66DDR bit.

OEB	0	1	
P66DDR	0	1	—
Pin Function	P66 input pin	P66 output pin	FTOB output pin
	$\overline{\text{IRQ6}}$ input pin, $\overline{\text{KIN6}}$ input pin, CIN6 input pin*		

Note: * This pin is used as the $\overline{\text{IRQ6}}$ input pin when bit IRQ6E is set to 1 in IER while the KMIMR6 bit in KMIMR is 0. It can always be used as the $\overline{\text{KIN6}}$ or CIN6 input pin.

- P65/FTID/CIN5/$\overline{\text{KIN5}}$

P65DDR	0	1
Pin Function	P65 input pin	P65 output pin
	FTID input pin, $\overline{\text{KIN5}}$ input pin, CIN5 input pin*	

Note: * This pin can always be used as the FTID, $\overline{\text{KIN5}}$, or CIN5 input pin.

- P64/FTIC/CIN4/$\overline{\text{KIN4}}$/CLAMPO

  The pin function is switched as shown below according to the combination of the CLOE bit in TCONRO of the timer connection function and the P64DDR bit.

CLOE	0		1
P64DDR	0	1	—
Pin Function	P64 input pin	P64 output pin	CLAMPO output pin
	FTIC input pin, $\overline{\text{KIN4}}$ input pin, CIN4 input pin*		

Note: * This pin can always be used as the FTIC, $\overline{\text{KIN4}}$, or CIN4 input pin.

- P63/FTIB/CIN3/$\overline{\text{KIN3}}$/VFBACKI

P63DDR	0	1
Pin Function	P63 input pin	P63 output pin
	FTIB input pin, VFBACKI input pin, $\overline{\text{KIN3}}$ input pin, CIN3 input pin*	

Note: * This pin can always be used as the FTIB, $\overline{\text{KIN3}}$, CIN3, or VFBACKI input pin.

- P62/FTIA/CIN2/$\overline{\text{KIN2}}$/VSYNCI/TMIY

P62DDR	0	1
Pin Function	P62 input pin	P62 output pin
	FTIA input pin, VSYNCI input pin, TMIY input pin, $\overline{\text{KIN2}}$ input pin, CIN2 input pin*	

Note: * This pin can always be used as the FTIA, TMIY, $\overline{\text{KIN2}}$, CIN2, or VSYNCI input pin.

- P61/FTOA/CIN1/$\overline{\text{KIN1}}$/VSYNCO

  The pin function is switched as shown below according to the combination of the OEA bit in TOCR of the FRT, the VOE bit in TCONRO of the timer connection function, and the P61DDR bit.

VOE	0			1
OEA	0		1	—
P61DDR	0	1	—	—
Pin Function	P61 input pin	P61 output pin	FTOA output pin	VSYNCO output pin
	$\overline{\text{KIN1}}$ input pin, CIN1 input pin*			

Note: * When this pin is used as the VSYNCO pin, bit OEA in TOCR of the FRT must be cleared to 0. This pin can always be used as the $\overline{\text{KIN1}}$ or CIN1 input pin.

- P60/FTCI/CIN0/$\overline{\text{KIN0}}$/HFBACKI/TMIX

P60DDR	0	1
Pin Function	P60 input pin	P60 output pin
	FTCI input pin, HFBACKI input pin, TMIX input pin, $\overline{\text{KIN0}}$ input pin, CIN0 input pin*	

Note: * This pin is used as the FTCI input pin when an external clock is selected with bits CKS1 and CKS0 in TCR of the FRT. It can always be used as the TMIX, $\overline{\text{KIN0}}$, CIN0, or HFBACKI input pin.

8.15.4 Port E and Port F Nch-OD Control Register (PENOCR, PFNOCR)

PENOCR and PFNOCR specify the output driver type for pins on ports E and F which are configured as outputs on a bit-by-bit basis.

Bit	Bit Name	Initial Value	R/W	Description
7	PE7NOCR	0	R/W	0: CMOS (p-channel driver enabled)
6	PE6NOCR	0	R/W	1: N-channel open drain (p-channel driver disabled)
5	PE5NOCR	0	R/W	
4	PE4NOCR	0	R/W	
3	PE3NOCR	0	R/W	
2	PE2NOCR	0	R/W	
1	PE1NOCR	0	R/W	
0	PE0NOCR	0	R/W	

Bit	Bit Name	Initial Value	R/W	Description
7	PF7NOCR	0	R/W	0: CMOS (p-channel driver enabled)
6	PF6NOCR	0	R/W	1: N-channel open drain (p-channel driver disabled)
5	PF5NOCR	0	R/W	
4	PF4NOCR	0	R/W	
3	PF3NOCR	0	R/W	
2	PF2NOCR	0	R/W	
1	PF1NOCR	0	R/W	
0	PF0NOCR	0	R/W	

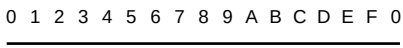
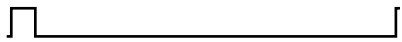
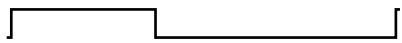
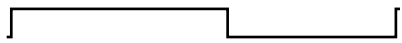
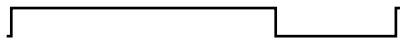
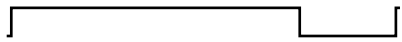
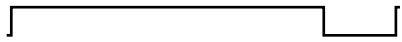
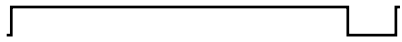
8.15.5 Pin Functions

DDR	0		1			
NOCR	—		0		1	
ODR	0	1	0	1	0	1
N-ch. driver	OFF		ON	OFF	ON	OFF
P-ch. driver	OFF		OFF	ON	OFF	
Input pull-up MOS	OFF	ON	OFF			
Pin function	Input pin		Output pin			

9.4 Operation

The upper four bits of PWDR specify the duty cycle of the basic pulse as 0/16 to 15/16 with a resolution of 1/16. Table 9.4 shows the duty cycles of the basic pulse.

Table 9.4 Duty Cycle of Basic Pulse

Upper 4 Bits	Basic Pulse Waveform (Internal)
0000	
0001	
0010	
0011	
0100	
0101	
0110	
0111	
1000	
1001	
1010	
1011	
1100	
1101	
1110	
1111	

The lower four bits of PWDR specify the position of pulses added to the 16 basic pulses. An additional pulse adds a high period (when OS = 0) with a width equal to the resolution before the rising edge of a basic pulse. When the upper four bits of PWDR are 0000, there is no rising edge of the basic pulse, but the timing for adding pulses is the same. Table 9.5 shows the positions of

9.5 Usage Note

9.5.1 Module Stop Mode Setting

PWM operation can be enabled or disabled using the module stop control register. The initial setting is for PWM operation to be halted. Register access is enabled by canceling the module stop mode. For details, refer to section 26, Power-Down Modes.

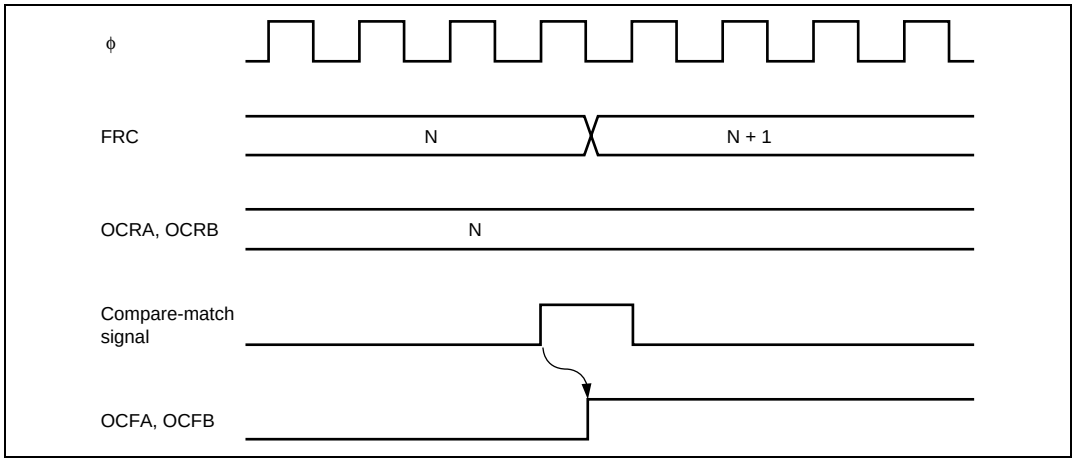


Figure 11.12 Timing of Output Compare Flag (OCFA or OCFB) Setting

11.5.8 Timing of FRC Overflow Flag Setting

The FRC overflow flag (OVF) is set to 1 when FRC overflows (changes from H'FFFF to H'0000). Figure 11.13 shows the timing of setting the OVF flag.

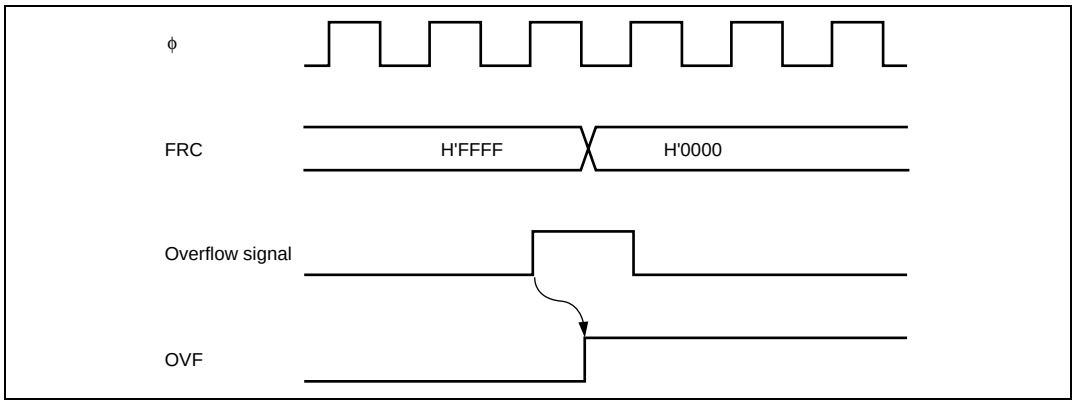


Figure 11.13 Timing of Overflow Flag (OVF) Setting

Figure 16.1 shows a block diagram of the I²C bus interface. Figure 16.2 shows an example of I/O pin connections to external circuits. Since I²C bus interface I/O pins are different in structure from normal port pins, they have different specifications for permissible applied voltages. For details, see section 28, Electrical Characteristics.

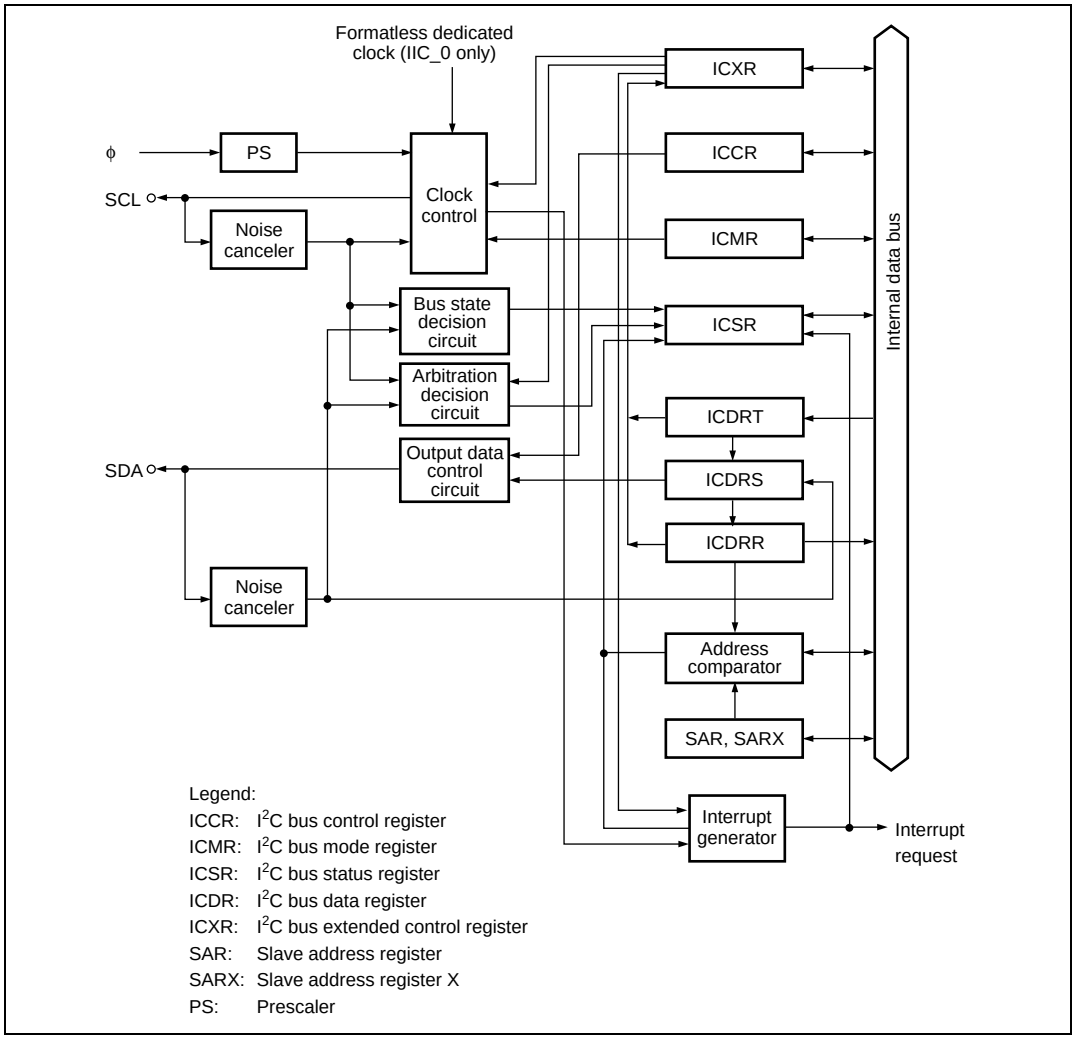


Figure 16.1 Block Diagram of I²C Bus Interface

transfer using the DTC. The ICDRE or ICDRF flag is cleared, however, since the specified number of ICDR reads or writes have been completed.

Tables 16.4 and 16.5 show the relationship between the flags and the transfer states.

Table 16.4 Flags and Transfer States (Master Mode)

MST	TRS	BBSY	ESTP	STOP	IRTR	AASX	AL	AAS	ADZ	ACKB	ICDRF	ICDRE	State
1	1	0	0	0	0	0↓	0	0↓	0↓	0	—	0	Idle state (flag clearing required)
1	1	1↑	0	0	1↑	0	0	0	0	0	—	1↑	Start condition detected
1	—	1	0	0	—	0	0	0	0	—	—	—	Wait state
1	1	1	0	0	—	0	0	0	0	1↑	—	—	Transmission end (ACKE=1 and ACKB=1)
1	1	1	0	0	1↑	0	0	0	0	0	—	1↑	Transmission end with ICDRE=0
1	1	1	0	0	—	0	0	0	0	0	—	0↓	ICDR write with the above state
1	1	1	0	0	—	0	0	0	0	0	—	1	Transmission end with ICDRE=1
1	1	1	0	0	—	0	0	0	0	0	—	0↓	ICDR write with the above state or after start condition detected
1	1	1	0	0	1↑	0	0	0	0	0	—	1↑	Automatic data transfer from ICDRT to ICDRS with the above state
1	0	1	0	0	1↑	0	0	0	0	—	1↑	—	Reception end with ICDRF=0
1	0	1	0	0	—	0	0	0	0	—	0↓	—	ICDR read with the above state
1	0	1	0	0	—	0	0	0	0	—	1	—	Reception end with ICDRF=1
1	0	1	0	0	—	0	0	0	0	—	0↓	—	ICDR read with the above state
1	0	1	0	0	1↑	0	0	0	0	—	1↑	—	Automatic data transfer from ICDRS to ICDRR with the above state
0↓	0↓	1	0	0	—	0	1↑	0	0	—	—	—	Arbitration lost
1	—	0↓	0	0	—	0	0	0	0	—	—	0↓	Stop condition detected

Legend:

0: 0-state retained

1: 1-state retained

—: Previous state retained

0↓: Cleared to 0

1↑: Set to 1

16.4.6 Slave Transmit Operation

If the slave address matches to the address in the first frame (address reception frame) following the start condition detection when the 8th bit data (R/$\overline{W}$) is 1 (read), the TRS bit in ICCR is automatically set to 1 and the mode changes to slave transmit mode.

Figure 16.24 shows the sample flowchart for the operations in slave transmit mode.

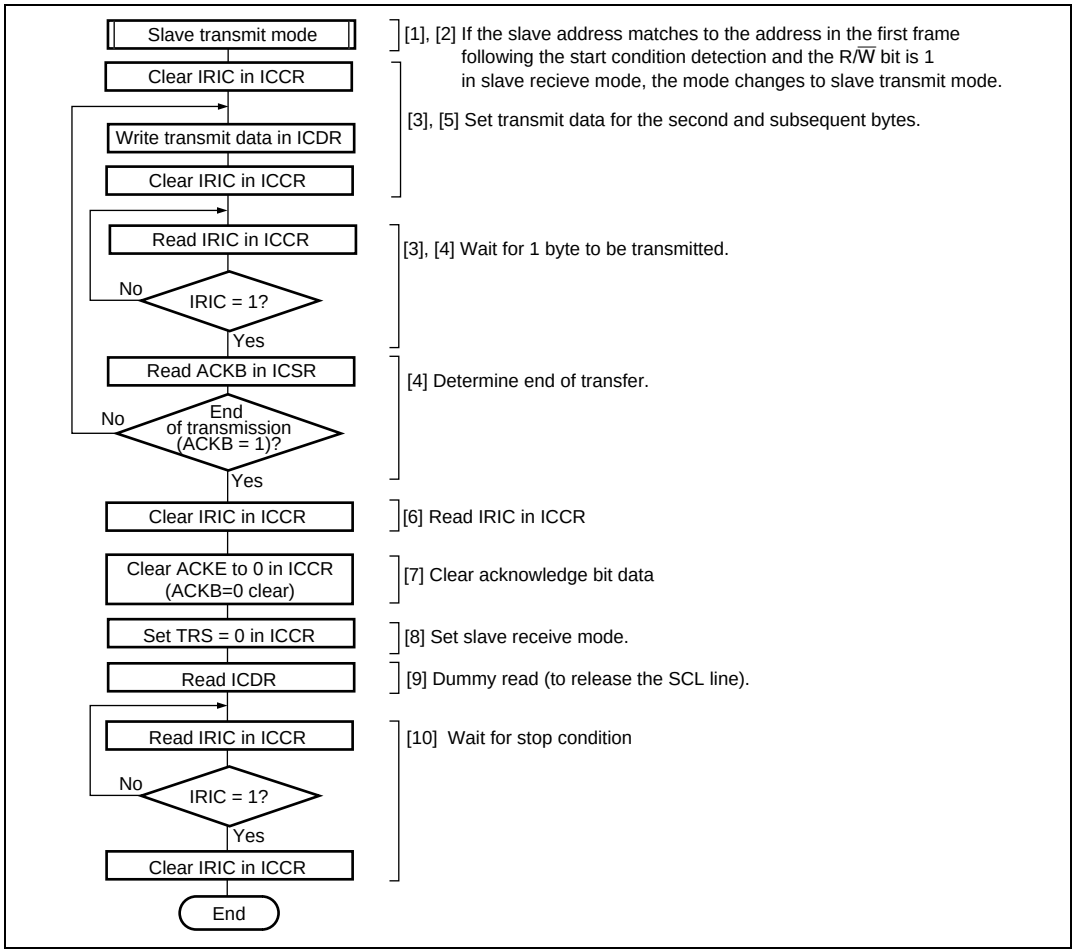


Figure 16.24 Sample Flowchart for Slave Transmit Mode

Bit	Bit Name	Initial Value	R/W Slave	R/W Host	Description
6	CLKREQ	0	R	—	LCLK Request Indicates that the host interface's SERIRQ output is requesting a restart of LCLK. 0: No LCLK restart request [Clearing conditions] • LPC hardware reset or LPC software reset • LPC hardware shutdown or LPC software shutdown • SERIRQ is set to continuous mode • There are no further interrupts for transfer to the host in quiet mode 1: LCLK restart request issued [Setting condition] In quiet mode, SERIRQ interrupt output becomes necessary while LCLK is stopped
5	IRQBSY	0	R	—	SERIRQ Busy Indicates that the host interface's SERIRQ signal is engaged in transfer processing. 0: SERIRQ transfer frame wait state [Clearing conditions] • LPC hardware reset or LPC software reset • LPC hardware shutdown or LPC software shutdown • End of SERIRQ transfer frame 1: SERIRQ transfer processing in progress [Setting condition] Start of SERIRQ transfer frame

Section 23 ROM

This LSI has an on-chip flash memory. The features of the flash memory are summarized below.

A block diagram of the flash memory is shown in figure 23.1.

23.1 Features

- Size

Product Classification	RAM Capacitance	RAM Address
H8S/2161B	128 kbytes	H'000000–H'01FFFF (mode 2) H'0000–H'DFFF (mode 3)
H8S/2160B	64 kbytes	H'000000–H'00FFFF (mode 2) H'0000–H'DFFF (mode 3)
H8S/2141B	128 kbytes	H'000000–H'01FFFF (mode 2) H'0000–H'DFFF (mode 3)
H8S/2140B	64 kbytes	H'000000–H'00FFFF (mode 2) H'0000–H'DFFF (mode 3)
H8S/2145B	256 kbytes	H'000000–H'03FFFF (mode 2) H'0000–H'DFFF (mode 3)
H8S/2148B	128 kbytes	H'000000–H'01FFFF (mode 2) H'0000–H'DFFF (mode 3)

- Programming/erase methods

  The flash memory is programmed 128 bytes at a time. Erase is performed in single-block units. The flash memory is configured as follows:

  — 64-kbyte version: 8 kbytes × 2 blocks, 16 kbytes × 1 block, 28 kbytes × 1 block, and 1 kbyte × 4 blocks

  — 128-kbyte version: 32 kbytes × 2 blocks, 8 kbytes × 2 blocks, 16 kbytes × 1 block, 28 kbytes × 1 block, and 1 kbyte × 4 blocks

  — 256-kbyte version: 64 kbytes × 3 blocks, 32 kbytes × 1 block, and 4 kbytes × 8 blocks.

  To erase the entire flash memory, each block must be erased in turn.

- Programming/erase time

  It takes 10 ms (typ.) to program the flash memory 128 bytes at a time; 80 µs (typ.) per 1 byte. Erasing one block takes 100 ms (typ.).

23.5.2 Flash Memory Control Register 2 (FLMCR2)

FLMCR2 monitors the state of flash memory programming/erasing protection (error protection) and sets up the flash memory to transit to programming/erasing mode. FLMCR2 is initialized to H'00 by a reset or in hardware standby mode. The ESU and PSU bits are cleared to 0 in software standby mode, sub-active mode, sub-sleep mode, or watch mode, or when the SWE bit in FLMCR1 is cleared to 0.

Bit	Bit Name	Initial Value	R/W	Description
7	FLER	0	R	Flash memory error Indicates that an error has occurred during flash memory programming/erasing. When this bit is set to 1, flash memory goes to the error-protection state. For details, see section 23.9.3, Error Protection.
6 to 2	—	All 0	R/(W)	Reserved The initial values should not be modified.
1	ESU	0	R/W	Erase Setup When this bit is set to 1 while SWE = 1, the flash memory transits to the erase setup state. When it is cleared to 0, the erase setup state is cancelled. Set this bit to 1 before setting the E bit in FLMCR1 to 1.
0	PSU	0	R/W	Program Setup When this bit is set to 1 while SWE = 1, the flash memory transits to the program setup state. When it is cleared to 0, the program setup state is cancelled. Set this bit to 1 before setting the P bit in FLMCR1 to 1.

Table 27.7 Bus Timing (2) (Advanced Mode)

Conditions: V_{CC} = 2.7 V to 3.6 V, $V_{CC}B$ = 2.7 V to 5.5 V, V_{SS} = 0 V, ϕ = 2 MHz to maximum operating frequency, T_a = –20 to +75°C

		Condition			
		10 MHz			
Item	Symbol	Min	Max	Unit	Test Conditions
Address delay time	t_{AD}	—	60	ns	Figures 27.11 to 27.15
Address setup time	t_{AS}	$0.5 \times t_{cyc} - 30$	—	ns	
Address hold time	t_{AH}	$0.5 \times t_{cyc} - 20$	—	ns	
$\overline{CS}$ delay time ($\overline{IOS}$)	t_{CSD}	—	60	ns	
$\overline{AS}$ delay time	t_{ASD}	—	60	ns	
$\overline{RD}$ delay time 1	t_{RSD1}	—	60	ns	
$\overline{RD}$ delay time 2	t_{RSD2}	—	60	ns	
Read data setup time	t_{RDS}	35	—	ns	
Read data hold time	t_{RDH}	0	—	ns	
Read data access time 1	t_{ACC1}	—	$1.0 \times t_{cyc} - 80$	ns	
Read data access time 2	t_{ACC2}	—	$1.5 \times t_{cyc} - 50$	ns	
Read data access time 3	t_{ACC3}	—	$2.0 \times t_{cyc} - 80$	ns	
Read data access time 4	t_{ACC4}	—	$2.5 \times t_{cyc} - 50$	ns	
Read data access time 5	t_{ACC5}	—	$3.0 \times t_{cyc} - 80$	ns	
$\overline{HWR}$, $\overline{LWR}$ delay time 1	t_{WRD1}	—	60	ns	
$\overline{HWR}$, $\overline{LWR}$ delay time 2	t_{WRD2}	—	60	ns	
$\overline{HWR}$, $\overline{LWR}$ pulse width 1	t_{WSW1}	$1.0 \times t_{cyc} - 40$	—	ns	
$\overline{HWR}$, $\overline{LWR}$ pulse width 2	t_{WSW2}	$1.5 \times t_{cyc} - 40$	—	ns	
Write data delay time	t_{WDD}	—	60	ns	
Write data setup time	t_{WDS}	0	—	ns	
Write data hold time	t_{WDH}	20	—	ns	
$\overline{WAIT}$ setup time	t_{WTS}	60	—	ns	
$\overline{WAIT}$ hold time	t_{WTH}	10	—	ns	

Table 27.17 DC Characteristics (4)

Conditions: V_{CC} = 4.0 V to 5.5 V, $V_{CC}B$ = 4.0 V to 5.5 V, AV_{CC}*1 = 4.0 V to 5.5 V, AV_{ref}*1 = 4.0 V to AV_{CC}, V_{SS} = AV_{SS}*1 = 0 V, T_a = –20 to +75°C (normal specification product), T_a = –40 to +85°C (wide range temperature specification product)

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Input leakage current	$\overline{RES}$	$\lvert I_{in} \rvert$	—	—	10.0	µA	V_{in} = 0.5 to V_{CC} – 0.5 V
	$\overline{STBY}$, NMI, MD1, MD0		—	—	1.0		
	Port 7		—	—	1.0		V_{in} = 0.5 to AV_{CC} – 0.5 V
Three-state leakage current (off state)	Ports 1 to 6, 8, 9, A*4, B	$\lvert I_{TSI} \rvert$	—	—	1.0	µA	V_{in} = 0.5 to V_{CC} – 0.5 V, V_{in} = 0.5 to $V_{CC}B$ – 0.5 V
Input pull-up MOS current	Ports 1 to 3	$-I_P$	30	—	300	µA	V_{in} = 0 V, V_{CC} = 4.5 V to 5.5 V, $V_{CC}B$ = 4.5 V to 5.5 V
	Ports A*4, B, 6 (P6PUE = 0)		60	—	600		
	Port 6 (P6PUE = 1)		15	—	200		
	Ports 1 to 3		20	—	200	µA	V_{in} = 0 V, V_{CC} = 4.0 V to 4.5 V, $V_{CC}B$ = 4.0 V to 4.5 V
	Ports A*4, B, 6 (P6PUE = 0)		40	—	500		
	Port 6 (P6PUE = 1)		10	—	150		
Input capacitance	$\overline{RES}$ (4)	C_{in}	—	—	80	pF	V_{in} = 0 V, f = 1 MHz, T_a = 25°C
	NMI		—	—	50		
	P52, P97, P42, P86, PA7 to PA2		—	—	20		
	Input pins except (4) above		—	—	15		
Current dissipation*2	Normal operation	I_{CC}	—	45	58	mA	f = 16 MHz
	Sleep mode		—	30	46	mA	f = 16 MHz
	Standby mode*3		—	1.0	5.0	µA	$T_a \leq$ 50°C
			—	—	20.0		50°C < T_a

Table 27.28 A/D Conversion Characteristics
(CIN15 to CIN0 Input: 134/266-State Conversion)

Condition A: V_{CC} = 5.0 V ±10%, AV_{CC} = 5.0 V ±10%, AV_{ref} = 4.5 V to AV_{CC},
V_{SS} = AV_{SS} = 0 V, φ = 2 MHz to maximum operating frequency,
T_a = –20 to +75°C (normal specification product),
T_a = –40 to +85°C (wide range temperature specification product)

Condition B: V_{CC} = 4.0 V to 5.5 V, AV_{CC} = 4.0 V to 5.5 V, AV_{ref} = 4.0 V to AV_{CC},
V_{SS} = AV_{SS} = 0 V, φ = 2 MHz to maximum operating frequency,
T_a = –20 to +75°C (normal specification product),
T_a = –40 to +85°C (wide range temperature specification product)

Condition C: V_{CC} = 3.0 V to 3.6 V*4, AV_{CC} = 3.0 V to 3.6 V*4, AV_{ref} = 3.0 V to AV_{CC}*4,
$V_{CC}B$ = 3.0 V to 5.5 V*4, V_{SS} = AV_{SS} = 0 V, φ = 2 MHz to maximum operating frequency, T_a = –20 to +75°C

	Condition C			Condition B			Condition A			
	10 MHz			16 MHz			20 MHz			
Item	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
Resolution	10	10	10	10	10	10	10	10	10	bits
Conversion time*3	—	—	13.4	—	—	8.4	—	—	6.7	µs
Analog input capacitance	—	—	20	—	—	20	—	—	20	pF
Permissible signal-source impedance	—	—	5	—	—	10*1 5*2	—	—	10*1 5*2	kΩ
Nonlinearity error	—	—	±11.0	—	—	±5.0	—	—	±5.0	LSB
Offset error	—	—	±11.5	—	—	±5.5	—	—	±5.5	LSB
Full-scale error	—	—	±11.5	—	—	±5.5	—	—	±5.5	LSB
Quantization error	—	—	±0.5	—	—	±0.5	—	—	±0.5	LSB
Absolute accuracy	—	—	±12.0	—	—	±6.0	—	—	±6.0	LSB

Notes: 1. When conversion time ≥ 11.17 µs (CKS = 0, or φ ≤ 12 MHz at CKS = 1)
2. When conversion time < 11.17 µs (φ > 12 MHz at CKS = 1)
3. At the maximum operating frequency in single mode.
4. When using CIN, ensure that V_{CC} = 3.0 V to 3.6 V, AV_{CC} = 3.0 V to 3.6 V, AV_{ref} = 3.0 V to 3.6 V, $V_{CC}B$ = 3.0 V to 5.5 V.

27.2.6 Flash Memory Characteristics

Table 27.30 shows the flash memory characteristics.

Table 27.30 Flash Memory Characteristics (Operation Range at Programming/Erasing)

5-V version conditions: V_{CC} = 4.0 V to 5.5 V, V_{SS} = 0 V, T_a = –20 to +75°C (normal specification product), T_a = –40 to +85°C (wide range temperature specification product)

3-V version conditions: V_{CC} = 3.0 V to 3.6 V, V_{SS} = 0 V, T_a = –20 to +75°C

Item		Symbol	Min	Typ	Max	Unit	Test Condition
Programming time*1 *2 *4		t_P	—	10	200	ms/ 128 bytes	
Erase time*1 *3 *6		t_E	—	100	1200	ms/block	
Reprogramming count		N_{WEC}	—	—	100	times	
Programming	Wait time after SWE-bit setting*1	x	1	—	—	µs	
	Wait time after PSU-bit setting*1	y	50	—	—	µs	
	Wait time after P-bit setting*1 *4	z1	28	30	32	µs	1 ≤ n ≤ 6
		z2	198	200	202	µs	7 ≤ n ≤ 1000
		z3	8	10	12	µs	Additional write
	Wait time after P-bit clear*1	α	5	—	—	µs	
	Wait time after PSU-bit clear*1	β	5	—	—	µs	
	Wait time after PV-bit setting*1	γ	4	—	—	µs	
	Wait time after dummy write*1	ε	2	—	—	µs	
	Wait time after PV-bit clear*1	η	2	—	—	µs	
	Wait time after SWE-bit clear*1	θ	100	—	—	µs	
	Maximum programming count*1 *4 *5	N	—	—	1000	times	
Erase	Wait time after SWE-bit setting*1	x	1	—	—	µs	
	Wait time after ESU-bit setting*1	y	100	—	—	µs	
	Wait time after E-bit setting*1 *6	z	10	—	100	ms	
	Wait time after E-bit clear*1	α	10	—	—	µs	
	Wait time after ESU-bit clear*1	β	10	—	—	µs	
	Wait time after EV-bit setting*1	γ	20	—	—	µs	
	Wait time after dummy write*1	ε	2	—	—	µs	
	Wait time after EV-bit clear*1	η	4	—	—	µs	
	Wait time after SWE-bit clear*1	θ	100	—	—	µs	
	Maximum erase count*1 *6 *7	N	—	—	120	times	

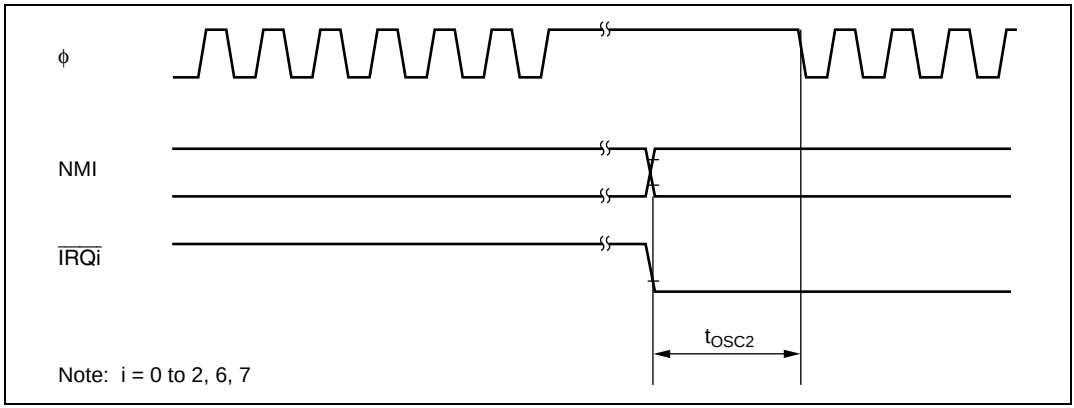


Figure 27.8 Oscillation Setting Timing (Exiting Software Standby Mode)