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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	H8S/2000
Core Size	16-Bit
Speed	20MHz
Connectivity	I²C, IrDA, SCI, X-Bus
Peripherals	PWM, WDT
Number of I/O	74
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 8x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	100-BFQFP
Supplier Device Package	100-QFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df2145bfa20v

Pin No.	Pin Name			
	Extended modes		Single-Chip Modes	Flash Memory Programmer Mode
TFP-144	Mode 1	Mode 2, Mode 3 (EXPE = 1)	Mode 2, Mode 3 (EXPE = 0)	
25	PE7	PE7	PE7	NC
26	PE6	PE6	PE6	NC
27	PE5	PE5	PE5	NC
28	PE4	PE4	PE4	NC
29	PE3	PE3	PE3	NC
30	PE2	PE2	PE2	NC
31	PE1	PE1	PE1	NC
32	PE0	PE0	PE0	NC
33 (B)	PA7/CIN15/$\overline{\text{KIN15}}$/ PS2CD	PA7/A23/CIN15/ $\overline{\text{KIN15}}$/PS2CD	PA7/CIN15/$\overline{\text{KIN15}}$/ PS2CD	NC
34 (B)	PA6/CIN14/$\overline{\text{KIN14}}$/ PS2CC	PA6/A22/CIN14/ $\overline{\text{KIN14}}$/PS2CC	PA6/CIN14/$\overline{\text{KIN14}}$/ PS2CC	NC
35 (B)	PA5/CIN13/$\overline{\text{KIN13}}$/ PS2BD	PA5/A21/CIN13/ $\overline{\text{KIN13}}$/PS2BD	PA5/CIN13/$\overline{\text{KIN13}}$/ PS2BD	NC
36	VCCB	VCCB	VCCB	VCC
37 (B)	PA4/CIN12/$\overline{\text{KIN12}}$/ PS2BC	PA4/A20/CIN12/ $\overline{\text{KIN12}}$/PS2BC	PA4/CIN12/$\overline{\text{KIN12}}$/ PS2BC	NC
38 (B)	PA3/CIN11/$\overline{\text{KIN11}}$/ PS2AD	PA3/A19/CIN11/ $\overline{\text{KIN11}}$/PS2AD	PA3/CIN11/$\overline{\text{KIN11}}$/ PS2AD	NC
39 (B)	PA2/CIN10/$\overline{\text{KIN10}}$/ PS2AC	PA2/A18/CIN10/ $\overline{\text{KIN10}}$/PS2AC	PA2/CIN10/$\overline{\text{KIN10}}$/ PS2AC	NC
40 (B)	PA1/CIN9/$\overline{\text{KIN9}}$	PA1/A17/CIN9/$\overline{\text{KIN9}}$	PA1/CIN9/$\overline{\text{KIN9}}$	NC
41 (B)	PA0/CIN8/$\overline{\text{KIN8}}$	PA0/A16/CIN8/$\overline{\text{KIN8}}$	PA0/CIN8/$\overline{\text{KIN8}}$	NC
42	VSS	VSS	VSS	VSS
43	PF7	PF7	PF7	NC
44	PF6	PF6	PF6	NC
45	PF5	PF5	PF5	NC
46	PF4	PF4	PF4	NC
47	PF3	PF3	PF3	NC
48	PF2	PF2	PF2	NC

Section 3 MCU Operating Modes

3.1 MCU Operating Mode Selection

This LSI has three operating modes (modes 1 to 3). The operating mode is determined by the setting of the mode pins (MD1 and MD0). Table 3.1 shows the MCU operating mode selection.

Table 3.1 lists the MCU operating modes.

Table 3.1 MCU Operating Mode Selection

MCU Operating Mode	MD1	MD0	CPU Operating Mode	Description	On-Chip ROM
0	0	0	—	—	—
1		1	Normal	Expanded mode with on-chip ROM disabled	Disabled
2	1	0	Advanced	Expanded mode with on-chip ROM enabled	Enabled
				Single-chip mode	
3		1	Normal	Expanded mode with on-chip ROM enabled	
				Single-chip mode	

Mode 1 is an expanded mode that allows access to external memory and peripheral devices. With modes 2 and 3, operation begins in single-chip mode after reset release, but a transition can be made to external expansion mode by setting the EXPE bit in MDCR to 1.

Mode 0 cannot be used in this LSI. Thus, mode pins should be set to enable mode 1, 2 or 3 in normal program execution state. Mode pins should not be changed during operation.

3.2 Register Descriptions

The following registers are related to the operating mode. For details on the bus control register (BCR), refer to section 6.3.1, Bus Control Register (BCR).

- Mode control register (MDCR)
- System control register (SYSCR)
- Serial timer control register (STCR)

Bit	Bit Name	Initial Value	R/W	Description
2	NMIEG	0	R/W	NMI Edge Select Selects the valid edge of the NMI interrupt input. 0: An interrupt is requested at the falling edge of NMI input 1: An interrupt is requested at the rising edge of NMI input
1	HIE	0	R/W	Host Interface Enable Controls CPU access to the host interface registers (HICR, IDR1, ODR1, STR1, IDR2, ODR2, and STR2), the keyboard matrix interrupt and MOS input pull-up control registers (KMIMR, KMPCR, and KMIMRA), the 8-bit timer (TMR_X and TMR_Y) registers (TCR_X/TCR_Y, TCSR_X/TCSR_Y, TICRR/TCORA_Y, TICRF/TCORB_Y, TCNT_X/TCNT_Y, TCORC/TISR, TCORA_X, and TCORB_X), and the timer connection registers (TCONRI, TCONRO, TCONRS, and SEDGR). 0: In areas H'(FF)FFF0 to H'(FF)FFF7 and H'(FF)FFFC to H'(FF)FFFF, CPU access to 8-bit timer (TMR_X and TMR_Y) registers and timer connection registers is permitted 1: In areas H'(FF)FFF0 to H'(FF)FFF7 and H'(FF)FFFC to H'(FF)FFFF, CPU access to host interface registers and keyboard matrix interrupt and MOS input pull-up control registers is permitted
0	RAME	1	R/W	RAM Enable Enables or disables on-chip RAM. The RAME bit is initialized when the reset state is released. 0: On-chip RAM is disabled 1: On-chip RAM is enabled

3.2.3 Serial Timer Control Register (STCR)

STCR enables or disables register access, IIC operating mode, and on-chip flash memory, and selects the input clock of the timer counter.

6.3.2 Wait State Control Register (WSCR)

WSCR is used to specify the data bus width for external address space access, the number of access states, the wait mode, and the number of wait states for access to external address spaces. The bus width and the number of access states for internal memory and internal I/O registers are fixed regardless of the WSCR settings.

Bit	Bit Name	Initial Value	R/W	Description
7, 6	—	All 0	R/W	Reserved These bits should not be written by 1.
5	ABW	1	R/W	Bus Width Control Selects 8 or 16 bits for access to the external address space. 0: 16-bit access space 1: 8-bit access space
4	AST	1	R/W	Access State Control Selects 2 or 3 access states for access to the external address space. This bit also enables or disables wait-state insertion. 0: 2-state access space. Wait state insertion disabled in external address space access 1: 3-state access space. Wait state insertion enabled in external address space access
3	WMS1	0	R/W	Wait Mode Select 1, 0
2	WMS0	0	R/W	Select the wait mode for access to the external address space when the AST bit is set to 1. 00: Program wait mode 01: Wait disabled mode 10: Pin wait mode 11: Pin auto-wait mode

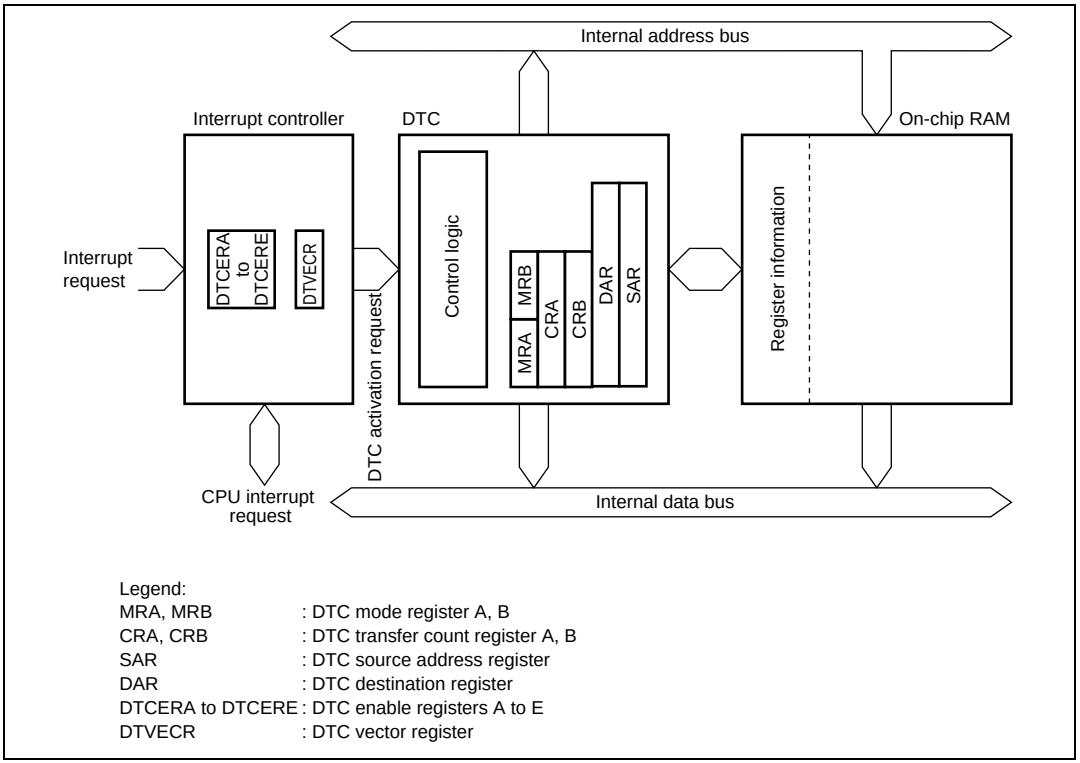


Figure 7.1 Block Diagram of DTC

7.2.5 DTC Transfer Count Register A (CRA)

CRA is a 16-bit register that designates the number of times data is to be transferred by the DTC.

In normal mode, the entire CRA functions as a 16-bit transfer counter (1 to 65536). It is decremented by 1 every time data is transferred, and transfer ends when the count reaches H'0000.

In repeat mode or block transfer mode, the CRA is divided into two parts; the upper 8 bits (CRAH) and the lower 8 bits (CRAL). CRAH holds the number of transfers while CRAL functions as an 8-bit transfer counter (1 to 256). CRAL is decremented by 1 every time data is transferred, and the contents of CRAH are sent when the count reaches H'00.

7.2.6 DTC Transfer Count Register B (CRB)

CRB is a 16-bit register that designates the number of times data is to be transferred by the DTC in block transfer mode. It functions as a 16-bit transfer counter (1 to 65536) that is decremented by 1 every time data is transferred, and transfer ends when the count reaches H'0000.

7.2.7 DTC Enable Registers (DTCER)

DTCER specifies DTC activation interrupt sources. DTCER is comprised of five registers: DTCERA to DTCERE. The correspondence between interrupt sources and DTCE bits is shown in table 7.1. For DTCE bit setting, use bit manipulation instructions such as BSET and BCLR. Multiple DTC activation sources can be set at one time (only at the initial setting) by masking all interrupts and writing data after executing a dummy read on the relevant register.

Bit	Bit Name	Initial Value	R/W	Description
7	DTCE7	0	R/W	DTC Activation Enable
6	DTCE6	0	R/W	Setting this bit to 1 specifies a relevant interrupt source as a DTC activation source.
5	DTCE5	0	R/W	[Clearing conditions]
4	DTCE4	0	R/W	• When data transfer has ended with the DISEL bit in MRB set to 1.
3	DTCE3	0	R/W	• When the specified number of transfers have ended.
2	DTCE2	0	R/W	[Holding condition]
1	DTCE1	0	R/W	When the DISEL bit is 0 and the specified number of transfers have not been completed.
0	DTCE0	0	R/W	

8.7.5 Port 6 Input Pull-Up MOS

Port 6 has an on-chip input pull-up MOS function that can be controlled by software. This input pull-up MOS function can be specified as on or off on a bit-by-bit basis.

The input pull-up MOS current specification can be changed by means of the P6PUE bit. When a pin is designated as an on-chip peripheral module output pin, the input pull-up MOS is always off.

Table 8.5 summarizes the input pull-up MOS states.

Table 8.5 Input Pull-Up MOS States (Port 6)

Mode	Reset	Hardware Standby Mode	Software Standby Mode	In Other Operations
1 to 3	Off	Off	On/Off	On/Off

Legend:
Off: Input pull-up MOS is always off.
On/Off: On when the pin is in the input state, P6DDR = 0, and KMPCR = 1; otherwise off.

8.8 Port 7

Port 7 is an 8-bit input only port. Port 7 pins also function as the A/D converter analog input pins and D/A converter analog output pins. Port 7 functions are the same in all operating modes. Port 7 has the following register.

- Port 7 input data register (P7PIN)

- P80/HA0/$\overline{\text{PME}}$*3

  The pin function is switched as shown below according to the combination of the HI12E bit in SYSCR2, the PMEE bit in HICR0, and the P80DDR bit.

PMEE	0			1
HI12E	0		1	0*1
P80DDR	0	1	—	0*1
Pin Function	P80 input pin	P80 output pin	HA0 input pin*2	$\overline{\text{PME}}$ output pin
	$\overline{\text{PME}}$ input pin*2*3			

Notes: 1. When bit PMEE is set to 1 in HICR0, bits HI12E and P80DDR should be cleared to 0.
2. The HA0 input pin can only be used in mode 2 or 3 (EXPE = 0).
3. Not supported by the H8S/2148B and H8S/2145B (5-V version).

8.10 Port 9

Port 9 is an 8-bit I/O port. Port 9 pins also function as external interrupt input pins, the A/D converter input pin, host interface (XBS) input pins, the IIC_0 I/O pin, the subclock input pin, bus control signal I/O pins, and the system clock (ϕ) output pin. P97 is an NMOS push-pull output. SDA0 is an NMOS open-drain output, and has direct bus drive capability. Port 9 has the following registers.

- Port 9 data direction register (P9DDR)
- Port 9 data register (P9DR)

Bit	Bit Name	Initial Value	R/W	Description
2	OEA	0	R/W	Output Enable A Enables or disables output on PWM (D/A) channel A. 0: PWM (D/A) channel A output (at the PWX0 pin) is disabled 1: PWM (D/A) channel A output (at the PWX0 pin) is enabled
1	OS	0	R/W	Output Select Selects the phase of the PWM (D/A) output. 0: Direct PWM (D/A) output 1: Inverted PWM (D/A) output
0	CKS	0	R/W	Clock Select Selects the PWM (D/A) resolution. If the system clock (ϕ) frequency is 10 MHz, resolutions of 100 ns and 200 ns, can be selected. 0: Operates at resolution (T) = system clock cycle time (t_{cyc}) 1: Operates at resolution (T) = system clock cycle time (t_{cyc}) $\times$ 2

10.5 Operation

A PWM waveform like the one shown in figure 10.2 is output from the PWMX pin. The value in DADR corresponds to the total width (T_L) of the low (0) pulses output in one conversion cycle (256 pulses when CFS = 0, 64 pulses when CFS = 1). When OS = 0, this waveform is directly output. When OS = 1, the output waveform is inverted, and the DADR value corresponds to the total width (T_H) of the high (1) output pulses. Figures 10.3 and 10.4 show the types of waveform output available.

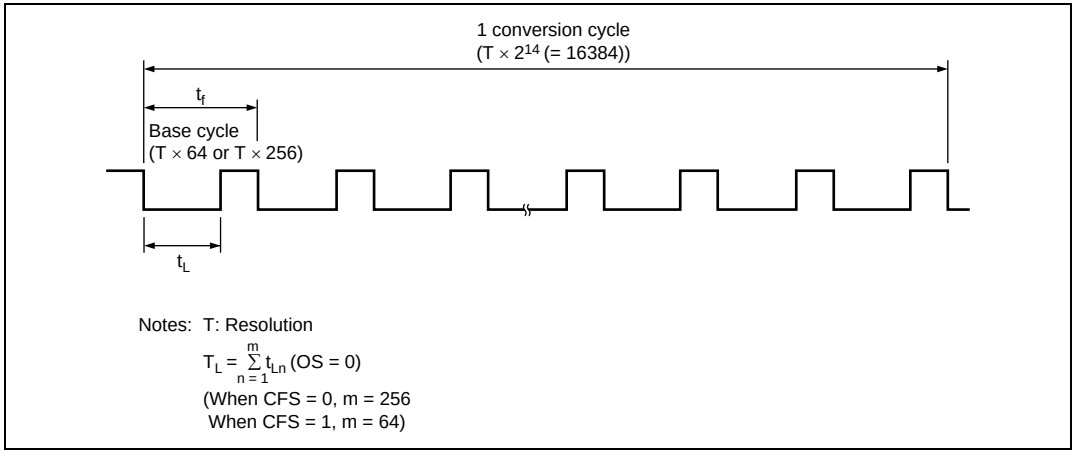


Figure 10.2 PWM D/A Operation

11.2 Input/Output Pins

Table 11.1 lists the FRT input and output pins.

Table 11.1 Pin Configuration

Name	Abbreviation	I/O	Function
Counter clock input pin	FTCI	Input	FRC counter clock input
Output compare A output pin	FTOA	Output	Output compare A output
Output compare B output pin	FTOB	Output	Output compare B output
Input capture A input pin	FTIA	Input	Input capture A input
Input capture B input pin	FTIB	Input	Input capture B input
Input capture C input pin	FTIC	Input	Input capture C input
Input capture D input pin	FTID	Input	Input capture D input

11.3 Register Descriptions

The FRT has the following registers.

- Free-running counter (FRC)
- Output compare register A (OCRA)
- Output compare register B (OCRB)
- Input capture register A (ICRA)
- Input capture register B (ICRB)
- Input capture register C (ICRC)
- Input capture register D (ICRD)
- Output compare register AR (OCRAR)
- Output compare register AF (OCRAF)
- Output compare register DM (OCRDM)
- Timer interrupt enable register (TIER)
- Timer control/status register (TCSR)
- Timer control register (TCR)
- Timer output compare control register (TOCR)

Note: OCRA and OCRB share the same address. Register selection is controlled by the OCRS bit in TOCR. ICRA, ICRB, and ICRC share the same addresses with OCRAR, OCRAF, and OCRDM. Register selection is controlled by the ICRS bit in TOCR.

13.4.3 Measurement of 8-Bit Timer Divided Waveform Period

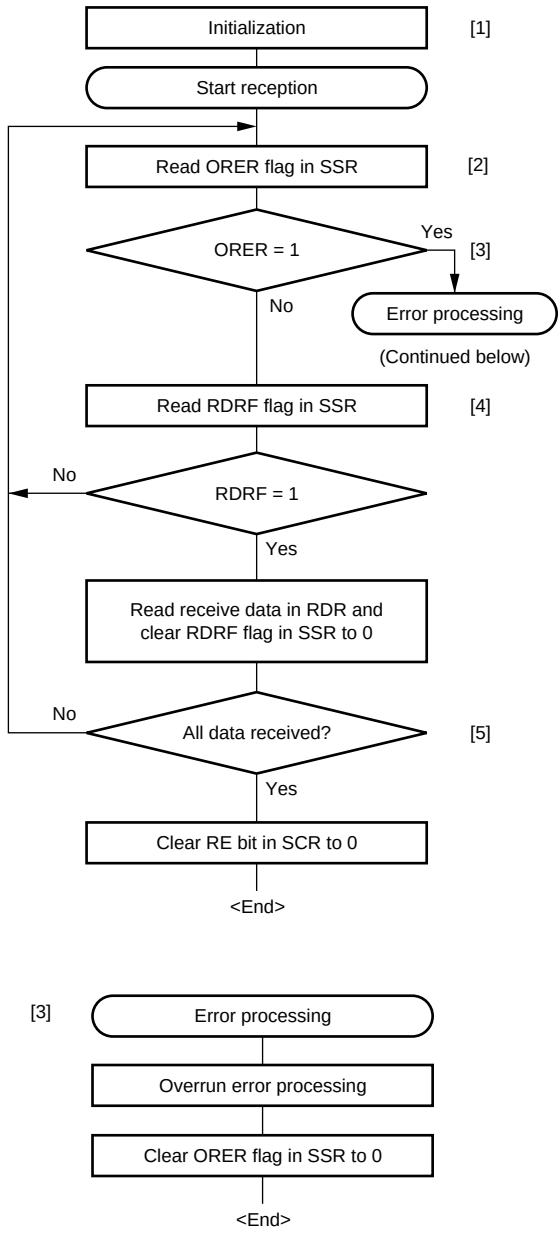
The timer connection facility, TMR_1, and the free-running timer (FRT) can be used to measure the period of an IHI signal divided waveform. Since TMR_1 can be cleared by a rising edge of the inverted IVI signal, the rise and fall of the IHI signal divided waveform can be synchronized with the IVI signal. This enables period measurement to be carried out efficiently.

To measure the period of an IHI signal divided waveform, TCNT in TMR_1 is set to count the external clock (IHI signal) pulses and to be cleared on the rising edge of the external reset signal (inverse of the IVI signal). The value to be used as the division factor is written in TCORA, and the TMO output method is specified by the OS bits in TCSR.

Examples of TCR and TCSR settings in TMR_1, and TCR and TCSR settings in the FRT are shown in table 13.6, and the timing chart for measurement of the IVI signal and IHI signal divided waveform periods is shown in figure 13.5. The period of the IHI signal divided waveform is given by (ICRD(3) – ICRD(2)) × resolution.

Bit	Bit Name	Initial Value	R/W	Description
4	FER	0	R/(W)*	Framing Error [Setting condition] When the stop bit is 0 [Clearing condition] When 0 is written to FER after reading FER = 1 In 2-stop-bit mode, only the first stop bit is checked.
3	PER	0	R/(W)*	Parity Error [Setting condition] When a parity error is detected during reception [Clearing condition] When 0 is written to PER after reading PER = 1
2	TEND	1	R	Transmit End [Setting conditions] • When the TE bit in SCR is 0 • When TDRE = 1 at transmission of the last bit of a 1-byte serial transmit character [Clearing conditions] • When 0 is written to TDRE after reading TDRE = 1 • When a TXI interrupt request is issued allowing the DTC to write data to TDR
1	MPB	0	R	Multiprocessor Bit MPB stores the multiprocessor bit in the receive frame. When the RE bit in SCR is cleared to 0 its previous state is retained.
0	MPBT	0	R/W	Multiprocessor Bit Transfer MPBT stores the multiprocessor bit to be added to the transmit frame.

Note: * Only 0 can be written, to clear the flag.



[1] SCI initialization:
The RxD pin is automatically designated as the receive data input pin.

[2] [3] Receive error processing:
If a receive error occurs, read the ORER flag in SSR, and after performing the appropriate error processing, clear the ORER flag to 0. Transfer cannot be resumed if the ORER flag is set to 1.

[4] SCI status check and receive data read:
Read SSR and check that the RDRF flag is set to 1, then read the receive data in RDR and clear the RDRF flag to 0.
Transition of the RDRF flag from 0 to 1 can also be identified by an RXI interrupt.

[5] Serial reception continuation procedure:
To continue serial reception, before the MSB (bit 7) of the current frame is received, reading the RDRF flag, reading RDR, and clearing the RDRF flag to 0 should be finished.
However, the RDRF flag is cleared automatically when the DTC is initiated by a receive data full interrupt (RXI) and reads data from RDR.

Figure 15.19 Sample Serial Reception Flowchart

This state is maintained while the HIFSD pin is low, and when the HIFSD pin returns to the high-level state, the pins are restored to their normal operation as host interface pins.

Table 18.7 shows the scope of HIF pin shutdown.

Table 18.7 Scope of HIF Pin Shutdown

Abbreviation	Port	Scope of Shutdown in Slave Mode	I/O	Selection Conditions
IOP	P93	O	Input	HI12E = 1
IOΩ	P94	O	Input	HI12E = 1
XΣ1	P95	O	Input	HI12E = 1
XΣ2	P81	Δ	Input	HI12E = 1 and CS2E = 1 and FGA20E = 0
EXΣ2	P90	Δ	Input	HI12E = 1 and CS2E = 1 and FGA20E = 1
XΣ3	PB2	Δ	Input	HI12E = 1 and CS3E = 1
XΣ4	PB3	Δ	Input	HI12E = 1 and CS4E = 1
HA0	P80	O	Input	HI12E = 1
HDB7 to HDB0	P37 to P30	O	I/O	HI12E = 1
HIRQ11	P43	Δ	Output	HI12E = 1 and CS2E = 1 and P43DDR = 1
HIRQ1	P44	Δ	Output	HI12E = 1 and P44DDR = 1
HIRQ12	P45	Δ	Output	HI12E = 1 and P45DDR = 1
HIRQ3	PB0	Δ	Output	HI12E = 1 and CS3E = 1 and PB0DDR = 1
HIRQ4	PB1	Δ	Output	HI12E = 1 and CS4E = 1 and PB1DDR = 1
GA20	P81	Δ	Output	HI12E = 1 and FGA20E = 1
HIFSD	P82	—	Input	HI12E = 1 and SDE = 1

Legend:

O: Pins shut down by shutdown function

The IPΘ2/AΔTPΓ input signal is also fixed in the case of P90 shutdown, the TMCI1/HSYNCI signal in the case of P43 shutdown, and the TMRI/CSYNCI in the case of P45 shutdown.

Δ: Pins shut down only when the XBS function is selected by means of a register setting

—: Pin not shut down

Register Name	Abbreviation	Number of Bits	Address	Module	Data Bus Width	Number of Access States
Keyboard control register L_1	KBCRL_1	8	H'FEDD	Keyboard buffer controller_1	8	2
Keyboard data buffer register_1	KBBR_1	8	H'FEDE	Keyboard buffer controller_1	8	2
Keyboard control register H_2	KBCRH_2	8	H'FEE0	Keyboard buffer controller_2	8	2
Keyboard control register L_2	KBCRL_2	8	H'FEE1	Keyboard buffer controller_2	8	2
Keyboard data buffer register_2	KBBR_2	8	H'FEE2	Keyboard buffer controller_2	8	2
Keyboard comparator control register	KBCOMP	8	H'FEE4	IrDA/ Extended A/D	8	2
DDC switch register	DDCSWR	8	H'FEE6	IIC_0	8	2
Interrupt control register A	ICRA	8	H'FEE8	INT	8	2
Interrupt control register B	ICRB	8	H'FEE9	INT	8	2
Interrupt control register C	ICRC	8	H'FEEA	INT	8	2
IRQ status register	ISR	8	H'FEEB	INT	8	2
IRQ sense control register H	ISCRH	8	H'FEEC	INT	8	2
IRQ sense control register L	ISCRL	8	H'FEED	INT	8	2
DTC enable register A	DTCERA	8	H'FEEE	DTC	8	2
DTC enable register B	DTCERB	8	H'FEEF	DTC	8	2
DTC enable register C	DTCERC	8	H'FEF0	DTC	8	2
DTC enable register D	DTCERD	8	H'FEF1	DTC	8	2
DTC enable register E	DTCERE	8	H'FEF2	DTC	8	2
DTC vector register	DTVECR	8	H'FEF3	DTC	8	2
Address break control register	ABRKCR	8	H'FEF4	INT	8	2

Register Abbreviation	Reset	High-Speed/ Medium-Speed	Watch	Sleep	Sub-Active	Sub-Sleep	Module Stop	Software Standby	Hardware Standby	Module
TCONRO	Initialized							Initialized		Timer connection
STR_2	Initialized							Initialized	XBS	
TCONRS	Initialized							Initialized		Timer connection
SEDGR	Initialized							Initialized		

Notes: 1. Can be used on the H8S/2160B and H8S/2161B.
2. Not supported by the H8S/2148B and H8S/2145B (5-V version).

When the SCK0, SCK1, or SCK2 pin is used as an output, an external pull-up resistor must be connected in order to output high level.

5. When IICS = 0, ICE = 0, and KBIOE = 0. Low-level output when the bus drive function is selected is determined separately.
6. The upper limit of the port 6 applied voltage is V_{cc} + 0.3 V when CIN input is not selected, and the lower of V_{cc} + 0.3 V and AV_{cc} + 0.3 V when CIN input is selected. When a pin is in output mode, the output voltage is equivalent to the applied voltage.
7. The upper limit of the port A applied voltage is $V_{cc}B$ + 0.3 V when CIN input is not selected, and the lower of $V_{cc}B$ + 0.3 V and AV_{cc} + 0.3 V when CIN input is selected. When a pin is in output mode, the output voltage is equivalent to the applied voltage.
8. The port A characteristics depend on $V_{cc}B$, and the other pins characteristics depend on V_{cc}.

Item	Symbol	Value	Unit
Operating temperature (flash memory programming/erasing)	T_{opr}	Normal specification product: –20 to +75	°C
		Wide range temperature specification product: –40 to +85	
Storage temperature	T_{stg}	–55 to +125	°C

Caution: Permanent damage to the chip may result if absolute maximum ratings are exceeded.

Ensure that for 5-V/4-V version products, the input pin voltage does not exceed 7.0 V, and for 3-V version products, all the input voltage except for port A does not exceed 4.3 V.

Notes: 1. Voltage applied to the VCC1 pin. Since both the VCC1 pin and VCL pin are connected to the VCC power supply on low-power voltage (3-V) products, VCL ratings should not be exceeded.

2. Power supply voltage pin used for operation within the chip. Do not apply power supply voltage to the VCL pin on 5-V/4-V products. Be sure to insert an external capacitor between the VCL pin and GND to regulate the internal voltage.