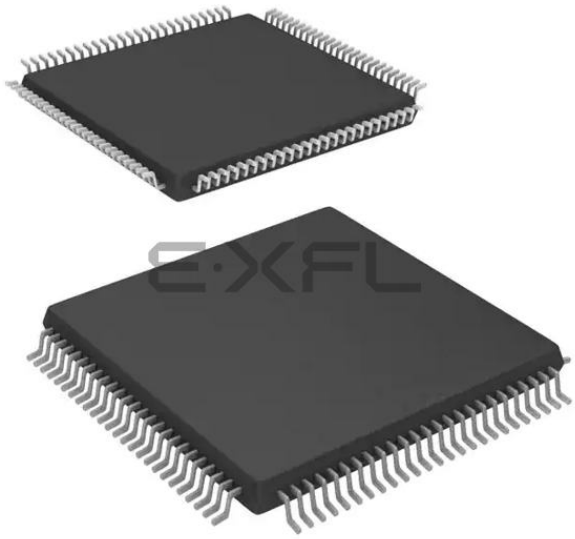

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	H8S/2000
Core Size	16-Bit
Speed	10MHz
Connectivity	Host Interface (LPC), I²C, IrDA, SCI, X-Bus
Peripherals	PWM, WDT
Number of I/O	74
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df2145bvte10v

General Precautions on Handling of Product

1. Treatment of NC Pins

Note: Do not connect anything to the NC pins.
The NC (not connected) pins are either not connected to any of the internal circuitry or are used as test pins or to reduce noise. If something is connected to the NC pins, the operation of the LSI is not guaranteed.

2. Treatment of Unused Input Pins

Note: Fix all unused input pins to high or low level.
Generally, the input pins of CMOS products are high-impedance input pins. If unused pins are in their open states, intermediate levels are induced by noise in the vicinity, a pass-through current flows internally, and a malfunction may occur.

3. Processing before Initialization

Note: When power is first supplied, the product's state is undefined.
The states of internal circuits are undefined until full power is supplied throughout the chip and a low level is input on the reset pin. During the period where the states are undefined, the register settings and the output state of each pin are also undefined. Design your system so that it does not malfunction because of processing while it is in this undefined state. For those products which have a reset function, reset the LSI immediately after the power supply has been turned on.

4. Prohibition of Access to Undefined or Reserved Addresses

Note: Access to undefined or reserved addresses is prohibited.
The undefined or reserved addresses may be used to expand functions, or test registers may have been be allocated to these addresses. Do not access these registers; the system's operation is not guaranteed if they are accessed.

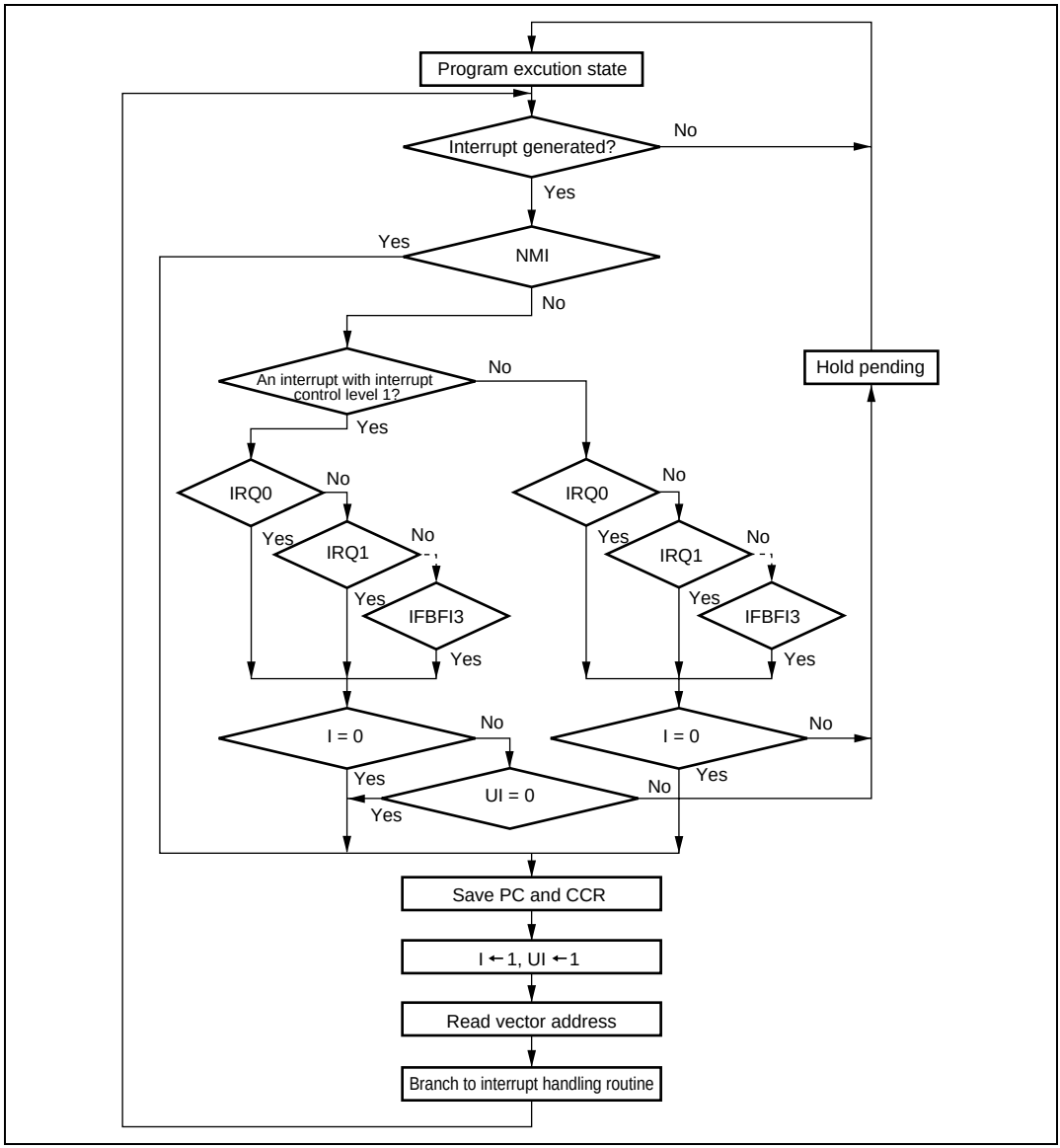


Figure 5.6 Flowchart of Procedure up to Interrupt Acceptance in Interrupt Control Mode 1

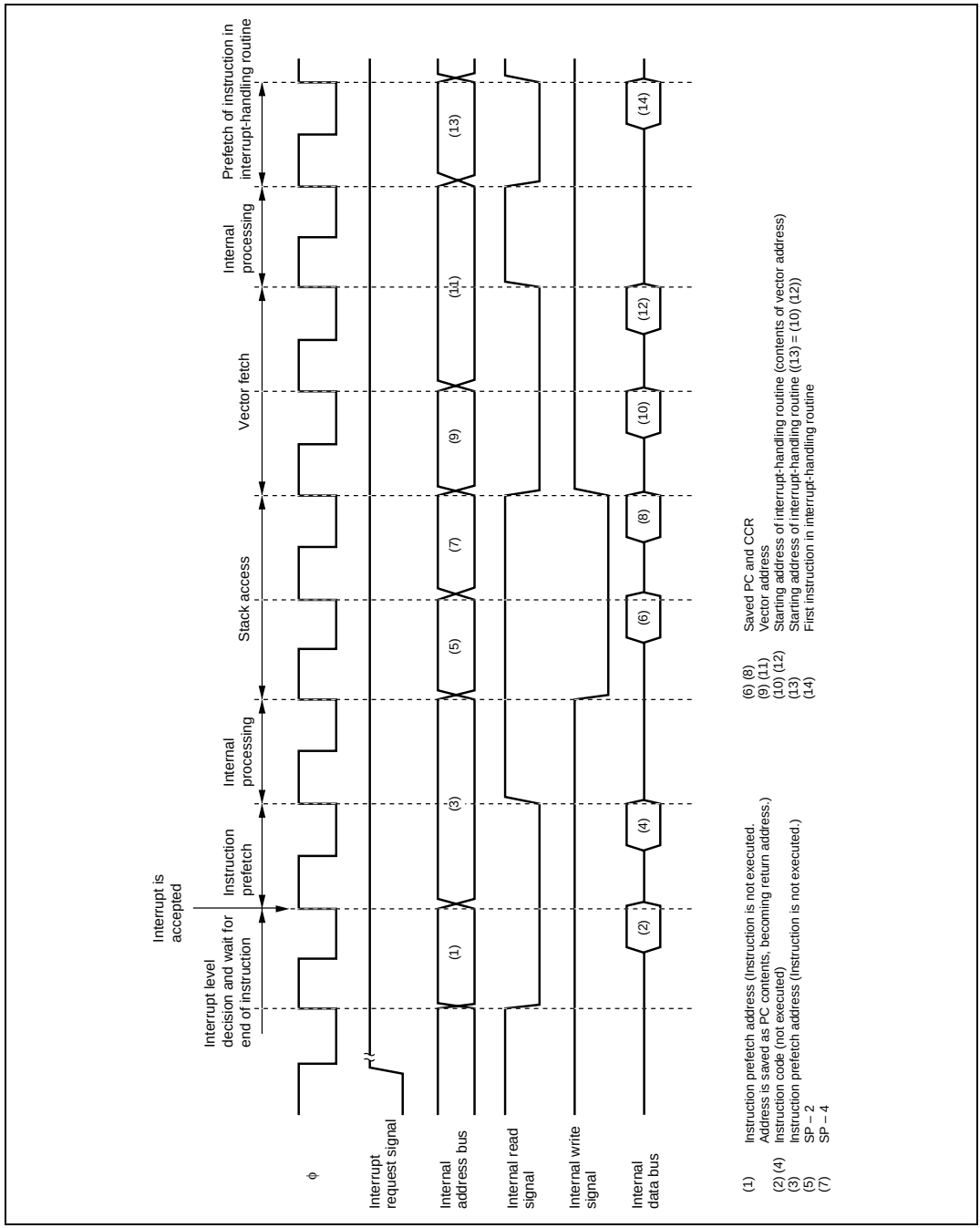


Figure 5.7 Interrupt Exception Handling

- P40/TMCI0/TxD2/IrTxD

  The pin function is switched as shown below according to the combination of the TE bit in SCR of SCI_2 and the P40DDR bit.

TE	0		1
P40DDR	0	1	—
Pin Function	P40 input pin	P40 output pin	TxD2/IrTxD output pin
	TMCI0 input pin*		

Note: * When an external clock is selected with bits CKS2 to CKS0 in TCR0 of TMR_0, this pin is used as the TMCI0 input pin.

8.6 Port 5

Port 5 is a 3-bit I/O port. Port 5 pins also function as SCI_0 I/O pins, and the IIC_0 I/O pin. P52 and SCK0 are NMOS push-pull outputs, and SCL0 is an NMOS open-drain output. Port 5 has the following registers.

- Port 5 data direction register (P5DDR)
- Port 5 data register (P5DR)

8.6.1 Port 5 Data Direction Register (P5DDR)

P5DDR specifies input or output for the pins of port 5 on a bit-by-bit basis.

Bit	Bit Name	Initial Value	R/W	Description
7 to 3	—	All 1	—	Reserved The initial value must not be changed.
2	P52DDR	0	W	The corresponding port 5 pins are output ports when P5DDR bits are set to 1, and input ports when cleared to 0. As SCI_0 is initialized in software standby mode, the pin states are determined by the IIC_0 ICCR, P5DDR, and P5DR specifications.
1	P51DDR	0	W	
0	P50DDR	0	W	

the additional pulses added to the basic pulses, and figure 9.2 shows an example of additional pulse timing.

Table 9.5 Position of Pulses Added to Basic Pulses

Lower 4 Bits	Basic Pulse No.															
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0000																
0001																Yes
0010								Yes								Yes
0011								Yes				Yes				Yes
0100				Yes				Yes				Yes				Yes
0101				Yes				Yes				Yes		Yes		Yes
0110				Yes		Yes		Yes				Yes		Yes		Yes
0111				Yes		Yes		Yes		Yes		Yes		Yes		Yes
1000		Yes		Yes		Yes		Yes		Yes		Yes		Yes		Yes
1001		Yes		Yes		Yes		Yes		Yes		Yes		Yes	Yes	Yes
1010		Yes		Yes		Yes	Yes	Yes		Yes		Yes		Yes	Yes	Yes
1011		Yes		Yes		Yes	Yes	Yes		Yes	Yes	Yes		Yes	Yes	Yes
1100		Yes	Yes	Yes		Yes	Yes	Yes		Yes	Yes	Yes		Yes	Yes	Yes
1101		Yes	Yes	Yes		Yes	Yes	Yes		Yes	Yes	Yes	Yes	Yes	Yes	Yes
1110		Yes	Yes	Yes	Yes	Yes	Yes	Yes		Yes	Yes	Yes	Yes	Yes	Yes	Yes
1111		Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes

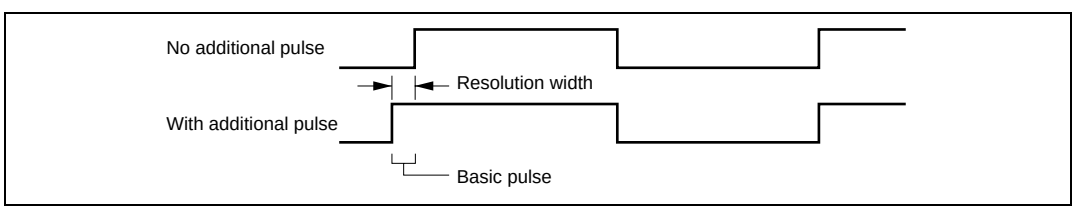


Figure 9.2 Example of Additional Pulse Timing (when Upper 4 Bits of PWDR = 1000)

12.5.6 Timing of Overflow Flag (OVF) Setting

The OVF bit in TCSR is set to 1 when the TCNT overflows (changes from H'FF to H'00). Figure 12.10 shows the timing of OVF flag setting.

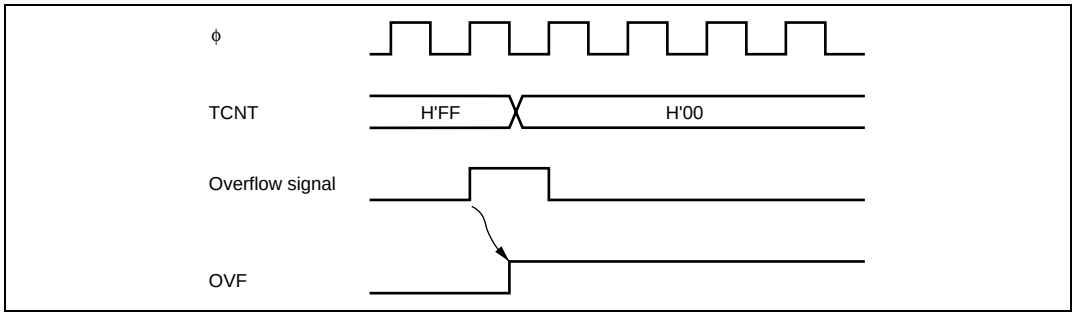


Figure 12.10 Timing of OVF Flag Setting

12.6 Operation with Cascaded Connection

If bits CKS2 to CKS0 in either TCR_0 or TCR_1 are set to B'100, the 8-bit timers of the two channels are cascaded. With this configuration, a single 16-bit timer can be used (16-bit count mode) or the compare-matches of the 8-bit timer of channel 0 can be counted by the 8-bit timer of channel 1 (compare-match count mode).

12.6.1 16-Bit Count Mode

When bits CKS2 to CKS0 in TCR_0 are set to B'100, the timer functions as a single 16-bit timer with channel 0 occupying the upper 8 bits and channel 1 occupying the lower 8 bits.

Setting of Compare-Match Flags:

- The CMF flag in TCSR_0 is set to 1 when a 16-bit compare-match occurs.
- The CMF flag in TCSR_1 is set to 1 when a lower 8-bit compare-match occurs.

13.4 Operation

13.4.1 PWM Decoding (PDC Signal Generation)

The timer connection facility and TMR_X can be used to decode a PWM signal in which 0 and 1 are represented by the pulse width. To do this, a signal in which a rising edge is generated at regular intervals must be selected as the IHI signal.

The timer counter (TCNT) in TMR_X is set to count the internal clock pulses and to be cleared on the rising edge of the external reset signal (IHI signal). The value to be used as the threshold for deciding the pulse width is written in TCORB. The PWM decoder contains a delay latch which uses the IHI signal as data and compare-match signal B (CMB) as a clock, and the state of the IHI signal (the result of the pulse width decision) at the first compare-match signal B timing after TCNT is reset by the rise of the IHI signal is output as the PDC signal.

The pulse width setting using TICRR and TICRF of TMR_X can be used to determine the pulse width decision threshold. Examples of TCR and TCORB settings of TMR_X are shown in tables 13.4 and 13.5, and the PWM decoding timing chart is shown in figure 13.2.

Table 13.4 Examples of TCR Settings

Bit	Abbreviation	Contents	Description
7	CMIEB	0	Interrupts due to compare-match and overflow are disabled
6	CMIEA	0	
5	OVIE	0	
4 and 3	CCLR1 and CCLR0	11	TCNT is cleared by the rising edge of the external reset signal (IHI signal)
2 to 0	CKS2 to CKS0	001	Incremented on internal clock (φ)

Table 13.5 Examples of TCORB (Pulse Width Threshold) Settings

	φ: 10 MHz	φ: 12 MHz	φ: 16 MHz	φ: 20 MHz
H'07	0.8 µs	0.67 µs	0.5 µs	0.4 µs
H'0F	1.6 µs	1.33 µs	1 µs	0.8 µs
H'1F	3.2 µs	2.67 µs	2 µs	1.6 µs
H'3F	6.4 µs	5.33 µs	4 µs	3.2 µs
H'7F	12.8 µs	10.67 µs	8 µs	6.4 µs

Section 14 Watchdog Timer (WDT)

This LSI incorporates two watchdog timer channels (WDT_0 and WDT_1). The watchdog timer can generate an internal reset signal or an internal NMI interrupt signal if a system crash prevents the CPU from writing to the timer counter, thus allowing it to overflow. Simultaneously, it can output an overflow signal ($\overline{\text{RESO}}$) externally.

When this watchdog function is not needed, the WDT can be used as an interval timer. In interval timer operation, an interval timer interrupt is generated each time the counter overflows. A block diagram of the WDT_0 and WDT_1 is shown in figure 14.1.

14.1 Features

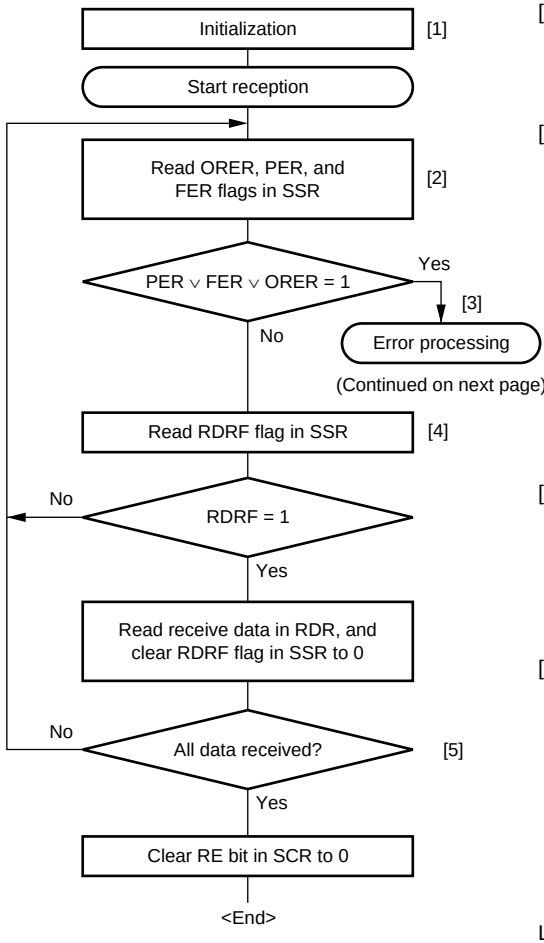
- Selectable from eight (WDT_0) or 16 (WDT_1) counter input clocks.
- Switchable between watchdog timer mode and interval timer mode

Watchdog Timer Mode:

- If the counter overflows, an internal reset or an internal NMI interrupt is generated.
- When the LSI is selected to be internally reset at counter overflow, a low level signal is output from the $\overline{\text{RESO}}$ pin if the counter overflows.

Internal Timer Mode:

- If the counter overflows, an internal timer interrupt (WOVI) is generated.



[1] SCI initialization:
The RxD pin is automatically designated as the receive data input pin.

[2] [3] Receive error processing and break detection:
If a receive error occurs, read the ORER, PER, and FER flags in SSR to identify the error. After performing the appropriate error processing, ensure that the ORER, PER, and FER flags are all cleared to 0. Reception cannot be resumed if any of these flags are set to 1. In the case of a framing error, a break can be detected by reading the value of the input port corresponding to the RxD pin.

[4] SCI status check and receive data read:
Read SSR and check that RDRF = 1, then read the receive data in RDR and clear the RDRF flag to 0. Transition of the RDRF flag from 0 to 1 can also be identified by an RXI interrupt.

[5] Serial reception continuation procedure:
To continue serial reception, before the stop bit for the current frame is received, read the RDRF flag, read RDR, and clear the RDRF flag to 0. However, the RDRF flag is cleared automatically when the DTC is initiated by an RXI interrupt and reads data from RDR.

Legend:
∨ : Logical OR

Figure 15.9 Sample Serial Reception Flowchart (1)

Section 16 I²C Bus Interface (IIC) (Optional)

The I²C bus interface is provided as an optional function. Note the following point when using this optional function.

- Although the product type name is identical, please contact Renesas before using this optional function on an F-ZTAT version product.

This LSI has a two-channel I²C bus interface. The I²C bus interface conforms to and provides a subset of the Philips I²C bus (inter-IC bus) interface functions. The register configuration that controls the I²C bus differs partly from the Philips configuration, however.

16.1 Features

- Selection of addressing format or non-addressing format
  - I²C bus format: addressing format with an acknowledge bit, for master/slave operation
  - Clocked synchronous serial format: non-addressing format without an acknowledge bit, for master operation only
  - Formatless (for IIC_0 only): non-addressing format with a clock pin dedicated for formatless; for slave operation only
- Conforms to Philips I²C bus interface (I²C bus format)
- Two ways of setting slave address (I²C bus format)
- Start and stop conditions generated automatically in master mode (I²C bus format)
- Selection of the acknowledge output level in reception (I²C bus format)
- Automatic loading of an acknowledge bit in transmission (I²C bus format)
- Wait function in master mode (I²C bus format)
  - A wait can be inserted by driving the SCL pin low after data transfer, excluding acknowledgement.
  - The wait can be cleared by clearing the interrupt flag.
- Wait function (I²C bus format)
  - A wait request can be generated by driving the SCL pin low after data transfer.
  - The wait request is cleared when the next transfer becomes possible.
- Interrupt sources
  - Data transfer end (including when a transition to transmit mode with I²C bus format occurs, when ICDR data is transferred, or during a wait state)

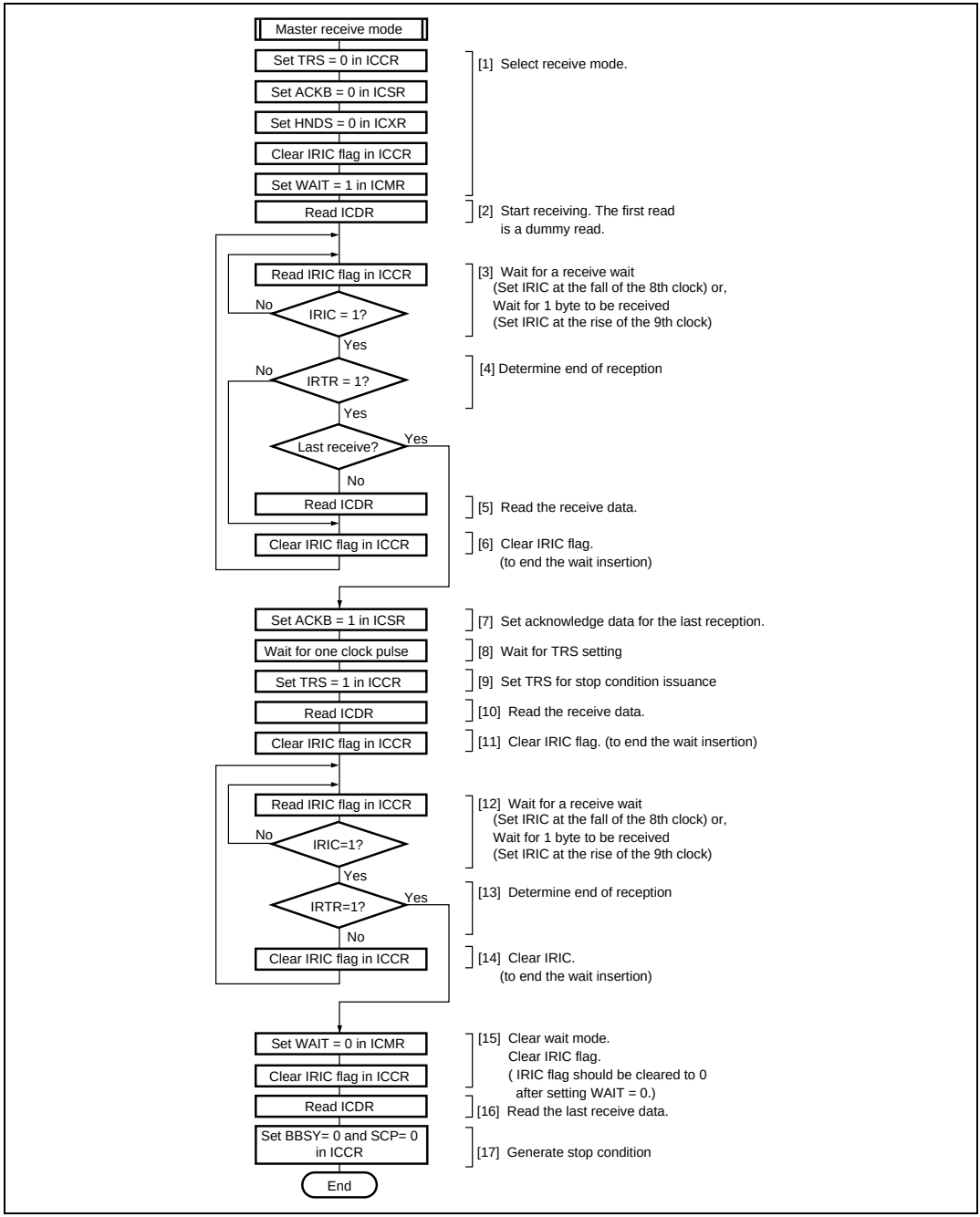


Figure 16.14 Sample Flowchart for Operations in Master Receive Mode (Receiving Multiple Bytes) (WAIT = 1)

19.4.3 A20 Gate

The A20 gate signal can mask address A20 to emulate an addressing mode used by personal computers with an 8086*-family CPU. A regular-speed A20 gate signal can be output under firmware control. The fast A20 gate function that is speeded up by hardware is enabled by setting the FGA20E bit to 1 in HICR0.

Note: An Intel microprocessor

Regular A20 Gate Operation: Output of the A20 gate signal can be controlled by an H'D1 command followed by data. When the slave processor (this LSI) receives data, it normally uses an interrupt routine activated by the IBF1 interrupt to read IDR1. At this time, firmware copies bit 1 of data following an H'D1 command and outputs it at the gate A20 pin.

Fast A20 Gate Operation: The internal state of GA20 output is initialized to 1 when FGA20E = 0. When the FGA20E bit is set to 1, P81/GA20 is used for output of a fast A20 gate signal. The state of the P81/GA20 pin can be monitored by reading the GA20 bit in HICR2.

The initial output from this pin will be a logic 1, which is the initial value. Afterward, the host processor can manipulate the output from this pin by sending commands and data. This function is only available via the IDR1 register. The host interface decodes commands input from the host. When an H'D1 host command is detected, bit 1 of the data following the host command is output from the GA20 output pin. This operation does not depend on firmware or interrupts, and is faster than the regular processing using interrupts. Table 19.3 shows the conditions that set and clear GA20 (P81). Figure 19.4 shows the GA20 output in flowchart form. Table 19.4 indicates the GA20 output signal values.

Table 19.3 GA20 (P81) Set/Clear Timing

Pin Name	Setting Condition	Clearing Condition
GA20 (P81)	When bit 1 of the data that follows an H'D1 host command is 1	When bit 1 of the data that follows an H'D1 host command is 0

- MSTPCRL

Bit	Bit Name	Initial Value	R/W	Corresponding Module
7	MSTP7	1	R/W	Serial communication interface_0 (SCI_0)
6	MSTP6	1	R/W	Serial communication interface_1 (SCI_1)
5	MSTP5	1	R/W	Serial communication interface_2 (SCI_2)
4	MSTP4	1	R/W	I^2C bus interface_0 (IIC_0)
3	MSTP3	1	R/W	I^2C bus interface_1 (IIC_1)
2	MSTP2	1	R/W	Host interface (XBS), keyboard buffer controller, keyboard matrix interrupt mask register (KMIMR), keyboard matrix interrupt mask register A (KMIMRA), port 6 pull-up MOS control register (KMPCR)
1	MSTP1	1*	R/W	—
0	MSTP0	1	R/W	Host interface (LPC), wake-up event interrupt mask register B (WUEMRB)

Note: * This bit can be read from or written to, however, operation is not affected.

25.2 Mode Transitions and LSI States

Figure 25.1 shows the enabled mode transition diagram. The mode transition from program execution state to program halt state is performed by the SLEEP instruction. The mode transition from program halt state to program execution state is performed by an interrupt. The $\overline{\text{STBY}}$ input causes a mode transition from any state to hardware standby mode. The $\overline{\text{RES}}$ input causes a mode transition from a state other than hardware standby mode to the reset state. Table 25.2 shows the LSI internal states in each operating mode.

Register Name	Abbreviation	Number of Bits	Address	Module	Data Bus Width	Number of Access States
Serial status register_2	SSR_2	8	H'FFA4	SCI_2	8	2
Receive data register_2	RDR_2	8	H'FFA5	SCI_2	8	2
Smart card mode register_2	SCMR_2	8	H'FFA6	SCI_2	8	2
PWM (D/A) counter H	DACNTH	8	H'FFA6	PWMX	8	2
PWM (D/A) data register BH	DADRBH	8	H'FFA6	PWMX	8	2
PWM (D/A) counter L	DACNTL	8	H'FFA7	PWMX	8	2
PWM (D/A) data register BL	DADRBL	8	H'FFA7	PWMX	8	2
Timer control/status register_0	TCSR_0	8	H'FFA8	WDT	8	2
Timer counter_0	TCNT_0	8	H'FFA8 (write)	WDT_0	8	2
Timer counter_0	TCNT_0	8	H'FFA9 (read)	WDT_0	8	2
Port A output data register	PAODR	8	H'FFAA	PORT	8	2
Port A input data register	PAPIN	8	H'FFAB	PORT	8	2
Port A data direction register	PADDR	8	H'FFAB	PORT	8	2
Port 1 pull-up MOS control register	P1PCR	8	H'FFAC	PORT	8	2
Port 2 pull-up MOS control register	P2PCR	8	H'FFAD	PORT	8	2
Port 3 pull-up MOS control register	P3PCR	8	H'FFAE	PORT	8	2
Port 1 data direction register	P1DDR	8	H'FFB0	PORT	8	2
Port 2 data direction register	P2DDR	8	H'FFB1	PORT	8	2
Port 1 data register	P1DR	8	H'FFB2	PORT	8	2
Port 2 data register	P2DR	8	H'FFB3	PORT	8	2
Port 3 data direction register	P3DDR	8	H'FFB4	PORT	8	2
Port 4 data direction register	P4DDR	8	H'FFB5	PORT	8	2
Port 3 data register	P3DR	8	H'FFB6	PORT	8	2
Port 4 data register	P4DR	8	H'FFB7	PORT	8	2
Port 5 data direction register	P5DDR	8	H'FFB8	PORT	8	2
Port 6 data direction register	P6DDR	8	H'FFB9	PORT	8	2
Port 5 data register	P5DR	8	H'FFBA	PORT	8	2

Port Name Pin Name	MCU Operating Mode	Reset	Hardware Standby Mode	Software Standby Mode	Watch Mode	Sleep Mode	Sub-sleep Mode	Subactive Mode	Program Execution State
Port 96 φ EXCL	1	Clock output	T	[DDR = 1] H [DDR = 0] T	EXCL input	[DDR = 1] clock output [DDR = 0] T	EXCL input	EXCL input	Clock output/ EXCL input/ input port
	2, 3 (EXPE = 1)	T							
	2, 3 (EXPE = 0)								
Ports 95 to 93 $\overline{AS}$, $\overline{HWR}$, $\overline{RD}$	1	H	T	H	H	H	H	$\overline{AS}$, $\overline{HWR}$, $\overline{RD}$	$\overline{AS}$, $\overline{HWR}$, $\overline{RD}$
	2, 3 (EXPE = 1)	T							
	2, 3 (EXPE = 0)			kept	kept	kept	kept	I/O port	I/O port
Ports 92, 91	1	T	T	kept	kept	kept	kept	I/O port	I/O port
	2, 3 (EXPE = 1)								
	2, 3 (EXPE = 0)								
Port 90 $\overline{LWR}$	1	T	T	H/kept	H/kept	H/kept	H/kept	$\overline{LWR}$/ I/O port	$\overline{LWR}$/ I/O port
	2, 3 (EXPE = 1)								
	2, 3 (EXPE = 0)			kept	kept	kept	kept	I/O port	I/O port
Port A A23 to A16	1	T	T	kept*	kept*	kept*	kept*	I/O port	I/O port
	2, 3 (EXPE = 1)							A23 to A16/ I/O port	A23 to A16/ I/O port
	2, 3 (EXPE = 0)							I/O port	I/O port
Port B D7 to D0	1	T	T	T/kept	T/kept	T/kept	T/kept	D7 to D0/ I/O port	D7 to D0/ I/O port
	2, 3 (EXPE = 1)								
	2, 3 (EXPE = 0)			kept	kept	kept	kept	I/O port	I/O port
Ports C to G (H8S/2160B, H8S/2161B)	1	T	T	kept	kept	kept	kept	I/O port	I/O port
	2, 3 (EXPE = 1)								
	2, 3 (EXPE = 0)								

Legend:

H: High

L: Low

T: High-impedance state

kept: Input ports are in the high-impedance state (when DDR = 0 and PCR = 1, input pull-up MOSs remain on).

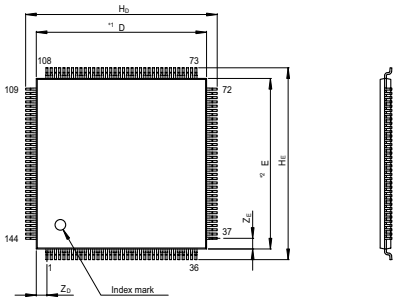
Output ports maintain their previous state.

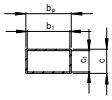
Depending on the pins, the on-chip peripheral modules may be initialized and the I/O port function determined by DDR and DR used.

DDR: Data direction register

Note: * In the case of address output, the last address accessed is retained.

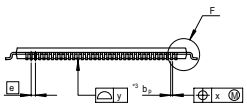
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-TQFP144-16x16-0.40	PTQP0144LC-A	TFP-144/TFP-144V	0.6g

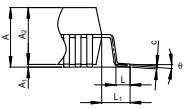




Terminal cross section

NOTE)
1. DIMENSIONS"*1"AND"*2" DO NOT INCLUDE MOLD FLASH
2. DIMENSION"*3"DOES NOT INCLUDE TRIM OFFSET.





Detail F

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	16	—
E	—	16	—
A_2	—	1.00	—
H_D	17.8	18.0	18.2
H_E	17.8	18.0	18.2
A	—	—	1.20
A_1	0.05	0.10	0.15
b_p	0.13	0.18	0.23
b_1	—	0.16	—
c	0.12	0.17	0.22
c_1	—	0.15	—
θ	0°	—	8°
e	—	0.4	—
x	—	—	0.07
y	—	—	0.08
Z_D	—	1.0	—
Z_E	—	1.0	—
L	0.4	0.5	0.6
L_1	—	1.0	—

Figure C.3 Package Dimensions (TFP-144)

Renesas Technology Corp. Sales Strategic Planning Div. Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan

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