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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	H8S/2000
Core Size	16-Bit
Speed	10MHz
Connectivity	Host Interface (LPC), I²C, IrDA, SCI, X-Bus
Peripherals	PWM, WDT
Number of I/O	114
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	144-TQFP
Supplier Device Package	144-TQFP (16x16)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df2161bvt10v

Section 25 Power-Down Modes

Section 27 Electrical Characteristics

Tables

1.3.2 Pin Functions in Each Operating Mode

Table 1.1 Pin Functions of H8S/2140B, H8S/2141B, H8S/2145B, and H8S/2148B in Each Operating Mode

Pin No.	Pin Name			
	Extended Modes		Single-Chip Modes	Flash Memory Programmer Mode
FP-100B TFP-100B	Mode 1	Mode 2, Mode 3 (EXPE = 1)	Mode 2, Mode 3 (EXPE = 0)	
1	$\overline{RES}$	$\overline{RES}$	$\overline{RES}$	$\overline{RES}$
2	XTAL	XTAL	XTAL	XTAL
3	EXTAL	EXTAL	EXTAL	EXTAL
4	VCCB	VCCB	VCCB	VCC
5	MD1	MD1	MD1	VSS
6	MD0	MD0	MD0	VSS
7	NMI	NMI	NMI	FA9
8	$\overline{STBY}$	$\overline{STBY}$	$\overline{STBY}$	VCC
9	VCL	VCL	VCL	VCC
10 (B)	PA7/CIN15/$\overline{KIN15}$/ PS2CD	PA7/A23/CIN15/ $\overline{KIN15}$/PS2CD	PA7/CIN15/$\overline{KIN15}$/ PS2CD	NC
11 (B)	PA6/CIN14/$\overline{KIN14}$/ PS2CC	PA6/A22/CIN14/ $\overline{KIN14}$/PS2CC	PA6/CIN14/$\overline{KIN14}$/ PS2CC	NC
12 (N)	P52/SCK0/SCL0	P52/SCK0/SCL0	P52/SCK0/SCL0	NC
13	P51/RxD0	P51/RxD0	P51/RxD0	FA17
14	P50/TxD0	P50/TxD0	P50/TxD0	NC
15	VSS	VSS	VSS	VSS
16 (N)	P97/$\overline{WAIT}$/SDA0	P97/$\overline{WAIT}$/SDA0	P97/SDA0	VCC
17	P96/ϕ/EXCL	P96/ϕ/EXCL	P96/ϕ/EXCL	NC
18	$\overline{AS}$/$\overline{IOS}$	$\overline{AS}$/$\overline{IOS}$	P95/$\overline{CS1}$	FA16
19	$\overline{HWR}$	$\overline{HWR}$	P94/$\overline{IOW}$	FA15
20 (B)	PA5/CIN13/$\overline{KIN13}$/ PS2BD	PA5/A21/CIN13/ $\overline{KIN13}$/PS2BD	PA5/CIN13/$\overline{KIN13}$/ PS2BD	NC
21 (B)	PA4/CIN12/$\overline{KIN12}$/ PS2BC	PA4/A20/CIN12/ $\overline{KIN12}$/PS2BC	PA4/CIN12/$\overline{KIN12}$/ PS2BC	NC

Section 3 MCU Operating Modes

3.1 MCU Operating Mode Selection

This LSI has three operating modes (modes 1 to 3). The operating mode is determined by the setting of the mode pins (MD1 and MD0). Table 3.1 shows the MCU operating mode selection.

Table 3.1 lists the MCU operating modes.

Table 3.1 MCU Operating Mode Selection

MCU Operating Mode	MD1	MD0	CPU Operating Mode	Description	On-Chip ROM
0	0	0	—	—	—
1		1	Normal	Expanded mode with on-chip ROM disabled	Disabled
2	1	0	Advanced	Expanded mode with on-chip ROM enabled	Enabled
				Single-chip mode	
3		1	Normal	Expanded mode with on-chip ROM enabled	
				Single-chip mode	

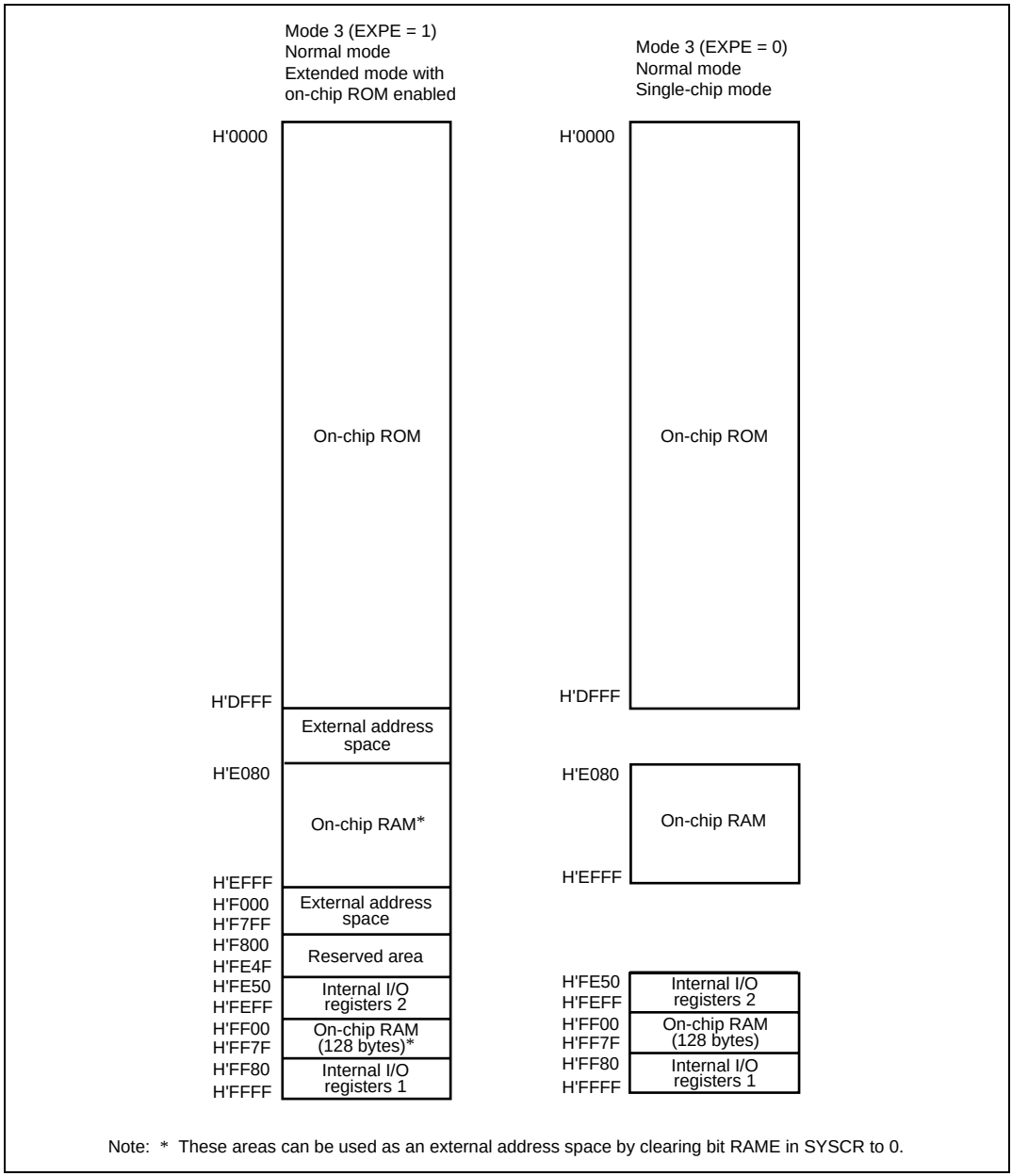
Mode 1 is an expanded mode that allows access to external memory and peripheral devices. With modes 2 and 3, operation begins in single-chip mode after reset release, but a transition can be made to external expansion mode by setting the EXPE bit in MDCR to 1.

Mode 0 cannot be used in this LSI. Thus, mode pins should be set to enable mode 1, 2 or 3 in normal program execution state. Mode pins should not be changed during operation.

3.2 Register Descriptions

The following registers are related to the operating mode. For details on the bus control register (BCR), refer to section 6.3.1, Bus Control Register (BCR).

- Mode control register (MDCR)
- System control register (SYSCR)
- Serial timer control register (STCR)



Note: * These areas can be used as an external address space by clearing bit RAME in SYSCR to 0.

Figure 3.10 Address Map for H8S/2148B (2)

8.4 Port 3

Port 3 is an 8-bit I/O port. Port 3 pins also function as a bidirectional data bus, XBS bidirectional data bus, and LPC input/output pins. Port 3 functions change according to the operating mode. Port 3 has the following registers.

- Port 3 data direction register (P3DDR)
- Port 3 data register (P3DR)
- Port 3 pull-up MOS control register (P3PCR)

8.4.1 Port 3 Data Direction Register (P3DDR)

P3DDR specifies input or output for the pins of port 3 on a bit-by-bit basis.

Bit	Bit Name	Initial Value	R/W	Description
7	P37DDR	0	W	Modes 1, 2, and 3 (EXPE = 1) The input/output direction specified by P3DDR is ignored, and pins automatically function as data I/O pins. Modes 2 and 3 (EXPE = 0) The corresponding port 3 pins are output ports when P3DDR bits are set to 1, and input ports when cleared to 0.
6	P36DDR	0	W	
5	P35DDR	0	W	
4	P34DDR	0	W	
3	P33DDR	0	W	
2	P32DDR	0	W	
1	P31DDR	0	W	
0	P30DDR	0	W	

- P80/HA0/$\overline{\text{PME}}$*3

  The pin function is switched as shown below according to the combination of the HI12E bit in SYSCR2, the PMEE bit in HICR0, and the P80DDR bit.

PMEE	0			1
HI12E	0		1	0*1
P80DDR	0	1	—	0*1
Pin Function	P80 input pin	P80 output pin	HA0 input pin*2	$\overline{\text{PME}}$ output pin
	$\overline{\text{PME}}$ input pin*2*3			

Notes: 1. When bit PMEE is set to 1 in HICR0, bits HI12E and P80DDR should be cleared to 0.
2. The HA0 input pin can only be used in mode 2 or 3 (EXPE = 0).
3. Not supported by the H8S/2148B and H8S/2145B (5-V version).

8.10 Port 9

Port 9 is an 8-bit I/O port. Port 9 pins also function as external interrupt input pins, the A/D converter input pin, host interface (XBS) input pins, the IIC_0 I/O pin, the subclock input pin, bus control signal I/O pins, and the system clock (ϕ) output pin. P97 is an NMOS push-pull output. SDA0 is an NMOS open-drain output, and has direct bus drive capability. Port 9 has the following registers.

- Port 9 data direction register (P9DDR)
- Port 9 data register (P9DR)

8.10.2 Port 9 Data Register (P9DR)

P9DR stores output data for the port 9 pins.

Bit	Bit Name	Initial Value	R/W	Description
7	P97DR	0	R/W	With the exception of P96, if a port 9 read is performed while P9DDR bits are set to 1, the P9DR values are read directly, regardless of the actual pin states. If a port 9 read is performed while P9DDR bits are cleared to 0, the pin states are read. For P96, the pin state is always read.
6	P96DR	Undefined*	R	
5	P95DR	0	R/W	
4	P94DR	0	R/W	
3	P93DR	0	R/W	
2	P92DR	0	R/W	
1	P91DR	0	R/W	
0	P90DR	0	R/W	

Note: * The initial value of bit 6 is determined according to the P96 pin state.

8.10.3 Pin Functions

- P97/$\overline{\text{WAIT}}$/SDA0

  The pin function is switched as shown below according to the combination of operating mode, the WMS1 bit in WSCR, the ICE bit in ICCR of IIC_0, and the P97DDR bit.

Operating Mode	Modes 1, 2, 3 (EXPE = 1)				Modes 2, 3 (EXPE = 0)		
WMS1	0			1	—		
ICE	0		1	—	0		1
P97DDR	0	1	—	—	0	1	—
Pin Function	P97 input pin	P97 output pin	SDA0 I/O pin	$\overline{\text{WAIT}}$ input pin	P97 input pin	P97 output pin	SDA0 I/O pin

Note: When this pin is set as the P97 output pin, it is an NMOS push-pull output. SDA0 is an NMOS open-drain output, and has direct bus drive capability.

11.7 Usage Notes

11.7.1 Conflict between FRC Write and Clear

If an internal counter clear signal is generated during the state after an FRC write cycle, the clear signal takes priority and the write is not performed. Figure 11.17 shows the timing for this type of conflict.

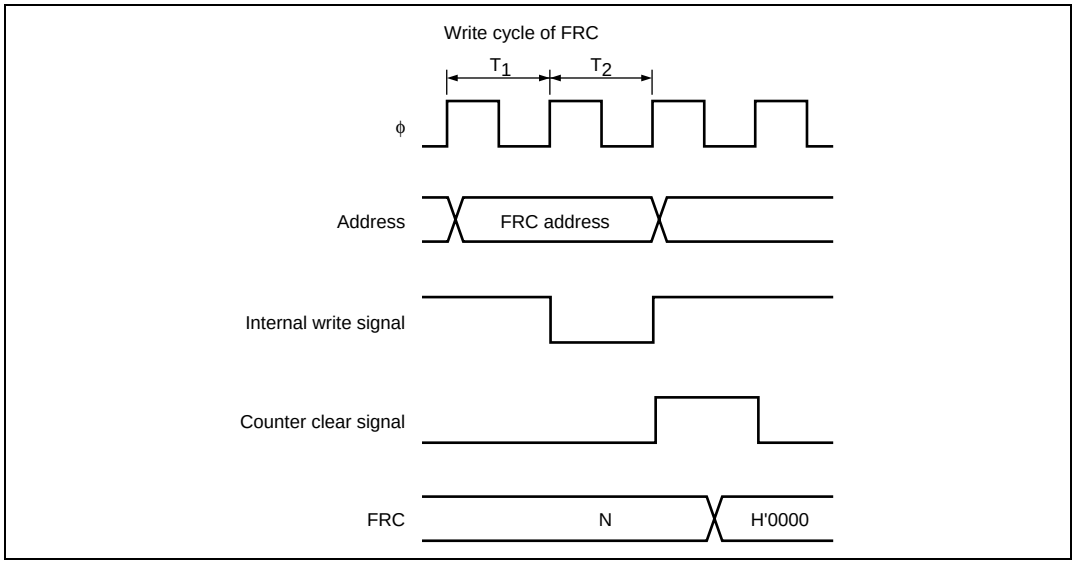


Figure 11.17 FRC Write-Clear Conflict

15.3.10 Keyboard Comparator Control Register (KBCOMP)

KBCOMP selects the functions of the SCI and A/D converter.

Bit	Bit Name	Initial Value	R/W	Description
7	IrE	0	R/W	IrDA Enable Specifies SCI_2 I/O pins for either normal SCI or IrDA. 0: TxD2/IrTxD and RxD2/IrRxD pins function as TxD2 and RxD2 pins, respectively 1: TxD2/IrTxD and RxD2/IrRxD pins function as IrTxD and IrRxD pins, respectively
6	IrCKS2	0	R/W	IrDA Clock Select 2 to 0 These bits specify the high-level width of the clock pulse during IrTxD output pulse encoding when the IrDA function is enabled. 000: B × 3/16 (B: Bit rate) 001: φ/2 010: φ/4 011: φ/8 100: φ/16 101: φ/32 110: φ/64 111: φ/128
5	IrCKS1	0	R/W	
4	IrCKS0	0	R/W	
3	KBADE	0	R/W	Bits related to the A/D converter For details, refer to section 21.3.4, Keyboard Comparator Control Register (KBCOMP).
2	KBCH2	0	R/W	
1	KBCH1	0	R/W	
0	KBCH0	0	R/W	

Bit	Bit Name	Initial Value	R/W	Description
3	AL	0	R/(W)*	Arbitration Lost Flag Indicates that arbitration was lost in master mode. [Setting conditions] When ALSL = 0 • If the internal SDA and SDA pin disagree at the rise of SCL in master transmit mode • If the internal SCL line is high at the fall of SCL in master transmit mode When ALSL = 1 • If the internal SDA and SDA pin disagree at the rise of SCL in master transmit mode • If the SDA pin is driven low by another device before the I²C bus interface drives the SDA pin low, after the start condition instruction was executed in master transmit mode [Clearing conditions] • When ICDR is written to (transmit mode) or read from (receive mode) • When 0 is written in AL after reading AL = 1
2	AAS	0	R/(W)*	Slave Address Recognition Flag In I²C bus format slave receive mode, this flag is set to 1 if the first frame following a start condition matches bits SVA6 to SVA0 in SAR, or if the general call address (H'00) is detected. [Setting condition] When the slave address or general call address (one frame including a R/$\overline{W}$ bit is H'00) is detected in slave receive mode and FS = 0 in SAR [Clearing conditions] • When ICDR is written to (transmit mode) or read from (receive mode) • When 0 is written in AAS after reading AAS = 1 • In master mode

Table 16.11 I²C Bus Timing (with Maximum Influence of t_{Sr}/t_{Sf})

Item	t_{cyc} Indication		Time Indication (at Maximum Transfer Rate) [ns]						
			t_{Sr}/t_{Sf} Influence (Max.)	I²C Bus Specification (Min.)	ϕ = 5 MHz	ϕ = 8 MHz	ϕ = 10 MHz	ϕ = 16 MHz	ϕ = 20 MHz
t_{SCLHO}	0.5 t_{SCLO} ($-t_{Sr}$)	Standard mode	–1000	4000	4000	4000	4000	4000	4000
		High-speed mode	–300	600	950	950	950	950	950
t_{SCLLO}	0.5 t_{SCLO} ($-t_{Sf}$)	Standard mode	–250	4700	4750	4750	4750	4750	4750
		High-speed mode	–250	1300	1000*1	1000*1	1000*1	1000*1	1000*1
t_{BUFO}	0.5 t_{SCLO} –1 t_{cyc} ($-t_{Sr}$)	Standard mode	–1000	4700	3800*1	3875*1	3900*1	3938*1	3950*1
		High-speed mode	–300	1300	750*1	825*1	850*1	888*1	900*1
t_{STAHO}	0.5 t_{SCLO} –1 t_{cyc} ($-t_{Sf}$)	Standard mode	–250	4000	4550	4625	4650	4688	4700
		High-speed mode	–250	600	800	875	900	938	950
t_{STASO}	1 t_{SCLO} ($-t_{Sr}$)	Standard mode	–1000	4700	9000	9000	9000	9000	9000
		High-speed mode	–300	600	2200	2200	2200	2200	2200
t_{STOSO}	0.5 t_{SCLO} + 2 t_{cyc} ($-t_{Sr}$)	Standard mode	–1000	4000	4400	4250	4200	4125	4100
		High-speed mode	–300	600	1350	1200	1150	1075	1050
t_{SDASO} (master)	1 t_{SCLLO}*3 –3 t_{cyc} ($-t_{Sr}$)	Standard mode	–1000	250	3100	3325	3400	3513	3550
		High-speed mode	–300	100	400	625	700	813	850
t_{SDASO} (slave)	1 t_{SCLL}*3 –12 t_{cyc}*2 ($-t_{Sr}$)	Standard mode	–1000	250	1300	2200	2500	2950	3100
		High-speed mode	–300	100	–1400*1	–500*1	–200*1	250	400
t_{SDAHO}	3 t_{cyc}	Standard mode	0	0	600	375	300	188	150
		High-speed mode	0	0	600	375	300	188	150

Notes: 1. Does not meet the I²C bus interface specification. Remedial action such as the following is necessary: (a) secure a start/stop condition issuance interval; (b) adjust the rise and fall times by means of a pull-up resistor and capacitive load; (c) reduce the transfer rate; (d) select slave devices whose input timing permits this output timing.

The values in the above table will vary depending on the settings of the IICX bit and bits CKS0 to CKS2. Depending on the frequency it may not be possible to achieve the maximum transfer rate; therefore, whether or not the I²C bus interface specifications are met must be determined in accordance with the actual setting conditions.

2. Value when the IICX bit is set to 1. When the IICX bit is cleared to 0, the value is ($t_{SCLL} - 6t_{cyc}$).
3. Calculated using the I²C bus specification values (standard mode: 4700 ns min.; high-speed mode: 1300 ns min.).

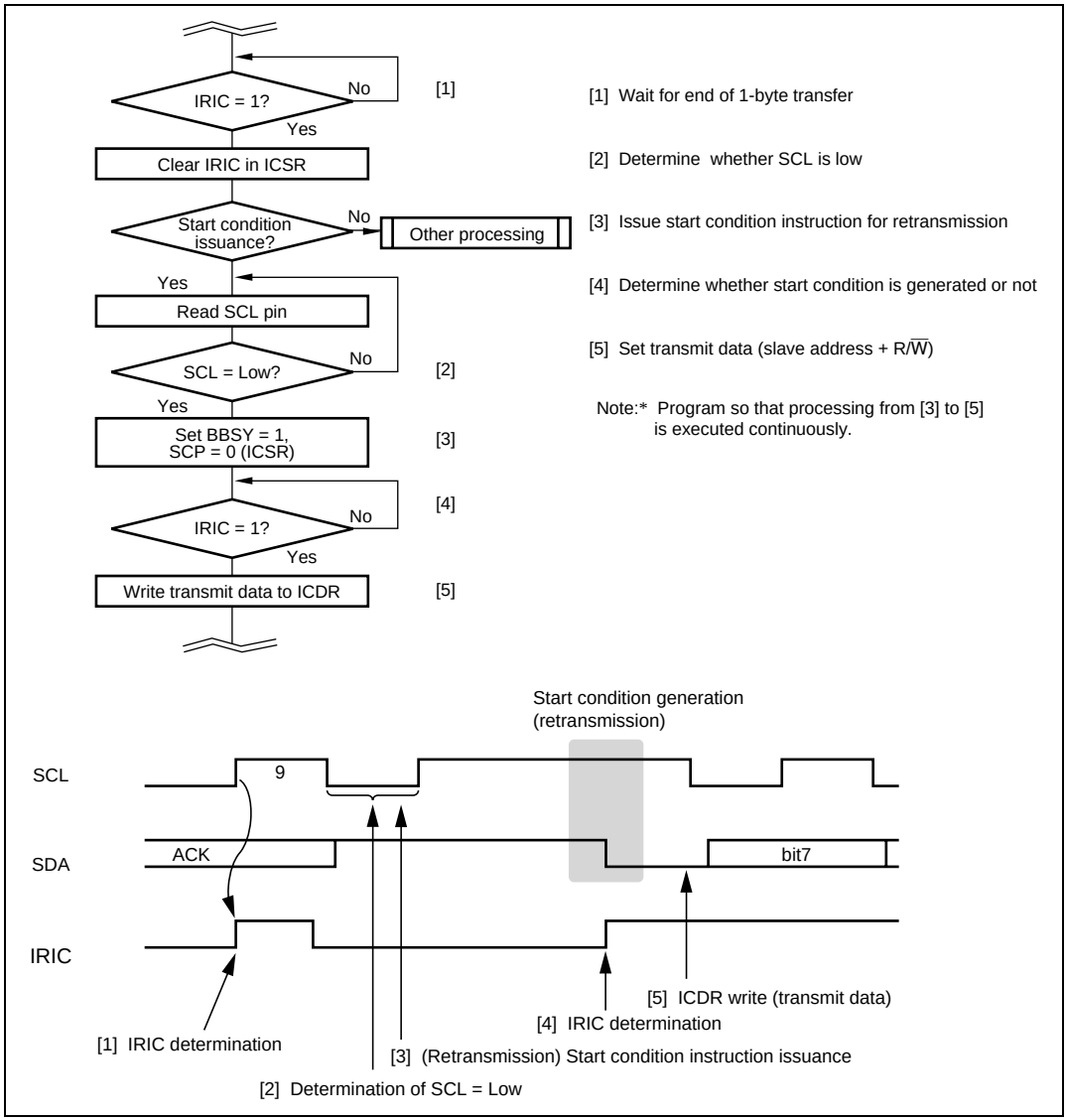


Figure 16.31 Flowchart for Start Condition Issuance Instruction for Retransmission and Timing

Note: This restriction on usage can be canceled by setting the FNC1 and FNC0 bits to 1 in ICXR.

19.5 Interrupt Sources

19.5.1 IBFI1 to IBFI3, and ERRI

The host interface has four interrupt requests for the slave processor (this LSI): IBF1 to IBF3, and ERRI. IBFI1 to IBFI3 are IDR receive complete interrupts for IDR1 to IDR3 and TWR, respectively. The ERRI interrupt indicates the occurrence of a special state such as an LPC reset, LPC shutdown, or transfer cycle abort. An interrupt request is enabled by setting the corresponding enable bit.

Table 19.7 Receive Complete Interrupts and Error Interrupt

Interrupt	Description
IBFI1	When IBFIE1 is set to 1 and IDR1 reception is completed
IBFI2	When IBFIE2 is set to 1 and IDR2 reception is completed
IBFI3	When IBFIE3 is set to 1 and IDR3 reception is completed, or when TWRE and IBFIE3 are set to 1 and reception is completed up to TWR15
ERRI	When ERRIE is set to 1 and one of LRST, SDWN and ABRT is set to 1

19.5.2 SMI, HIRQ1, HIRQ6, HIRQ9 to HIRQ12

The host interface can request seven kinds of host interrupt by means of SERIRQ. HIRQ1 and HIRQ12 are used on LPC channel 1 only, while SMI, HIRQ6, HIRQ9 to HIRQ11 can be requested from LPC channel 2 or 3.

There are two ways of clearing a host interrupt request.

When the IEDIR bit is cleared to 0 in SIRQCR0, host interrupt sources and LPC channels are all linked to the host interrupt request enable bits. When the OBF flag is cleared to 0 by a read of ODR or TWR15 by the host in the corresponding LPC channel, the corresponding host interrupt enable bit is automatically cleared to 0, and the host interrupt request is cleared.

When the IEDIR bit is set to 1 in SIRQCR0, LPC channel 2 and 3 interrupt requests are dependent only upon the host interrupt enable bits. The host interrupt enable bit is not cleared when OBF for channel 2 or 3 is cleared. Therefore, SMIE2, SMIE3A and SMIE3B, IRQ6E2 and IRQ6E3, IRQ9E2 and IRQ9E3, IRQ10E2 and IRQ10E3, and IRQ11E2 and IRQ11E3 lose their respective functional differences. In order to clear a host interrupt request, it is necessary to clear the host interrupt enable bit.

24.4 Bus Master Clock Select Circuit

The bus master clock select circuit selects a clock to supply the bus master with either the system clock (φ) or medium-speed clock (φ/2, φ/4, φ/8, φ/16, or φ/32) by the SCK2 to SCK0 bits in SBYCR.

24.5 Subclock Input Circuit

The subclock input circuit controls subclock input from the EXCL pin.

Inputting the Subclock: To use the subclock, a 32.768-kHz external clock should be input from the EXCL pin. At this time, the P96DDR bit in P9DDR should be cleared to 0, and the EXCLE bit in LPWRCR should be set to 1.

Subclock input conditions are shown in table 24.5. When the subclock is not used, subclock input should not be enabled.

Table 24.5 Subclock Input Conditions

		Vcc = 2.7 to 5.5 V				
Item	**Symbol**	**Min**	**Typ**	**Max**	**Unit**	**Measurement Condition**
Subclock input pulse width low level	t_{EXCLL}	—	15.26	—	µs	Figure 24.7
Subclock input pulse width high level	t_{EXCLH}	—	15.26	—	µs	
Subclock input rising time	t_{EXCLr}	—	—	10	ns	
Subclock input falling time	t_{EXCLf}	—	—	10	ns	

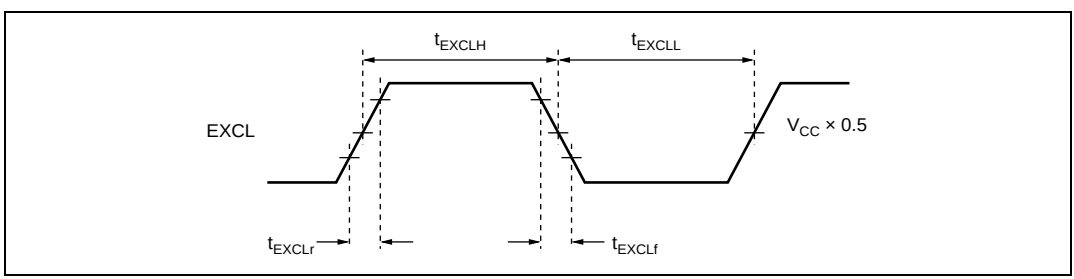


Figure 24.7 Subclock Input Timing

25.1.1 Standby Control Register (SBYCR)

SBYCR controls power-down modes.

Bit	Bit Name	Initial Value	R/W	Description
7	SSBY	0	R/W	Software Standby Specifies the operating mode to be entered after executing the SLEEP instruction. When the SLEEP instruction is executed in high-speed mode or medium-speed mode: 0: Shifts to sleep mode 1: Shifts to software standby mode, subactive mode, or watch mode When the SLEEP instruction is executed in subactive mode: 0: Shifts to subsleep mode 1: Shifts to watch mode or high-speed mode Note that the SSBY bit is not changed even if a mode transition occurs by an interrupt.
6	STS2	0	R/W	Standby Timer Select 2 to 0 Selects the wait time for clock stabilization from clock oscillation start when canceling software standby mode, watch mode, or subactive mode. Select a wait time of 8 ms (oscillation stabilization time) or more, depending on the operating frequency. Table 25.1 shows the relationship between the STS2 to STS0 values and wait time. With an external clock, there are no specific wait requirements. Normally the minimum value is recommended.
5	STS1	0	R/W	
4	STS0	0	R/W	
3	—	0	R	Reserved This bit is always read as 0, and cannot be modified.

Bit	Bit Name	Initial Value	R/W	Description
2	SCK2	0	R/W	System Clock Select 2 to 0
1	SCK1	0	R/W	Selects a clock for the bus master in high-speed mode or medium-speed mode.
0	SCK0	0	R/W	When making a transition to subactive mode or watch mode, SCK2 to SCK0 must be cleared to B'000.
				000: High-speed mode
				001: Medium-speed clock: ϕ/2
				010: Medium-speed clock: ϕ/4
				011: Medium-speed clock: ϕ/8
				100: Medium-speed clock: ϕ/16
				101: Medium-speed clock: ϕ/32
				11X: —

Legend:
X: Don't care

Table 25.1 Operating Frequency and Wait Time

STS2	STS1	STS0	Wait Time	20 MHz	10 MHz	8 MHz	6 MHz	4 MHz	2 MHz	Unit
0	0	0	8192 states	0.4	0.8	1.0	1.3	2.0	4.1	ms
0	0	1	16384 states	0.8	1.6	2.0	2.7	4.1	8.2	
0	1	0	32768 states	2.0	3.3	4.1	5.5	8.2	16.4	
0	1	1	65536 states	4.1	6.6	8.2	10.9	16.4	32.8	
1	0	0	131072 states	8.2	13.1	16.4	21.8	32.8	65.5	
1	0	1	262144 states	16.4	26.2	32.8	43.6	65.6	131.2	
1	1	0	Reserved	—	—	—	—	—	—	—
1	1	1	16 states*	0.8	1.6	2.0	2.7	4.0	8.0	µs

Shaded cells indicate the recommended specification.

Note: * This setting cannot be made in the flash-memory version of this LSI.

Register Abbreviation	Reset	High-Speed/ Medium-Speed	Watch	Sleep	Sub-Active	Sub-Sleep	Module Stop	Software Standby	Hardware Standby	Module
TCONRO	Initialized	—	—	—	—	—	—	—	Initialized	Timer connection
STR_2	Initialized	—	—	—	—	—	—	—	Initialized	XBS
TCONRS	Initialized	—	—	—	—	—	—	—	Initialized	Timer connection
SEDGR	Initialized	—	—	—	—	—	—	—	Initialized	

Notes: 1. Can be used on the H8S/2160B and H8S/2161B.
2. Not supported by the H8S/2148B and H8S/2145B (5-V version).

Lower Address	Register Name	H8S/2140B, H8S/2141B, H8S/2145B, H8S/2148B Register Select Condition	H8S/2160B, H8S/2161B Register Select Condition	Module Name
H'FE4E	PCPIN (read)	—	No condition	PORT
	PCDDR (write)			
H'FE4F	PDPIN (read)			
	PDDDR (write)			
H'FE80	HICR2	MSTP2 = 0	MSTP2 = 0	XBS
H'FE81	IDR_3			
H'FE82	ODR_3			
H'FE83	STR_3			
H'FE84	IDR_4			
H'FE85	ODR_4			
H'FE86	STR_4			
H'FED4	ICXR_0	No condition	No condition	IIC_0
H'FED5	ICXR_1			IIC_1
H'FED8	KBCRH_0	MSTP2 = 0	MSTP2 = 0	Keyboard buffer controller
H'FED9	KBCRL_0			
H'FEDA	KBBR_0			
H'FEDC	KBCRH_1			
H'FEDD	KBCRL_1			
H'FEDE	KBBR_1			
H'FEE0	KBCRH_2			
H'FEE1	KBCRL_2			
H'FEE2	KBBR_2			
H'FEE4	KBCOMP	No condition	No condition	IrDA/ expanded A/D
H'FEE6	DDCSWR	MSTP4 = 0	MSTP4 = 0	IIC_0
H'FEE8	ICRA	No condition	No condition	INT
H'FEE9	ICRB			
H'FEEA	ICRC			
H'FEEB	ISR			
H'FEEC	ISCRH			
H'FEED	ISCRL			

Item	Symbol	Condition A 10 MHz Min	Condition A 10 MHz Max	Condition B 16 MHz Min	Condition B 16 MHz Max	Condition C 20 MHz Min	Condition C 20 MHz Max	Unit	Test Conditions
Read data access time 4	t_{ACC4}	—	$2.5 \times t_{cyc} - 50$	—	$2.5 \times t_{cyc} - 35$	—	$2.5 \times t_{cyc} - 25$	ns	Figures 27.11 to 27.15
Read data access time 5	t_{ACC5}	—	$3.0 \times t_{cyc} - 80$	—	$3.0 \times t_{cyc} - 55$	—	$3.0 \times t_{cyc} - 40$	ns	
$\overline{HWR}$, $\overline{LWR}$ delay time 1	t_{WRD1}	—	60	—	45	—	30	ns	
$\overline{HWR}$, $\overline{LWR}$ delay time 2	t_{WRD2}	—	60	—	45	—	30	ns	
$\overline{HWR}$, $\overline{LWR}$ pulse width 1	t_{WSW1}	$1.0 \times t_{cyc} - 40$	—	$1.0 \times t_{cyc} - 30$	—	$1.0 \times t_{cyc} - 20$	—	ns	
$\overline{HWR}$, $\overline{LWR}$ pulse width 2	t_{WSW2}	$1.5 \times t_{cyc} - 40$	—	$1.5 \times t_{cyc} - 30$	—	$1.5 \times t_{cyc} - 20$	—	ns	
Write data delay time	t_{WDD}	—	60	—	45	—	30	ns	
Write data setup time	t_{WDS}	0	—	0	—	0	—	ns	
Write data hold time	t_{WDH}	20	—	15	—	10	—	ns	
$\overline{WAIT}$ setup time	t_{WTS}	60	—	45	—	30	—	ns	
$\overline{WAIT}$ hold time	t_{WTH}	10	—	5	—	5	—	ns	