NXP USA Inc. - KMPC859TVR133A Datasheet



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Details

Product Status	Obsolete
Core Processor	MPC8xx
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	133MHz
Co-Processors/DSP	Communications; CPM
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10Mbps (1), 10/100Mbps (1)
SATA	-
USB	-
Voltage - I/O	3.3V
Operating Temperature	0°C ~ 95°C (TA)
Security Features	-
Package / Case	357-BBGA
Supplier Device Package	357-PBGA (25x25)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmpc859tvr133a

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Features

Table 1 shows the functionality supported by the members of the MPC866/859 family.

2 Features

Part	Ca	Ethe	ernet	500	SMC	
Fait	Instruction	Data	10T	10/100	300	SMC
MPC866P	16 Kbytes	8 Kbytes	Up to 4	1	4	2
MPC866T	4 Kbytes	4 Kbytes	Up to 4	1	4	2
MPC859P	16 Kbytes	8 Kbytes	1	1	1	2
MPC859T	4 Kbytes	4 Kbytes	1	1	1	2
MPC859DSL	4 Kbytes	4 Kbytes	1	1	1 ¹	1 ²
MPC852T ³	4 KBytes	4 Kbytes	2	1	2	1

Table 1. MPC866 Family Functionality

¹ On the MPC859DSL, the SCC (SCC1) is for ethernet only. Also, the MPC859DSL does not support the Time Slot Assigner (TSA).

² On the MPC859DSL, the SMC (SMC1) is for UART only.

³ For more details on the MPC852T, please refer to the MPC852T Hardware Specifications.

The following list summarizes the key MPC866/859 features:

- Embedded single-issue, 32-bit PowerPCTM core (implementing the PowerPC architecture) with thirty-two 32-bit general-purpose registers (GPRs)
 - The core performs branch prediction with conditional prefetch, without conditional execution
 - 4- or 8-Kbyte data cache and 4- or 16-Kbyte instruction cache (see Table 1)
 - 16-Kbyte instruction cache (MPC866P and MPC859P) is four-way, set-associative with 256 sets;
 4-Kbyte instruction cache (MPC866T, MPC859T, and MPC859DSL) is two-way, set-associative with 128 sets.
 - 8-Kbyte data cache (MPC866P and MPC859P) is two-way, set-associative with 256 sets; 4-Kbyte data cache(MPC866T, MPC859T, and MPC859DSL) is two-way, set-associative with 128 sets.
 - Cache coherency for both instruction and data caches is maintained on 128-bit (4-word) cache blocks
 - Caches are physically addressed, implement a least recently used (LRU) replacement algorithm, and are lockable on a cache block basis.
 - MMUs with 32-entry TLB, fully associative instruction and data TLBs
 - MMUs support multiple page sizes of 4, 16, and 512 Kbytes, and 8 Mbytes; 16 virtual address spaces and 16 protection groups.
 - Advanced on-chip-emulation debug mode
- The MPC866/859 provides enhanced ATM functionality over that of the MPC860SAR. The MPC866/859 adds major new features available in 'enhanced SAR' (ESAR) mode, including the following:
 - Improved operation, administration, and maintenance (OAM) support
 - OAM performance monitoring (PM) support
 - Multiple APC priority levels available to support a range of traffic pace requirements



Features

- One serial peripheral interface (SPI)
 - Supports master and slave modes
 - Supports multiple-master operation on the same bus
- One inter-integrated circuit (I²C) port
 - Supports master and slave modes
 - Multiple-master environment support
- Time slot assigner (TSA) (MPC859DSL does not have TSA.)
 - Allows SCCs and SMCs to run in multiplexed and/or non-multiplexed operation
 - Supports T1, CEPT, PCM highway, ISDN basic rate, ISDN primary rate, user-defined
 - 1- or 8-bit resolution
 - Allows independent transmit and receive routing, frame synchronization, and clocking
 - Allows dynamic changes
 - On MPC866P and MPC866T, can be internally connected to six serial channels (four SCCs and two SMCs); on MPC859P and MPC859T, can be connected to three serial channels (one SCC and two SMCs).
- Parallel interface port (PIP)
 - Centronics interface support
 - Supports fast connection between compatible ports on MPC866/859 or MC68360
- PCMCIA interface
 - Master (socket) interface, compliant with PCI Local Bus Specification (Rev 2.1)
 - Supports one or two PCMCIA sockets whether ESAR functionality is enabled
 - Eight memory or I/O windows supported
- Debug interface
 - Eight comparators: four operate on instruction address, two operate on data address, and two operate on data.
 - Supports conditions: = $\neq < >$
 - Each watchpoint can generate a breakpoint internally
- Normal high and normal low power modes to conserve power
- 1.8 V core and 3.3 V I/O operation with 5-V TTL compatibility; refer to Table 6 for a listing of the 5-V tolerant pins.
- 357-pin plastic ball grid array (PBGA) package
- Operation up to 133 MHz





- [†] The MPC859P has a 16-Kbyte instruction cache and a 8-Kbyte data cache.
- * The MPC859DSL does not contain SMC2 nor the time slot assigner, and provides eight SDMA controllers.

Figure 2. MPC859P/859T/MPC859DSL Block Diagram



Maximum Tolerated Ratings

3 Maximum Tolerated Ratings

This section provides the maximum tolerated voltage and temperature ranges for the MPC866/859. Table 2 shows the maximum tolerated ratings, and Table 3 shows the operating temperatures.

Rating	Symbol	Value	Unit
Supply voltage ¹	VDDH	– 0.3 to 4.0	V
	VDDL	– 0.3 to 2.0	V
	VDDSYN	– 0.3 to 2.0	V
	Difference between VDDL to VDDSYN	100	mV
Input voltage ²	V _{in}	GND – 0.3 to VDDH	V
Storage temperature range	T _{stg}	–55 to +150	°C

Table 2. Maximum Tolerated Ratings

¹ The power supply of the device must start its ramp from 0.0 V.

² Functional operating conditions are provided with the DC electrical specifications in Table 6. Absolute maximum ratings are stress ratings only; functional operation at the maxima is not guaranteed. Stress beyond those listed may affect device reliability or cause permanent damage to the device. See page 15.

Caution: All inputs that tolerate 5 V cannot be more than 2.5 V greater than VDDH. This restriction applies to power-up and normal operation (that is, if the MPC866/859 is unpowered, a voltage greater than 2.5 V must not be applied to its inputs).

Rating	Symbol	Value	Unit						
Temperature ¹ (standard)	T _{A(min)}	0	°C						
	T _{j(max)}	95	°C						
Temperature (extended)	T _{A(min)}	-40	°C						
	T _{j(max)}	100	°C						

Table 3. Operating Temperatures

Minimum temperatures are guaranteed as ambient temperature, T_A. Maximum temperatures are guaranteed as junction temperature, T_i.

This device contains circuitry protecting against damage due to high-static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for example, either GND or V_{DD}).



	Characteristic	33	MHz	40	MHz	50 I	MHz	66 MHz		
Num	Characteristic	Min	Max	Min	Мах	Min	Max	Min	Max	Unit
B1d	CLKOUT phase jitter peak-to-peak for OSCLK \geq 15 MHz	_	4	—	4		4	—	4	ns
	CLKOUT phase jitter peak-to-peak for OSCLK < 15 MHz	—	5	—	5		5	—	5	ns
B2	CLKOUT pulse width low (MIN = 0.4 x B1, MAX = 0.6 x B1)	12.1	18.2	10.0	15.0	8.0	12.0	6.1	9.1	ns
B3	CLKOUT pulse width high (MIN = 0.4 x B1, MAX = 0.6 x B1)	12.1	18.2	10.0	15.0	8.0	12.0	6.1	9.1	ns
B4	CLKOUT rise time	—	4.00	—	4.00		4.00	—	4.00	ns
B5	CLKOUT fall time	—	4.00	—	4.00		4.00	—	4.00	ns
B7	CLKOUT to A(0:31), BADDR(28:30), RD/WR, BURST, D(0:31), DP(0:3) output hold (MIN = 0.25 x B1)	7.60	_	6.30		5.00	—	3.80		ns
B7a	CLKOUT to TSIZ(0:1), $\overline{\text{REG}}$, $\overline{\text{RSV}}$, AT(0:3), $\overline{\text{BDIP}}$, PTR output hold (MIN = 0.25 x B1)	7.60	_	6.30	_	5.00	_	3.80	_	ns
B7b	CLKOUT to \overline{BR} , \overline{BG} , FRZ, VFLS(0:1), VF(0:2), IWP(0:2), LWP(0:1), \overline{STS} output hold (MIN = 0.25 x B1)	7.60	_	6.30	_	5.00	_	3.80	_	ns
B8	CLKOUT to A(0:31), BADDR(28:30) RD/WR, BURST, D(0:31), DP(0:3), valid (MAX = 0.25 x B1 + 6.3)	—	13.80	—	12.50	_	11.30	—	10.00	ns
B8a	CLKOUT to TSIZ(0:1), REG, RSV, AT(0:3), BDIP, PTR valid (MAX = 0.25 x B1 + 6.3)	—	13.80		12.50	_	11.30		10.00	ns
B8b	CLKOUT to BR, BG, VFLS(0:1), VF(0:2), IWP(0:2), FRZ, LWP(0:1), STS valid ⁴ (MAX = 0.25 x B1 + 6.3)		13.80		12.50	_	11.30		10.00	ns
B9	CLKOUT to A(0:31), BADDR(28:30), RD/WR, BURST, D(0:31), DP(0:3), TSIZ(0:1), REG, RSV, AT(0:3), PTR High-Z (MAX = 0.25 x B1 + 6.3)	7.60	13.80	6.30	12.50	5.00	11.30	3.80	10.00	ns
B11	CLKOUT to \overline{TS} , \overline{BB} assertion (MAX = 0.25 x B1 + 6.0)	7.60	13.60	6.30	12.30	5.00	11.00	3.80	9.80	ns
B11a	CLKOUT to \overline{TA} , \overline{BI} assertion (when driven by the memory controller or PCMCIA interface) (MAX = 0.00 x B1 + 9.30 ¹)	2.50	9.30	2.50	9.30	2.50	9.30	2.50	9.80	ns
B12	CLKOUT to \overline{TS} , \overline{BB} negation (MAX = 0.25 x B1 + 4.8)	7.60	12.30	6.30	11.00	5.00	9.80	3.80	8.50	ns



Bus Signal Timing

	Oh ann atamiatia	33 I	MHz	40	MHz	50 I	MHz	66 MHz		
NUM	Characteristic	Min	Max	Min	Мах	Min	Max	Min	Max	Unit
B12a	CLKOUT to \overline{TA} , \overline{BI} negation (when driven by the memory controller or PCMCIA interface) (MAX = 0.00 x B1 + 9.00)	2.50	9.00	2.50	9.00	2.50	9.00	2.50	9.00	ns
B13	CLKOUT to \overline{TS} , \overline{BB} High-Z (MIN = 0.25 x B1)	7.60	21.60	6.30	20.30	5.00	19.00	3.80	14.00	ns
B13a	CLKOUT to \overline{TA} , \overline{BI} High-Z (when driven by the memory controller or PCMCIA interface) (MIN = 0.00 x B1 + 2.5)	2.50	15.00	2.50	15.00	2.50	15.00	2.50	15.00	ns
B14	CLKOUT to TEA assertion (MAX = 0.00 x B1 + 9.00)	2.50	9.00	2.50	9.00	2.50	9.00	2.50	9.00	ns
B15	CLKOUT to $\overline{\text{TEA}}$ High-Z (MIN = 0.00 x B1 + 2.50)	2.50	15.00	2.50	15.00	2.50	15.00	2.50	15.00	ns
B16	TA, BI valid to CLKOUT (setup time) (MIN = 0.00 x B1 + 6.00)	6.00	_	6.00	_	6.00	_	6.00	_	ns
B16a	TEA, KR, RETRY, CR valid to CLKOUT (setup time) (MIN = 0.00 x B1 + 4.5)	4.50	_	4.50	_	4.50	_	4.50	_	ns
B16b	$\overline{\text{BB}}$, $\overline{\text{BG}}$, $\overline{\text{BR}}$, valid to CLKOUT (setup time) ² (4 MIN = 0.00 x B1 + 0.00)	4.00	_	4.00	_	4.00	_	4.00	_	ns
B17	CLKOUT to TA, TEA, BI, BB, BG, BR valid (hold time) (MIN = $0.00 \times B1 + 1.00^{3}$)	1.00	_	1.00	—	1.00	—	2.00	—	ns
B17a	CLKOUT to $\overline{\text{KR}}$, $\overline{\text{RETRY}}$, $\overline{\text{CR}}$ valid (hold time) (MIN = 0.00 x B1 + 2.00)	2.00	—	2.00	_	2.00	—	2.00	—	ns
B18	D(0:31), DP(0:3) valid to CLKOUT rising edge (setup time) 4 (MIN = 0.00 x B1 + 6.00)	6.00	—	6.00	_	6.00	_	6.00	_	ns
B19	CLKOUT rising edge to D(0:31), DP(0:3) valid (hold time) 4 (MIN = 0.00 x B1 + 1.00 5)	1.00	—	1.00	_	1.00	_	2.00	_	ns
B20	D(0:31), DP(0:3) valid to CLKOUT falling edge (setup time) 6 (MIN = 0.00 x B1 + 4.00)	4.00	_	4.00	_	4.00	_	4.00	_	ns
B21	CLKOUT falling edge to D(0:31), DP(0:3) valid (hold Time) 6 (MIN = 0.00 x B1 + 2.00)	2.00	_	2.00	_	2.00	_	2.00	_	ns
B22	CLKOUT rising edge to \overline{CS} asserted GPCM ACS = 00 (MAX = 0.25 x B1 + 6.3)	7.60	13.80	6.30	12.50	5.00	11.30	3.80	10.00	ns
B22a	CLKOUT falling edge to \overline{CS} asserted GPCM ACS = 10, TRLX = 0 (MAX = 0.00 x B1 + 8.00)	_	8.00		8.00		8.00	_	8.00	ns



Niuma	Characteristic	33	MHz	40 I	MHz	50 MHz		66 MHz		11
NUM	Characteristic	Min	Max	Min	Мах	Min	Max	Min	Max	Unit
B22b	CLKOUT falling edge to \overline{CS} asserted GPCM ACS = 11, TRLX = 0, EBDF = 0 (MAX = 0.25 x B1 + 6.3)	7.60	13.80	6.30	12.50	5.00	11.30	3.80	10.00	ns
B22c	CLKOUT falling edge to \overline{CS} asserted GPCM ACS = 11, TRLX = 0, EBDF = 1 (MAX = 0.375 x B1 + 6.6)	10.90	18.00	10.90	16.00	7.00	14.10	5.20	12.30	ns
B23	CLKOUT rising edge to \overline{CS} negated GPCM read access, GPCM write access ACS = 00, TRLX = 0 & CSNT = 0 (MAX = 0.00 x B1 + 8.00)	2.00	8.00	2.00	8.00	2.00	8.00	2.00	8.00	ns
B24	A(0:31) and BADDR(28:30) to \overline{CS} asserted GPCM ACS = 10, TRLX = 0 (MIN = 0.25 x B1 - 2.00)	5.60	—	4.30	_	3.00		1.80	—	ns
B24a	A(0:31) and BADDR(28:30) to \overline{CS} asserted GPCM ACS = 11, TRLX = 0 (MIN = 0.50 x B1 - 2.00)	13.20	—	10.50	_	8.00	_	5.60	_	ns
B25	CLKOUT rising edge to \overline{OE} , $\overline{WE}(0:3)$ asserted (MAX = 0.00 x B1 + 9.00)	_	9.00	_	9.00	_	9.00	_	9.00	ns
B26	CLKOUT rising edge to \overline{OE} negated (MAX = 0.00 x B1 + 9.00)	2.00	9.00	2.00	9.00	2.00	9.00	2.00	9.00	ns
B27	A(0:31) and BADDR(28:30) to \overline{CS} asserted GPCM ACS = 10, TRLX = 1 (MIN = 1.25 x B1 - 2.00)	35.90	—	29.30		23.00		16.90	_	ns
B27a	A(0:31) and BADDR(28:30) to \overline{CS} asserted GPCM ACS = 11, TRLX = 1 (MIN = 1.50 x B1 - 2.00)	43.50	—	35.50	_	28.00	_	20.70	_	ns
B28	CLKOUT rising edge to $\overline{WE}(0:3)$ negated GPCM write access CSNT = 0 (MAX = 0.00 x B1 + 9.00)		9.00		9.00	_	9.00	—	9.00	ns
B28a	CLKOUT falling edge to $\overline{WE}(0:3)$ negated GPCM write access TRLX = 0,1, CSNT = 1, EBDF = 0 (MAX = 0.25 x B1 + 6.80)	7.60	14.30	6.30	13.00	5.00	11.80	3.80	10.50	ns
B28b	CLKOUT falling edge to \overline{CS} negated GPCM write access TRLX = 0,1, CSNT = 1, ACS = 10 or ACS = 11, EBDF = 0 (MAX = 0.25 x B1 + 6.80)	_	14.30	_	13.00	_	11.80	_	10.50	ns
B28c	CLKOUT falling edge to $\overline{WE}(0:3)$ negated GPCM write access TRLX = 0, CSNT = 1 write access TRLX = 0,1, CSNT = 1, EBDF = 1 (MAX = 0.375 x B1 + 6.6)	10.90	18.00	10.90	18.00	7.00	14.30	5.20	12.30	ns



Bus Signal Timing

	Oh ann atariatha	33	MHz	40 1	MHz	50 I	MHz	66 MHz		
NUM	Characteristic	Min	Max	Min	Мах	Min	Max	Min	Max	Unit
B31d	CLKOUT falling edge to \overline{CS} valid, as requested by control bit CST1 in the corresponding word in the UPM EBDF = 1 (MAX = 0.375 x B1 + 6.6)	13.30	18.00	11.30	16.00	9.40	14.10	7.60	12.30	ns
B32	CLKOUT falling edge to \overline{BS} valid, as requested by control bit BST4 in the corresponding word in the UPM (MAX = 0.00 x B1 + 6.00)	1.50	6.00	1.50	6.00	1.50	6.00	1.50	6.00	ns
B32a	CLKOUT falling edge to $\overline{\text{BS}}$ valid, as requested by control bit BST1 in the corresponding word in the UPM, EBDF = 0 (MAX = 0.25 x B1 + 6.80)	7.60	14.30	6.30	13.00	5.00	11.80	3.80	10.50	ns
B32b	CLKOUT rising edge to \overline{BS} valid, as requested by control bit BST2 in the corresponding word in the UPM (MAX = 0.00 x B1 + 8.00)	1.50	8.00	1.50	8.00	1.50	8.00	1.50	8.00	ns
B32c	CLKOUT rising edge to \overline{BS} valid, as requested by control bit BST3 in the corresponding word in the UPM (MAX = 0.25 x B1 + 6.80)	7.60	14.30	6.30	13.00	5.00	11.80	3.80	10.50	ns
B32d	CLKOUT falling edge to $\overline{\text{BS}}$ valid- as requested by control bit BST1 in the corresponding word in the UPM, EBDF = 1 (MAX = 0.375 x B1 + 6.60)	13.30	18.00	11.30	16.00	9.40	14.10	7.60	12.30	ns
B33	CLKOUT falling edge to $\overline{\text{GPL}}$ valid, as requested by control bit GxT4 in the corresponding word in the UPM (MAX = 0.00 x B1 + 6.00)	1.50	6.00	1.50	6.00	1.50	6.00	1.50	6.00	ns
B33a	CLKOUT rising edge to $\overline{\text{GPL}}$ valid, as requested by control bit GxT3 in the corresponding word in the UPM (MAX = 0.25 x B1 + 6.80)	7.60	14.30	6.30	13.00	5.00	11.80	3.80	10.50	ns
B34	A(0:31), BADDR(28:30), and D(0:31) to \overline{CS} valid, as requested by control bit CST4 in the corresponding word in the UPM (MIN = 0.25 x B1 - 2.00)	5.60	_	4.30	_	3.00	_	1.80	_	ns
B34a	A(0:31), BADDR(28:30), and D(0:31) to \overline{CS} valid, as requested by control bit CST1 in the corresponding word in the UPM (MIN = 0.50 x B1 - 2.00)	13.20	_	10.50	_	8.00	_	5.60	_	ns
B34b	A(0:31), BADDR(28:30), and D(0:31) to \overline{CS} valid, as requested by CST2 in the corresponding word in UPM (MIN = 0.75 x B1 - 2.00)	20.70	_	16.70	_	13.00	_	9.40	_	ns



Num	Charactariatia	33	MHz	40 MHz		50 MHz		66 MHz		Unit
Num	Characteristic	Min	Max	Min	Max	Min	Max	Min	Max	Unit
B35	A(0:31), BADDR(28:30) to \overline{CS} valid, as requested by control bit BST4 in the corresponding word in the UPM (MIN = 0.25 x B1 - 2.00)	5.60	_	4.30	_	3.00	_	1.80	_	ns
B35a	A(0:31), BADDR(28:30), and D(0:31) to \overline{BS} valid, as Requested by BST1 in the corresponding word in the UPM (MIN = 0.50 x B1 - 2.00)	13.20	_	10.50	_	8.00	_	5.60	_	ns
B35b	A(0:31), BADDR(28:30), and D(0:31) to \overline{BS} valid, as requested by control bit BST2 in the corresponding word in the UPM (MIN = 0.75 x B1 - 2.00)	20.70	_	16.70	_	13.00	_	9.40	_	ns
B36	A(0:31), BADDR(28:30), and D(0:31) to GPL valid as requested by control bit GxT4 in the corresponding word in the UPM (MIN = $0.25 \times B1 - 2.00$)	5.60	_	4.30	_	3.00	_	1.80	_	ns
B37	UPWAIT valid to CLKOUT falling edge ⁸ (MIN = 0.00 x B1 + 6.00)	6.00	_	6.00	_	6.00	_	6.00	—	ns
B38	CLKOUT falling edge to UPWAIT valid ⁸ (MIN = 0.00 x B1 + 1.00)	1.00		1.00	_	1.00	—	1.00	—	ns
B39	$\overline{\text{AS}}$ valid to CLKOUT rising edge ⁹ (MIN = 0.00 x B1 + 7.00)	7.00		7.00	_	7.00	—	7.00	_	ns
B40	A(0:31), TSIZ(0:1), RD/WR, BURST, valid to CLKOUT rising edge (MIN = 0.00 x B1 + 7.00)	7.00		7.00		7.00		7.00		ns
B41	$\overline{\text{TS}}$ valid to CLKOUT rising edge (setup time) (MIN = 0.00 x B1 + 7.00)	7.00	_	7.00	_	7.00	_	7.00	_	ns
B42	CLKOUT rising edge to \overline{TS} valid (hold time) (MIN = 0.00 x B1 + 2.00)	2.00	_	2.00	—	2.00	—	2.00	—	ns
B43	$\overline{\text{AS}}$ negation to memory controller signals negation (MAX = TBD)	—	TBD	—	TBD	—	TBD	—	TBD	ns

Table 9. Bus Operation Timings (continued)

¹ For part speeds above 50 MHz, use 9.80 ns for B11a.

² The timing required for BR input is relevant when the MPC866/859 is selected to work with the internal bus arbiter. The timing for BG input is relevant when the MPC866/859 is selected to work with the external bus arbiter.

³ For part speeds above 50 MHz, use 2 ns for B17.

⁴ The D(0:31) and DP(0:3) input timings B18 and B19 refer to the rising edge of CLKOUT, in which the TA input signal is asserted.

⁵ For part speeds above 50 MHz, use 2 ns for B19.

⁶ The D(0:31) and DP(0:3) input timings B20 and B21 refer to the falling edge of CLKOUT. This timing is valid only for read accesses controlled by chip-selects under control of the UPM in the memory controller, for data beats, where DLT3 = 1 in the UPM RAM words. (This is only the case where data is latched on the falling edge of CLKOUT.)

⁷ The timing B30 refers to \overline{CS} when ACS = 00 and to $\overline{WE}(0:3)$ when CSNT = 0.



Bus Signal Timing

- ⁸ The signal UPWAIT is considered asynchronous to CLKOUT and synchronized internally. The timings specified in B37 and B38 are specified to enable the freeze of the UPM output signals as described in Figure 20.
- ⁹ The AS signal is considered asynchronous to CLKOUT. The timing B39 is specified in order to allow the behavior specified in Figure 23.

Figure 5 shows the control timing diagram.





Bus Signal Timing

Figure 27 shows the PCMCIA access cycle timing for the external bus read.



Figure 27. PCMCIA Access Cycles Timing External Bus Read



CPM Electrical Characteristics



Figure 41. PIP Rx (Interlock Mode) Timing Diagram



Figure 42. PIP Tx (Interlock Mode) Timing Diagram



Figure 43. PIP Rx (Pulse Mode) Timing Diagram



Num	Characteristic	All F	Frequencies	Unit
Num	Characteristic	Min	Max	Unit
74	L1CLK edge to L1RSYNC, L1TSYNC, invalid (SYNC hold time)	35.00	_	ns
75	L1RSYNC, L1TSYNC rise/fall time	_	15.00	ns
76	L1RXD valid to L1CLK edge (L1RXD setup time)	17.00	—	ns
77	L1CLK edge to L1RXD invalid (L1RXD hold time)	13.00	—	ns
78	L1CLK edge to L1ST(1–4) valid ⁴	10.00	45.00	ns
78A	L1SYNC valid to L1ST(1-4) valid	10.00	45.00	ns
79	L1CLK edge to L1ST(1-4) invalid	10.00	45.00	ns
80	L1CLK edge to L1TXD valid	10.00	55.00	ns
80A	L1TSYNC valid to L1TXD valid ⁴	10.00	55.00	ns
81	L1CLK edge to L1TXD high impedance	0.00	42.00	ns
82	L1RCLK, L1TCLK frequency (DSC =1)		16.00 or SYNCCLK/2	MHz
83	L1RCLK, L1TCLK width low (DSC =1)	P + 10	—	ns
83a	L1RCLK, L1TCLK width high (DSC = 1) ³	P + 10	—	ns
84	L1CLK edge to L1CLKO valid (DSC = 1)		30.00	ns
85	L1RQ valid before falling edge of L1TSYNC ⁴	1.00	—	L1TCLK
86	L1GR setup time ²	42.00	—	ns
87	L1GR hold time	42.00	—	ns
88	L1CLK edge to L1SYNC valid (FSD = 00) CNT = 0000, BYT = 0, DSC = 0)	—	0.00	ns

Table 21. SI Timing (continued)

¹ The ratio SyncCLK/L1RCLK must be greater than 2.5/1.

² These specs are valid for IDL mode only.

³ Where P = 1/CLKOUT. Thus, for a 25-MHz CLKO1 rate, P = 40 ns.

⁴ These strobes and TxD on the first bit of the frame become valid after L1CLK edge or L1SYNC, whichever is later.



CPM Electrical Characteristics





12.7 SCC in NMSI Mode Electrical Specifications

Table 22 shows the NMSI external clock timings.

Num	Chavastavistia	All Frequencie	s	l l mit
Num	Characteristic	Min	Мах	Unit
100	RCLK1 and TCLK1 width high ¹	1/SYNCCLK	_	ns
101	RCLK1 and TCLK1 width low	1/SYNCCLK +5	—	ns
102	RCLK1 and TCLK1 rise/fall time	—	15.00	ns
103	TXD1 active delay (from TCLK1 falling edge)	0.00	50.00	ns
104	RTS1 active/inactive delay (from TCLK1 falling edge)	0.00	50.00	ns
105	CTS1 setup time to TCLK1 rising edge	5.00	-	ns
106	RXD1 setup time to RCLK1 rising edge	5.00	-	ns
107	RXD1 hold time from RCLK1 rising edge ²	5.00	-	ns
108	CD1 setup time to RCLK1 rising edge	5.00	—	ns

Table 22. NMSI External Clock Timings

¹ The ratios SyncCLK/RCLK1 and SyncCLK/TCLK1 must be greater than or equal to 2.25/1.

² Also applies to $\overline{\text{CD}}$ and $\overline{\text{CTS}}$ hold time when they are used as an external sync signal.

Table 23 shows the NMSI internal clock timings.

Table 23. NMSI Internal Clock Timings

Num	Characteristic	All Fr	equencies	Unit	
Nulli		Min	Max	Onic	
100	RCLK1 and TCLK1 frequency ¹	0.00	SYNCCLK/3	MHz	
102	RCLK1 and TCLK1 rise/fall time	_	_	ns	
103	TXD1 active delay (from TCLK1 falling edge)	0.00	30.00	ns	
104	RTS1 active/inactive delay (from TCLK1 falling edge)	0.00	30.00	ns	
105	CTS1 setup time to TCLK1 rising edge	40.00	-	ns	
106	RXD1 setup time to RCLK1 rising edge	40.00	-	ns	
107	RXD1 hold time from RCLK1 rising edge ²	0.00	-	ns	
108	CD1 setup time to RCLK1 rising edge	40.00	—	ns	

¹ The ratios SyncCLK/RCLK1 and SyncCLK/TCLK1 must be greater or equal to 3/1.

² Also applies to $\overline{\text{CD}}$ and $\overline{\text{CTS}}$ hold time when they are used as an external sync signals.



CPM Electrical Characteristics

Figure 58 through Figure 60 show the NMSI timings.





CPM Electrical Characteristics



Figure 69. SPI Slave (CP = 0) Timing Diagram



FEC Electrical Characteristics

Figure 75 shows the MII transmit signal timing diagram.



Figure 75. MII Transmit Signal Timing Diagram

14.3 MII Async Inputs Signal Timing (MII_CRS, MII_COL)

Table 35 shows the timing for on the MII async inputs signal.

Table 35. MII Async Inputs Signal Timing

Num	Characteristic	Min	Мах	Unit
M9	MII_CRS, MII_COL minimum pulse width	1.5	_	MII_TX_CLK period

Figure 76 shows the MII asynchronous inputs signal timing diagram.



Figure 76. MII Async Inputs Timing Diagram

14.4 MII Serial Management Channel Timing (MII_MDIO, MII_MDC)

Table 36 shows the timing for the MII serial management channel signal. The FEC functions correctly with a maximum MDC frequency in excess of 2.5 MHz. The exact upper bound is under investigation.

Table 36. MII Serial Management Channel Timing

Num	Characteristic	Min	Мах	Unit
M10	MII_MDC falling edge to MII_MDIO output invalid (minimum propagation delay)	0		ns
M11	MII_MDC falling edge to MII_MDIO output valid (maximum propagation delay)	_	25	ns
M12	MII_MDIO (input) to MII_MDC rising edge setup	10		ns



Mechanical Data and Ordering Information

Table 39 contains a list of the MPC866 input and output signals and shows multiplexing and pin assignments.

Name	Pin Number	Туре
A[0:31]	B19, B18, A18, C16, B17, A17, B16, A16, D15, C15, B15, A15, C14, B14, A14, D12, C13, B13, D9, D11, C12, B12, B10, B11, C11, D10, C10, A13, A10, A12, A11, A9	Bidirectional Three-state
TSIZ0 REG	В9	Bidirectional Three-state
TSIZ1	С9	Bidirectional Three-state
RD/WR	B2	Bidirectional Three-state
BURST	F1	Bidirectional Three-state
BDIP GPL_B5	D2	Output
TS	F3	Bidirectional Active Pull-up
TA	C2	Bidirectional Active Pull-up
TEA	D1	Open-drain
BI	E3	Bidirectional Active Pull-up
IRQ2 RSV	НЗ	Bidirectional Three-state
IRQ4 KR RETRY SPKROUT	К1	Bidirectional Three-state
CR IRQ3	F2	Input
D[0:31]	W14, W12, W11, W10, W13, W9, W7, W6, U13, T11, V11, U11, T13, V13, V10, T10, U10, T12, V9, U9, V8, U8, T9, U12, V7, T8, U7, V12, V6, W5, U6, T7	Bidirectional Three-state
DP0 IRQ3	V3	Bidirectional Three-state
DP1 IRQ4	V5	Bidirectional Three-state
DP2 IRQ5	W4	Bidirectional Three-state
DP3 IRQ6	V4	Bidirectional Three-state

Table 39. Pin Assignments



Mechanical Data and Ordering Information

Table 39. Pin Assignments (continued)

Name	Pin Number	Туре
MII_COL	H4	Input
VSSSYN1	V1	PLL analog VDD and GND
VSSSYN	U1	Power
VDDSYN	T1	Power
GND	F6, F7, F8, F9, F10, F11, F12, F13, F14, G6, G7, G8, G9, G10, G11, G12, G13, G14, H6, H7, H8, H9, H10, H11, H12, H13, H14, J6, J7, J8, J9, J10, J11, J12, J13, J14, K6, K7, K8, K9, K10, K11, K12, K13, K14, L6, L7, L8, L9, L10, L11, L12, L13, L14, M6, M7, M8, M9, M10, M11, M12, M13, M14, N6, N7, N8, N9, N10, N11, N12, N13, N14, P6, P7, P8, P9, P10, P11, P12, P13, P14	Power
VDDL	A8, M1, W8, H19, F4, F16, P4, P16, R1	Power
VDDH	E5, E6, E7, E8, E9, E10, E11, E12, E13, E14, E15, F5, F15, G5, G15, H5, H15, J5, J15, K5, K15, L5, L15, M5, M15, N5, N15, P5, P15, R5, R6, R7, R8, R9, R10, R11, R12, R13, R14, R15, T14	Power
N/C	D6, D13, D14, U2, V2, T2	No-connect

¹ Classic SAR mode only

² ESAR mode only