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Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	MPC8xx
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	100MHz
Co-Processors/DSP	Communications; CPM
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10Mbps (1), 10/100Mbps (1)
SATA	-
USB	-
Voltage - I/O	3.3V
Operating Temperature	0°C ~ 95°C (TA)
Security Features	-
Package / Case	357-BBGA
Supplier Device Package	357-PBGA (25x25)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc859pvr100a

4 Thermal Characteristics

Table 4 shows the thermal characteristics for the MPC866/859.

Table 4. MPC866/859 Thermal Resistance Data

Rating	Environment		Symbol	Value	Unit
Junction-to-ambient ¹	Natural Convection	Single-layer board (1s)	$R_{\theta JA}$ ²	37	°C/W
		Four-layer board (2s2p)	$R_{\theta JMA}$ ³	23	
	Airflow (200 ft/min)	Single-layer board (1s)	$R_{\theta JMA}$ ³	30	
		Four-layer board (2s2p)	$R_{\theta JMA}$ ³	19	
Junction-to-board ⁴			$R_{\theta JB}$	13	
Junction-to-case ⁵			$R_{\theta JC}$	6	
Junction-to-package top ⁶	Natural Convection		Ψ_{JT}	2	
	Airflow (200 ft/min)		Ψ_{JT}	2	

¹ Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, airflow, power dissipation of other components on the board, and board thermal resistance.

² Per SEMI G38-87 and JEDEC JESD51-2 with the single-layer board horizontal.

³ Per JEDEC JESD51-6 with the board horizontal.

⁴ Thermal resistance between the die and the printed-circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

⁵ Indicates the average thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1) with the cold plate temperature used for the case temperature. For exposed pad packages where the pad would be expected to be soldered, junction-to-case thermal resistance is a simulated value from the junction to the exposed pad without contact resistance.

⁶ Thermal characterization parameter indicating the temperature difference between package top and junction temperature per JEDEC JESD51-2.

5 Power Dissipation

Table 5 shows power dissipation information. The modes are 1:1, where CPU and bus speeds are equal, and 2:1 mode, where CPU frequency is twice the bus speed.

Table 5. Power Dissipation (P_D)

Die Revision	Bus Mode	CPU Frequency	Typical ¹	Maximum ²	Unit
0	1:1	50 MHz	110	140	mW
		66 MHz	150	180	mW
	2:1	66 MHz	140	160	mW
		80 MHz	170	200	mW
		100 MHz	210	250	mW
		133 MHz	260	320	mW

¹ Typical power dissipation at VDDL and VDDSYN is at 1.8 V, and VDDH is at 3.3 V.

² Maximum power dissipation at VDDL and VDDSYN is at 1.9 V, and VDDH is at 3.465 V.

NOTE

Values in Table 5 represent VDDL based power dissipation and do not include I/O power dissipation over VDDH. I/O power dissipation varies widely by application due to buffer current, depending on external circuitry. The VDDSYN power dissipation is negligible.

6 DC Characteristics

Table 6 shows the DC electrical characteristics for the MPC866/859.

Table 6. DC Electrical Specifications

Characteristic	Symbol	Min	Max	Unit
Operating voltage	VDDL (core)	1.7	1.9	V
	VDDH (I/O)	3.135	3.465	V
	VDDSYN ¹	1.7	1.9	V
	Difference between VDDL to VDDSYN	—	100	mV
Input high voltage (all inputs except EXTAL and EXTCLK) ²	VIH	2.0	3.465	V

Table 9. Bus Operation Timings (continued)

Num	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
B22b	CLKOUT falling edge to $\overline{CS}$ asserted GPCM ACS = 11, TRLX = 0, EBDF = 0 (MAX = 0.25 x B1 + 6.3)	7.60	13.80	6.30	12.50	5.00	11.30	3.80	10.00	ns
B22c	CLKOUT falling edge to $\overline{CS}$ asserted GPCM ACS = 11, TRLX = 0, EBDF = 1 (MAX = 0.375 x B1 + 6.6)	10.90	18.00	10.90	16.00	7.00	14.10	5.20	12.30	ns
B23	CLKOUT rising edge to $\overline{CS}$ negated GPCM read access, GPCM write access ACS = 00, TRLX = 0 & CSNT = 0 (MAX = 0.00 x B1 + 8.00)	2.00	8.00	2.00	8.00	2.00	8.00	2.00	8.00	ns
B24	A(0:31) and BADDR(28:30) to $\overline{CS}$ asserted GPCM ACS = 10, TRLX = 0 (MIN = 0.25 x B1 - 2.00)	5.60	—	4.30	—	3.00	—	1.80	—	ns
B24a	A(0:31) and BADDR(28:30) to $\overline{CS}$ asserted GPCM ACS = 11, TRLX = 0 (MIN = 0.50 x B1 - 2.00)	13.20	—	10.50	—	8.00	—	5.60	—	ns
B25	CLKOUT rising edge to $\overline{OE}$, $\overline{WE}$ (0:3) asserted (MAX = 0.00 x B1 + 9.00)	—	9.00	—	9.00	—	9.00	—	9.00	ns
B26	CLKOUT rising edge to $\overline{OE}$ negated (MAX = 0.00 x B1 + 9.00)	2.00	9.00	2.00	9.00	2.00	9.00	2.00	9.00	ns
B27	A(0:31) and BADDR(28:30) to $\overline{CS}$ asserted GPCM ACS = 10, TRLX = 1 (MIN = 1.25 x B1 - 2.00)	35.90	—	29.30	—	23.00	—	16.90	—	ns
B27a	A(0:31) and BADDR(28:30) to $\overline{CS}$ asserted GPCM ACS = 11, TRLX = 1 (MIN = 1.50 x B1 - 2.00)	43.50	—	35.50	—	28.00	—	20.70	—	ns
B28	CLKOUT rising edge to $\overline{WE}$ (0:3) negated GPCM write access CSNT = 0 (MAX = 0.00 x B1 + 9.00)	—	9.00	—	9.00	—	9.00	—	9.00	ns
B28a	CLKOUT falling edge to $\overline{WE}$ (0:3) negated GPCM write access TRLX = 0,1, CSNT = 1, EBDF = 0 (MAX = 0.25 x B1 + 6.80)	7.60	14.30	6.30	13.00	5.00	11.80	3.80	10.50	ns
B28b	CLKOUT falling edge to $\overline{CS}$ negated GPCM write access TRLX = 0,1, CSNT = 1, ACS = 10 or ACS = 11, EBDF = 0 (MAX = 0.25 x B1 + 6.80)	—	14.30	—	13.00	—	11.80	—	10.50	ns
B28c	CLKOUT falling edge to $\overline{WE}$ (0:3) negated GPCM write access TRLX = 0, CSNT = 1 write access TRLX = 0,1, CSNT = 1, EBDF = 1 (MAX = 0.375 x B1 + 6.6)	10.90	18.00	10.90	18.00	7.00	14.30	5.20	12.30	ns

Table 9. Bus Operation Timings (continued)

Num	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
B30	$\overline{CS}$, $\overline{WE}(0:3)$ negated to A(0:31), BADDR(28:30) invalid GPCM write access ⁷ (MIN = 0.25 x B1 – 2.00)	5.60	—	4.30	—	3.00	—	1.80	—	ns
B30a	$\overline{WE}(0:3)$ negated to A(0:31), BADDR(28:30) invalid GPCM, write access, TRLX = 0, CSNT = 1, $\overline{CS}$ negated to A(0:31) invalid GPCM write access TRLX = 0, CSNT = 1 ACS = 10, or ACS == 11, EBDF = 0 (MIN = 0.50 x B1 – 2.00)	13.20	—	10.50	—	8.00	—	5.60	—	ns
B30b	$\overline{WE}(0:3)$ negated to A(0:31) invalid GPCM BADDR(28:30) invalid GPCM write access, TRLX = 1, CSNT = 1. $\overline{CS}$ negated to A(0:31) invalid GPCM write access TRLX = 1, CSNT = 1, ACS = 10, or ACS == 11 EBDF = 0 (MIN = 1.50 x B1 – 2.00)	43.50	—	35.50	—	28.00	—	20.70	—	ns
B30c	$\overline{WE}(0:3)$ negated to A(0:31), BADDR(28:30) invalid GPCM write access, TRLX = 0, CSNT = 1. $\overline{CS}$ negated to A(0:31) invalid GPCM write access, TRLX = 0, CSNT = 1 ACS = 10, ACS == 11, EBDF = 1 (MIN = 0.375 x B1 – 3.00)	8.40	—	6.40	—	4.50	—	2.70	—	ns
B30d	$\overline{WE}(0:3)$ negated to A(0:31), BADDR(28:30) invalid GPCM write access TRLX = 1, CSNT = 1, $\overline{CS}$ negated to A(0:31) invalid GPCM write access TRLX = 1, CSNT = 1, ACS = 10 or 11, EBDF = 1	38.67	—	31.38	—	24.50	—	17.83	—	ns
B31	CLKOUT falling edge to $\overline{CS}$ valid, as requested by control bit CST4 in the corresponding word in the UPM (MAX = 0.00 X B1 + 6.00)	1.50	6.00	1.50	6.00	1.50	6.00	1.50	6.00	ns
B31a	CLKOUT falling edge to $\overline{CS}$ valid, as requested by control bit CST1 in the corresponding word in the UPM (MAX = 0.25 x B1 + 6.80)	7.60	14.30	6.30	13.00	5.00	11.80	3.80	10.50	ns
B31b	CLKOUT rising edge to $\overline{CS}$ valid, as requested by control bit CST2 in the corresponding word in the UPM (MAX = 0.00 x B1 + 8.00)	1.50	8.00	1.50	8.00	1.50	8.00	1.50	8.00	ns
B31c	CLKOUT rising edge to $\overline{CS}$ valid, as requested by control bit CST3 in the corresponding word in the UPM (MAX = 0.25 x B1 + 6.30)	7.60	13.80	6.30	12.50	5.00	11.30	3.80	10.00	ns

Bus Signal Timing

Figure 19 shows the timing for the external bus controlled by the UPM.

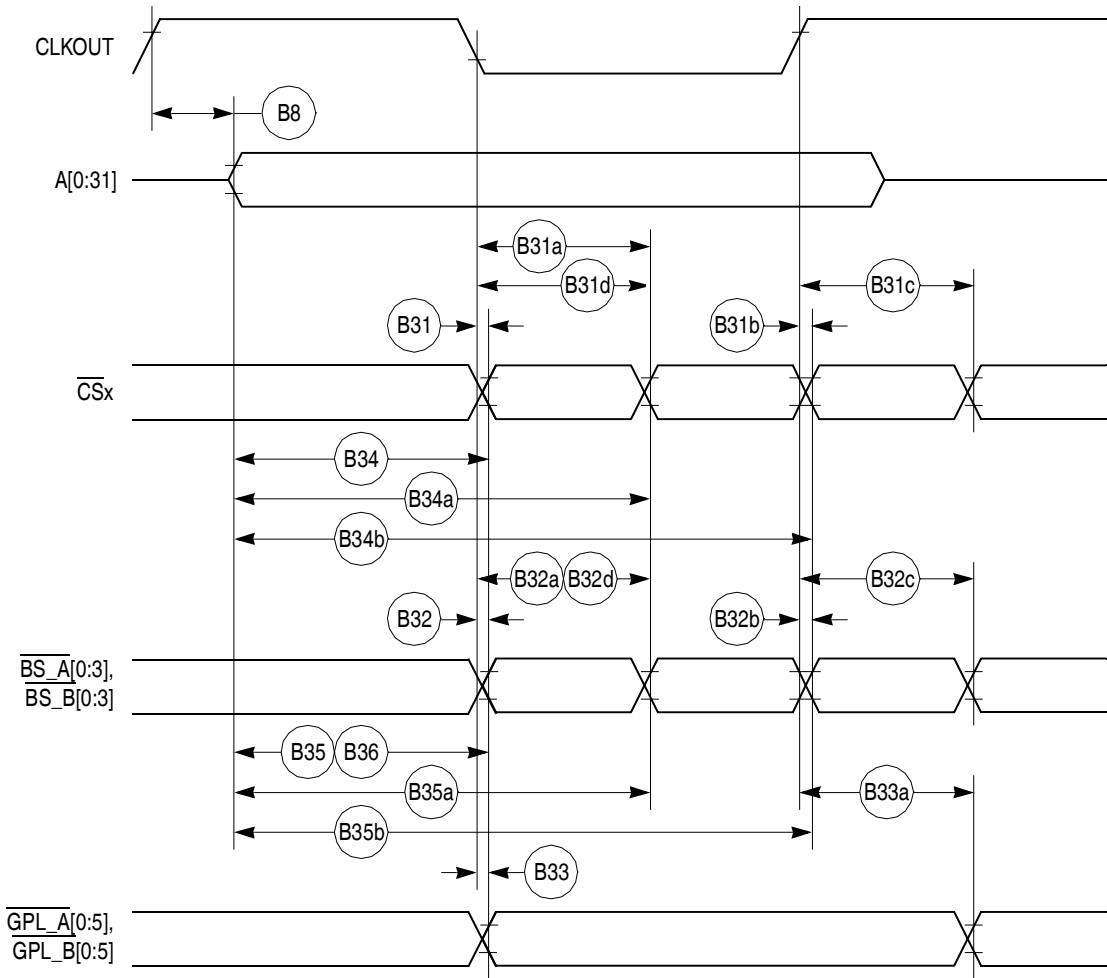


Figure 19. External Bus Timing (UPM Controlled Signals)

Bus Signal Timing

Figure 22 shows the timing for the synchronous external master access controlled by the GPCM.

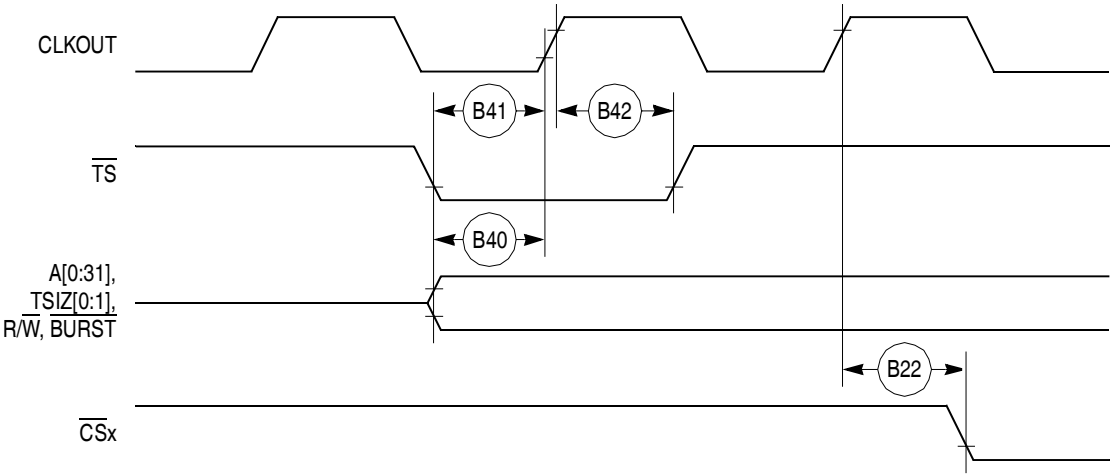


Figure 22. Synchronous External Master Access Timing (GPCM Handled ACS = 00)

Figure 27 shows the PCMCIA access cycle timing for the external bus read.

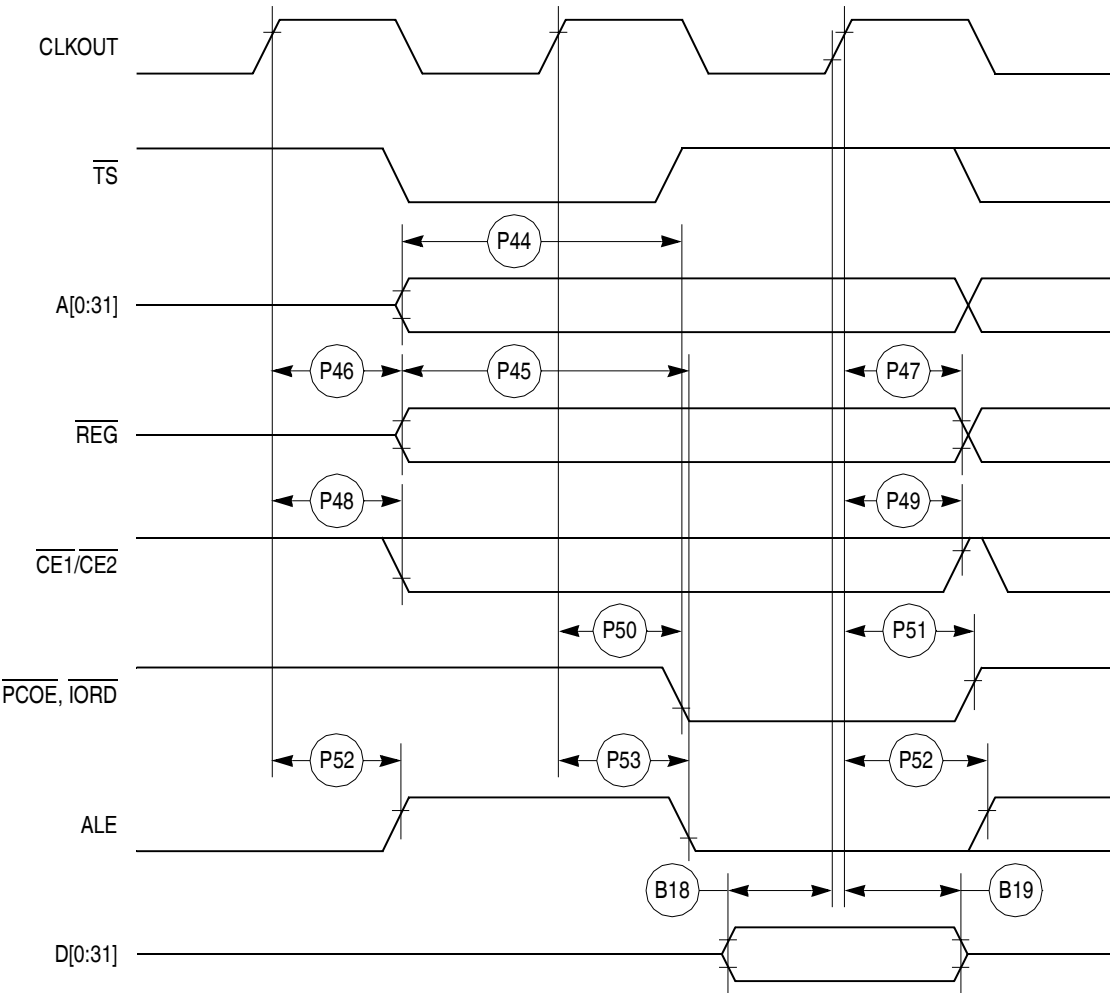


Figure 27. PCMCIA Access Cycles Timing External Bus Read

Table 13 shows the debug port timing for the MPC866/859.

Table 13. Debug Port Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
D61	DSCK cycle time	$3 \times T_{\text{CLOCKOUT}}$	—	
D62	DSCK clock pulse width	$1.25 \times T_{\text{CLOCKOUT}}$	—	
D63	DSCK rise and fall times	0.00	3.00	ns
D64	DSDI input data setup time	8.00	—	ns
D65	DSDI data hold time	5.00	—	ns
D66	DSCK low to DSDO data valid	0.00	15.00	ns
D67	DSCK low to DSDO invalid	0.00	2.00	ns

Figure 32 shows the input timing for the debug port clock.

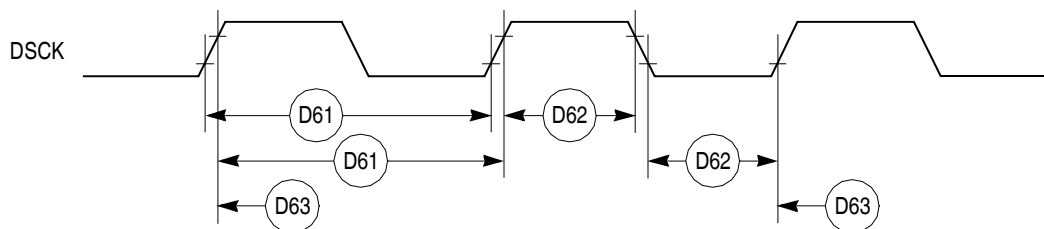


Figure 32. Debug Port Clock Input Timing

Figure 33 shows the timing for the debug port.

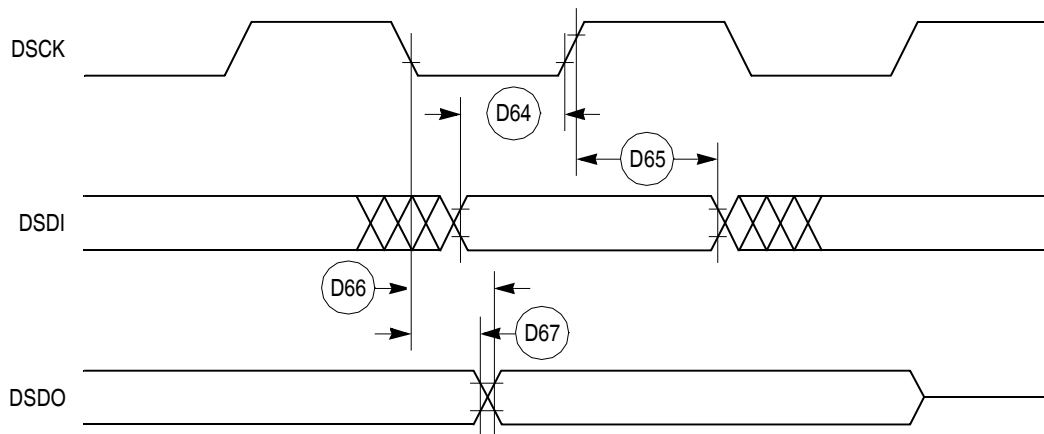


Figure 33. Debug Port Timings

Figure 36 shows the reset timing for the debug port configuration.

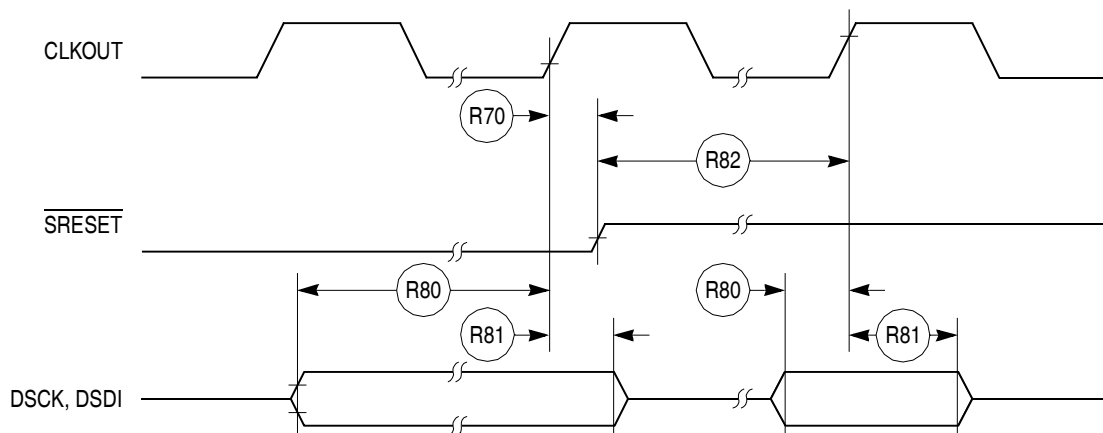


Figure 36. Reset Timing—Debug Port Configuration

11 IEEE 1149.1 Electrical Specifications

Table 15 shows the JTAG timings for the MPC866/859 shown in Figure 37 through Figure 40.

Table 15. JTAG Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
J82	TCK cycle time	100.00	—	ns
J83	TCK clock pulse width measured at 1.5 V	40.00	—	ns
J84	TCK rise and fall times	0.00	10.00	ns
J85	TMS, TDI data setup time	5.00	—	ns
J86	TMS, TDI data hold time	25.00	—	ns
J87	TCK low to TDO data valid	—	27.00	ns
J88	TCK low to TDO data invalid	0.00	—	ns
J89	TCK low to TDO high impedance	—	20.00	ns
J90	$\overline{\text{TRST}}$ assert time	100.00	—	ns
J91	$\overline{\text{TRST}}$ setup time to TCK low	40.00	—	ns
J92	TCK falling edge to output valid	—	50.00	ns
J93	TCK falling edge to output valid out of high impedance	—	50.00	ns
J94	TCK falling edge to output high impedance	—	50.00	ns
J95	Boundary scan input valid to TCK rising edge	50.00	—	ns
J96	TCK rising edge to boundary scan input invalid	50.00	—	ns

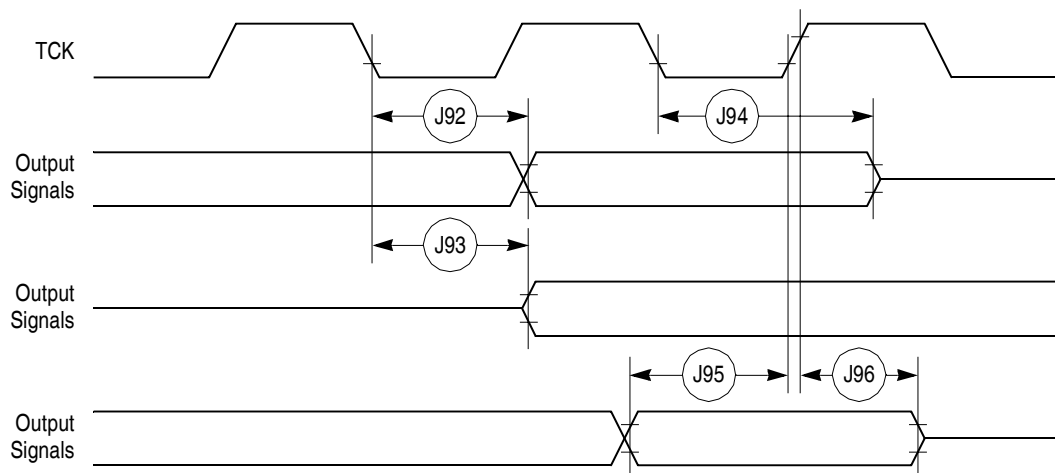


Figure 40. Boundary Scan (JTAG) Timing Diagram

12 CPM Electrical Characteristics

This section provides the AC and DC electrical specifications for the communications processor module (CPM) of the MPC866/859.

12.1 PIP/PIO AC Electrical Specifications

Table 16 shows the PIP/PIO AC timings as shown in Figure 41 through Figure 45.

Table 16. PIP/PIO Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
21	Data-in setup time to STBI low	0	—	ns
22	Data-In hold time to STBI high	2.5 – t ₃ ¹	—	clk
23	STBI pulse width	1.5	—	clk
24	STBO pulse width	1 clk – 5ns	—	ns
25	Data-out setup time to STBO low	2	—	clk
26	Data-out hold time from STBO high	5	—	clk
27	STBI low to STBO low (Rx interlock)	—	2	clk
28	STBI low to STBO high (Tx interlock)	2	—	clk
29	Data-in setup time to clock high	15	—	ns
30	Data-in hold time from clock high	7.5	—	ns
31	Clock low to data-out valid (CPU writes data, control, or direction)	—	25	ns

¹ t₃ = Specification 23

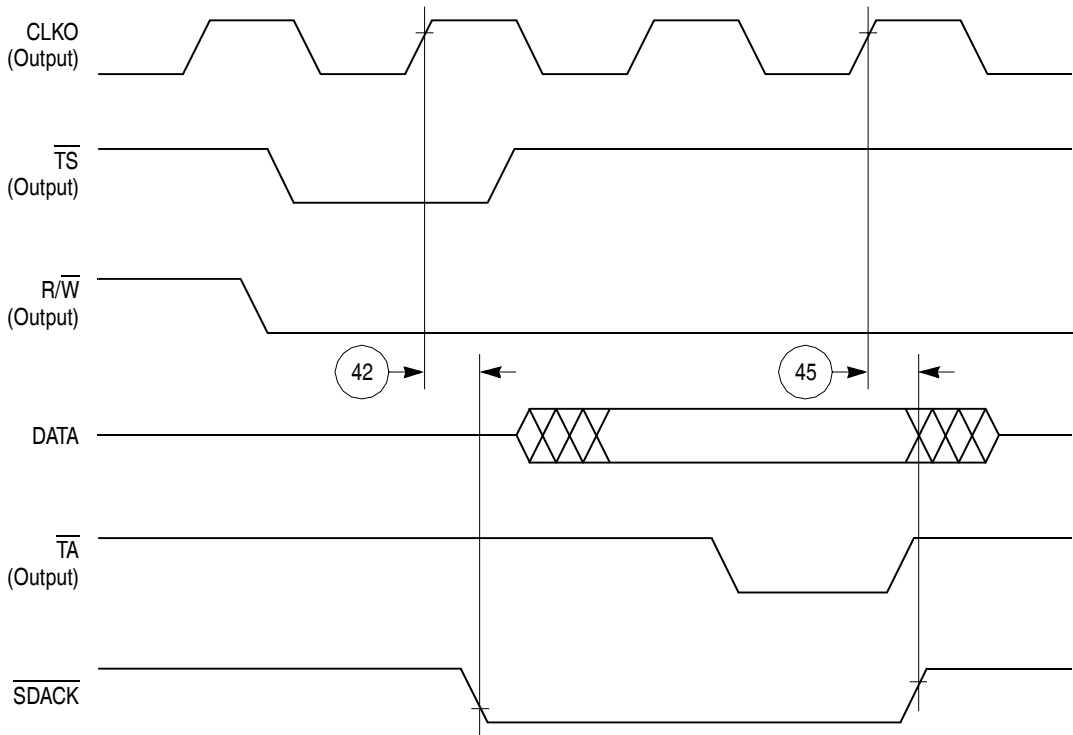


Figure 50. $\overline{\text{SDACK}}$ Timing Diagram—Peripheral Read, Internally-Generated $\overline{\text{TA}}$

12.4 Baud Rate Generator AC Electrical Specifications

Table 19 shows the baud rate generator timings as shown in Figure 51.

Table 19. Baud Rate Generator Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
50	BRGO rise and fall time	—	10	ns
51	BRGO duty cycle	40	60	%
52	BRGO cycle	40	—	ns

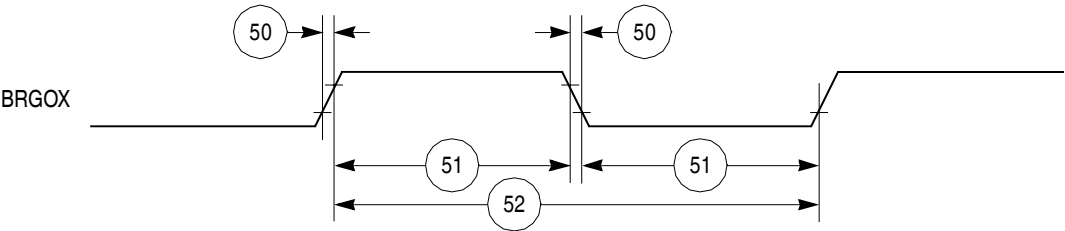


Figure 51. Baud Rate Generator Timing Diagram

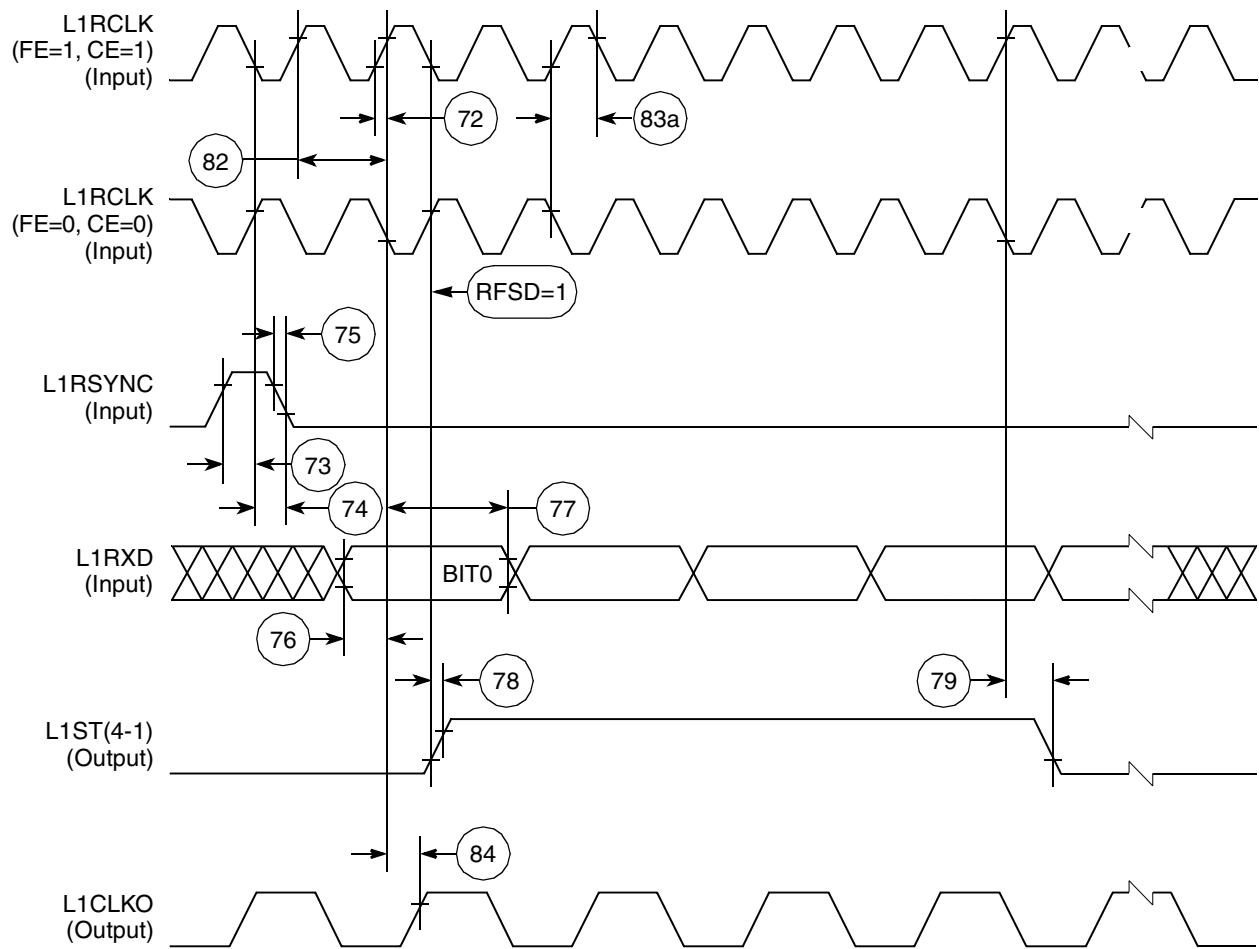


Table 24. Ethernet Timing (continued)

Num	Characteristic	All Frequencies		Unit
		Min	Max	
134	TENA inactive delay (from TCLK1 rising edge)	10	50	ns
135	$\overline{\text{RSTRT}}$ active delay (from TCLK1 falling edge)	10	50	ns
136	$\overline{\text{RSTRT}}$ inactive delay (from TCLK1 falling edge)	10	50	ns
137	$\overline{\text{REJECT}}$ width low	1	—	CLK
138	CLKO1 low to $\overline{\text{SDACK}}$ asserted ²	—	20	ns
139	CLKO1 low to $\overline{\text{SDACK}}$ negated ²	—	20	ns

¹ The ratios SyncCLK/RCLK1 and SyncCLK/TCLK1 must be greater or equal to 2/1.

² $\overline{\text{SDACK}}$ is asserted whenever the SDMA writes the incoming frame DA into memory.

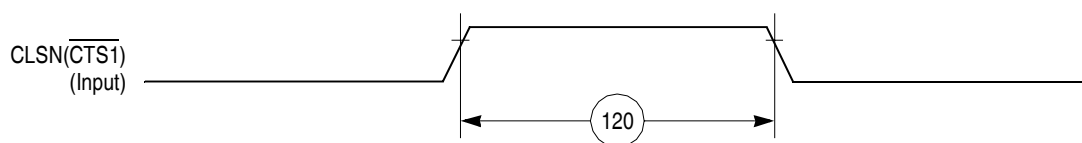


Figure 61. Ethernet Collision Timing Diagram

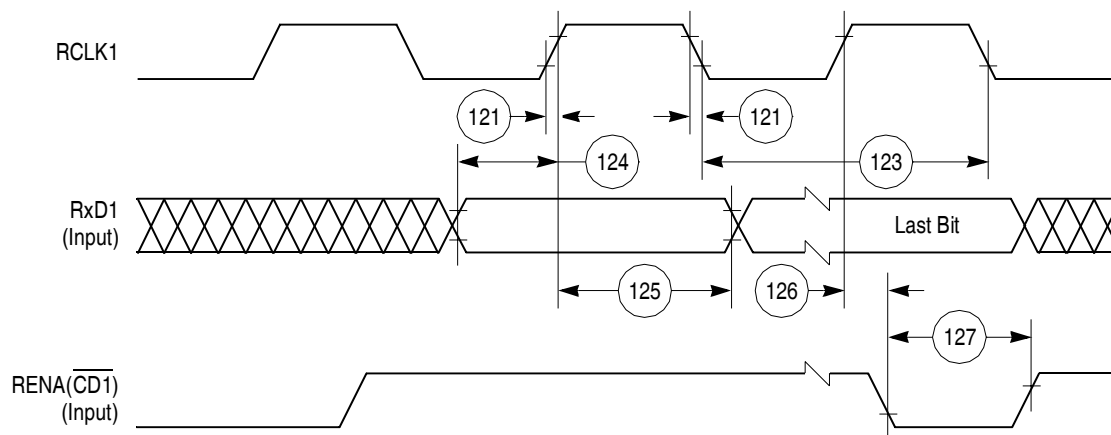


Figure 62. Ethernet Receive Timing Diagram

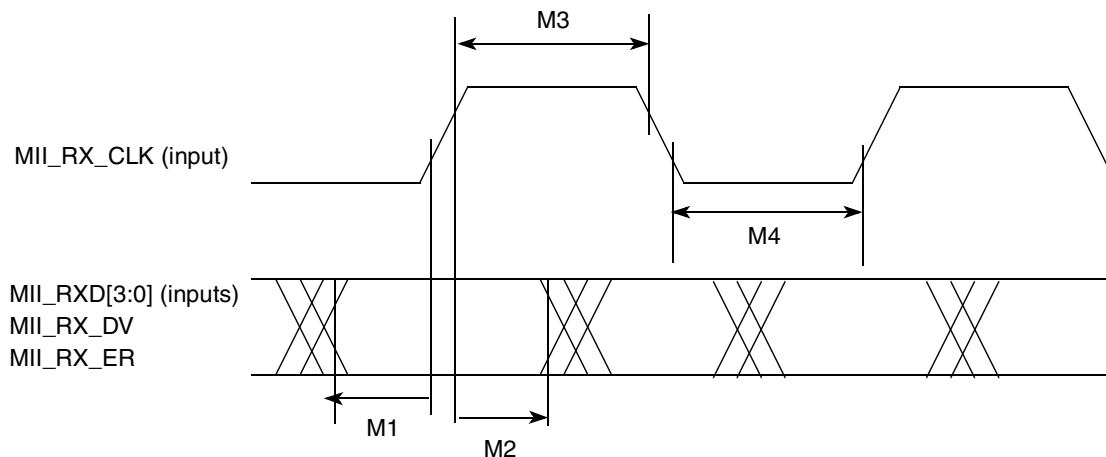


Figure 74. MII Receive Signal Timing Diagram

14.2 MII Transmit Signal Timing (MII_TXD[3:0], MII_TX_EN, MII_TX_ER, MII_TX_CLK)

The transmitter functions correctly up to a MII_TX_CLK maximum frequency of 25 MHz +1%. There is no minimum frequency requirement. In addition, the processor clock frequency must exceed the MII_TX_CLK frequency - 1%.

Table 34 shows information on the MII transmit signal timing.

Table 34. MII Transmit Signal Timing

Num	Characteristic	Min	Max	Unit
M5	MII_TX_CLK to MII_TXD[3:0], MII_TX_EN, MII_TX_ER invalid	5	—	ns
M6	MII_TX_CLK to MII_TXD[3:0], MII_TX_EN, MII_TX_ER valid	—	25	—
M7	MII_TX_CLK pulse width high	35%	65%	MII_TX_CLK period
M8	MII_TX_CLK pulse width low	35%	65%	MII_TX_CLK period

Figure 75 shows the MII transmit signal timing diagram.

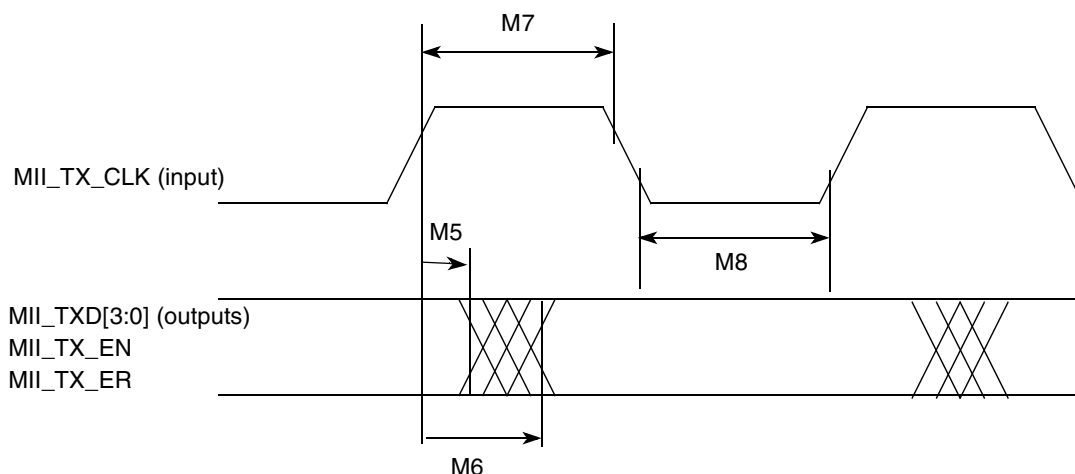


Figure 75. MII Transmit Signal Timing Diagram

14.3 MII Async Inputs Signal Timing (MII_CRCS, MII_COL)

Table 35 shows the timing for on the MII async inputs signal.

Table 35. MII Async Inputs Signal Timing

Num	Characteristic	Min	Max	Unit
M9	MII_CRCS, MII_COL minimum pulse width	1.5	—	MII_TX_CLK period

Figure 76 shows the MII asynchronous inputs signal timing diagram.

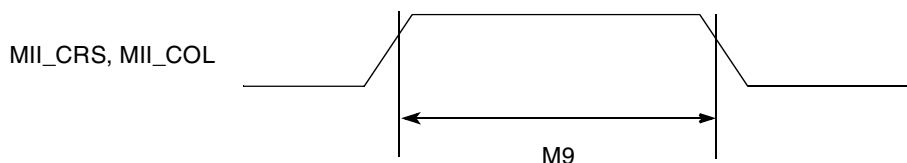


Figure 76. MII Async Inputs Timing Diagram

14.4 MII Serial Management Channel Timing (MII_MDIO, MII_MDC)

Table 36 shows the timing for the MII serial management channel signal. The FEC functions correctly with a maximum MDC frequency in excess of 2.5 MHz. The exact upper bound is under investigation.

Table 36. MII Serial Management Channel Timing

Num	Characteristic	Min	Max	Unit
M10	MII_MDC falling edge to MII_MDIO output invalid (minimum propagation delay)	0	—	ns
M11	MII_MDC falling edge to MII_MDIO output valid (maximum propagation delay)	—	25	ns
M12	MII_MDIO (input) to MII_MDC rising edge setup	10	—	ns

15 Mechanical Data and Ordering Information

Table 37 shows information on the MPC866/859 derivative devices.

Table 37. MPC866/859 Derivatives

Device	Number of SCCs ¹	Ethernet Support	Multi-Channel HDLC Support	ATM Support	Cache Size	
					Instruction	Data
MPC866T	4	10/100 Mbps	Yes	Yes	4 Kbyte	4 Kbytes
MPC866P	4	10/100 Mbps	Yes	Yes	16 Kbyte	8 Kbytes
MPC859T	1 (SCC1)	10/100 Mbps	Yes	Yes	4 Kbyte	4 Kbytes
MPC859DSL	1 (SCC1)	10/100 Mbps	No	Up to 4 addresses	4 Kbyte	4 Kbytes

¹ Serial communications controller (SCC).

Table 38 identifies the packages and operating frequencies orderable for the MPC866/859 derivative devices.

Table 38. MPC866/859 Package/Frequency Orderable

Package Type	Temperature (Tj)	Frequency (MHz)	Order Number
Plastic ball grid array (ZP suffix) Non lead free	0° to 95°C	50	MPC859DSLZP50A
		66	MPC859DSLZP66A
		100	MPC859PZP100A MPC859TZP100A MPC866PZP100A MPC866TZP100A
		133	MPC859PZP133A MPC859TZP133A MPC866PZP133A MPC866TZP133A
Plastic ball grid array (CZP suffix) Non lead free	-40° to 100°C	50	MPC859DSLCZP50A
		66	MPC859DSLCZP66A
		100	MPC859PCZP100A MPC859TCZP100A MPC866PCZP100A MPC866TCZP100A

Table 38. MPC866/859 Package/Frequency Orderable (continued)

Plastic ball grid array (VR suffix) Lead free	0° to 95°C	50	MPC859DSLVR50A
		66	MPC859DSLVR66A
		100	MPC859PVR100A MPC859TVR100A MPC866PVR100A MPC866TVR100A
		133	MPC859PVR133A MPC859TVR133A MPC866PVR133A MPC866TVR133A
Plastic ball grid array (CVR suffix) Lead free	–40° to 100°C	50	MPC859DSLCVR50A
		66	MPC859DSLCVR66A
		100	MPC859PCVR100A MPC859TCVR100A MPC866PCVR100A MPC866TCVR100A

Table 39. Pin Assignments (continued)

Name	Pin Number	Type
$\overline{\text{BR}}$	G4	Bidirectional
$\overline{\text{BG}}$	E2	Bidirectional
$\overline{\text{BB}}$	E1	Bidirectional Active Pull-up
$\overline{\text{FRZ}}$ $\overline{\text{IRQ6}}$	G3	Bidirectional
$\overline{\text{IRQ0}}$	V14	Input
$\overline{\text{IRQ1}}$	U14	Input
M_TX_CLK $\overline{\text{IRQ7}}$	W15	Input
$\overline{\text{CS}}[0:5]$	C3, A2, D4, E4, A4, B4	Output
$\overline{\text{CS6}}$ $\overline{\text{CE1_B}}$	D5	Output
$\overline{\text{CS7}}$ $\overline{\text{CE2_B}}$	C4	Output
$\overline{\text{WE0}}$ $\overline{\text{BS_B0}}$ $\overline{\text{IORD}}$	C7	Output
$\overline{\text{WE1}}$ $\overline{\text{BS_B1}}$ $\overline{\text{IOWR}}$	A6	Output
$\overline{\text{WE2}}$ $\overline{\text{BS_B2}}$ $\overline{\text{PCOE}}$	B6	Output
$\overline{\text{WE3}}$ $\overline{\text{BS_B3}}$ $\overline{\text{PCWE}}$	A5	Output
$\overline{\text{BS_A}}[0:3]$	D8, C8, A7, B8	Output
$\overline{\text{GPL_A0}}$ $\overline{\text{GPL_B0}}$	D7	Output
$\overline{\text{OE}}$ $\overline{\text{GPL_A1}}$ $\overline{\text{GPL_B1}}$	C6	Output
$\overline{\text{GPL_A}}[2:3]$ $\overline{\text{GPL_B}}[2:3]$ $\overline{\text{CS}}[2-3]$	B5, C5	Output
UPWAITA $\overline{\text{GPL_A4}}$	C1	Bidirectional

Table 39. Pin Assignments (continued)

Name	Pin Number	Type
UPWAITB GPL_B4	B1	Bidirectional
GPL_A5	D3	Output
PORESET	R2	Input
RSTCONF	P3	Input
HRESET	N4	Open-drain
SRESET	P2	Open-drain
XTAL	P1	Analog Output
EXTAL	N1	Analog Input (3.3V only)
CLKOUT	W3	Output
EXTCLK	N2	Input (3.3V only)
TEXP	N3	Output
ALE_A MII-TXD1	K2	Output
CE1_A MII-TXD2	B3	Output
CE2_A MII-TXD3	A3	Output
WAIT_A SOC_Split ²	R3	Input
WAIT_B	R4	Input
IP_A0 UTPB_Split0 ² MII-RXD3	T5	Input
IP_A1 UTPB_Split1 ² MII-RXD2	T4	Input
IP_A2 IOIS16_A UTPB_Split2 ² MII-RXD1	U3	Input
IP_A3 UTPB_Split3 ² MII-RXD0	W2	Input
IP_A4 UTPB_Split4 ² MII-RXCLK	U4	Input

Table 39. Pin Assignments (continued)

Name	Pin Number	Type
OP3 MODCK2 DSDO	M4	Bidirectional
BADDR30 $\overline{\text{REG}}$	K4	Output
BADDR[28:29]	M3, M2	Output
$\overline{\text{AS}}$	L3	Input
PA15 RXD1 RXD4	C18	Bidirectional
PA14 TXD1 TXD4	D17	Bidirectional (Optional: Open-drain)
PA13 RXD2	E17	Bidirectional
PA12 TXD2	F17	Bidirectional (Optional: Open-drain)
PA11 L1TXDB RXD3	G16	Bidirectional (Optional: Open-drain)
PA10 L1RXDB TXD3	J17	Bidirectional (Optional: Open-drain)
PA9 L1TXDA RXD4	K18	Bidirectional (Optional: Open-drain)
PA8 L1RXDA TXD4	L17	Bidirectional (Optional: Open-drain)
PA7 CLK1 L1RCLKA BRGO1 TIN1	M19	Bidirectional
PA6 CLK2 $\overline{\text{TOUT1}}$	M17	Bidirectional