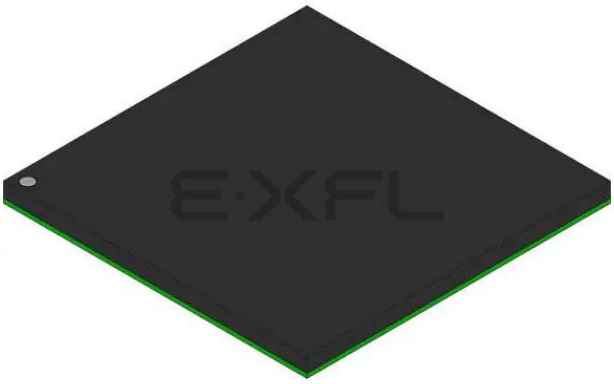

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	MPC8xx
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	133MHz
Co-Processors/DSP	Communications; CPM
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10Mbps (1), 10/100Mbps (1)
SATA	-
USB	-
Voltage - I/O	3.3V
Operating Temperature	0°C ~ 95°C (TA)
Security Features	-
Package / Case	357-BBGA
Supplier Device Package	357-PBGA (25x25)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mpc859pvr133a

Table 1 shows the functionality supported by the members of the MPC866/859 family.

2 Features

Table 1. MPC866 Family Functionality

Part	Cache		Ethernet		SCC	SMC
	Instruction	Data	10T	10/100		
MPC866P	16 Kbytes	8 Kbytes	Up to 4	1	4	2
MPC866T	4 Kbytes	4 Kbytes	Up to 4	1	4	2
MPC859P	16 Kbytes	8 Kbytes	1	1	1	2
MPC859T	4 Kbytes	4 Kbytes	1	1	1	2
MPC859DSL	4 Kbytes	4 Kbytes	1	1	1 [1]	1 [2]
MPC852T [3]	4 KBytes	4 Kbytes	2	1	2	1

[1] On the MPC859DSL, the SCC (SCC1) is for ethernet only. Also, the MPC859DSL does not support the Time Slot Assigner (TSA).

[2] On the MPC859DSL, the SMC (SMC1) is for UART only.

[3] For more details on the MPC852T, please refer to the *MPC852T Hardware Specifications.*

The following list summarizes the key MPC866/859 features:

- Embedded single-issue, 32-bit PowerPC™ core (implementing the PowerPC architecture) with thirty-two 32-bit general-purpose registers (GPRs)
  - — The core performs branch prediction with conditional prefetch, without conditional execution
  - — 4- or 8-Kbyte data cache and 4- or 16-Kbyte instruction cache (see Table 1)
    - – 16-Kbyte instruction cache (MPC866P and MPC859P) is four-way, set-associative with 256 sets; 4-Kbyte instruction cache (MPC866T, MPC859T, and MPC859DSL) is two-way, set-associative with 128 sets.
    - – 8-Kbyte data cache (MPC866P and MPC859P) is two-way, set-associative with 256 sets; 4-Kbyte data cache(MPC866T, MPC859T, and MPC859DSL) is two-way, set-associative with 128 sets.
    - – Cache coherency for both instruction and data caches is maintained on 128-bit (4-word) cache blocks
    - – Caches are physically addressed, implement a least recently used (LRU) replacement algorithm, and are lockable on a cache block basis.
  - — MMUs with 32-entry TLB, fully associative instruction and data TLBs
  - — MMUs support multiple page sizes of 4, 16, and 512 Kbytes, and 8 Mbytes; 16 virtual address spaces and 16 protection groups.
  - — Advanced on-chip-emulation debug mode
- The MPC866/859 provides enhanced ATM functionality over that of the MPC860SAR. The MPC866/859 adds major new features available in 'enhanced SAR' (ESAR) mode, including the following:
  - — Improved operation, administration, and maintenance (OAM) support
  - — OAM performance monitoring (PM) support
  - — Multiple APC priority levels available to support a range of traffic pace requirements

- One serial peripheral interface (SPI)
  - Supports master and slave modes
  - Supports multiple-master operation on the same bus
- One inter-integrated circuit (I^2C) port
  - Supports master and slave modes
  - Multiple-master environment support
- Time slot assigner (TSA) (MPC859DSL does not have TSA.)
  - Allows SCCs and SMCs to run in multiplexed and/or non-multiplexed operation
  - Supports T1, CEPT, PCM highway, ISDN basic rate, ISDN primary rate, user-defined
  - 1- or 8-bit resolution
  - Allows independent transmit and receive routing, frame synchronization, and clocking
  - Allows dynamic changes
  - On MPC866P and MPC866T, can be internally connected to six serial channels (four SCCs and two SMCs); on MPC859P and MPC859T, can be connected to three serial channels (one SCC and two SMCs).
- Parallel interface port (PIP)
  - Centronics interface support
  - Supports fast connection between compatible ports on MPC866/859 or MC68360
- PCMCIA interface
  - Master (socket) interface, compliant with PCI Local Bus Specification (Rev 2.1)
  - Supports one or two PCMCIA sockets whether ESAR functionality is enabled
  - Eight memory or I/O windows supported
- Debug interface
  - Eight comparators: four operate on instruction address, two operate on data address, and two operate on data.
  - Supports conditions: $= \neq < >$
  - Each watchpoint can generate a breakpoint internally
- Normal high and normal low power modes to conserve power
- 1.8 V core and 3.3 V I/O operation with 5-V TTL compatibility; refer to Table 6 for a listing of the 5-V tolerant pins.
- 357-pin plastic ball grid array (PBGA) package
- Operation up to 133 MHz

Table 9. Bus Operation Timings (continued)

Num	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
B22b	CLKOUT falling edge to $\overline{CS}$ asserted GPCM ACS = 11, TRLX = 0, EBDF = 0 (MAX = 0.25 x B1 + 6.3)	7.60	13.80	6.30	12.50	5.00	11.30	3.80	10.00	ns
B22c	CLKOUT falling edge to $\overline{CS}$ asserted GPCM ACS = 11, TRLX = 0, EBDF = 1 (MAX = 0.375 x B1 + 6.6)	10.90	18.00	10.90	16.00	7.00	14.10	5.20	12.30	ns
B23	CLKOUT rising edge to $\overline{CS}$ negated GPCM read access, GPCM write access ACS = 00, TRLX = 0 & CSNT = 0 (MAX = 0.00 x B1 + 8.00)	2.00	8.00	2.00	8.00	2.00	8.00	2.00	8.00	ns
B24	A(0:31) and BADDR(28:30) to $\overline{CS}$ asserted GPCM ACS = 10, TRLX = 0 (MIN = 0.25 x B1 - 2.00)	5.60	—	4.30	—	3.00	—	1.80	—	ns
B24a	A(0:31) and BADDR(28:30) to $\overline{CS}$ asserted GPCM ACS = 11, TRLX = 0 (MIN = 0.50 x B1 - 2.00)	13.20	—	10.50	—	8.00	—	5.60	—	ns
B25	CLKOUT rising edge to $\overline{OE}$, $\overline{WE}$(0:3) asserted (MAX = 0.00 x B1 + 9.00)	—	9.00	—	9.00	—	9.00	—	9.00	ns
B26	CLKOUT rising edge to $\overline{OE}$ negated (MAX = 0.00 x B1 + 9.00)	2.00	9.00	2.00	9.00	2.00	9.00	2.00	9.00	ns
B27	A(0:31) and BADDR(28:30) to $\overline{CS}$ asserted GPCM ACS = 10, TRLX = 1 (MIN = 1.25 x B1 - 2.00)	35.90	—	29.30	—	23.00	—	16.90	—	ns
B27a	A(0:31) and BADDR(28:30) to $\overline{CS}$ asserted GPCM ACS = 11, TRLX = 1 (MIN = 1.50 x B1 - 2.00)	43.50	—	35.50	—	28.00	—	20.70	—	ns
B28	CLKOUT rising edge to $\overline{WE}$(0:3) negated GPCM write access CSNT = 0 (MAX = 0.00 x B1 + 9.00)	—	9.00	—	9.00	—	9.00	—	9.00	ns
B28a	CLKOUT falling edge to $\overline{WE}$(0:3) negated GPCM write access TRLX = 0,1, CSNT = 1, EBDF = 0 (MAX = 0.25 x B1 + 6.80)	7.60	14.30	6.30	13.00	5.00	11.80	3.80	10.50	ns
B28b	CLKOUT falling edge to $\overline{CS}$ negated GPCM write access TRLX = 0,1, CSNT = 1, ACS = 10 or ACS = 11, EBDF = 0 (MAX = 0.25 x B1 + 6.80)	—	14.30	—	13.00	—	11.80	—	10.50	ns
B28c	CLKOUT falling edge to $\overline{WE}$(0:3) negated GPCM write access TRLX = 0, CSNT = 1 write access TRLX = 0,1, CSNT = 1, EBDF = 1 (MAX = 0.375 x B1 + 6.6)	10.90	18.00	10.90	18.00	7.00	14.30	5.20	12.30	ns

Table 9. Bus Operation Timings (continued)

Num	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
B35	A(0:31), BADDR(28:30) to $\overline{CS}$ valid, as requested by control bit BST4 in the corresponding word in the UPM (MIN = 0.25 x B1 – 2.00)	5.60	—	4.30	—	3.00	—	1.80	—	ns
B35a	A(0:31), BADDR(28:30), and D(0:31) to $\overline{BS}$ valid, as Requested by BST1 in the corresponding word in the UPM (MIN = 0.50 x B1 – 2.00)	13.20	—	10.50	—	8.00	—	5.60	—	ns
B35b	A(0:31), BADDR(28:30), and D(0:31) to $\overline{BS}$ valid, as requested by control bit BST2 in the corresponding word in the UPM (MIN = 0.75 x B1 – 2.00)	20.70	—	16.70	—	13.00	—	9.40	—	ns
B36	A(0:31), BADDR(28:30), and D(0:31) to $\overline{GPL}$ valid as requested by control bit GxT4 in the corresponding word in the UPM (MIN = 0.25 x B1 – 2.00)	5.60	—	4.30	—	3.00	—	1.80	—	ns
B37	UPWAIT valid to CLKOUT falling edge [8] (MIN = 0.00 x B1 + 6.00)	6.00	—	6.00	—	6.00	—	6.00	—	ns
B38	CLKOUT falling edge to UPWAIT valid[8] (MIN = 0.00 x B1 + 1.00)	1.00	—	1.00	—	1.00	—	1.00	—	ns
B39	$\overline{AS}$ valid to CLKOUT rising edge [9] (MIN = 0.00 x B1 + 7.00)	7.00	—	7.00	—	7.00	—	7.00	—	ns
B40	A(0:31), TSIZ(0:1), RD/$\overline{WR}$, $\overline{BURST}$, valid to CLKOUT rising edge (MIN = 0.00 x B1 + 7.00)	7.00	—	7.00	—	7.00	—	7.00	—	ns
B41	$\overline{TS}$ valid to CLKOUT rising edge (setup time) (MIN = 0.00 x B1 + 7.00)	7.00	—	7.00	—	7.00	—	7.00	—	ns
B42	CLKOUT rising edge to $\overline{TS}$ valid (hold time) (MIN = 0.00 x B1 + 2.00)	2.00	—	2.00	—	2.00	—	2.00	—	ns
B43	$\overline{AS}$ negation to memory controller signals negation (MAX = TBD)	—	TBD	—	TBD	—	TBD	—	TBD	ns

1 For part speeds above 50 MHz, use 9.80 ns for B11a.

2 The timing required for $\overline{BR}$ input is relevant when the MPC866/859 is selected to work with the internal bus arbiter. The timing for $\overline{BG}$ input is relevant when the MPC866/859 is selected to work with the external bus arbiter.

3 For part speeds above 50 MHz, use 2 ns for B17.

4 The D(0:31) and DP(0:3) input timings B18 and B19 refer to the rising edge of CLKOUT, in which the $\overline{TA}$ input signal is asserted.

5 For part speeds above 50 MHz, use 2 ns for B19.

6 The D(0:31) and DP(0:3) input timings B20 and B21 refer to the falling edge of CLKOUT. This timing is valid only for read accesses controlled by chip-selects under control of the UPM in the memory controller, for data beats, where DLT3 = 1 in the UPM RAM words. (This is only the case where data is latched on the falling edge of CLKOUT.)

7 The timing B30 refers to $\overline{CS}$ when ACS = 00 and to $\overline{WE}$(0:3) when CSNT = 0.

Figure 6 shows the timing for the external clock.

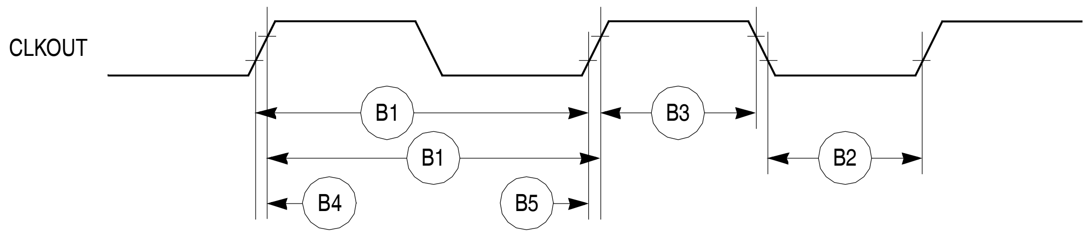


Figure 6. External Clock Timing

Figure 7 shows the timing for the synchronous output signals.

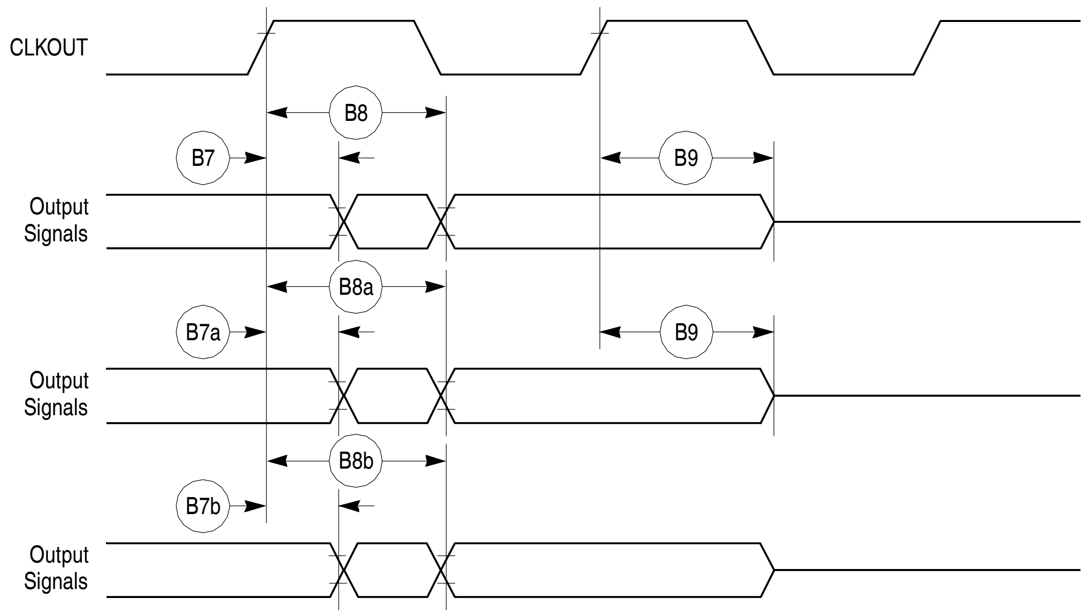


Figure 7. Synchronous Output Signals Timing

Figure 12 through Figure 15 show the timing for the external bus read controlled by various GPCM factors.

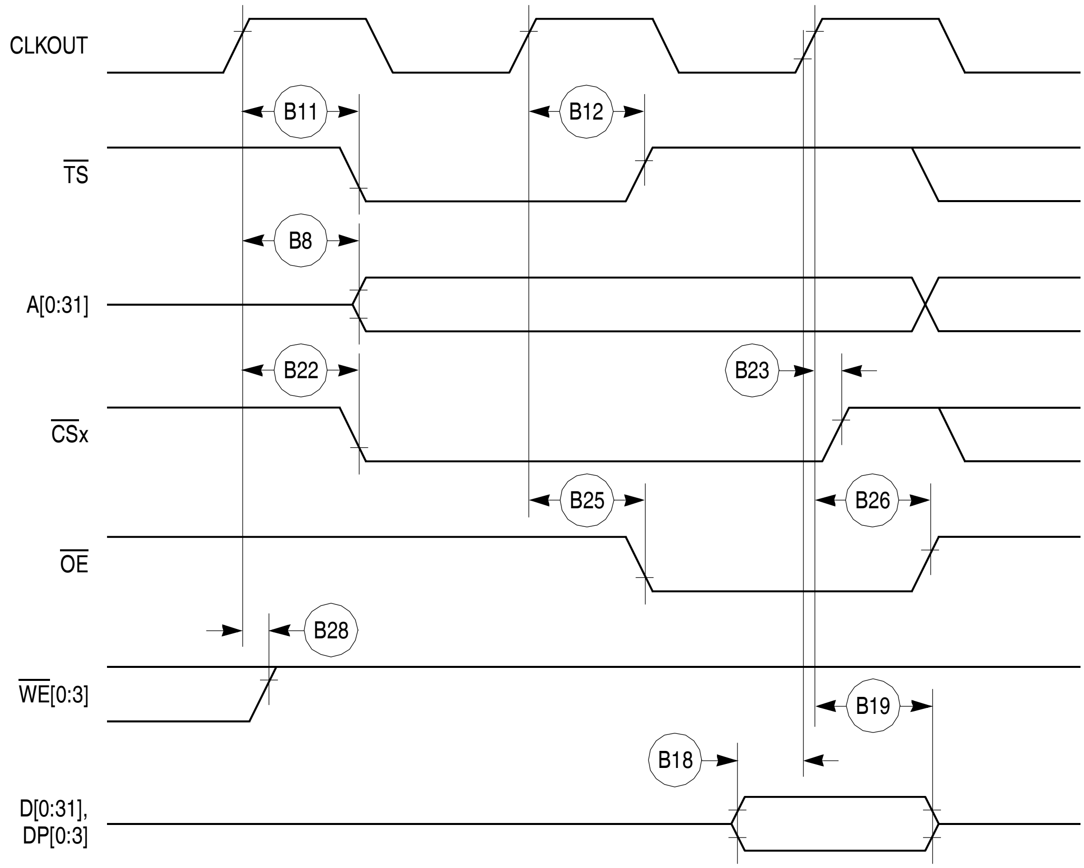


Figure 12. External Bus Read Timing (GPCM Controlled—ACS = 00)

Figure 22 shows the timing for the synchronous external master access controlled by the GPCM.

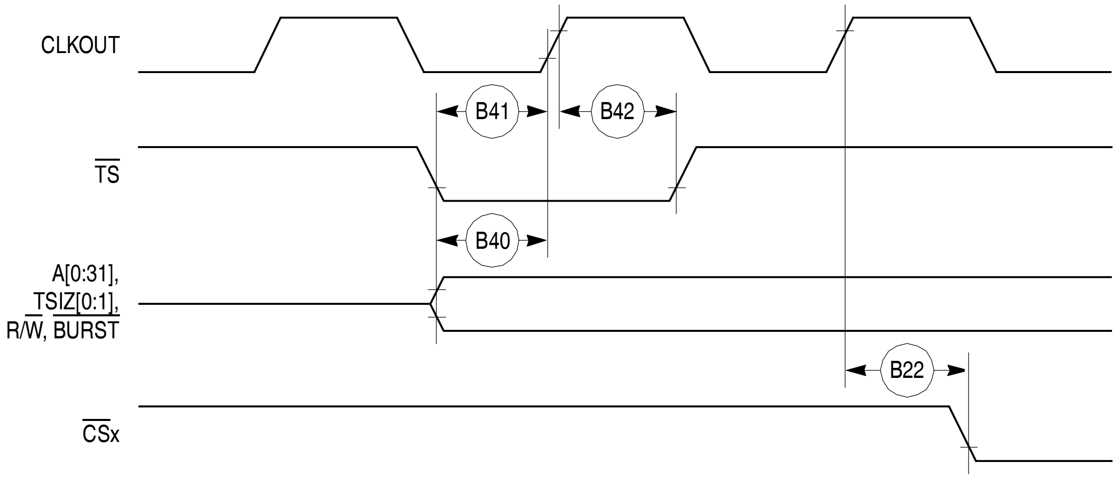


Figure 22. Synchronous External Master Access Timing (GPCM Handled ACS = 00)

Figure 23 shows the timing for the asynchronous external master memory access controlled by the GPCM.

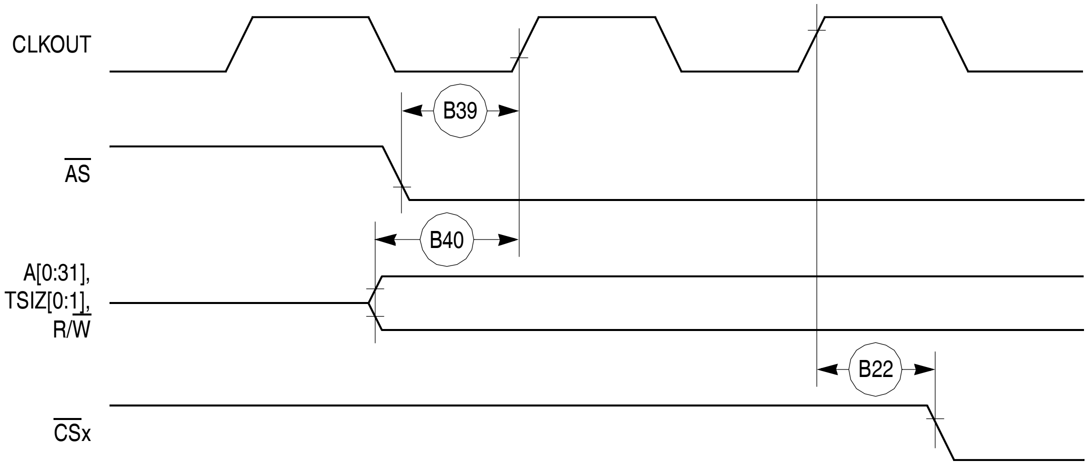


Figure 23. Asynchronous External Master Memory Access Timing (GPCM Controlled—ACS = 00)

Figure 24 shows the timing for the asynchronous external master control signals negation.

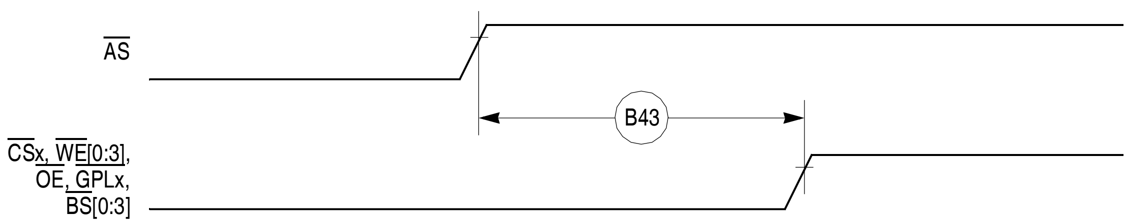


Figure 24. Asynchronous External Master—Control Signals Negation Timing

Table 10 shows the interrupt timing for the MPC866/859.

Table 10. Interrupt Timing

Num	Characteristic [1]	All Frequencies		Unit
		Min	Max	
I39	IRQx valid to CLKOUT rising edge (setup time)	6.00	—	ns
I40	IRQx hold time after CLKOUT	2.00	—	ns
I41	IRQx pulse width low	3.00	—	ns
I42	IRQx pulse width high	3.00	—	ns
I43	IRQx edge-to-edge time	4xT$_{CLOCKOUT}$	—	—

[1] The timings I39 and I40 describe the testing conditions under which the IRQ lines are tested when being defined as level sensitive. The IRQ lines are synchronized internally and do not have to be asserted or negated with reference to the CLKOUT.
The timings I41, I42, and I43 are specified to allow the correct function of the IRQ lines detection circuitry, and has no direct relation with the total system interrupt latency that the MPC866/859 is able to support.

Table 11. PCMCIA Timing (continued)

Num	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
P50	CLKOUT to PCOE, IORD, PCWE, IOWR assert time (MAX = 0.00 x B1 + 11.00)	—	11.00	—	11.00	—	11.00	—	11.00	ns
P51	CLKOUT to PCOE, IORD, PCWE, IOWR negate time (MAX = 0.00 x B1 + 11.00)	2.00	11.00	2.00	11.00	2.00	11.00	2.00	11.00	ns
P52	CLKOUT to ALE assert time (MAX = 0.25 x B1 + 6.30)	7.60	13.80	6.30	12.50	5.00	11.30	3.80	10.00	ns
P53	CLKOUT to ALE negate time (MAX = 0.25 x B1 + 8.00)	—	15.60	—	14.30	—	13.00	—	11.80	ns
P54	PCWE, IOWR negated to D(0:31) invalid[1] (MIN = 0.25 x B1 – 2.00)	5.60	—	4.30	—	3.00	—	1.80	—	ns
P55	WAITA and WAITB valid to CLKOUT rising edge[1] (MIN = 0.00 x B1 + 8.00)	8.00	—	8.00	—	8.00	—	8.00	—	ns
P56	CLKOUT rising edge to WAITA and WAITB invalid[1] (MIN = 0.00 x B1 + 2.00)	2.00	—	2.00	—	2.00	—	2.00	—	ns

[1] PSST = 1. Otherwise, add PSST times cycle time.
PSHT = 0. Otherwise, add PSHT times cycle time.
These synchronous timings define when the WAITx signals are detected in order to freeze (or relieve) the PCMCIA current cycle. The WAITx assertion will be effective only if it is detected 2 cycles before the PSL timer expiration. See PCMCIA Interface in the *MPC866 PowerQUICC User's Manual*.

Table 13 shows the debug port timing for the MPC866/859.

Table 13. Debug Port Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
D61	DSCK cycle time	$3xT_{CLOCKOUT}$	—	
D62	DSCK clock pulse width	$1.25xT_{CLOCKOUT}$	—	
D63	DSCK rise and fall times	0.00	3.00	ns
D64	DSDI input data setup time	8.00	—	ns
D65	DSDI data hold time	5.00	—	ns
D66	DSCK low to DSDO data valid	0.00	15.00	ns
D67	DSCK low to DSDO invalid	0.00	2.00	ns

Figure 32 shows the input timing for the debug port clock.

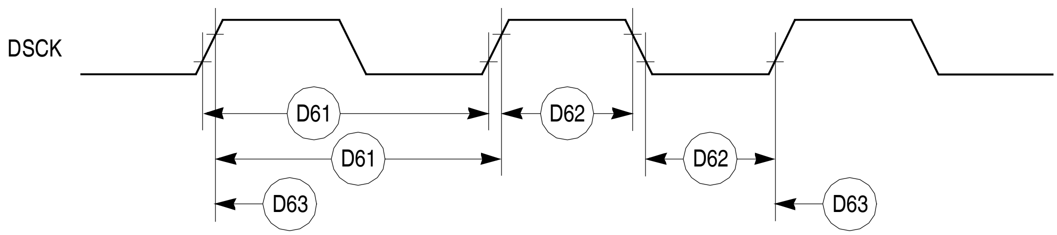


Figure 32. Debug Port Clock Input Timing

Figure 33 shows the timing for the debug port.

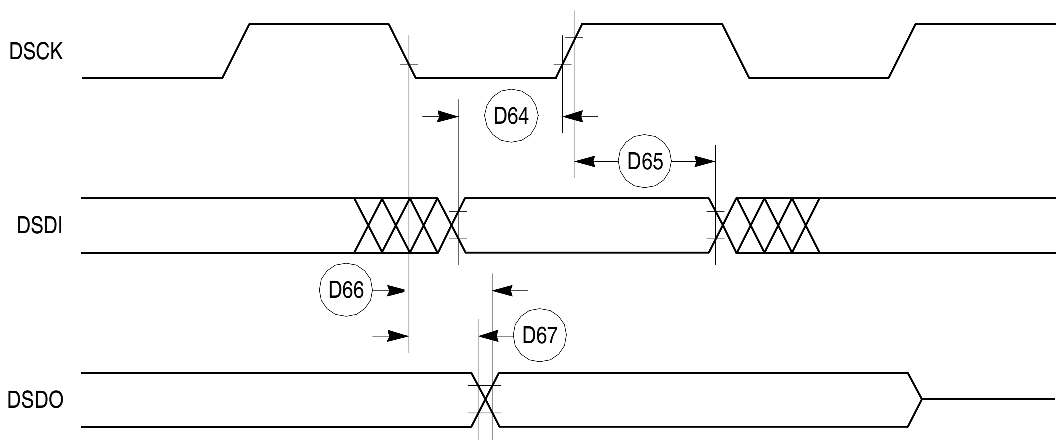


Figure 33. Debug Port Timings

Table 14 shows the reset timing for the MPC866/859.

Table 14. Reset Timing

Num	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
R69	CLKOUT to $\overline{\text{HRESET}}$ high impedance (MAX = 0.00 x B1 + 20.00)	—	20.00	—	20.00	—	20.00	—	20.00	ns
R70	CLKOUT to $\overline{\text{SRESET}}$ high impedance (MAX = 0.00 x B1 + 20.00)	—	20.00	—	20.00	—	20.00	—	20.00	ns
R71	$\overline{\text{RSTCONF}}$ pulse width (MIN = 17.00 x B1)	515.20	—	425.00	—	340.00	—	257.60	—	ns
R72	—	—	—	—	—	—	—	—	—	—
R73	Configuration data to HRESET rising edge setup time (MIN = 15.00 x B1 + 50.00)	504.50	—	425.00	—	350.00	—	277.30	—	ns
R74	Configuration data to $\overline{\text{RSTCONF}}$ rising edge setup time (MIN = 0.00 x B1 + 350.00)	350.00	—	350.00	—	350.00	—	350.00	—	ns
R75	Configuration data hold time after $\overline{\text{RSTCONF}}$ negation (MIN = 0.00 x B1 + 0.00)	0.00	—	0.00	—	0.00	—	0.00	—	ns
R76	Configuration data hold time after $\overline{\text{HRESET}}$ negation (MIN = 0.00 x B1 + 0.00)	0.00	—	0.00	—	0.00	—	0.00	—	ns
R77	$\overline{\text{HRESET}}$ and $\overline{\text{RSTCONF}}$ asserted to data out drive (MAX = 0.00 x B1 + 25.00)	—	25.00	—	25.00	—	25.00	—	25.00	ns
R78	$\overline{\text{RSTCONF}}$ negated to data out high impedance (MAX = 0.00 x B1 + 25.00)	—	25.00	—	25.00	—	25.00	—	25.00	ns
R79	CLKOUT of last rising edge before chip three-states $\overline{\text{HRESET}}$ to data out high impedance (MAX = 0.00 x B1 + 25.00)	—	25.00	—	25.00	—	25.00	—	25.00	ns
R80	DSDI, DSCK setup (MIN = 3.00 x B1)	90.90	—	75.00	—	60.00	—	45.50	—	ns
R81	DSDI, DSCK hold time (MIN = 0.00 x B1 + 0.00)	0.00	—	0.00	—	0.00	—	0.00	—	ns
R82	$\overline{\text{SRESET}}$ negated to CLKOUT rising edge for DSDI and DSCK sample (MIN = 8.00 x B1)	242.40	—	200.00	—	160.00	—	121.20	—	ns

Figure 34 shows the reset timing for the data bus configuration.

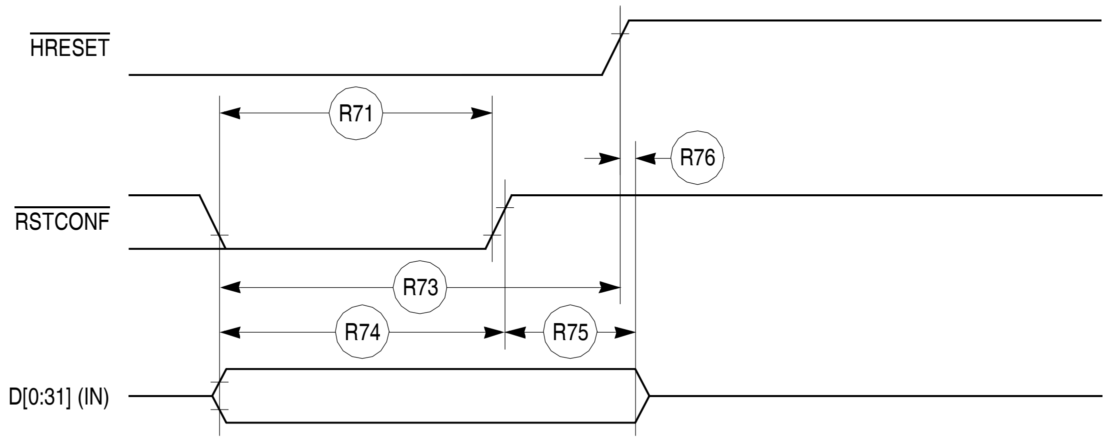


Figure 34. Reset Timing—Configuration from Data Bus

Figure 35 shows the reset timing for the data bus weak drive during configuration.

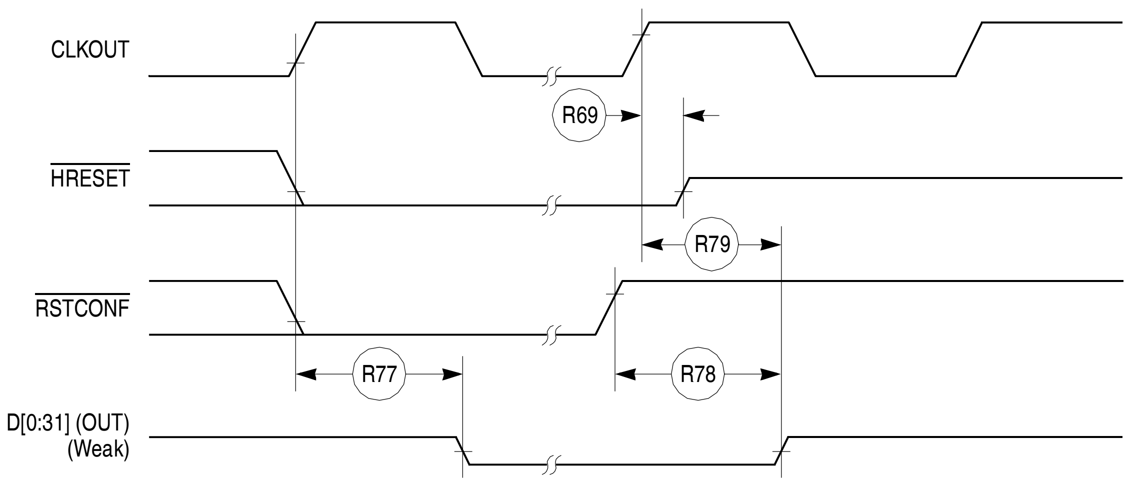


Figure 35. Reset Timing—Data Bus Weak Drive During Configuration

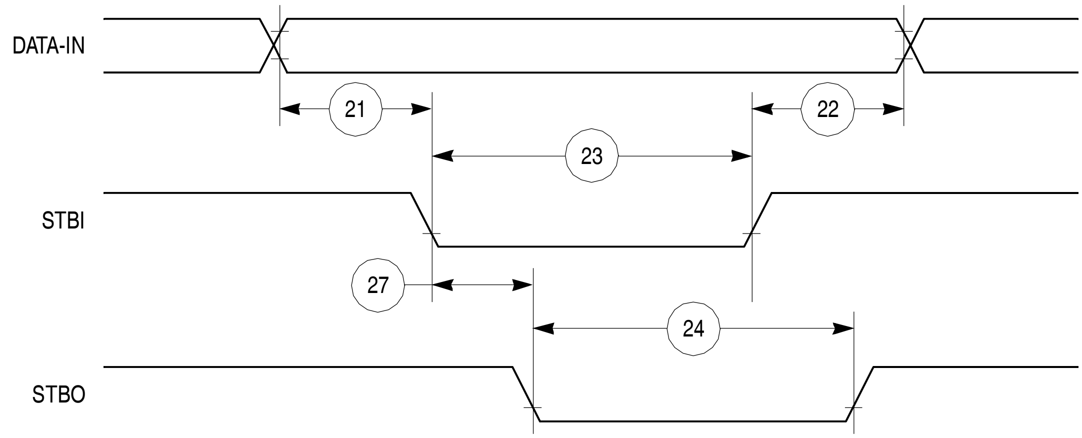


Figure 41. PIP Rx (Interlock Mode) Timing Diagram

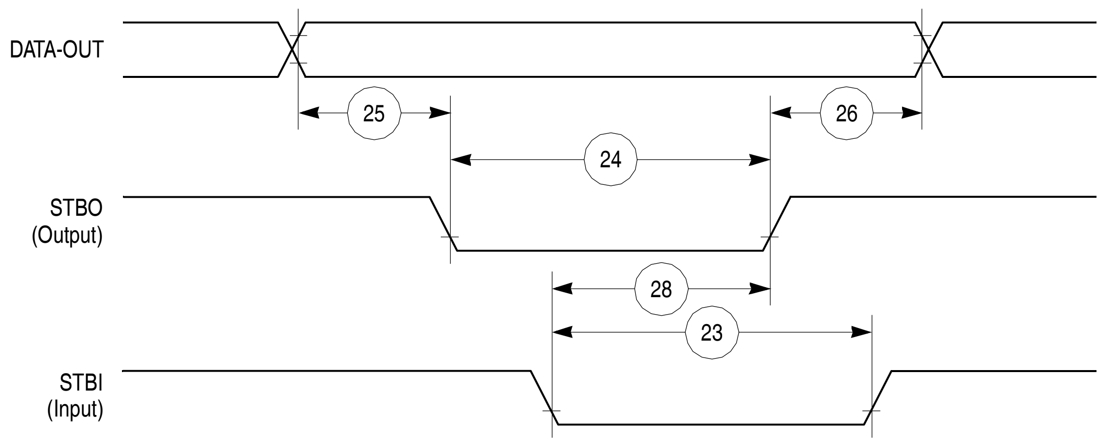


Figure 42. PIP Tx (Interlock Mode) Timing Diagram

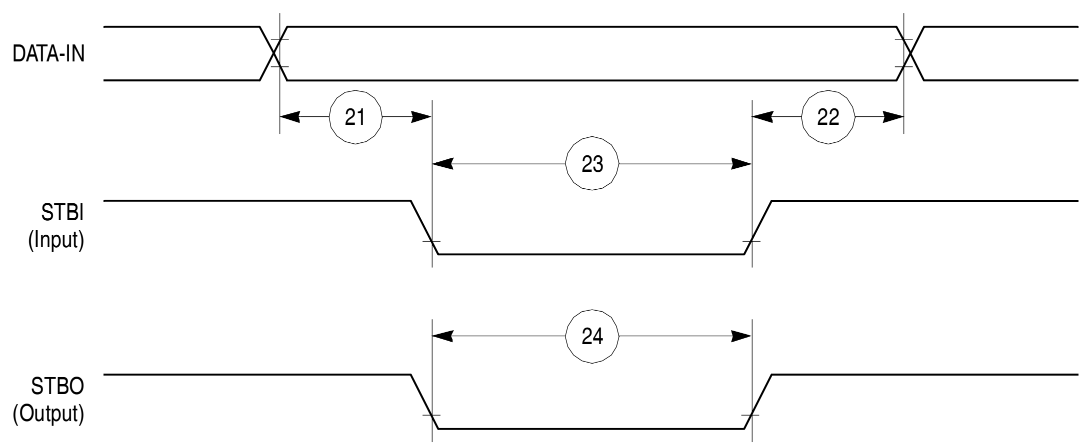


Figure 43. PIP Rx (Pulse Mode) Timing Diagram

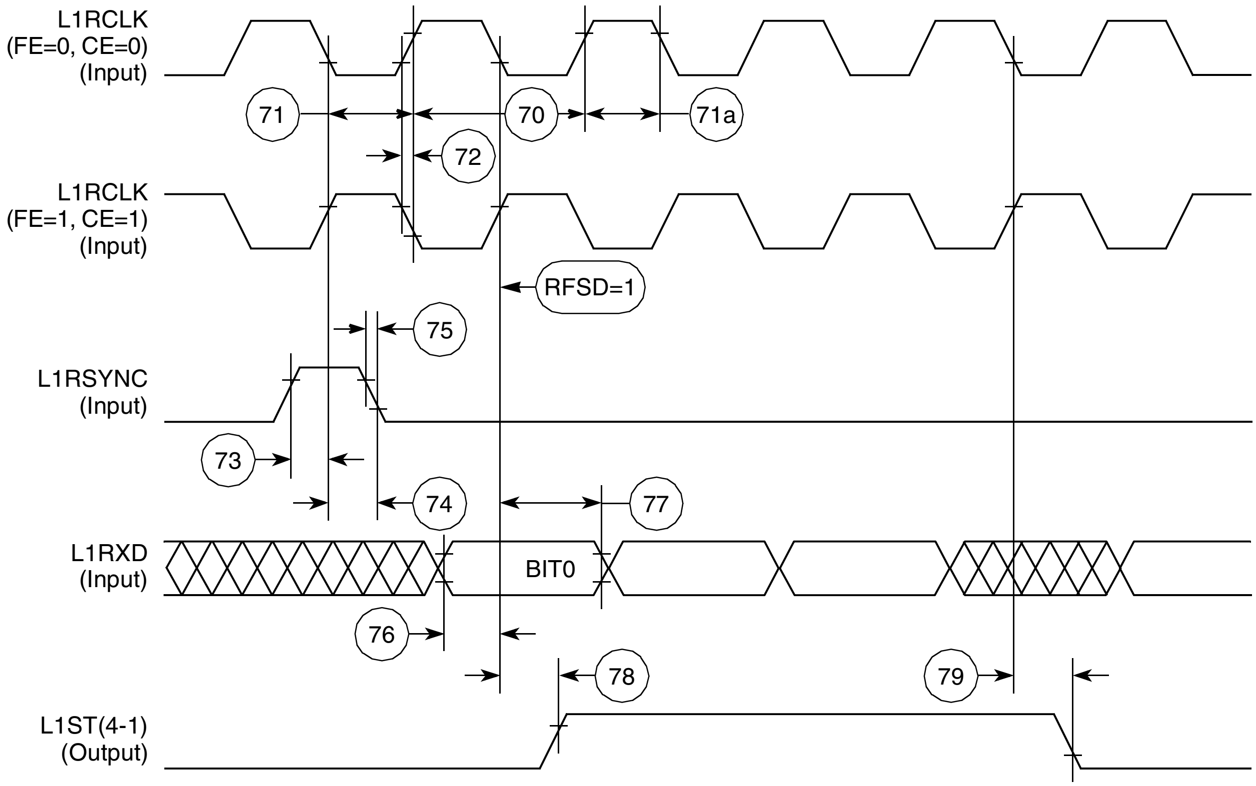


Figure 53. SI Receive Timing Diagram with Normal Clocking (DSC = 0)

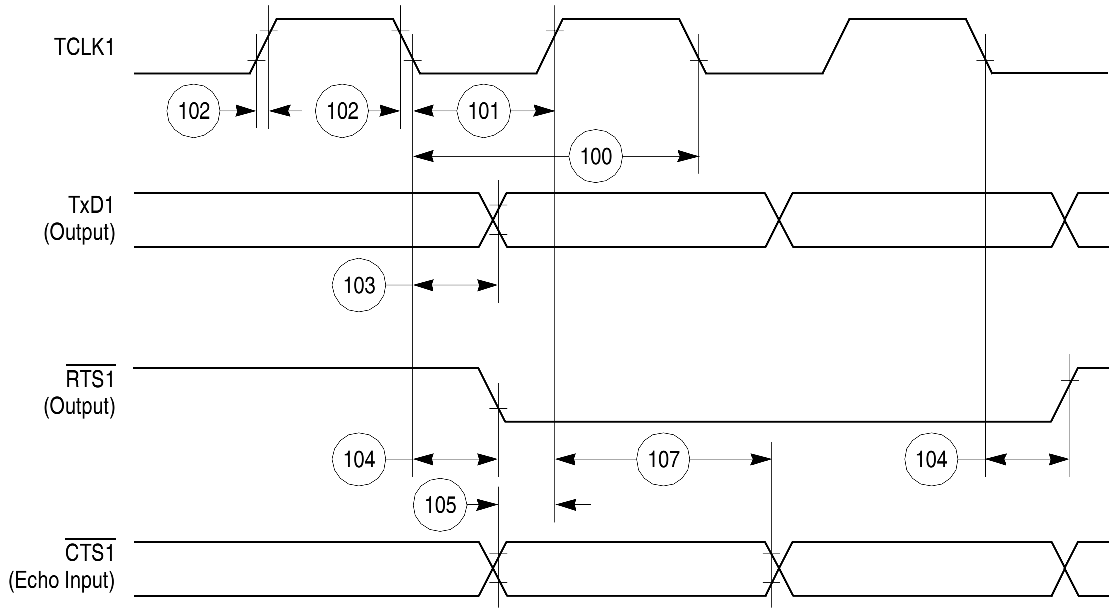


Figure 60. HDLC Bus Timing Diagram

12.8 Ethernet Electrical Specifications

Table 24 shows the Ethernet timings as shown in Figure 61 through Figure 65.

Table 24. Ethernet Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
120	CLSN width high	40	—	ns
121	RCLK1 rise/fall time	—	15	ns
122	RCLK1 width low	40	—	ns
123	RCLK1 clock period [1]	80	120	ns
124	RXD1 setup time	20	—	ns
125	RXD1 hold time	5	—	ns
126	RENA active delay (from RCLK1 rising edge of the last data bit)	10	—	ns
127	RENA width low	100	—	ns
128	TCLK1 rise/fall time	—	15	ns
129	TCLK1 width low	40	—	ns
130	TCLK1 clock period [1]	99	101	ns
131	TXD1 active delay (from TCLK1 rising edge)	—	50	ns
132	TXD1 inactive delay (from TCLK1 rising edge)	6.5	50	ns
133	TENA active delay (from TCLK1 rising edge)	10	50	ns

Table 24. Ethernet Timing (continued)

Num	Characteristic	All Frequencies		Unit
		Min	Max	
134	TENA inactive delay (from TCLK1 rising edge)	10	50	ns
135	RSTRT active delay (from TCLK1 falling edge)	10	50	ns
136	RSTRT inactive delay (from TCLK1 falling edge)	10	50	ns
137	REJECT width low	1	—	CLK
138	CLKO1 low to SDACK asserted [2]	—	20	ns
139	CLKO1 low to SDACK negated [2]	—	20	ns

[1] The ratios SyncCLK/RCLK1 and SyncCLK/TCLK1 must be greater or equal to 2/1.

[2] SDACK is asserted whenever the SDMA writes the incoming frame DA into memory.

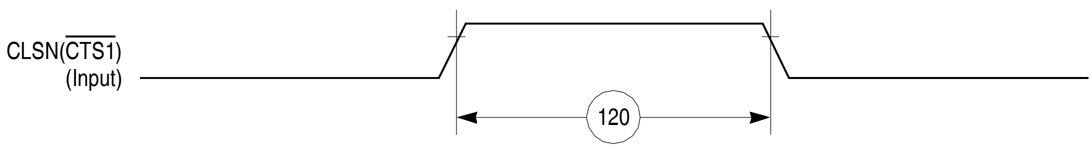


Figure 61. Ethernet Collision Timing Diagram

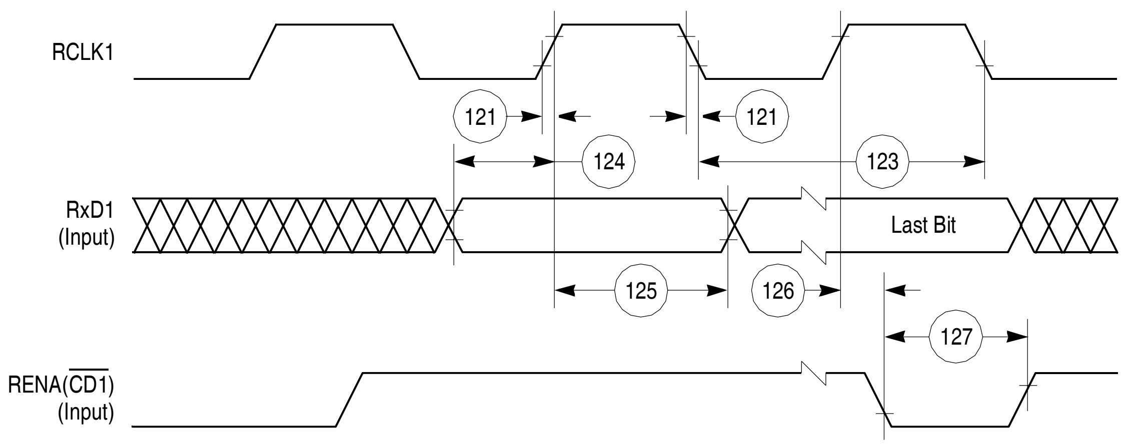
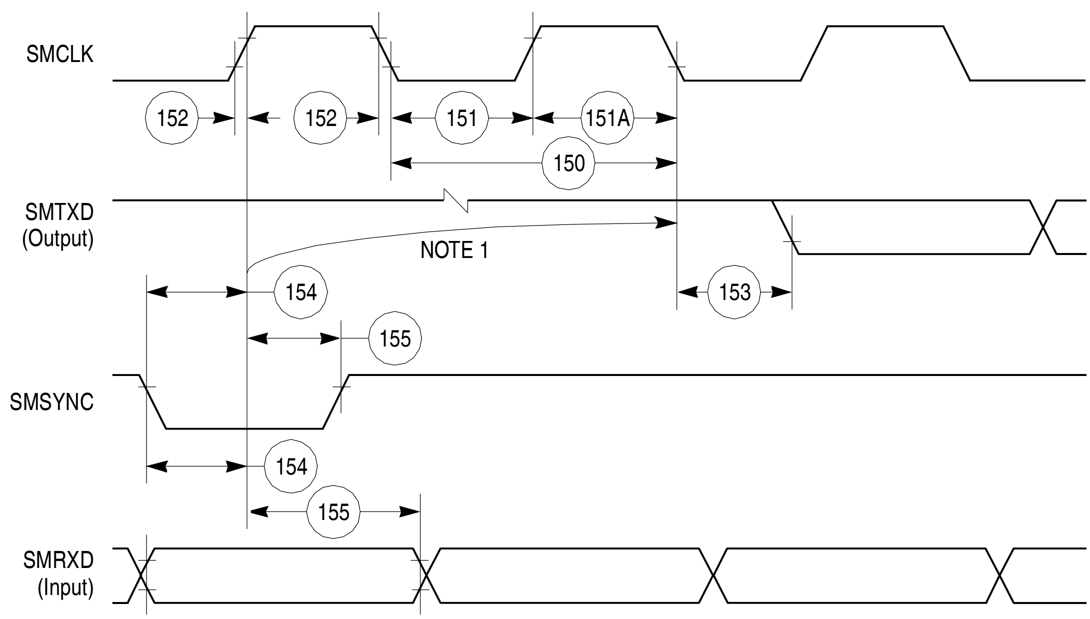


Figure 62. Ethernet Receive Timing Diagram

Table 25. SMC Transparent Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
150	SMCLK clock period [1]	100	—	ns
151	SMCLK width low	50	—	ns
151A	SMCLK width high	50	—	ns
152	SMCLK rise/fall time	—	15	ns
153	SMTXD active delay (from SMCLK falling edge)	10	50	ns
154	SMRXD/SMSYNC setup time	20	—	ns
155	RXD1/SMSYNC hold time	5	—	ns

[1] Sync CLK must be at least twice as fast as SMCLK.



NOTE:
1. This delay is equal to an integer number of character-length clocks.

Figure 66. SMC Transparent Timing Diagram

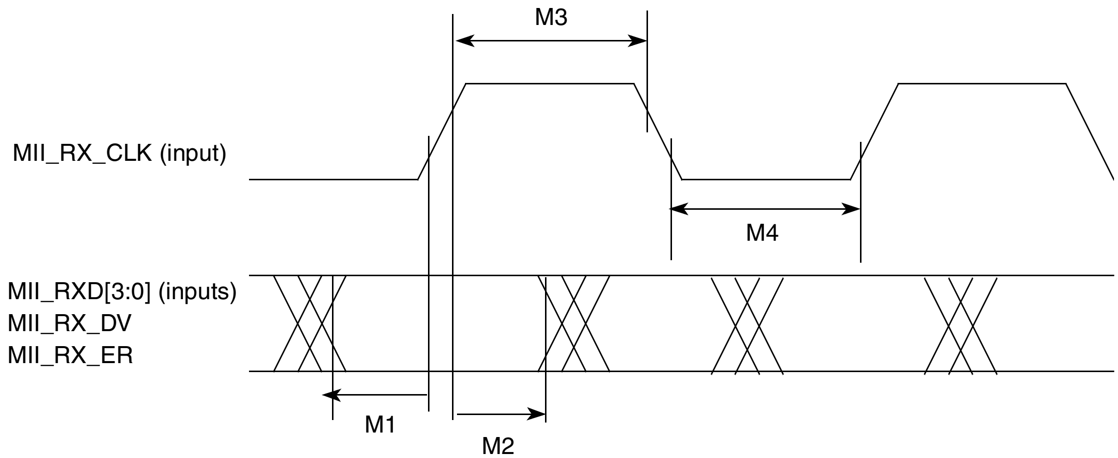


Figure 74. MII Receive Signal Timing Diagram

14.2 MII Transmit Signal Timing (MII_TXD[3:0], MII_TX_EN, MII_TX_ER, MII_TX_CLK)

The transmitter functions correctly up to a MII_TX_CLK maximum frequency of 25 MHz +1%. There is no minimum frequency requirement. In addition, the processor clock frequency must exceed the MII_TX_CLK frequency - 1%.

Table 34 shows information on the MII transmit signal timing.

Table 34. MII Transmit Signal Timing

Num	Characteristic	Min	Max	Unit
M5	MII_TX_CLK to MII_TXD[3:0], MII_TX_EN, MII_TX_ER invalid	5	—	ns
M6	MII_TX_CLK to MII_TXD[3:0], MII_TX_EN, MII_TX_ER valid	—	25	—
M7	MII_TX_CLK pulse width high	35%	65%	MII_TX_CLK period
M8	MII_TX_CLK pulse width low	35%	65%	MII_TX_CLK period

Table 39. Pin Assignments (continued)

Name	Pin Number	Type
UPWAITB GPL_B4	B1	Bidirectional
GPL_A5	D3	Output
PORESET	R2	Input
RSTCONF	P3	Input
HRESET	N4	Open-drain
SRESET	P2	Open-drain
XTAL	P1	Analog Output
EXTAL	N1	Analog Input (3.3V only)
CLKOUT	W3	Output
EXTCLK	N2	Input (3.3V only)
TEXP	N3	Output
ALE_A MII-TXD1	K2	Output
CE1_A MII-TXD2	B3	Output
CE2_A MII-TXD3	A3	Output
WAIT_A SOC_Split[2]	R3	Input
WAIT_B	R4	Input
IP_A0 UTPB_Split0[2] MII-RXD3	T5	Input
IP_A1 UTPB_Split1[2] MII-RXD2	T4	Input
IP_A2 IOIS16_A UTPB_Split2[2] MII-RXD1	U3	Input
IP_A3 UTPB_Split3[2] MII-RXD0	W2	Input
IP_A4 UTPB_Split4[2] MII-RXCLK	U4	Input

Table 39. Pin Assignments (continued)

Name	Pin Number	Type
PA5 CLK3 L1TCLKA BRGO2 TIN2	N18	Bidirectional
PA4 CLK4 $\overline{\text{TOUT2}}$	P19	Bidirectional
PA3 CLK5 BRGO3 TIN3	P17	Bidirectional
PA2 CLK6 $\overline{\text{TOUT3}}$ L1RCLKB	R18	Bidirectional
PA1 CLK7 BRGO4 TIN4	T19	Bidirectional
PA0 CLK8 $\overline{\text{TOUT4}}$ L1TCLKB	U19	Bidirectional
PB31 $\overline{\text{SPISEL}}$ $\overline{\text{REJECT1}}$	C17	Bidirectional (Optional: Open-drain)
PB30 SPICLK $\overline{\text{RSTRT2}}$	C19	Bidirectional (Optional: Open-drain)
PB29 SPIMOSI	E16	Bidirectional (Optional: Open-drain)
PB28 SPIMISO BRGO4	D19	Bidirectional (Optional: Open-drain)
PB27 I2CSDA BRGO1	E19	Bidirectional (Optional: Open-drain)
PB26 I2CSCL BRGO2	F19	Bidirectional (Optional: Open-drain)