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7 Thermal Calculation and Measurement

For the following discussions, $P_D = (VDDL \times IDDL) + PI/O$, where PI/O is the power dissipation of the I/O drivers. The VDDSYN power dissipation is negligible.

7.1 Estimation with Junction-to-Ambient Thermal Resistance

An estimation of the chip junction temperature, T_J , in °C can be obtained from the equation:

$$T_J = T_A + (R_{\theta JA} \times P_D)$$

where:

T_A = ambient temperature (°C)

$R_{\theta JA}$ = package junction-to-ambient thermal resistance (°C/W)

P_D = power dissipation in package

The junction-to-ambient thermal resistance is an industry standard value that provides a quick and easy estimation of thermal performance. However, the answer is only an estimate; test cases have demonstrated that errors of a factor of two (in the quantity $T_J - T_A$) are possible.

7.2 Estimation with Junction-to-Case Thermal Resistance

Historically, the thermal resistance has frequently been expressed as the sum of a junction-to-case thermal resistance and a case-to-ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$$

where:

$R_{\theta JA}$ = junction-to-ambient thermal resistance (°C/W)

$R_{\theta JC}$ = junction-to-case thermal resistance (°C/W)

$R_{\theta CA}$ = case-to-ambient thermal resistance (°C/W)

$R_{\theta JC}$ is device related and cannot be influenced by the user. The user adjusts the thermal environment to affect the case-to-ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the airflow around the device, add a heat sink, change the mounting arrangement on the printed-circuit board, or change the thermal dissipation on the printed-circuit board surrounding the device. This thermal model is most useful for ceramic packages with heat sinks where some 90% of the heat flows through the case and the heat sink to the ambient environment. For most packages, a better model is required.

7.3 Estimation with Junction-to-Board Thermal Resistance

A simple package thermal model that has demonstrated reasonable accuracy (about 20%) is a two-resistor model consisting of a junction-to-board and a junction-to-case thermal resistance. The junction-to-case covers the situation where a heat sink is used or where a substantial amount of heat is dissipated from the top of the package. The junction-to-board thermal resistance describes the thermal performance when most of the heat is conducted to the printed-circuit board. It has been observed that the thermal performance of most plastic packages and especially PBGA packages is strongly dependent on the board temperature; see [Figure 3](#).

7.5 Experimental Determination

To determine the junction temperature of the device in the application after prototypes are available, the thermal characterization parameter (Ψ_{JT}) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D)$$

where:

Ψ_{JT} = thermal characterization parameter

T_T = thermocouple temperature on top of package

P_D = power dissipation in package

The thermal characterization parameter is measured per JESD51-2 specification published by JEDEC using a 40 gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

7.6 References

Semiconductor Equipment and Materials International(415) 964-5111
805 East Middlefield Rd.
Mountain View, CA 94043

MIL-SPEC and EIA/JESD (JEDEC) specifications 800-854-7179 or
(Available from Global Engineering Documents) 303-397-7956

JEDEC Specifications <http://www.jedec.org>

1. C.E. Triplett and B. Joiner, "An Experimental Characterization of a 272 PBGA Within an Automotive Engine Controller Module," Proceedings of SemiTherm, San Diego, 1998, pp. 47-54.
2. B. Joiner and V. Adams, "Measurement and Simulation of Junction to Board Thermal Resistance and Its Application in Thermal Modeling," Proceedings of SemiTherm, San Diego, 1999, pp. 212-220.

8 Power Supply and Power Sequencing

This section provides design considerations for the MPC866/859 power supply. The MPC866/859 has a core voltage (VDDL) and PLL voltage (VDDSYN) that operates at a lower voltage than the I/O voltage VDDH. The I/O section of the MPC866/859 is supplied with 3.3 V across VDDH and V_{SS} (GND).

Signals PA[0:15], PB[14:31], PC[4:15], PD[3:15], TDI, TDO, TCK, TRST_B, TMS, MII_TXEN, and MII_MDIO are 5-V tolerant. All inputs cannot be more than 2.5 V greater than VDDH. In addition, 5-V tolerant pins cannot exceed 5.5 V and the remaining input pins cannot exceed 3.465 V. This restriction applies to power up/down and normal operation.

One consequence of multiple power supplies is that when power is initially applied the voltage rails ramp up at different rates. The rates depend on the nature of the power supply, the type of load on each power supply, and the manner in which different voltages are derived. The following restrictions apply:

- VDDL must not exceed VDDH during power up and power down.
- VDDL must not exceed 1.9 V and VDDH must not exceed 3.465 V.

These cautions are necessary for the long term reliability of the part. If they are violated, the electrostatic discharge (ESD) protection diodes are forward-biased and excessive current can flow through these diodes. If the system power supply design does not control the voltage sequencing, the circuit shown in [Figure 4](#) can be added to meet these requirements. The MUR420 Schottky diodes control the maximum potential difference between the external bus and core power supplies on powerup and the 1N5820 diodes regulate the maximum potential difference on powerdown.

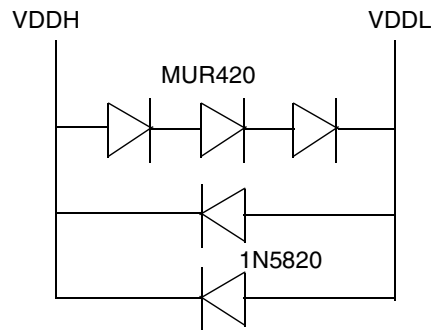


Figure 4. Example Voltage Sequencing Circuit

9 Layout Practices

Each V_{DD} pin on the MPC866/859 should be provided with a low-impedance path to the board's supply. Furthermore, each GND pin should be provided with a low-impedance path to ground. The power supply pins drive distinct groups of logic on chip. The V_{DD} power supply should be bypassed to ground using at least four 0.1 μF bypass capacitors located as close as possible to the four sides of the package. Each board designed should be characterized and additional appropriate decoupling capacitors should be used if required. The capacitor leads and associated printed-circuit traces connecting to chip V_{DD} and GND should be kept to less than 1/2" per capacitor lead. At a minimum, a four-layer board employing two inner layers as V_{DD} and GND planes should be used.

All output pins on the MPC866/859 have fast rise and fall times. Printed-circuit (PC) trace interconnection length should be minimized in order to minimize undershoot and reflections caused by these fast output switching times.

Table 9. Bus Operation Timings (continued)

Num	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
B31d	CLKOUT falling edge to \overline{CS} valid, as requested by control bit CST1 in the corresponding word in the UPM EBDF = 1 (MAX = $0.375 \times B1 + 6.6$)	13.30	18.00	11.30	16.00	9.40	14.10	7.60	12.30	ns
B32	CLKOUT falling edge to \overline{BS} valid, as requested by control bit BST4 in the corresponding word in the UPM (MAX = $0.00 \times B1 + 6.00$)	1.50	6.00	1.50	6.00	1.50	6.00	1.50	6.00	ns
B32a	CLKOUT falling edge to \overline{BS} valid, as requested by control bit BST1 in the corresponding word in the UPM, EBDF = 0 (MAX = $0.25 \times B1 + 6.80$)	7.60	14.30	6.30	13.00	5.00	11.80	3.80	10.50	ns
B32b	CLKOUT rising edge to \overline{BS} valid, as requested by control bit BST2 in the corresponding word in the UPM (MAX = $0.00 \times B1 + 8.00$)	1.50	8.00	1.50	8.00	1.50	8.00	1.50	8.00	ns
B32c	CLKOUT rising edge to \overline{BS} valid, as requested by control bit BST3 in the corresponding word in the UPM (MAX = $0.25 \times B1 + 6.80$)	7.60	14.30	6.30	13.00	5.00	11.80	3.80	10.50	ns
B32d	CLKOUT falling edge to \overline{BS} valid- as requested by control bit BST1 in the corresponding word in the UPM, EBDF = 1 (MAX = $0.375 \times B1 + 6.60$)	13.30	18.00	11.30	16.00	9.40	14.10	7.60	12.30	ns
B33	CLKOUT falling edge to \overline{GPL} valid, as requested by control bit GxT4 in the corresponding word in the UPM (MAX = $0.00 \times B1 + 6.00$)	1.50	6.00	1.50	6.00	1.50	6.00	1.50	6.00	ns
B33a	CLKOUT rising edge to \overline{GPL} valid, as requested by control bit GxT3 in the corresponding word in the UPM (MAX = $0.25 \times B1 + 6.80$)	7.60	14.30	6.30	13.00	5.00	11.80	3.80	10.50	ns
B34	A(0:31), BADDR(28:30), and D(0:31) to \overline{CS} valid, as requested by control bit CST4 in the corresponding word in the UPM (MIN = $0.25 \times B1 - 2.00$)	5.60	—	4.30	—	3.00	—	1.80	—	ns
B34a	A(0:31), BADDR(28:30), and D(0:31) to \overline{CS} valid, as requested by control bit CST1 in the corresponding word in the UPM (MIN = $0.50 \times B1 - 2.00$)	13.20	—	10.50	—	8.00	—	5.60	—	ns
B34b	A(0:31), BADDR(28:30), and D(0:31) to \overline{CS} valid, as requested by CST2 in the corresponding word in UPM (MIN = $0.75 \times B1 - 2.00$)	20.70	—	16.70	—	13.00	—	9.40	—	ns

Bus Signal Timing

Figure 8 shows the timing for the synchronous active pull-up and open-drain output signals.

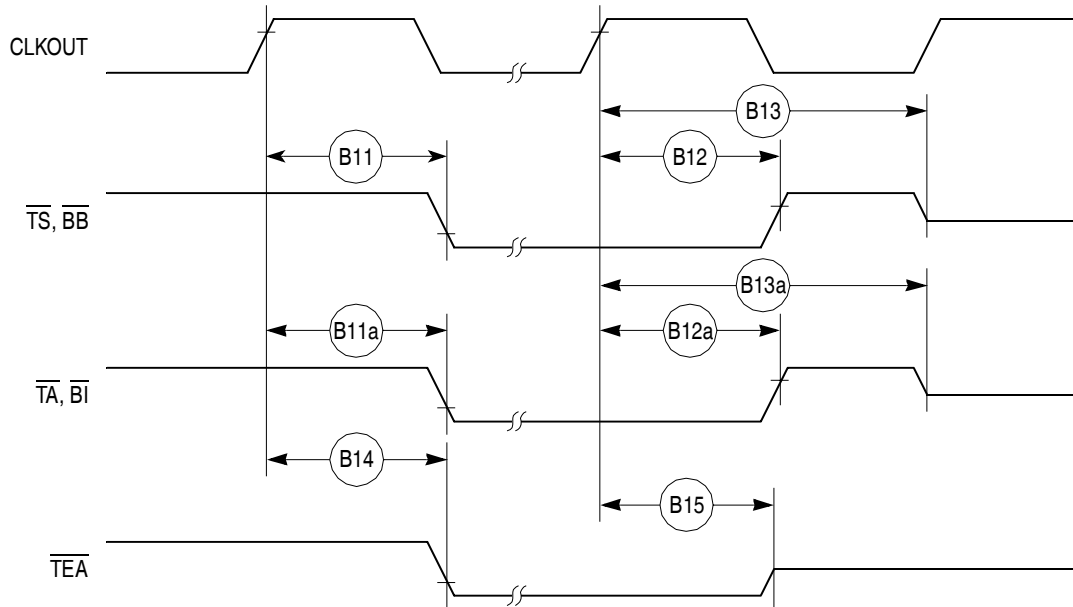


Figure 8. Synchronous Active Pull-Up Resistor and Open-Drain Output Signals Timing

Figure 9 shows the timing for the synchronous input signals.

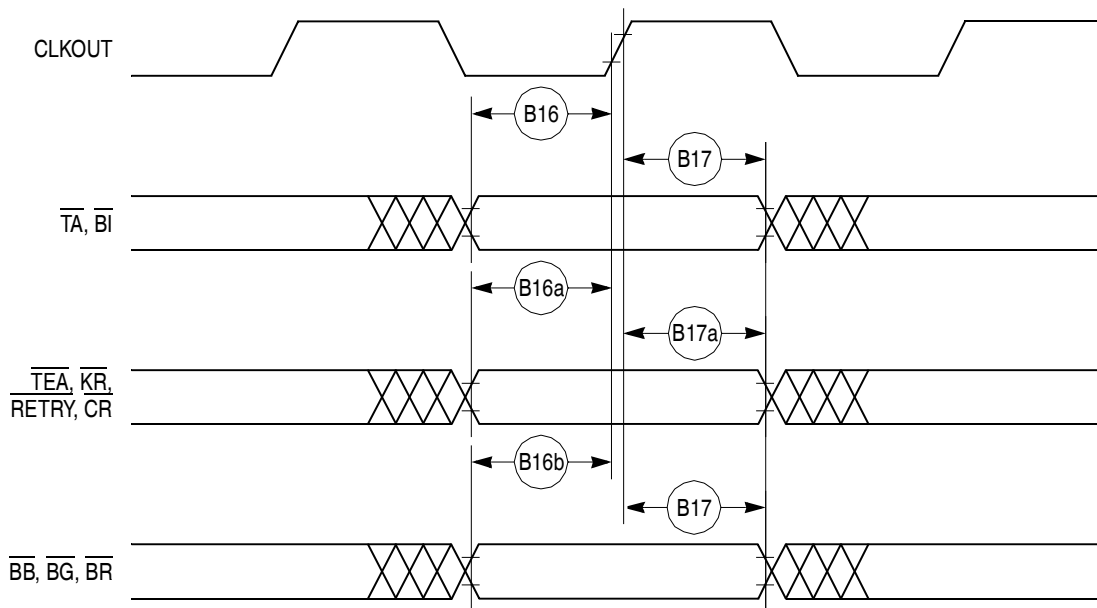


Figure 9. Synchronous Input Signals Timing

Bus Signal Timing

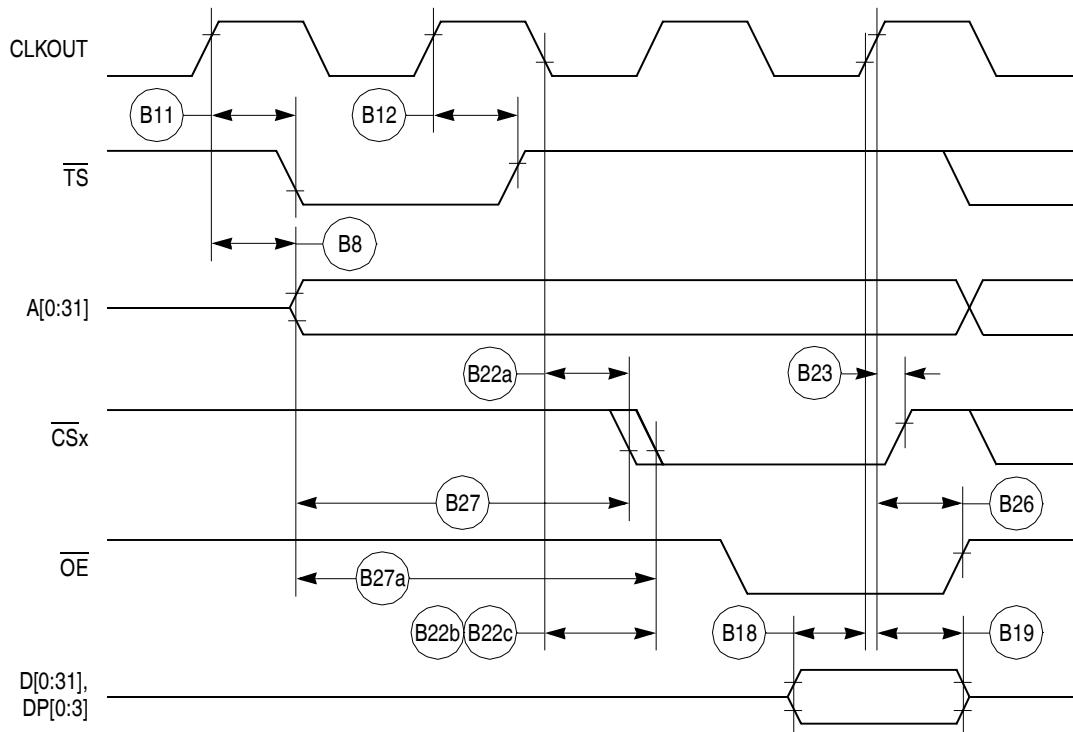


Figure 15. External Bus Read Timing (GPCM Controlled—TRLX = 0 or 1, ACS = 10, ACS = 11)

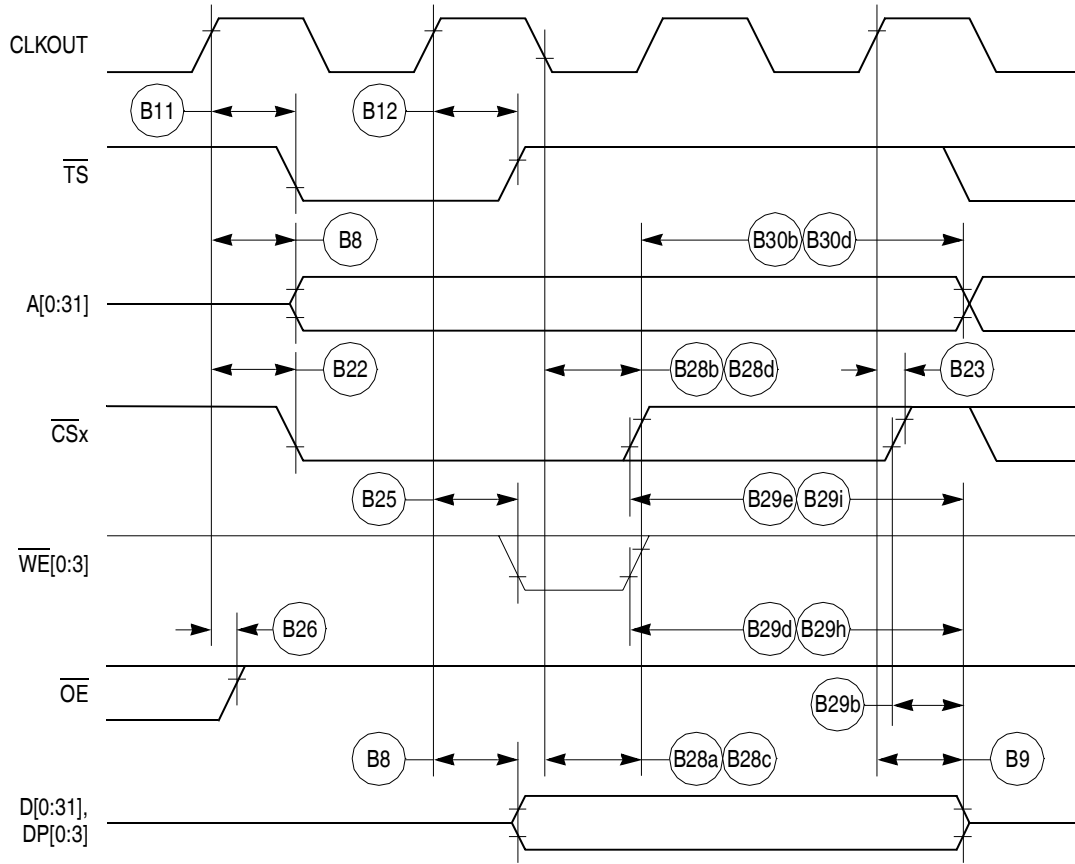


Figure 18. External Bus Write Timing (GPCM Controlled—TRLX = 1, CSNT = 1)

Figure 23 shows the timing for the asynchronous external master memory access controlled by the GPCM.

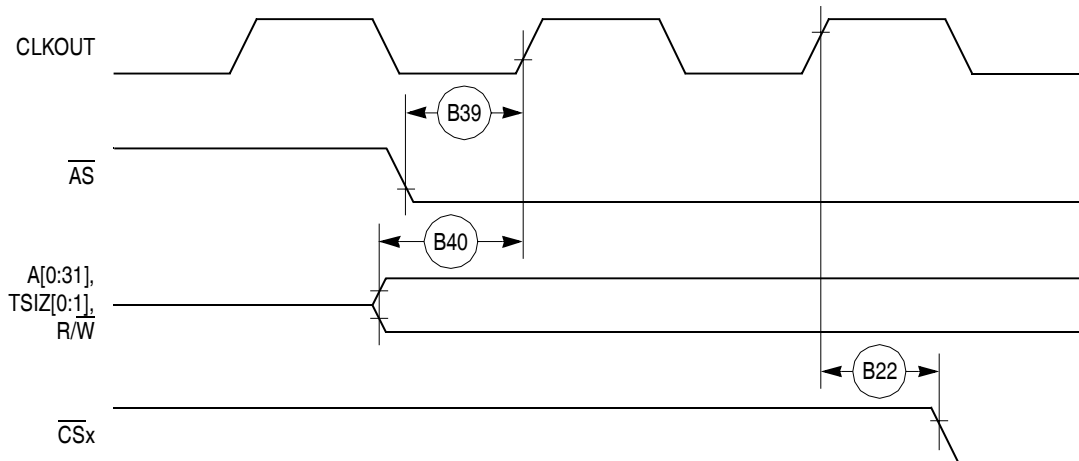


Figure 23. Asynchronous External Master Memory Access Timing (GPCM Controlled—ACS = 00)

Figure 24 shows the timing for the asynchronous external master control signals negation.

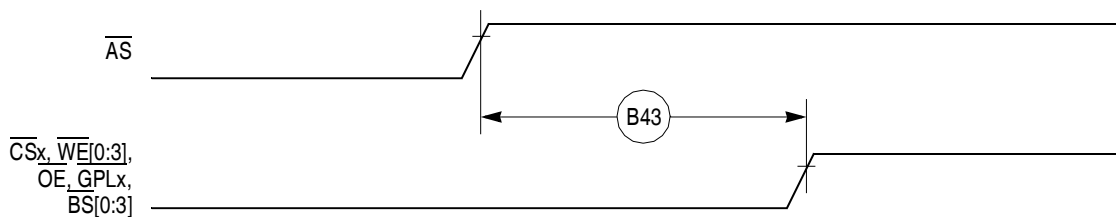


Figure 24. Asynchronous External Master—Control Signals Negation Timing

Table 10 shows the interrupt timing for the MPC866/859.

Table 10. Interrupt Timing

Num	Characteristic ¹	All Frequencies		Unit
		Min	Max	
I39	\overline{IRQ}_x valid to CLKOUT rising edge (setup time)	6.00	—	ns
I40	\overline{IRQ}_x hold time after CLKOUT	2.00	—	ns
I41	\overline{IRQ}_x pulse width low	3.00	—	ns
I42	\overline{IRQ}_x pulse width high	3.00	—	ns
I43	\overline{IRQ}_x edge-to-edge time	$4 \times T_{\text{CLOCKOUT}}$	—	—

¹ The timings I39 and I40 describe the testing conditions under which the \overline{IRQ} lines are tested when being defined as level sensitive. The \overline{IRQ} lines are synchronized internally and do not have to be asserted or negated with reference to the CLKOUT.

The timings I41, I42, and I43 are specified to allow the correct function of the \overline{IRQ} lines detection circuitry, and has no direct relation with the total system interrupt latency that the MPC866/859 is able to support.

Bus Signal Timing

Figure 25 shows the interrupt detection timing for the external level-sensitive lines.

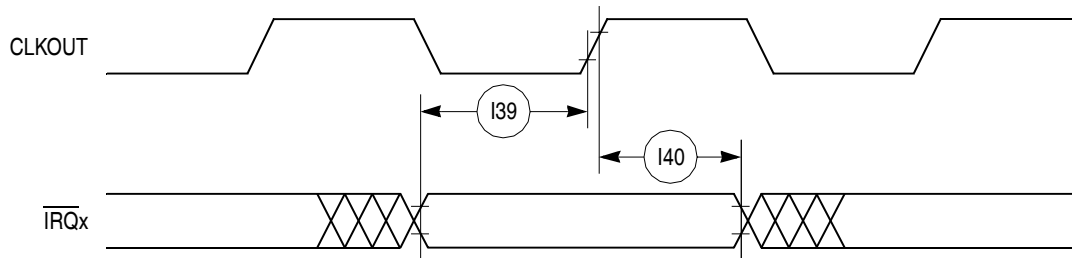


Figure 25. Interrupt Detection Timing for External Level Sensitive Lines

Figure 26 shows the interrupt detection timing for the external edge-sensitive lines.

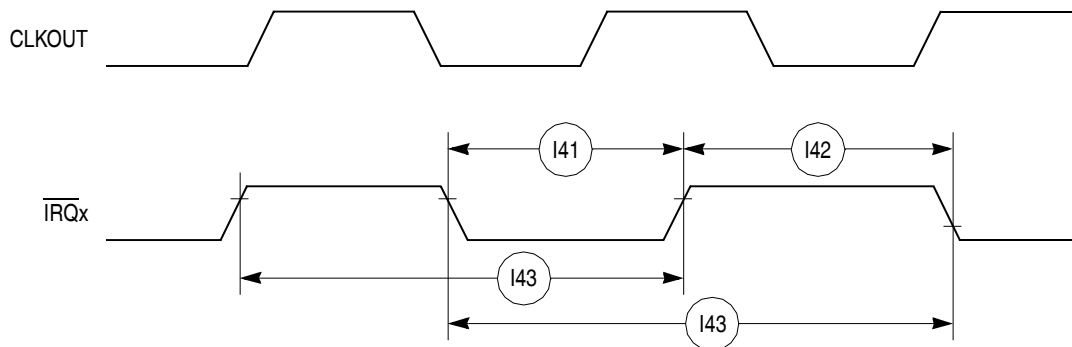


Figure 26. Interrupt Detection Timing for External Edge Sensitive Lines

Table 11 shows the PCMCIA timing for the MPC866/859.

Table 11. PCMCIA Timing

Num	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
P44	A(0:31), \overline{REG} valid to PCMCIA Strobe asserted ¹ (MIN = 0.75 x B1 - 2.00)	20.70	—	16.70	—	13.00	—	9.40	—	ns
P45	A(0:31), \overline{REG} valid to ALE negation ¹ (MIN = 1.00 x B1 - 2.00)	28.30	—	23.00	—	18.00	—	13.20	—	ns
P46	CLKOUT to \overline{REG} valid (MAX = 0.25 x B1 + 8.00)	7.60	15.60	6.30	14.30	5.00	13.00	3.80	11.80	ns
P47	CLKOUT to \overline{REG} invalid (MIN = 0.25 x B1 + 1.00)	8.60	—	7.30	—	6.00	—	4.80	—	ns
P48	CLKOUT to $\overline{CE1}$, $\overline{CE2}$ asserted (MAX = 0.25 x B1 + 8.00)	7.60	15.60	6.30	14.30	5.00	13.00	3.80	11.80	ns
P49	CLKOUT to $\overline{CE1}$, $\overline{CE2}$ negated (MAX = 0.25 x B1 + 8.00)	7.60	15.60	6.30	14.30	5.00	13.00	3.80	11.80	ns

Figure 34 shows the reset timing for the data bus configuration.

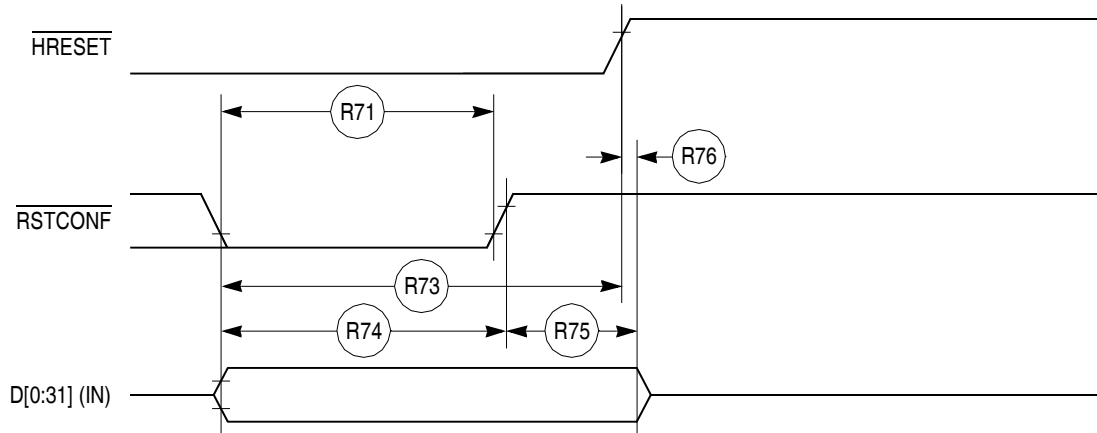


Figure 34. Reset Timing—Configuration from Data Bus

Figure 35 shows the reset timing for the data bus weak drive during configuration.

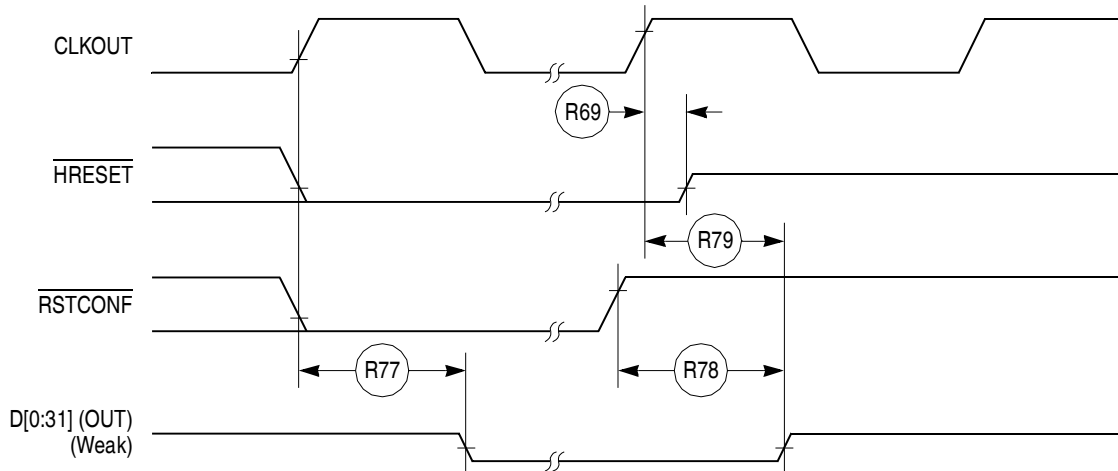


Figure 35. Reset Timing—Data Bus Weak Drive During Configuration

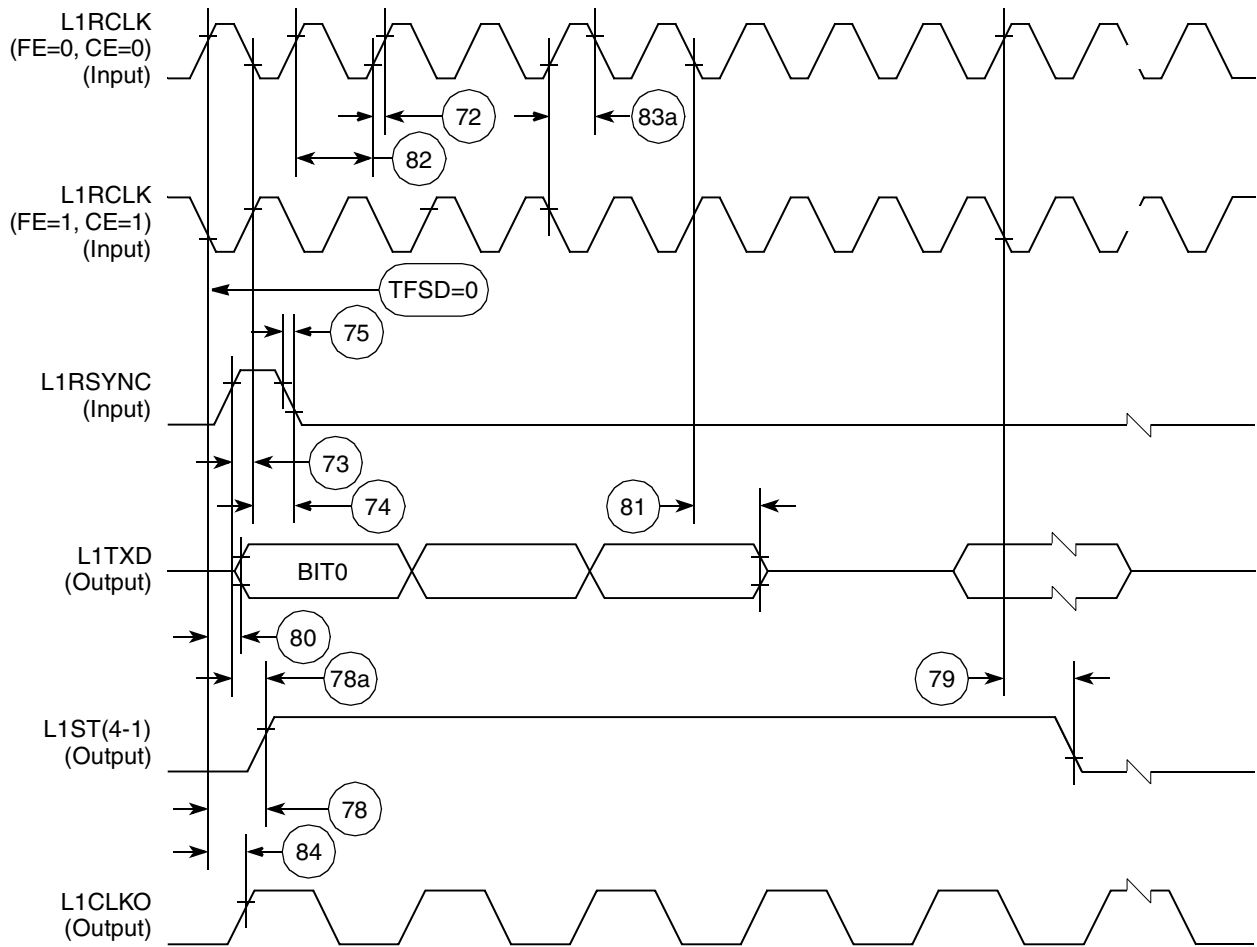


Figure 56. SI Transmit Timing with Double Speed Clocking (DSC = 1)

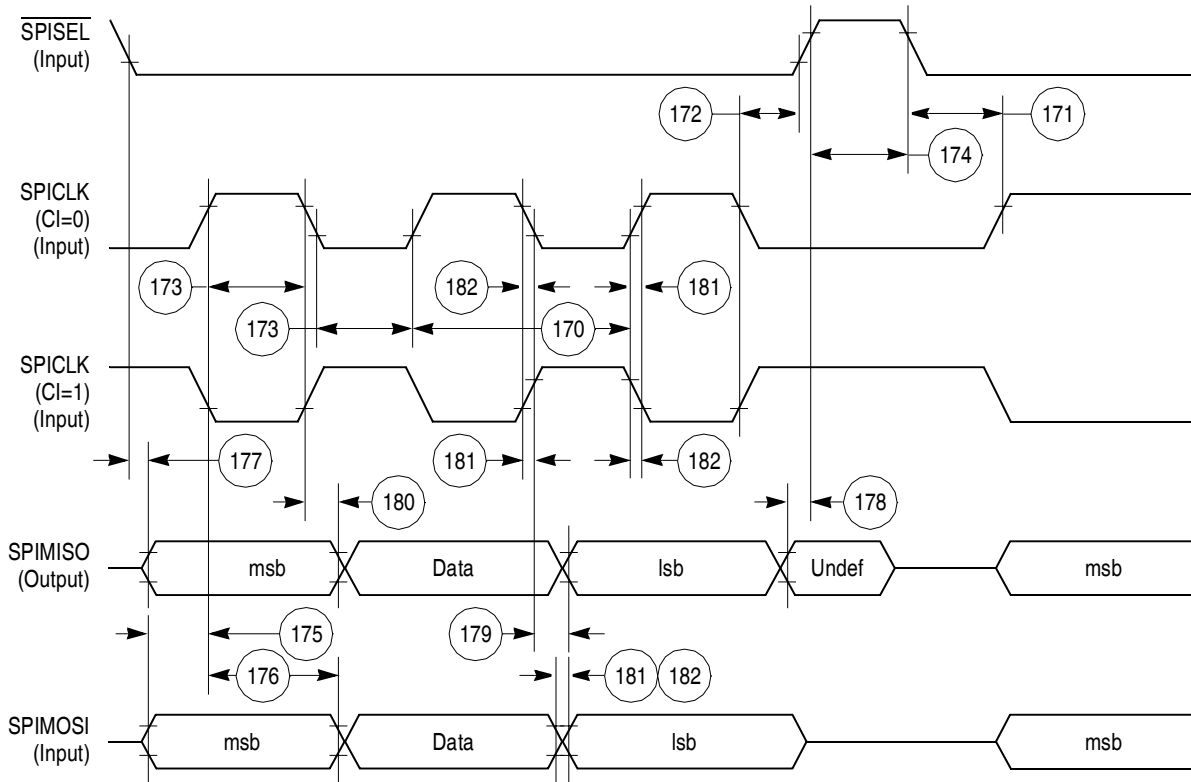


Figure 69. SPI Slave (CP = 0) Timing Diagram

Table 28 shows the I²C (SCL < 100 kHz) timings.

Table 28. I²C Timing (SCL < 100 kHz)

Num	Characteristic	All Frequencies		Unit
		Min	Max	
200	SCL clock frequency (slave)	0	100	kHz
200	SCL clock frequency (master) ¹	1.5	100	kHz
202	Bus free time between transmissions	4.7	—	μs
203	Low period of SCL	4.7	—	μs
204	High period of SCL	4.0	—	μs
205	Start condition setup time	4.7	—	μs
206	Start condition hold time	4.0	—	μs
207	Data hold time	0	—	μs
208	Data setup time	250	—	ns
209	SDL/SCL rise time	—	1	μs
210	SDL/SCL fall time	—	300	ns
211	Stop condition setup time	4.7	—	μs

¹ SCL frequency is given by $SCL = BRGCLK_frequency / ((BRG\ register + 3) * pre_scaler * 2)$.
The ratio $SyncClk/(BRGCLK/pre_scaler)$ must be greater or equal to 4/1.

Table 29 shows the I²C (SCL > 100 kHz) timings.

Table 29. I²C Timing (SCL > 100 kHz)

Num	Characteristic	Expression	All Frequencies		Unit
			Min	Max	
200	SCL clock frequency (slave)	fSCL	0	BRGCLK/48	Hz
200	SCL clock frequency (master) ¹	fSCL	BRGCLK/16512	BRGCLK/48	Hz
202	Bus free time between transmissions	—	$1/(2.2 * fSCL)$	—	s
203	Low period of SCL	—	$1/(2.2 * fSCL)$	—	s
204	High period of SCL	—	$1/(2.2 * fSCL)$	—	s
205	Start condition setup time	—	$1/(2.2 * fSCL)$	—	s
206	Start condition hold time	—	$1/(2.2 * fSCL)$	—	s
207	Data hold time	—	0	—	s
208	Data setup time	—	$1/(40 * fSCL)$	—	s
209	SDL/SCL rise time	—	—	$1/(10 * fSCL)$	s
210	SDL/SCL fall time	—	—	$1/(33 * fSCL)$	s
211	Stop condition setup time	—	$1/2(2.2 * fSCL)$	—	s

¹ SCL frequency is given by $SCL = BrgClk_frequency / ((BRG\ register + 3) * pre_scaler * 2)$.
The ratio $SyncClk/(Brg_Clk/pre_scaler)$ must be greater or equal to 4/1.

Table 32. UTOPIA Slave (Split Bus Mode) Electrical Specifications

Num	Signal Characteristic	Direction	Min	Max	Unit
U1	UtpClk rise/fall time (external clock option)	Input	—	4	ns
	Duty cycle		40	60	%
	Frequency		—	33	MHz
U2	UTPB, SOC, Rxclav and Txclav active delay	Output	2	16	ns
U3	UTPB_AUX, SOC_Aux, $\overline{\text{RxEnb}}$, $\overline{\text{TxEnb}}$, RxAddr, and TxAddr setup time	Input	4	—	ns
U4	UTPB_AUX, SOC_Aux, $\overline{\text{RxEnb}}$, $\overline{\text{TxEnb}}$, RxAddr, and TxAddr hold time	Input	1	—	ns

Figure 72 shows signal timings during UTOPIA receive operations.

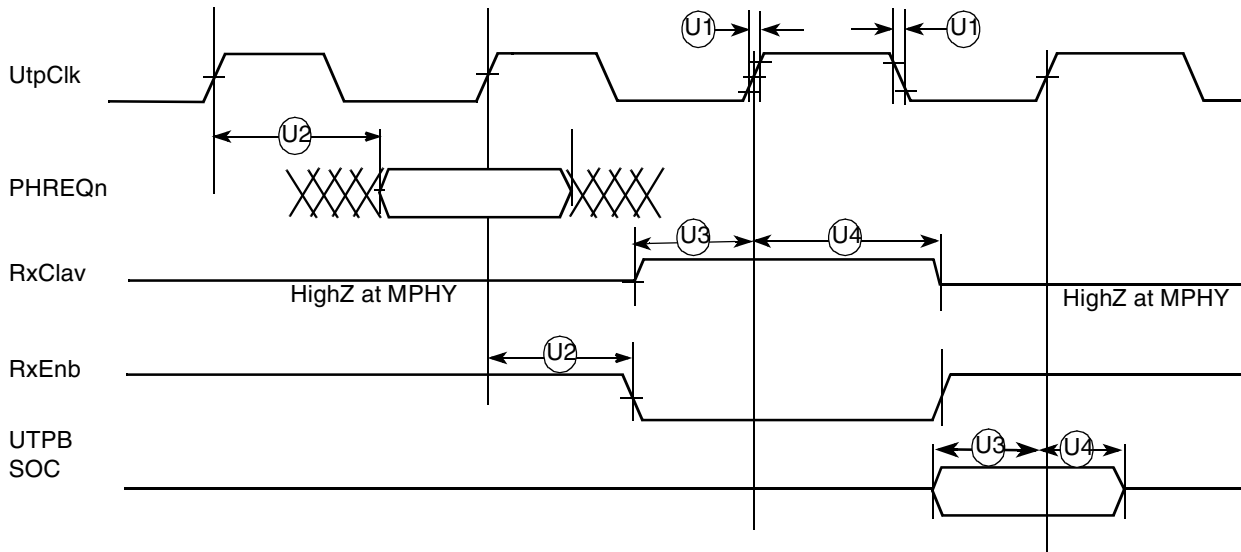


Figure 72. UTOPIA Receive Timing

Figure 73 shows signal timings during UTOPIA transmit operations.

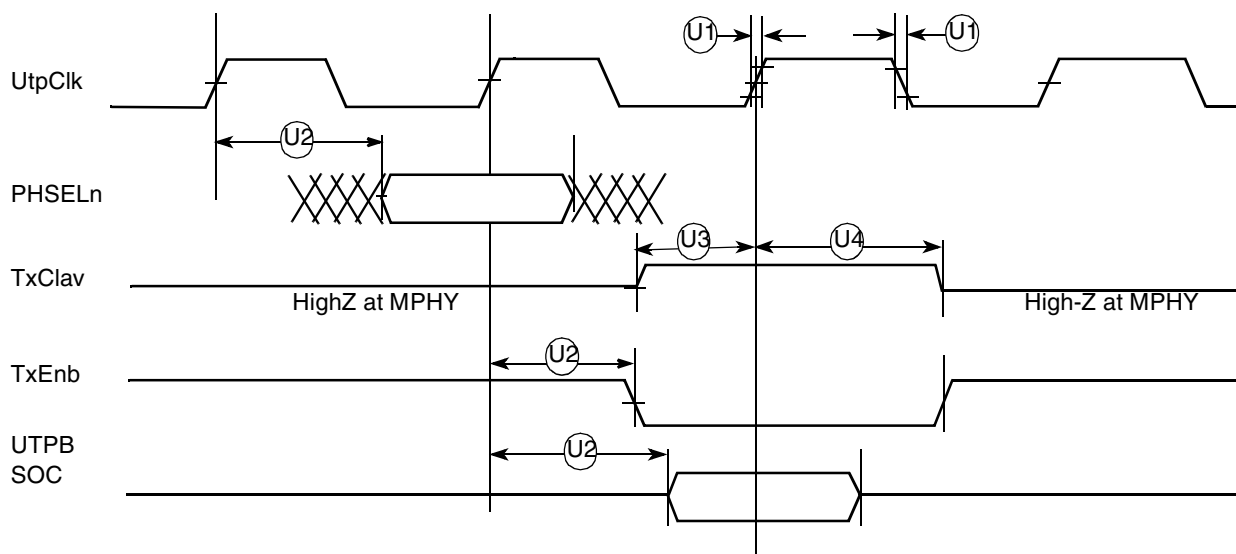


Figure 73. UTOPIA Transmit Timing

14 FEC Electrical Characteristics

This section provides the AC electrical specifications for the fast Ethernet controller (FEC). Note that the timing specifications for the MII signals are independent of system clock frequency (part speed designation). Also, MII signals use TTL signal levels compatible with devices operating at either 5.0 or 3.3 V.

14.1 MII Receive Signal Timing (MII_RXD [3:0], MII_RX_DV, MII_RX_ER, MII_RX_CLK)

The receiver functions correctly up to a MII_RX_CLK maximum frequency of 25 MHz + 1%. There is no minimum frequency requirement. In addition, the processor clock frequency must exceed the MII_RX_CLK frequency – 1%. Table 33 shows the timings for MII receive signal.

Table 33. MII Receive Signal Timing

Num	Characteristic	Min	Max	Unit
M1	MII_RXD[3:0], MII_RX_DV, MII_RX_ER to MII_RX_CLK setup	5	—	ns
M2	MII_RX_CLK to MII_RXD[3:0], MII_RX_DV, MII_RX_ER hold	5	—	ns
M3	MII_RX_CLK pulse width high	35%	65%	MII_RX_CLK period
M4	MII_RX_CLK pulse width low	35%	65%	MII_RX_CLK period

Figure 74 shows the timings for MII receive signal.

15 Mechanical Data and Ordering Information

Table 37 shows information on the MPC866/859 derivative devices.

Table 37. MPC866/859 Derivatives

Device	Number of SCCs ¹	Ethernet Support	Multi-Channel HDLC Support	ATM Support	Cache Size	
					Instruction	Data
MPC866T	4	10/100 Mbps	Yes	Yes	4 Kbyte	4 Kbytes
MPC866P	4	10/100 Mbps	Yes	Yes	16 Kbyte	8 Kbytes
MPC859T	1 (SCC1)	10/100 Mbps	Yes	Yes	4 Kbyte	4 Kbytes
MPC859DSL	1 (SCC1)	10/100 Mbps	No	Up to 4 addresses	4 Kbyte	4 Kbytes

¹ Serial communications controller (SCC).

Table 38 identifies the packages and operating frequencies orderable for the MPC866/859 derivative devices.

Table 38. MPC866/859 Package/Frequency Orderable

Package Type	Temperature (Tj)	Frequency (MHz)	Order Number
Plastic ball grid array (ZP suffix) Non lead free	0° to 95°C	50	MPC859DSLZP50A
		66	MPC859DSLZP66A
		100	MPC859PZP100A MPC859TZP100A MPC866PZP100A MPC866TZP100A
		133	MPC859PZP133A MPC859TZP133A MPC866PZP133A MPC866TZP133A
Plastic ball grid array (CZP suffix) Non lead free	-40° to 100°C	50	MPC859DSLZCP50A
		66	MPC859DSLZCP66A
		100	MPC859PCZP100A MPC859TCZP100A MPC866PCZP100A MPC866TCZP100A

Table 39. Pin Assignments (continued)

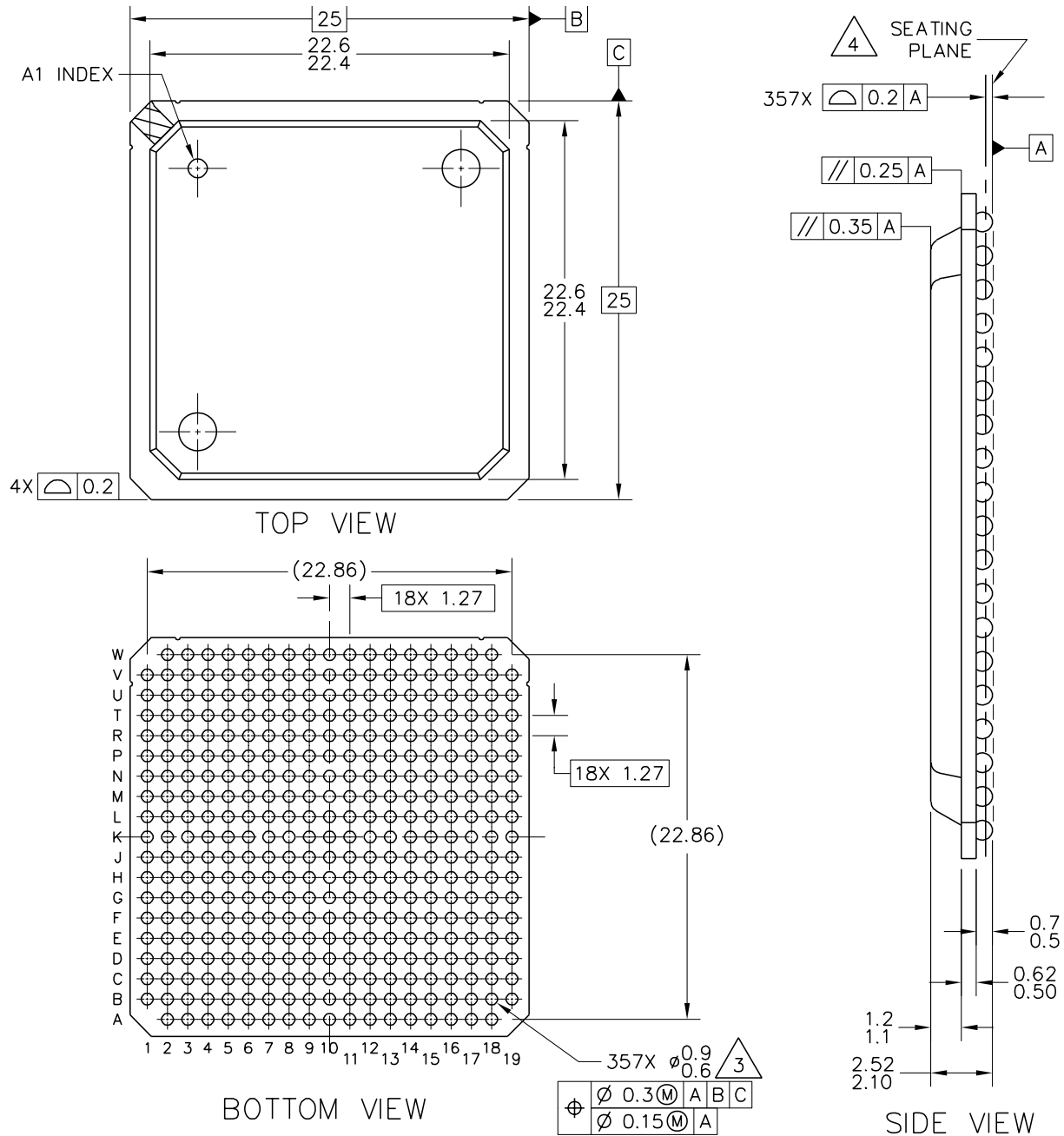
Name	Pin Number	Type
$\overline{\text{BR}}$	G4	Bidirectional
$\overline{\text{BG}}$	E2	Bidirectional
$\overline{\text{BB}}$	E1	Bidirectional Active Pull-up
$\overline{\text{FRZ}}$ $\overline{\text{IRQ6}}$	G3	Bidirectional
$\overline{\text{IRQ0}}$	V14	Input
$\overline{\text{IRQ1}}$	U14	Input
M_TX_CLK $\overline{\text{IRQ7}}$	W15	Input
$\overline{\text{CS}}[0:5]$	C3, A2, D4, E4, A4, B4	Output
$\overline{\text{CS6}}$ $\overline{\text{CE1_B}}$	D5	Output
$\overline{\text{CS7}}$ $\overline{\text{CE2_B}}$	C4	Output
$\overline{\text{WE0}}$ $\overline{\text{BS_B0}}$ $\overline{\text{IORD}}$	C7	Output
$\overline{\text{WE1}}$ $\overline{\text{BS_B1}}$ $\overline{\text{IOWR}}$	A6	Output
$\overline{\text{WE2}}$ $\overline{\text{BS_B2}}$ $\overline{\text{PCOE}}$	B6	Output
$\overline{\text{WE3}}$ $\overline{\text{BS_B3}}$ $\overline{\text{PCWE}}$	A5	Output
$\overline{\text{BS_A}}[0:3]$	D8, C8, A7, B8	Output
$\overline{\text{GPL_A0}}$ $\overline{\text{GPL_B0}}$	D7	Output
$\overline{\text{OE}}$ $\overline{\text{GPL_A1}}$ $\overline{\text{GPL_B1}}$	C6	Output
$\overline{\text{GPL_A}}[2:3]$ $\overline{\text{GPL_B}}[2:3]$ $\overline{\text{CS}}[2-3]$	B5, C5	Output
UPWAITA $\overline{\text{GPL_A4}}$	C1	Bidirectional

Table 39. Pin Assignments (continued)

Name	Pin Number	Type
PB25 RXADDR3 ² SMTXD1	J16	Bidirectional (Optional: Open-drain)
PB24 TXADDR3 ² SMRXD1	J18	Bidirectional (Optional: Open-drain)
PB23 TXADDR2 ² $\overline{\text{SDACK1}}$ $\overline{\text{SMSYN1}}$	K17	Bidirectional (Optional: Open-drain)
PB22 TXADDR4 ² $\overline{\text{SDACK2}}$ $\overline{\text{SMSYN2}}$	L19	Bidirectional (Optional: Open-drain)
PB21 SMTXD2 L1CLKOB PHSEL1 ¹ TXADDR1 ²	K16	Bidirectional (Optional: Open-drain)
PB20 SMRXD2 L1CLKOA PHSEL0 ¹ TXADDR0 ²	L16	Bidirectional (Optional: Open-drain)
PB19 $\overline{\text{RTS1}}$ L1ST1	N19	Bidirectional (Optional: Open-drain)
PB18 RXADDR4 ² $\overline{\text{RTS2}}$ L1ST2	N17	Bidirectional (Optional: Open-drain)
PB17 $\overline{\text{L1RQ6}}$ L1ST3 $\overline{\text{RTS3}}$ PHREQ1 ¹ RXADDR1 ²	P18	Bidirectional (Optional: Open-drain)

15.2 Mechanical Dimensions of the PBGA Package

For more information on the printed-circuit board layout of the PBGA package, including thermal via design and suggested pad layout, please refer to *Plastic Ball Grid Array Application Note* (order number: AN1231/D) available from your local Freescale sales office. [Figure 79](#) shows the mechanical dimensions of the PBGA package.



Note: Solder sphere composition for MPC866XZP, MPC859PZP, MPC859DSLZP, and MPC859TZP is 62%Sn 36%Pb 2%Ag

Figure 79. Mechanical Dimensions and Bottom Surface Nomenclature of the PBGA Package

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