Understanding <u>Embedded - Microprocessors</u>

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of <u>Embedded - Microprocessors</u>

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Active
Core Processor	MPC8xx
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	100MHz
Co-Processors/DSP	Communications; CPM
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10Mbps (4), 10/100Mbps (1)
SATA	-
USB	-
Voltage - I/O	3.3V
Operating Temperature	0°C ~ 95°C (TA)
Security Features	-
Package / Case	357-BBGA
Supplier Device Package	357-PBGA (25x25)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mpc866pzp100a

- One serial peripheral interface (SPI)
  — Supports master and slave modes
  — Supports multiple-master operation on the same bus
- One inter-integrated circuit (I^2C) port
  — Supports master and slave modes
  — Multiple-master environment support
- Time slot assigner (TSA) (MPC859DSL does not have TSA.)
  — Allows SCCs and SMCs to run in multiplexed and/or non-multiplexed operation
  — Supports T1, CEPT, PCM highway, ISDN basic rate, ISDN primary rate, user-defined
  — 1- or 8-bit resolution
  — Allows independent transmit and receive routing, frame synchronization, and clocking
  — Allows dynamic changes
  — On MPC866P and MPC866T, can be internally connected to six serial channels (four SCCs and two SMCs); on MPC859P and MPC859T, can be connected to three serial channels (one SCC and two SMCs).
- Parallel interface port (PIP)
  — Centronics interface support
  — Supports fast connection between compatible ports on MPC866/859 or MC68360
- PCMCIA interface
  — Master (socket) interface, compliant with PCI Local Bus Specification (Rev 2.1)
  — Supports one or two PCMCIA sockets whether ESAR functionality is enabled
  — Eight memory or I/O windows supported
- Debug interface
  — Eight comparators: four operate on instruction address, two operate on data address, and two operate on data.
  — Supports conditions: $= \neq < >$
  — Each watchpoint can generate a breakpoint internally
- Normal high and normal low power modes to conserve power
- 1.8 V core and 3.3 V I/O operation with 5-V TTL compatibility; refer to Table 6 for a listing of the 5-V tolerant pins.
- 357-pin plastic ball grid array (PBGA) package
- Operation up to 133 MHz

4 Thermal Characteristics

Table 4 shows the thermal characteristics for the MPC866/859.

Table 4. MPC866/859 Thermal Resistance Data

Rating	Environment		Symbol	Value	Unit
Junction-to-ambient [1]	Natural Convection	Single-layer board (1s)	$R_{\theta JA}$ [2]	37	°C/W
		Four-layer board (2s2p)	$R_{\theta JMA}$ [3]	23	
	Airflow (200 ft/min)	Single-layer board (1s)	$R_{\theta JMA}$ [3]	30	
		Four-layer board (2s2p)	$R_{\theta JMA}$ [3]	19	
Junction-to-board [4]			$R_{\theta JB}$	13	
Junction-to-case [5]			$R_{\theta JC}$	6	
Junction-to-package top [6]	Natural Convection		Ψ_{JT}	2	
	Airflow (200 ft/min)		Ψ_{JT}	2	

[1] Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, airflow, power dissipation of other components on the board, and board thermal resistance.

[2] Per SEMI G38-87 and JEDEC JESD51-2 with the single-layer board horizontal.

[3] Per JEDEC JESD51-6 with the board horizontal.

[4] Thermal resistance between the die and the printed-circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

[5] Indicates the average thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1) with the cold plate temperature used for the case temperature. For exposed pad packages where the pad would be expected to be soldered, junction-to-case thermal resistance is a simulated value from the junction to the exposed pad without contact resistance.

[6] Thermal characterization parameter indicating the temperature difference between package top and junction temperature per JEDEC JESD51-2.

5 Power Dissipation

Table 5 shows power dissipation information. The modes are 1:1, where CPU and bus speeds are equal, and 2:1 mode, where CPU frequency is twice the bus speed.

Table 5. Power Dissipation (P_D)

Die Revision	Bus Mode	CPU Frequency	Typical [1]	Maximum [2]	Unit
0	1:1	50 MHz	110	140	mW
		66 MHz	150	180	mW
	2:1	66 MHz	140	160	mW
		80 MHz	170	200	mW
		100 MHz	210	250	mW
		133 MHz	260	320	mW

[1]   Typical power dissipation at VDDL and VDDSYN is at 1.8 V. and VDDH is at 3.3 V.
[2]   Maximum power dissipation at VDDL and VDDSYN is at 1.9 V, and VDDH is at 3.465 V.

NOTE

Values in Table 5 represent VDDL based power dissipation and do not include I/O power dissipation over VDDH. I/O power dissipation varies widely by application due to buffer current, depending on external circuitry. The VDDSYN power dissipation is negligible.

6 DC Characteristics

Table 6 shows the DC electrical characteristics for the MPC866/859.

Table 6. DC Electrical Specifications

Characteristic	Symbol	Min	Max	Unit
Operating voltage	VDDL (core)	1.7	1.9	V
	VDDH (I/O)	3.135	3.465	V
	VDDSYN [1]	1.7	1.9	V
	Difference between VDDL to VDDSYN	—	100	mV
Input high voltage (all inputs except EXTAL and EXTCLK) [2]	VIH	2.0	3.465	V

7 Thermal Calculation and Measurement

For the following discussions, P_D = (VDDL x IDDL) + PI/O, where PI/O is the power dissipation of the I/O drivers. The VDDSYN power dissipation is negligible.

7.1 Estimation with Junction-to-Ambient Thermal Resistance

An estimation of the chip junction temperature, T_J, in °C can be obtained from the equation:

$$T_J = T_A + (R_{\theta JA} \times P_D)$$

where:

T_A = ambient temperature (ºC)

$R_{\theta JA}$ = package junction-to-ambient thermal resistance (ºC/W)

P_D = power dissipation in package

The junction-to-ambient thermal resistance is an industry standard value that provides a quick and easy estimation of thermal performance. However, the answer is only an estimate; test cases have demonstrated that errors of a factor of two (in the quantity T_J-T_A) are possible.

7.2 Estimation with Junction-to-Case Thermal Resistance

Historically, the thermal resistance has frequently been expressed as the sum of a junction-to-case thermal resistance and a case-to-ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$$

where:

$R_{\theta JA}$ = junction-to-ambient thermal resistance (ºC/W)

$R_{\theta JC}$ = junction-to-case thermal resistance (ºC/W)

$R_{\theta CA}$ = case-to-ambient thermal resistance (ºC/W)

$R_{\theta JC}$ is device related and cannot be influenced by the user. The user adjusts the thermal environment to affect the case-to-ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the airflow around the device, add a heat sink, change the mounting arrangement on the printed-circuit board, or change the thermal dissipation on the printed-circuit board surrounding the device. This thermal model is most useful for ceramic packages with heat sinks where some 90% of the heat flows through the case and the heat sink to the ambient environment. For most packages, a better model is required.

7.3 Estimation with Junction-to-Board Thermal Resistance

A simple package thermal model that has demonstrated reasonable accuracy (about 20%) is a two-resistor model consisting of a junction-to-board and a junction-to-case thermal resistance. The junction-to-case covers the situation where a heat sink is used or where a substantial amount of heat is dissipated from the top of the package. The junction-to-board thermal resistance describes the thermal performance when most of the heat is conducted to the printed-circuit board. It has been observed that the thermal performance of most plastic packages and especially PBGA packages is strongly dependent on the board temperature; see Figure 3.

Table 9. Bus Operation Timings (continued)

Num	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
B30	$\overline{CS}$, $\overline{WE}$(0:3) negated to A(0:31), BADDR(28:30) invalid GPCM write access [7] (MIN = 0.25 x B1 − 2.00)	5.60	—	4.30	—	3.00	—	1.80	—	ns
B30a	$\overline{WE}$(0:3) negated to A(0:31), BADDR(28:30) invalid GPCM, write access, TRLX = 0, CSNT = 1, $\overline{CS}$ negated to A(0:31) invalid GPCM write access TRLX = 0, CSNT =1 ACS = 10, or ACS == 11, EBDF = 0 (MIN = 0.50 x B1 − 2.00)	13.20	—	10.50	—	8.00	—	5.60	—	ns
B30b	$\overline{WE}$(0:3) negated to A(0:31) invalid GPCM BADDR(28:30) invalid GPCM write access, TRLX = 1, CSNT = 1. $\overline{CS}$ negated to A(0:31) invalid GPCM write access TRLX = 1, CSNT = 1, ACS = 10, or ACS == 11 EBDF = 0 (MIN = 1.50 x B1 − 2.00)	43.50	—	35.50	—	28.00	—	20.70	—	ns
B30c	$\overline{WE}$(0:3) negated to A(0:31), BADDR(28:30) invalid GPCM write access, TRLX = 0, CSNT = 1. $\overline{CS}$ negated to A(0:31) invalid GPCM write access, TRLX = 0, CSNT = 1 ACS = 10, ACS == 11, EBDF = 1 (MIN = 0.375 x B1 − 3.00)	8.40	—	6.40	—	4.50	—	2.70	—	ns
B30d	$\overline{WE}$(0:3) negated to A(0:31), BADDR(28:30) invalid GPCM write access TRLX = 1, CSNT =1, $\overline{CS}$ negated to A(0:31) invalid GPCM write access TRLX = 1, CSNT = 1, ACS = 10 or 11, EBDF = 1	38.67	—	31.38	—	24.50	—	17.83	—	ns
B31	CLKOUT falling edge to $\overline{CS}$ valid, as requested by control bit CST4 in the corresponding word in the UPM (MAX = 0.00 X B1 + 6.00)	1.50	6.00	1.50	6.00	1.50	6.00	1.50	6.00	ns
B31a	CLKOUT falling edge to $\overline{CS}$ valid, as requested by control bit CST1 in the corresponding word in the UPM (MAX = 0.25 x B1 + 6.80)	7.60	14.30	6.30	13.00	5.00	11.80	3.80	10.50	ns
B31b	CLKOUT rising edge to $\overline{CS}$ valid, as requested by control bit CST2 in the corresponding word in the UPM (MAX = 0.00 x B1 + 8.00)	1.50	8.00	1.50	8.00	1.50	8.00	1.50	8.00	ns
B31c	CLKOUT rising edge to $\overline{CS}$ valid, as requested by control bit CST3 in the corresponding word in the UPM (MAX = 0.25 x B1 + 6.30)	7.60	13.80	6.30	12.50	5.00	11.30	3.80	10.00	ns

MPC866/MPC859 Hardware Specifications, Rev. 2

Table 9. Bus Operation Timings (continued)

Num	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
B35	A(0:31), BADDR(28:30) to $\overline{CS}$ valid, as requested by control bit BST4 in the corresponding word in the UPM (MIN = 0.25 x B1 − 2.00)	5.60	—	4.30	—	3.00	—	1.80	—	ns
B35a	A(0:31), BADDR(28:30), and D(0:31) to $\overline{BS}$ valid, as Requested by BST1 in the corresponding word in the UPM (MIN = 0.50 x B1 − 2.00)	13.20	—	10.50	—	8.00	—	5.60	—	ns
B35b	A(0:31), BADDR(28:30), and D(0:31) to $\overline{BS}$ valid, as requested by control bit BST2 in the corresponding word in the UPM (MIN = 0.75 x B1 − 2.00)	20.70	—	16.70	—	13.00	—	9.40	—	ns
B36	A(0:31), BADDR(28:30), and D(0:31) to $\overline{GPL}$ valid as requested by control bit GxT4 in the corresponding word in the UPM (MIN = 0.25 x B1 − 2.00)	5.60	—	4.30	—	3.00	—	1.80	—	ns
B37	UPWAIT valid to CLKOUT falling edge [8] (MIN = 0.00 x B1 + 6.00)	6.00	—	6.00	—	6.00	—	6.00	—	ns
B38	CLKOUT falling edge to UPWAIT valid[8] (MIN = 0.00 x B1 + 1.00)	1.00	—	1.00	—	1.00	—	1.00	—	ns
B39	$\overline{AS}$ valid to CLKOUT rising edge [9] (MIN = 0.00 x B1 + 7.00)	7.00	—	7.00	—	7.00	—	7.00	—	ns
B40	A(0:31), TSIZ(0:1), RD/$\overline{WR}$, $\overline{BURST}$, valid to CLKOUT rising edge (MIN = 0.00 x B1 + 7.00)	7.00	—	7.00	—	7.00	—	7.00	—	ns
B41	$\overline{TS}$ valid to CLKOUT rising edge (setup time) (MIN = 0.00 x B1 + 7.00)	7.00	—	7.00	—	7.00	—	7.00	—	ns
B42	CLKOUT rising edge to $\overline{TS}$ valid (hold time) (MIN = 0.00 x B1 + 2.00)	2.00	—	2.00	—	2.00	—	2.00	—	ns
B43	$\overline{AS}$ negation to memory controller signals negation (MAX = TBD)	—	TBD	—	TBD	—	TBD	—	TBD	ns

[1] For part speeds above 50 MHz, use 9.80 ns for B11a.

[2] The timing required for $\overline{BR}$ input is relevant when the MPC866/859 is selected to work with the internal bus arbiter. The timing for $\overline{BG}$ input is relevant when the MPC866/859 is selected to work with the external bus arbiter.

[3] For part speeds above 50 MHz, use 2 ns for B17.

[4] The D(0:31) and DP(0:3) input timings B18 and B19 refer to the rising edge of CLKOUT, in which the $\overline{TA}$ input signal is asserted.

[5] For part speeds above 50 MHz, use 2 ns for B19.

[6] The D(0:31) and DP(0:3) input timings B20 and B21 refer to the falling edge of CLKOUT. This timing is valid only for read accesses controlled by chip-selects under control of the UPM in the memory controller, for data beats, where DLT3 = 1 in the UPM RAM words. (This is only the case where data is latched on the falling edge of CLKOUT.)

[7] The timing B30 refers to $\overline{CS}$ when ACS = 00 and to $\overline{WE}$(0:3) when CSNT = 0.

8 The signal UPWAIT is considered asynchronous to CLKOUT and synchronized internally. The timings specified in B37 and B38 are specified to enable the freeze of the UPM output signals as described in Figure 20.

9 The $\overline{AS}$ signal is considered asynchronous to CLKOUT. The timing B39 is specified in order to allow the behavior specified in Figure 23.
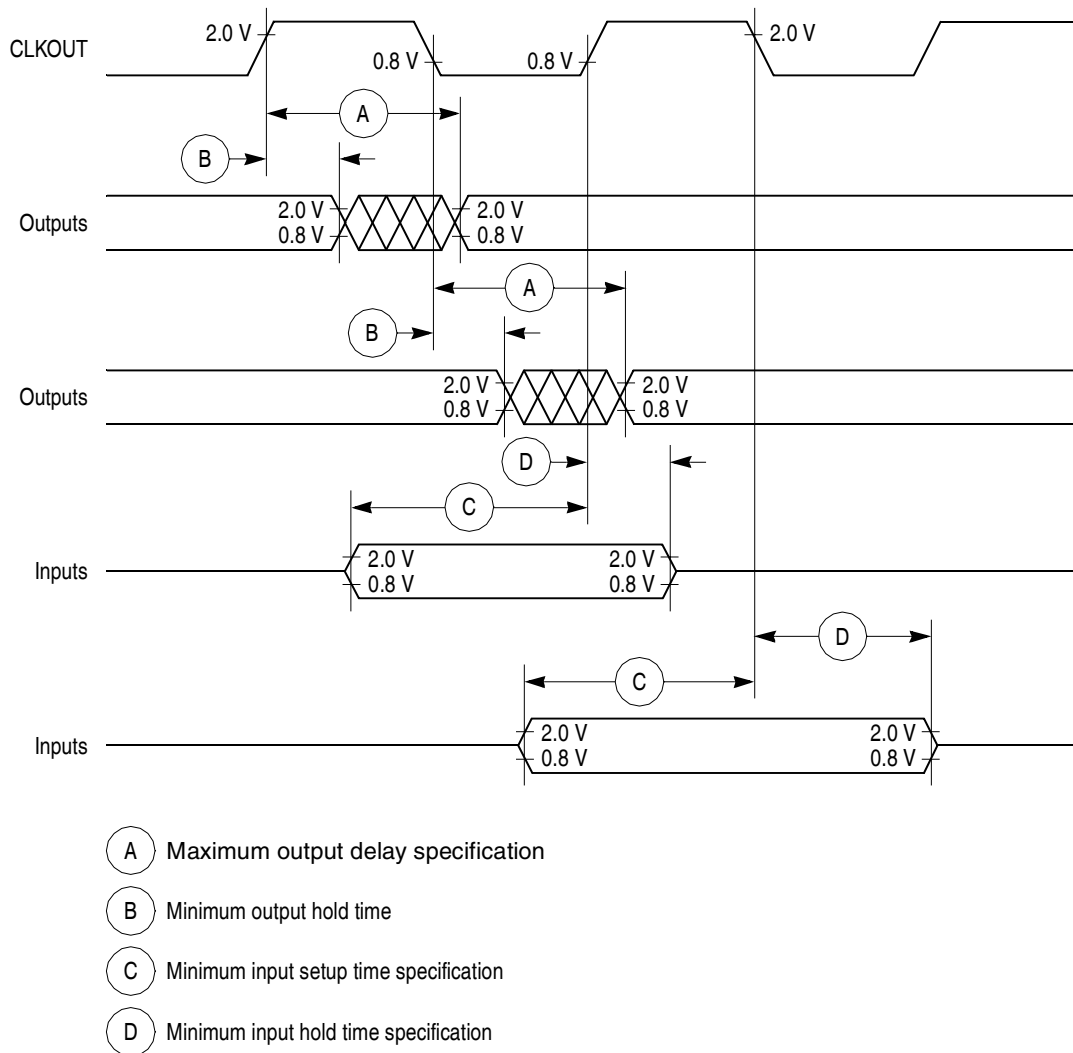
Figure 5 shows the control timing diagram.

A	Maximum output delay specification
B	Minimum output hold time
C	Minimum input setup time specification
D	Minimum input hold time specification

Figure 5. Control Timing

Figure 22 shows the timing for the synchronous external master access controlled by the GPCM.
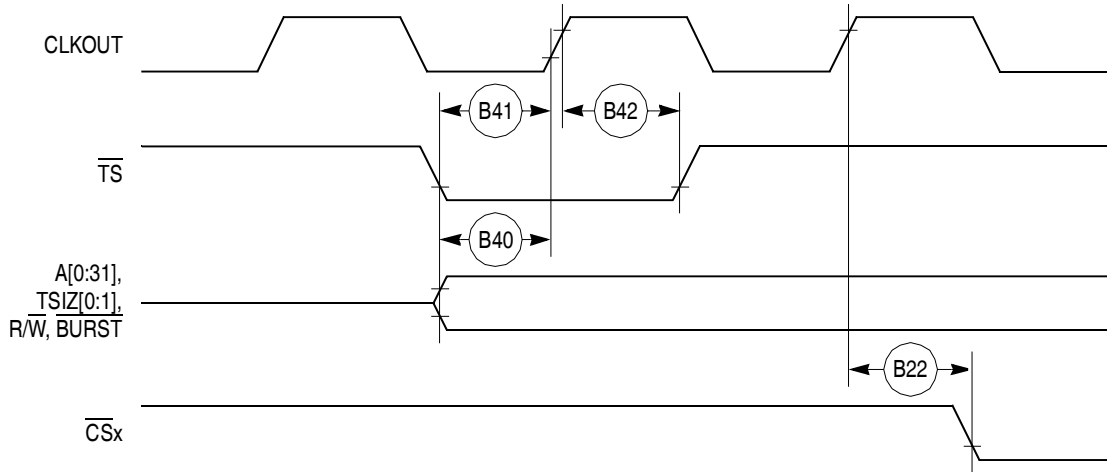
Figure 22. Synchronous External Master Access Timing (GPCM Handled ACS = 00)

Figure 25 shows the interrupt detection timing for the external level-sensitive lines.
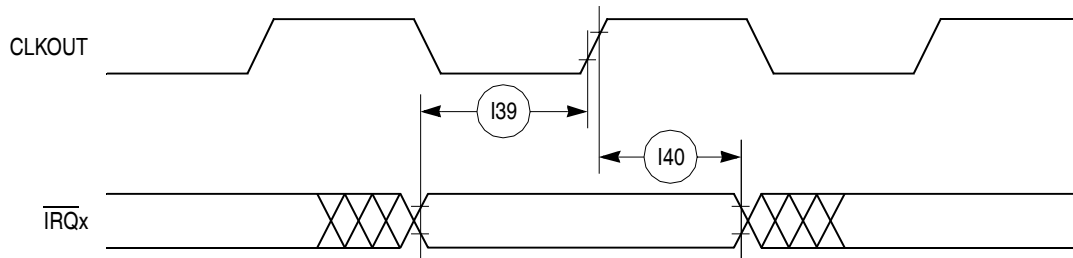
Figure 25. Interrupt Detection Timing for External Level Sensitive Lines

Figure 26 shows the interrupt detection timing for the external edge-sensitive lines.
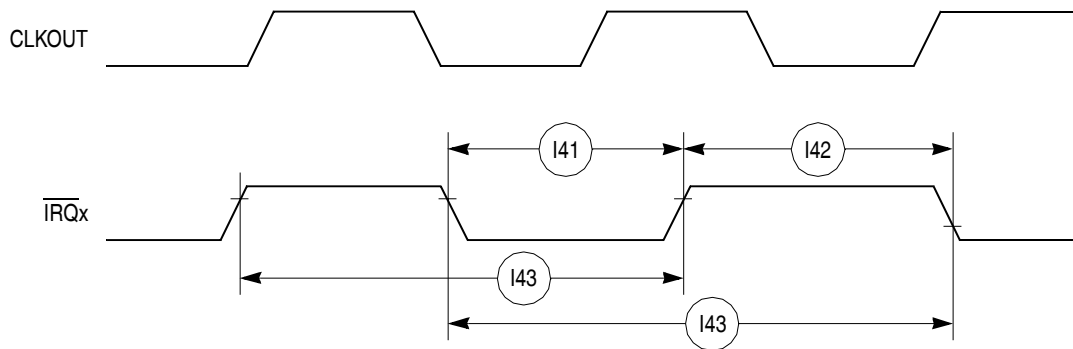

Figure 26. Interrupt Detection Timing for External Edge Sensitive Lines

Table 11 shows the PCMCIA timing for the MPC866/859.

Table 11. PCMCIA Timing

Num	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
P44	A(0:31), $\overline{REG}$ valid to PCMCIA Strobe asserted [1] (MIN = 0.75 x B1 – 2.00)	20.70	—	16.70	—	13.00	—	9.40	—	ns
P45	A(0:31), $\overline{REG}$ valid to ALE negation[1] (MIN = 1.00 x B1 – 2.00)	28.30	—	23.00	—	18.00	—	13.20	—	ns
P46	CLKOUT to $\overline{REG}$ valid (MAX = 0.25 x B1 + 8.00)	7.60	15.60	6.30	14.30	5.00	13.00	3.80	11.80	ns
P47	CLKOUT to $\overline{REG}$ invalid (MIN = 0.25 x B1 + 1.00)	8.60	—	7.30	—	6.00	—	4.80	—	ns
P48	CLKOUT to $\overline{CE1}$, $\overline{CE2}$ asserted (MAX = 0.25 x B1 + 8.00)	7.60	15.60	6.30	14.30	5.00	13.00	3.80	11.80	ns
P49	CLKOUT to $\overline{CE1}$, $\overline{CE2}$ negated (MAX = 0.25 x B1 + 8.00)	7.60	15.60	6.30	14.30	5.00	13.00	3.80	11.80	ns

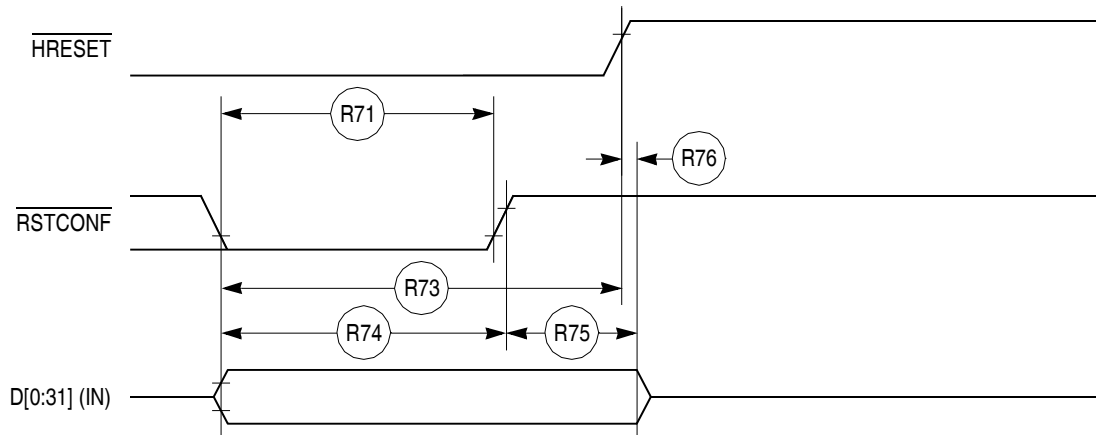Figure 34 shows the reset timing for the data bus configuration.

Figure 34. Reset Timing—Configuration from Data Bus

Figure 35 shows the reset timing for the data bus weak drive during configuration.
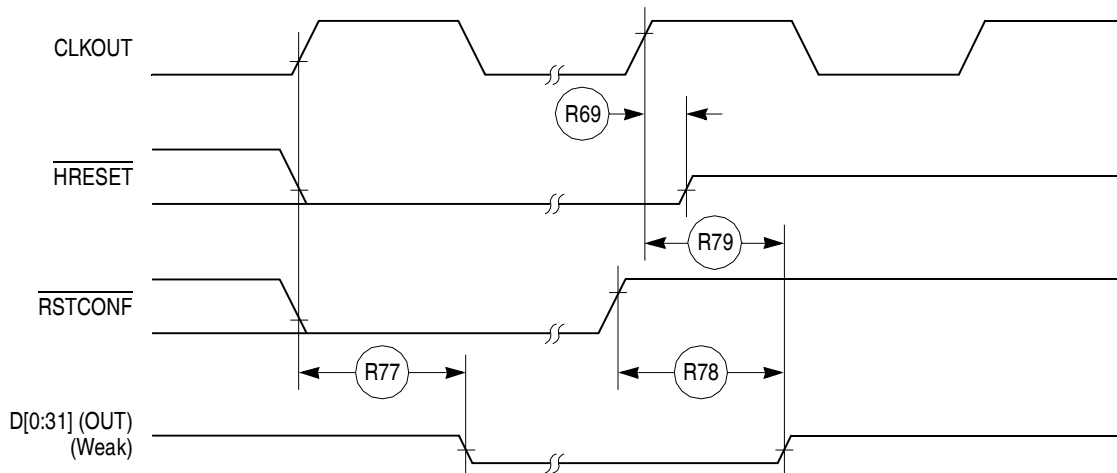

Figure 35. Reset Timing—Data Bus Weak Drive During Configuration

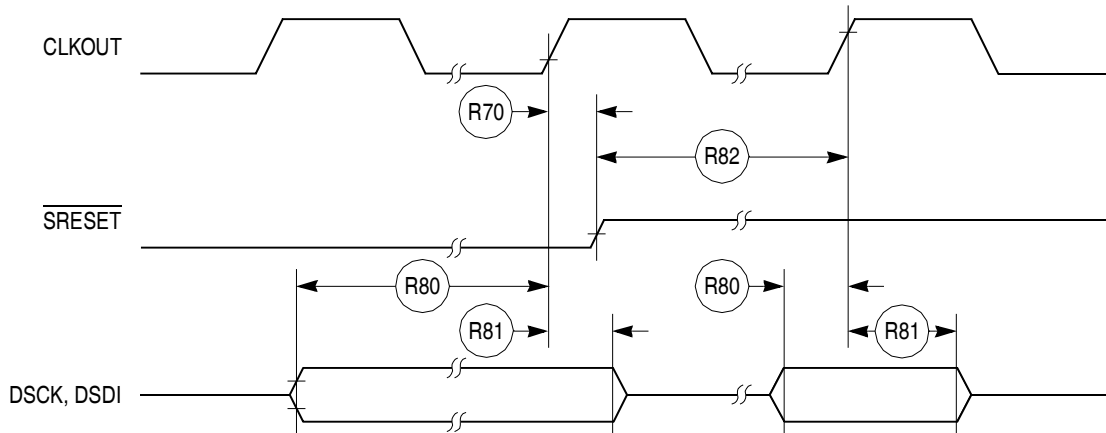Figure 36 shows the reset timing for the debug port configuration.

Figure 36. Reset Timing—Debug Port Configuration

11 IEEE 1149.1 Electrical Specifications

Table 15 shows the JTAG timings for the MPC866/859 shown in Figure 37 through Figure 40.

Table 15. JTAG Timing

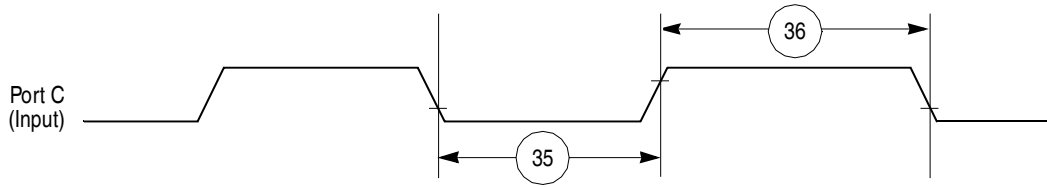| Num	Characteristic	All Frequencies		Unit
		Min	Max	
J82	TCK cycle time	100.00	—	ns
J83	TCK clock pulse width measured at 1.5 V	40.00	—	ns
J84	TCK rise and fall times	0.00	10.00	ns
J85	TMS, TDI data setup time	5.00	—	ns
J86	TMS, TDI data hold time	25.00	—	ns
J87	TCK low to TDO data valid	—	27.00	ns
J88	TCK low to TDO data invalid	0.00	—	ns
J89	TCK low to TDO high impedance	—	20.00	ns
J90	$\overline{TRST}$ assert time	100.00	—	ns
J91	$\overline{TRST}$ setup time to TCK low	40.00	—	ns
J92	TCK falling edge to output valid	—	50.00	ns
J93	TCK falling edge to output valid out of high impedance	—	50.00	ns
J94	TCK falling edge to output high impedance	—	50.00	ns
J95	Boundary scan input valid to TCK rising edge	50.00	—	ns
J96	TCK rising edge to boundary scan input invalid	50.00	—	ns

Figure 46. Port C Interrupt Detection Timing

12.3 IDMA Controller AC Electrical Specifications

Table 18 shows the IDMA controller timings as shown in Figure 47 through Figure 50.

Table 18. IDMA Controller Timing

| Num	Characteristic	All Frequencies		Unit
		Min	Max	
40	$\overline{DREQ}$ setup time to clock high	7	—	ns
41	$\overline{DREQ}$ hold time from clock high	3	—	ns
42	$\overline{SDACK}$ assertion delay from clock high	—	12	ns
43	$\overline{SDACK}$ negation delay from clock low	—	12	ns
44	$\overline{SDACK}$ negation delay from $\overline{TA}$ low	—	20	ns
45	$\overline{SDACK}$ negation delay from clock high	—	15	ns
46	$\overline{TA}$ assertion to falling edge of the clock setup time (applies to external $\overline{TA}$)	7	—	ns
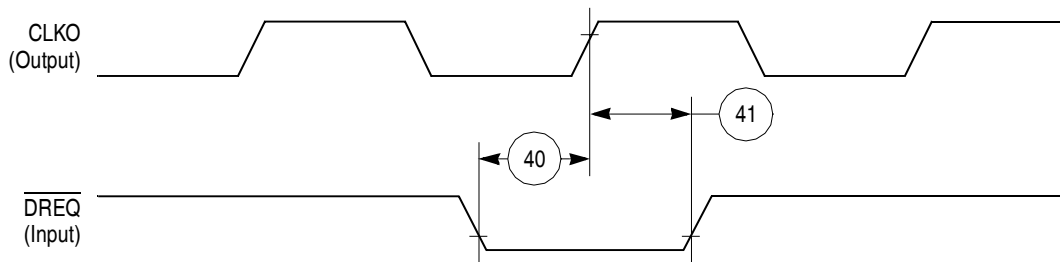
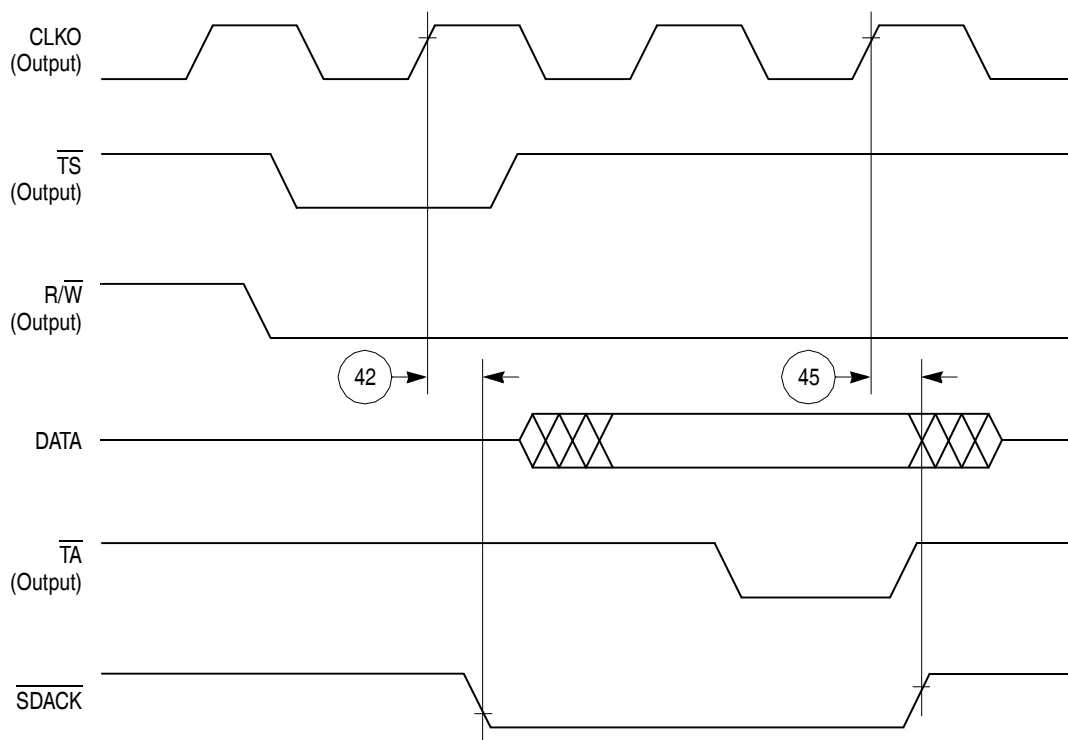**Figure 47. IDMA External Requests Timing Diagram**

Figure 50. $\overline{\text{SDACK}}$ Timing Diagram—Peripheral Read, Internally-Generated $\overline{\text{TA}}$

12.4 Baud Rate Generator AC Electrical Specifications

Table 19 shows the baud rate generator timings as shown in Figure 51.

Table 19. Baud Rate Generator Timing

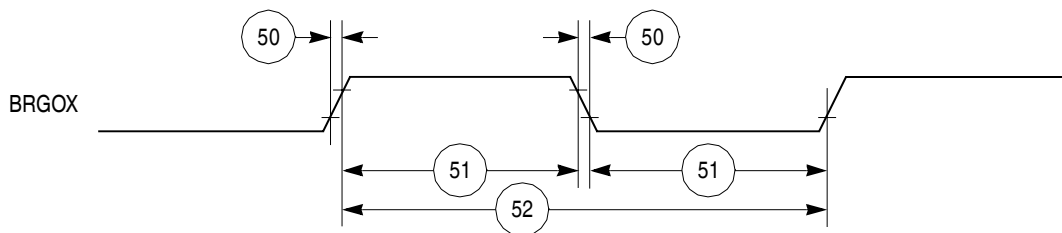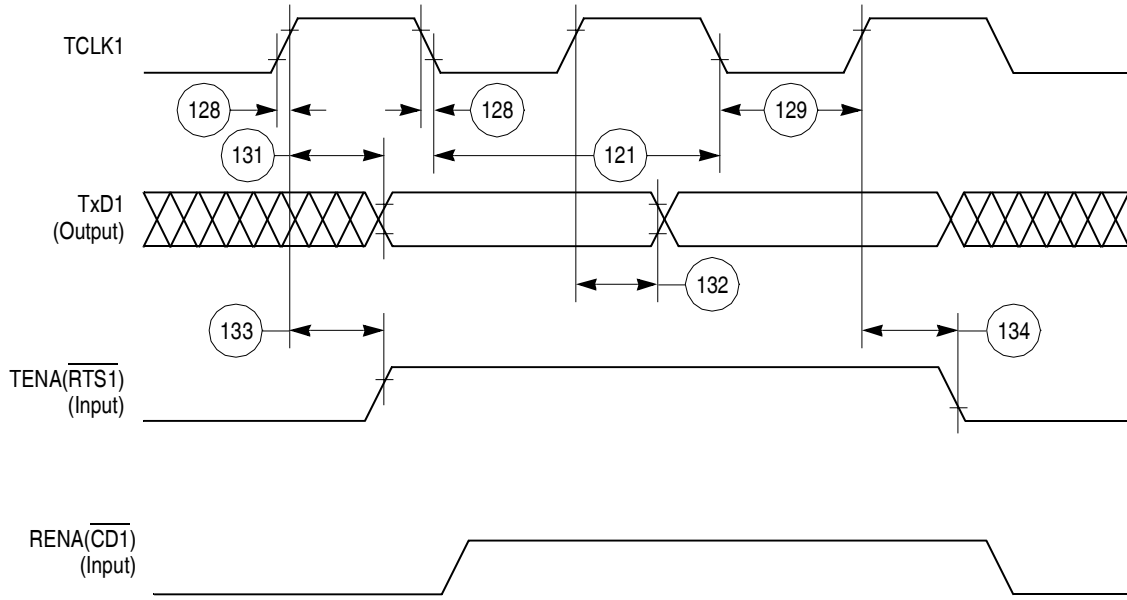| Num	Characteristic	All Frequencies		Unit
		Min	Max	
50	BRGO rise and fall time	—	10	ns
51	BRGO duty cycle	40	60	%
52	BRGO cycle	40	—	ns

Figure 51. Baud Rate Generator Timing Diagram

Notes:
1. Transmit clock invert (TCI) bit in GSMR is set.
2. If RENA is deasserted before TENA, or RENA is not asserted at all during transmit, then the CSL bit is set in the buffer descriptor at the end of the frame transmission.
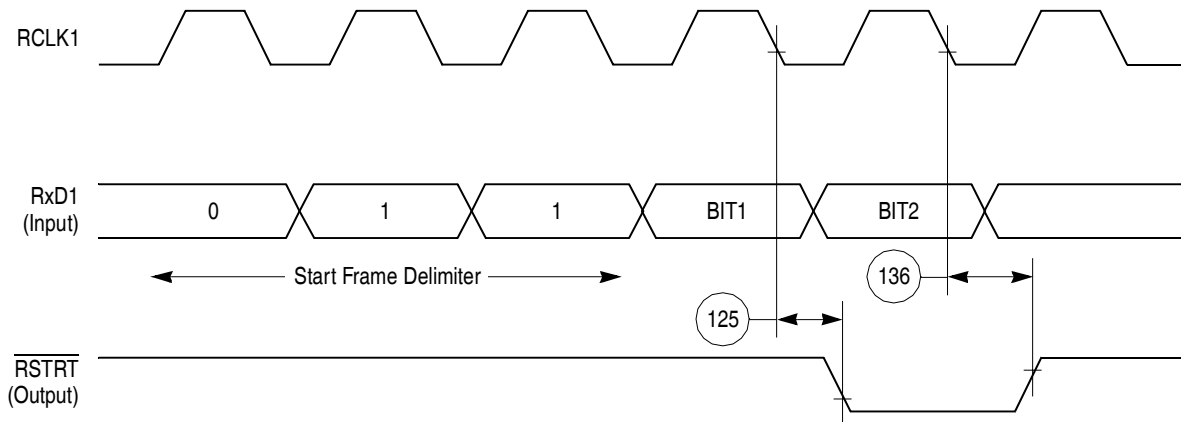
Figure 63. Ethernet Transmit Timing Diagram

Figure 64. CAM Interface Receive Start Timing Diagram

Figure 65. CAM Interface REJECT Timing Diagram

12.9 SMC Transparent AC Electrical Specifications

Table 25 shows the SMC transparent timings as shown in Figure 66.

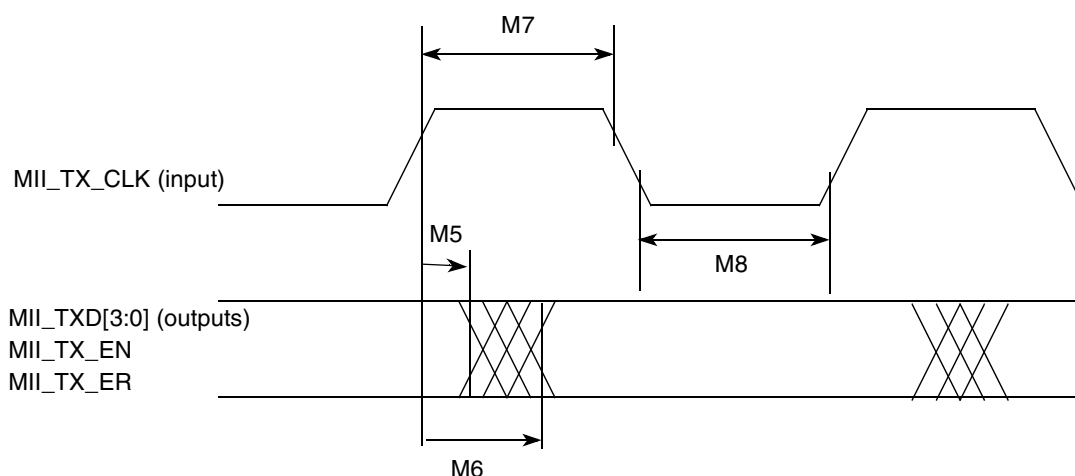Figure 75 shows the MII transmit signal timing diagram.

Figure 75. MII Transmit Signal Timing Diagram

14.3 MII Async Inputs Signal Timing (MII_CRS, MII_COL)

Table 35 shows the timing for on the MII async inputs signal.

Table 35. MII Async Inputs Signal Timing

Num	Characteristic	Min	Max	Unit
M9	MII_CRS, MII_COL minimum pulse width	1.5	—	MII_TX_CLK period

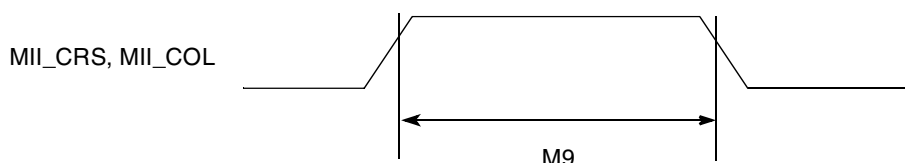Figure 76 shows the MII asynchronous inputs signal timing diagram.

Figure 76. MII Async Inputs Timing Diagram

14.4 MII Serial Management Channel Timing (MII_MDIO, MII_MDC)

Table 36 shows the timing for the MII serial management channel signal. The FEC functions correctly with a maximum MDC frequency in excess of 2.5 MHz. The exact upper bound is under investigation.

Table 36. MII Serial Management Channel Timing

Num	Characteristic	Min	Max	Unit
M10	MII_MDC falling edge to MII_MDIO output invalid (minimum propagation delay)	0	—	ns
M11	MII_MDC falling edge to MII_MDIO output valid (maximum propagation delay)	—	25	ns
M12	MII_MDIO (input) to MII_MDC rising edge setup	10	—	ns

15.1 Pin Assignments

Figure 78 shows the top view pinout of the PBGA package. For additional information, see the *MPC866 PowerQUICC Family User's Manual*.

NOTE: This is the top view of the device.

Figure 78. Pinout of the PBGA Package

Table 39. Pin Assignments (continued)

Name	Pin Number	Type
PB25 RXADDR3[2] SMTXD1	J16	Bidirectional (Optional: Open-drain)
PB24 TXADDR3[2] SMRXD1	J18	Bidirectional (Optional: Open-drain)
PB23 TXADDR2[2] $\overline{\text{SDACK1}}$ $\overline{\text{SMSYN1}}$	K17	Bidirectional (Optional: Open-drain)
PB22 TXADDR4[2] $\overline{\text{SDACK2}}$ $\overline{\text{SMSYN2}}$	L19	Bidirectional (Optional: Open-drain)
PB21 SMTXD2 L1CLKOB PHSEL1 [1] TXADDR1 [2]	K16	Bidirectional (Optional: Open-drain)
PB20 SMRXD2 L1CLKOA PHSEL0[1] TXADDR0[2]	L16	Bidirectional (Optional: Open-drain)
PB19 $\overline{\text{RTS1}}$ L1ST1	N19	Bidirectional (Optional: Open-drain)
PB18 RXADDR4[2] $\overline{\text{RTS2}}$ L1ST2	N17	Bidirectional (Optional: Open-drain)
PB17 $\overline{\text{L1RQb}}$ L1ST3 $\overline{\text{RTS3}}$ PHREQ1[1] RXADDR1[2]	P18	Bidirectional (Optional: Open-drain)

MPC866/MPC859 Hardware Specifications, Rev. 2

15.2 Mechanical Dimensions of the PBGA Package

For more information on the printed-circuit board layout of the PBGA package, including thermal via design and suggested pad layout, please refer to *Plastic Ball Grid Array Application Note* (order number: AN1231/D) available from your local Freescale sales office. Figure 79 shows the mechanical dimensions of the PBGA package.
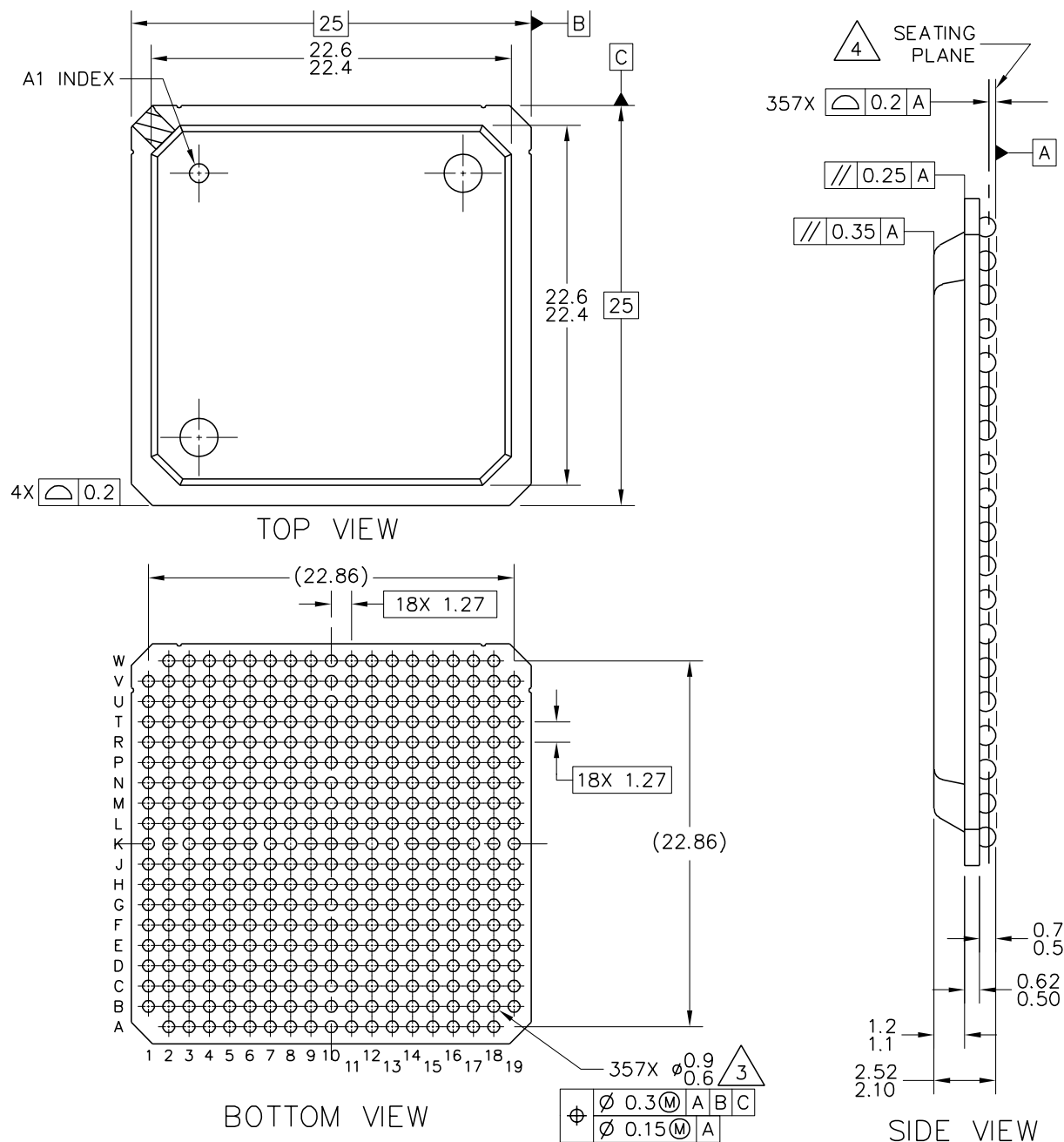
Note: Solder sphere composition for MPC866XZP, MPC859PZP, MPC859DSLZP, and MPC859TZP is 62%Sn 36%Pb 2%Ag

Figure 79. Mechanical Dimensions and Bottom Surface Nomenclature of the PBGA Package

16 Document Revision History

Table 40 lists significant changes between revisions of this document.

Table 40. Document Revision History

Revision Number	Date	Substantive Changes
0	5/2002	Initial revision
1	11/2002	Added the 5-V tolerant pins, new package dimensions, and other changes.
1.1	4/2003	Added the Spec. B1d and changed spec. B1a. Added the Note Solder sphere composition for MPC866XZP, MPC859DSLZP, and MPC859TZP is 62%Sn 36%Pb 2%Ag to Figure 15-79.
1.2	4/2003	Added the MPC859P.
1.3	5/2003	Changed the SPI Master Timing Specs. 162 and 164.
1.4	7-8/2003	• Added TxClav and RxClav to PB15 and PC15. Changed B28a through B28d and B29b to show that TRLX can be 0 or 1. • Added nontechnical reformatting.
1.5	3/14/2005	• Updated document template.
2	2/10/2006	• Updated orderable parts table.

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