NXP USA Inc. - MPC866TCZP100A Datasheet



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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of **Embedded - Microprocessors**

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	MPC8xx
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	100MHz
Co-Processors/DSP	Communications; CPM
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10Mbps (4), 10/100Mbps (1)
SATA	-
USB	-
Voltage - I/O	3.3V
Operating Temperature	-40°C ~ 100°C (TA)
Security Features	-
Package / Case	357-BBGA
Supplier Device Package	357-PBGA (25x25)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc866tczp100a

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



Features

- One serial peripheral interface (SPI)
 - Supports master and slave modes
 - Supports multiple-master operation on the same bus
- One inter-integrated circuit (I²C) port
 - Supports master and slave modes
 - Multiple-master environment support
- Time slot assigner (TSA) (MPC859DSL does not have TSA.)
 - Allows SCCs and SMCs to run in multiplexed and/or non-multiplexed operation
 - Supports T1, CEPT, PCM highway, ISDN basic rate, ISDN primary rate, user-defined
 - 1- or 8-bit resolution
 - Allows independent transmit and receive routing, frame synchronization, and clocking
 - Allows dynamic changes
 - On MPC866P and MPC866T, can be internally connected to six serial channels (four SCCs and two SMCs); on MPC859P and MPC859T, can be connected to three serial channels (one SCC and two SMCs).
- Parallel interface port (PIP)
 - Centronics interface support
 - Supports fast connection between compatible ports on MPC866/859 or MC68360
- PCMCIA interface
 - Master (socket) interface, compliant with PCI Local Bus Specification (Rev 2.1)
 - Supports one or two PCMCIA sockets whether ESAR functionality is enabled
 - Eight memory or I/O windows supported
- Debug interface
 - Eight comparators: four operate on instruction address, two operate on data address, and two operate on data.
 - Supports conditions: = $\neq < >$
 - Each watchpoint can generate a breakpoint internally
- Normal high and normal low power modes to conserve power
- 1.8 V core and 3.3 V I/O operation with 5-V TTL compatibility; refer to Table 6 for a listing of the 5-V tolerant pins.
- 357-pin plastic ball grid array (PBGA) package
- Operation up to 133 MHz



Thermal Calculation and Measurement

7 Thermal Calculation and Measurement

For the following discussions, $P_D = (VDDL \times IDDL) + PI/O$, where PI/O is the power dissipation of the I/O drivers. The VDDSYN power dissipation is negligible.

7.1 Estimation with Junction-to-Ambient Thermal Resistance

An estimation of the chip junction temperature, T_J, in °C can be obtained from the equation:

 $T_J = T_A + (R_{\theta JA} \times P_D)$

where:

 T_A = ambient temperature (°C)

 $R_{\theta JA}$ = package junction-to-ambient thermal resistance (°C/W)

 P_D = power dissipation in package

The junction-to-ambient thermal resistance is an industry standard value that provides a quick and easy estimation of thermal performance. However, the answer is only an estimate; test cases have demonstrated that errors of a factor of two (in the quantity T_{J} - T_{A}) are possible.

7.2 Estimation with Junction-to-Case Thermal Resistance

Historically, the thermal resistance has frequently been expressed as the sum of a junction-to-case thermal resistance and a case-to-ambient thermal resistance:

 $R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$

where:

 $R_{\theta JA}$ = junction-to-ambient thermal resistance (°C/W)

 $R_{\theta JC}$ = junction-to-case thermal resistance (°C/W)

 $R_{\theta CA}$ = case-to-ambient thermal resistance (°C/W)

 $R_{\theta JC}$ is device related and cannot be influenced by the user. The user adjusts the thermal environment to affect the case-to-ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the airflow around the device, add a heat sink, change the mounting arrangement on the printed-circuit board, or change the thermal dissipation on the printed-circuit board surrounding the device. This thermal model is most useful for ceramic packages with heat sinks where some 90% of the heat flows through the case and the heat sink to the ambient environment. For most packages, a better model is required.

7.3 Estimation with Junction-to-Board Thermal Resistance

A simple package thermal model that has demonstrated reasonable accuracy (about 20%) is a two-resistor model consisting of a junction-to-board and a junction-to-case thermal resistance. The junction-to-case covers the situation where a heat sink is used or where a substantial amount of heat is dissipated from the top of the package. The junction-to-board thermal resistance describes the thermal performance when most of the heat is conducted to the printed-circuit board. It has been observed that the thermal performance of most plastic packages and especially PBGA packages is strongly dependent on the board temperature; see Figure 3.



Thermal Calculation and Measurement

7.5 Experimental Determination

To determine the junction temperature of the device in the application after prototypes are available, the thermal characterization parameter (Ψ_{JT}) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using the following equation:

 $T_J = T_T + (\Psi_{JT} \times P_D)$

where:

 Ψ_{JT} = thermal characterization parameter

 T_T = thermocouple temperature on top of package

 P_D = power dissipation in package

The thermal characterization parameter is measured per JESD51-2 specification published by JEDEC using a 40 gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

7.6 References

Semiconductor Equipment and Materials International(415) 964-5111 805 East Middlefield Rd. Mountain View, CA 94043

MIL-SPEC and EIA/JESD (JEDEC) specifications800-854-7179 or (Available from Global Engineering Documents)303-397-7956

JEDEC Specifications http://www.jedec.org

1. C.E. Triplett and B. Joiner, "An Experimental Characterization of a 272 PBGA Within an Automotive Engine Controller Module," Proceedings of SemiTherm, San Diego, 1998, pp. 47-54.

2. B. Joiner and V. Adams, "Measurement and Simulation of Junction to Board Thermal Resistance and Its Application in Thermal Modeling," Proceedings of SemiTherm, San Diego, 1999, pp. 212-220.



Num	Ohovo stovistis	33 MHz		40 MHz		50 MHz		66 MHz		
NUM	Characteristic	Min	Max	Min	Мах	Min	Max	Min	Max	Unit
B28d	CLKOUT falling edge to \overline{CS} negated GPCM write access TRLX = 0,1, CSNT = 1, ACS = 10, or ACS = 11, EBDF = 1 (MAX = 0.375 x B1 + 6.6)	_	18.00	_	18.00	_	14.30	_	12.30	ns
B29	$\overline{\text{WE}}$ (0:3) negated to D(0:31), DP(0:3) High-Z GPCM write access, CSNT = 0, EBDF = 0 (MIN = 0.25 x B1 - 2.00)	5.60		4.30	—	3.00	_	1.80		ns
B29a	$\overline{\text{WE}}(0:3)$ negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 0, CSNT = 1, EBDF = 0 (MIN = 0.50 x B1 - 2.00)	13.20		10.50	_	8.00	_	5.60		ns
B29b	$\overline{\text{CS}}$ negated to D(0:31), DP(0:3), High Z GPCM write access, ACS = 00, TRLX = 0,1 & CSNT = 0 (MIN = 0.25 x B1-2.00)	5.60	_	4.30	_	3.00	_	1.80	_	ns
B29c	$\overline{\text{CS}}$ negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 0, CSNT = 1, ACS = 10, or ACS = 11, EBDF = 0 (MIN = 0.50 x B1 - 2.00)	13.20	_	10.50	_	8.00	_	5.60	_	ns
B29d	$\overline{\text{WE}}$ (0:3) negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 1, CSNT = 1, EBDF = 0 (MIN = 1.50 x B1 - 2.00)	43.50	_	35.50	_	28.00	_	20.70	_	ns
B29e	$\overline{\text{CS}}$ negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 1, CSNT = 1, ACS = 10, or ACS = 11, EBDF = 0 (MIN = 1.50 x B1 - 2.00)	43.50	_	35.50	_	28.00	_	20.70	_	ns
B29f	$\overline{\text{WE}}$ (0:3) negated to D(0:31), DP(0:3) High Z GPCM write access, TRLX = 0, CSNT = 1, EBDF = 1 (MIN = 0.375 x B1 - 6.30)	5.00	_	3.00	_	1.10	_	0.00	_	ns
B29g		5.00	_	3.00	_	1.10	_	0.00	_	ns
B29h	$\overline{\text{WE}}(0:3)$ negated to D(0:31), DP(0:3) High Z GPCM write access, TRLX = 1, CSNT = 1, EBDF = 1 (MIN = 0.375 x B1 - 3.30)	38.40	_	31.10	_	24.20	_	17.50	_	ns
B29i	$\overline{\text{CS}}$ negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 1, CSNT = 1, ACS = 10 or ACS = 11, EBDF = 1 (MIN = 0.375 x B1 - 3.30)	38.40	_	31.10	_	24.20	_	17.50	_	ns

Table 9. Bus Operation Timings (continued)



Figure 8 shows the timing for the synchronous active pull-up and open-drain output signals.



Figure 8. Synchronous Active Pull-Up Resistor and Open-Drain Output Signals Timing

Figure 9 shows the timing for the synchronous input signals.



Figure 9. Synchronous Input Signals Timing





Figure 15. External Bus Read Timing (GPCM Controlled—TRLX = 0 or 1, ACS = 10, ACS = 11)





Figure 17. External Bus Write Timing (GPCM Controlled—TRLX = 0, CSNT = 1)







Figure 18. External Bus Write Timing (GPCM Controlled—TRLX = 1, CSNT = 1)



Figure 23 shows the timing for the asynchronous external master memory access controlled by the GPCM.



Figure 23. Asynchronous External Master Memory Access Timing (GPCM Controlled—ACS = 00)

Figure 24 shows the timing for the asynchronous external master control signals negation.



Figure 24. Asynchronous External Master—Control Signals Negation Timing

Table 10 shows the interrupt timing for the MPC866/859.

Table 10. Interrupt Timing

Num	Characteristic ¹	All Frequenc	Unit	
Num	Characteristic	Min	Max	Unit
139	IRQx valid to CLKOUT rising edge (setup time)	6.00	_	ns
140	IRQx hold time after CLKOUT	2.00	_	ns
141	IRQx pulse width low	3.00	_	ns
142	IRQx pulse width high	3.00	_	ns
143	IRQx edge-to-edge time	4xT _{CLOCKOUT}	_	_
1 The	imings 130 and 140 describe the testing conditions under which the \overline{IRO} lines	are tested when h	aina daf	inod ac

The timings I39 and I40 describe the testing conditions under which the IRQ lines are tested when being defined as level sensitive. The IRQ lines are synchronized internally and do not have to be asserted or negated with reference to the CLKOUT.

The timings I41, I42, and I43 are specified to allow the correct function of the IRQ lines detection circuitry, and has no direct relation with the total system interrupt latency that the MPC866/859 is able to support.



Figure 27 shows the PCMCIA access cycle timing for the external bus read.



Figure 27. PCMCIA Access Cycles Timing External Bus Read







Figure 28. PCMCIA Access Cycles Timing External Bus Write

Figure 29 shows the PCMCIA WAIT signals detection timing.



Figure 29. PCMCIA WAIT Signals Detection Timing

MPC866/MPC859 Hardware Specifications, Rev. 2





Figure 41. PIP Rx (Interlock Mode) Timing Diagram



Figure 42. PIP Tx (Interlock Mode) Timing Diagram



Figure 43. PIP Rx (Pulse Mode) Timing Diagram





Figure 44. PIP TX (Pulse Mode) Timing Diagram



Figure 45. Parallel I/O Data-In/Data-Out Timing Diagram

12.2 Port C Interrupt AC Electrical Specifications

Table 17 shows timings for port C interrupts.

Table 17.	Port C	Interrupt	Timing
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Num	Characteristic		33.34 MHz		
Num			Мах	Om	
35	Port C interrupt pulse width low (edge-triggered mode)	55	_	ns	
36	Port C interrupt minimum time between active edges	55		ns	

Figure 46 shows the port C interrupt detection timing.



CPM Electrical Characteristics



Figure 54. SI Receive Timing with Double-Speed Clocking (DSC = 1)





MPC866/MPC859 Hardware Specifications, Rev. 2



Num	Characteristic	All Freq	Unit	
		Min	Max	Unit
134	TENA inactive delay (from TCLK1 rising edge)	10	50	ns
135	RSTRT active delay (from TCLK1 falling edge)	10	50	ns
136	RSTRT inactive delay (from TCLK1 falling edge)	10	50	ns
137	REJECT width low	1	—	CLK
138	CLKO1 low to SDACK asserted ²	—	20	ns
139	CLKO1 low to SDACK negated ²	_	20	ns

Table 24. Ethernet Timing (continued)

¹ The ratios SyncCLK/RCLK1 and SyncCLK/TCLK1 must be greater or equal to 2/1.

² SDACK is asserted whenever the SDMA writes the incoming frame DA into memory.



Figure 61. Ethernet Collision Timing Diagram









Figure 69. SPI Slave (CP = 0) Timing Diagram



UTOPIA AC Electrical Specifications

Figure 71 shows the I^2C bus timing.



Figure 71. I²C Bus Timing Diagram

13 UTOPIA AC Electrical Specifications

Table 30 through Table 32 show the AC electrical specifications for the UTOPIA interface.

Num	Signal Characteristic	Direction	Min	Max	Unit
U1	UtpClk rise/fall time (Internal clock option)	Output	_	4	ns
	Duty cycle		50	50	%
	Frequency		_	33	MHz
U2	UTPB, SOC, RXEnb, TXEnb, RXAddr, and TXAddr-active delay (and PHREQ and PHSEL active delay in MPHY mode)	Output	2	16	ns
U3	UTPB, SOC, Rxclav and Txclav setup time	Input	4	_	ns
U4	UTPB, SOC, Rxclav and Txclav hold time	Input	1	_	ns

Table 30. UTOPIA Master (Muxed Mode) Electrical Specifications

Table 31. UTOPIA Master (Split Bus Mode) Electrical Specifications

Num	Signal Characteristic	Direction	Min	Max	Unit
U1	UtpClk rise/fall time (Internal clock option)	Output	_	4	ns
	Duty cycle		50	50	%
	Frequency		—	33	MHz
U2	UTPB, SOC, RxEnb, TxEnb, RxAddr and TxAddr active delay (PHREQ and PHSEL active delay in MPHY mode)	Output	2	16	ns
U3	UTPB_Aux, SOC_Aux, Rxclav, and Txclav setup time	Input	4	—	ns
U4	UTPB_Aux, SOC_Aux, Rxclav, and Txclav hold time	Input	1	—	ns



Table 39. Pin Assignments (continued)

Name	Pin Number	Туре
PB25 RXADDR3 ² SMTXD1	J16	Bidirectional (Optional: Open-drain)
PB24 TXADDR3 ² SMRXD1	J18	Bidirectional (Optional: Open-drain)
PB23 TXADDR2 ² SDACK1 SMSYN1	K17	Bidirectional (Optional: Open-drain)
PB22 TXADDR4 ² SDACK2 SMSYN2	L19	Bidirectional (Optional: Open-drain)
PB21 SMTXD2 L1CLKOB PHSEL1 ¹ TXADDR1 ²	K16	Bidirectional (Optional: Open-drain)
PB20 SMRXD2 L1CLKOA PHSEL0 ¹ TXADDR0 ²	L16	Bidirectional (Optional: Open-drain)
PB19 RTS1 L1ST1	N19	Bidirectional (Optional: Open-drain)
PB18 RXADDR4 ² RTS2 L1ST2	N17	Bidirectional (Optional: Open-drain)
PB17 L1RQb L1ST3 RTS3 PHREQ1 ¹ RXADDR1 ²	P18	Bidirectional (Optional: Open-drain)



Mechanical Data and Ordering Information

Name	Pin Number	Туре
PB16 L1RQa L1ST4 RTS4 PHREQ0 ¹ RXADDR0 ²	N16	Bidirectional (Optional: Open-drain)
PB15 BRGO3 TxClav RxClav	R17	Bidirectional
PB14 RXADDR2 ² RSTRT1	U18	Bidirectional
PC15 DREQ0 RTS1 L1ST1 RxClav TxClav	D16	Bidirectional
PC14 DREQ1 RTS2 L1ST2	D18	Bidirectional
PC13 L1RQb L1ST3 RTS3	E18	Bidirectional
PC12 L1RQa L1ST4 RTS4	F18	Bidirectional
PC11 CTS1	J19	Bidirectional
PC10 CD1 TGATE1	К19	Bidirectional
PC9 CTS2	L18	Bidirectional
PC8 CD2 TGATE2	M18	Bidirectional

Table 39. Pin Assignments (continued)