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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	MPC8xx
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	133MHz
Co-Processors/DSP	Communications; CPM
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10Mbps (4), 10/100Mbps (1)
SATA	-
USB	-
Voltage - I/O	3.3V
Operating Temperature	0°C ~ 95°C (TA)
Security Features	-
Package / Case	357-BBGA
Supplier Device Package	357-PBGA (25x25)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc866tvr133a

- One serial peripheral interface (SPI)
  - Supports master and slave modes
  - Supports multiple-master operation on the same bus
- One inter-integrated circuit (I^2C) port
  - Supports master and slave modes
  - Multiple-master environment support
- Time slot assigner (TSA) (MPC859DSL does not have TSA.)
  - Allows SCCs and SMCs to run in multiplexed and/or non-multiplexed operation
  - Supports T1, CEPT, PCM highway, ISDN basic rate, ISDN primary rate, user-defined
  - 1- or 8-bit resolution
  - Allows independent transmit and receive routing, frame synchronization, and clocking
  - Allows dynamic changes
  - On MPC866P and MPC866T, can be internally connected to six serial channels (four SCCs and two SMCs); on MPC859P and MPC859T, can be connected to three serial channels (one SCC and two SMCs).
- Parallel interface port (PIP)
  - Centronics interface support
  - Supports fast connection between compatible ports on MPC866/859 or MC68360
- PCMCIA interface
  - Master (socket) interface, compliant with PCI Local Bus Specification (Rev 2.1)
  - Supports one or two PCMCIA sockets whether ESAR functionality is enabled
  - Eight memory or I/O windows supported
- Debug interface
  - Eight comparators: four operate on instruction address, two operate on data address, and two operate on data.
  - Supports conditions: $= \neq < >$
  - Each watchpoint can generate a breakpoint internally
- Normal high and normal low power modes to conserve power
- 1.8 V core and 3.3 V I/O operation with 5-V TTL compatibility; refer to Table 6 for a listing of the 5-V tolerant pins.
- 357-pin plastic ball grid array (PBGA) package
- Operation up to 133 MHz

The MPC866/859 is comprised of three modules that each use a 32-bit internal bus: MPC8xx core, system integration unit (SIU), and communication processor module (CPM). The MPC866P block diagram is shown in Figure 1. The MPC859P/859T/859DSL block diagram is shown in Figure 2.

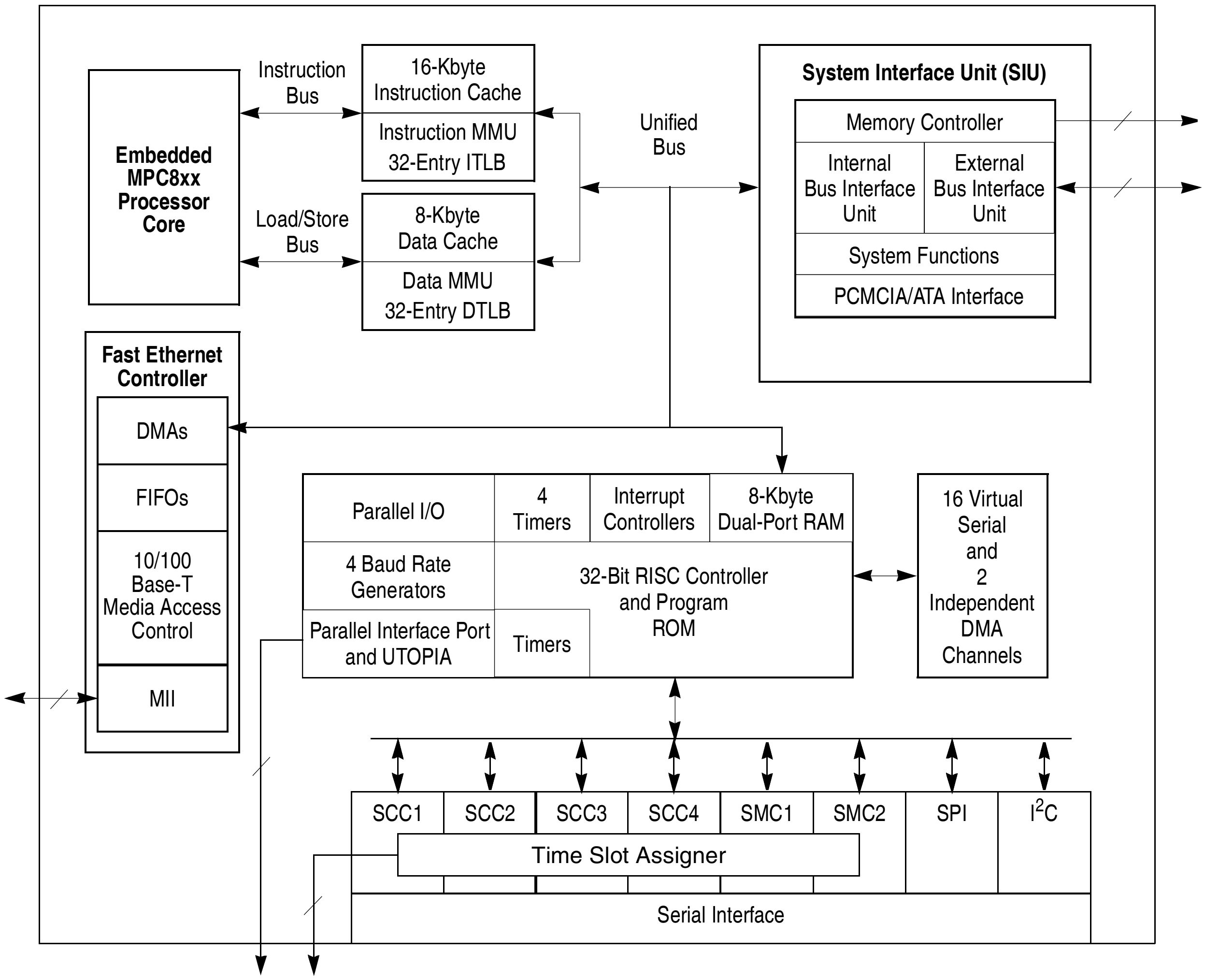


Figure 1. MPC866P Block Diagram

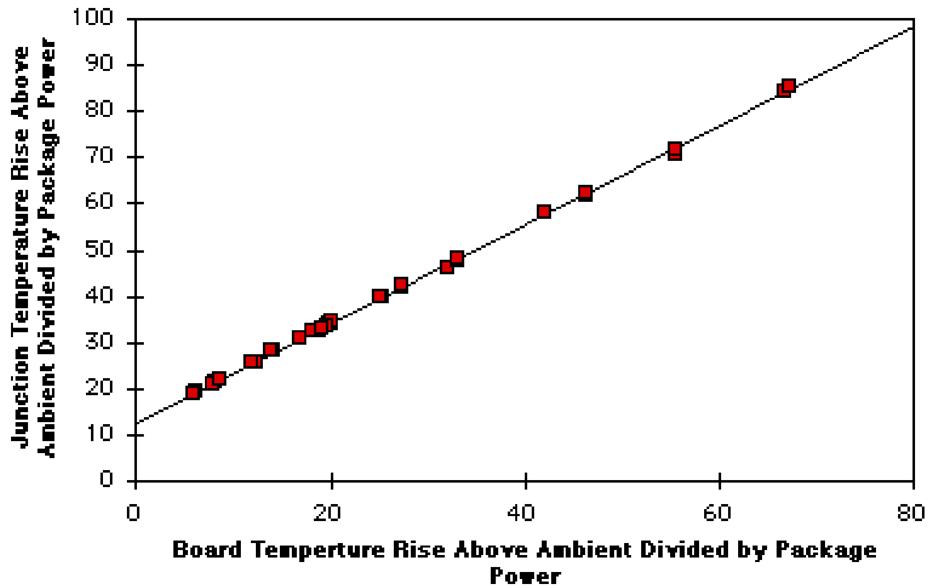


Figure 3. Effect of Board Temperature Rise on Thermal Behavior

If the board temperature is known, an estimate of the junction temperature in the environment can be made using the following equation:

$T_J = T_B + (R_{\theta JB} \times P_D)$

where:

$R_{\theta JB}$ = junction-to-board thermal resistance (ºC/W)

T_B = board temperature ºC

P_D = power dissipation in package

If the board temperature is known and the heat loss from the package case to the air can be ignored, acceptable predictions of junction temperature can be made. For this method to work, the board and board mounting must be similar to the test board used to determine the junction-to-board thermal resistance, namely a 2s2p (board with a power and a ground plane) and vias attaching the thermal balls to the ground plane.

7.4 Estimation Using Simulation

When the board temperature is not known, a thermal simulation of the application is needed. The simple two-resistor model can be used with the thermal simulation of the application [2], or a more accurate and complex model of the package can be used in the thermal simulation.

7.5 Experimental Determination

To determine the junction temperature of the device in the application after prototypes are available, the thermal characterization parameter (Ψ_{JT}) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D)$$

where:

Ψ_{JT} = thermal characterization parameter

T_T = thermocouple temperature on top of package

P_D = power dissipation in package

The thermal characterization parameter is measured per JESD51-2 specification published by JEDEC using a 40 gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

7.6 References

Semiconductor Equipment and Materials International(415) 964-5111
805 East Middlefield Rd.
Mountain View, CA 94043

MIL-SPEC and EIA/JESD (JEDEC) specifications800-854-7179 or
(Available from Global Engineering Documents)303-397-7956

JEDEC Specifications http://www.jedec.org

1. C.E. Triplett and B. Joiner, “An Experimental Characterization of a 272 PBGA Within an Automotive Engine Controller Module,” Proceedings of SemiTherm, San Diego, 1998, pp. 47-54.

2. B. Joiner and V. Adams, “Measurement and Simulation of Junction to Board Thermal Resistance and Its Application in Thermal Modeling,” Proceedings of SemiTherm, San Diego, 1999, pp. 212-220.

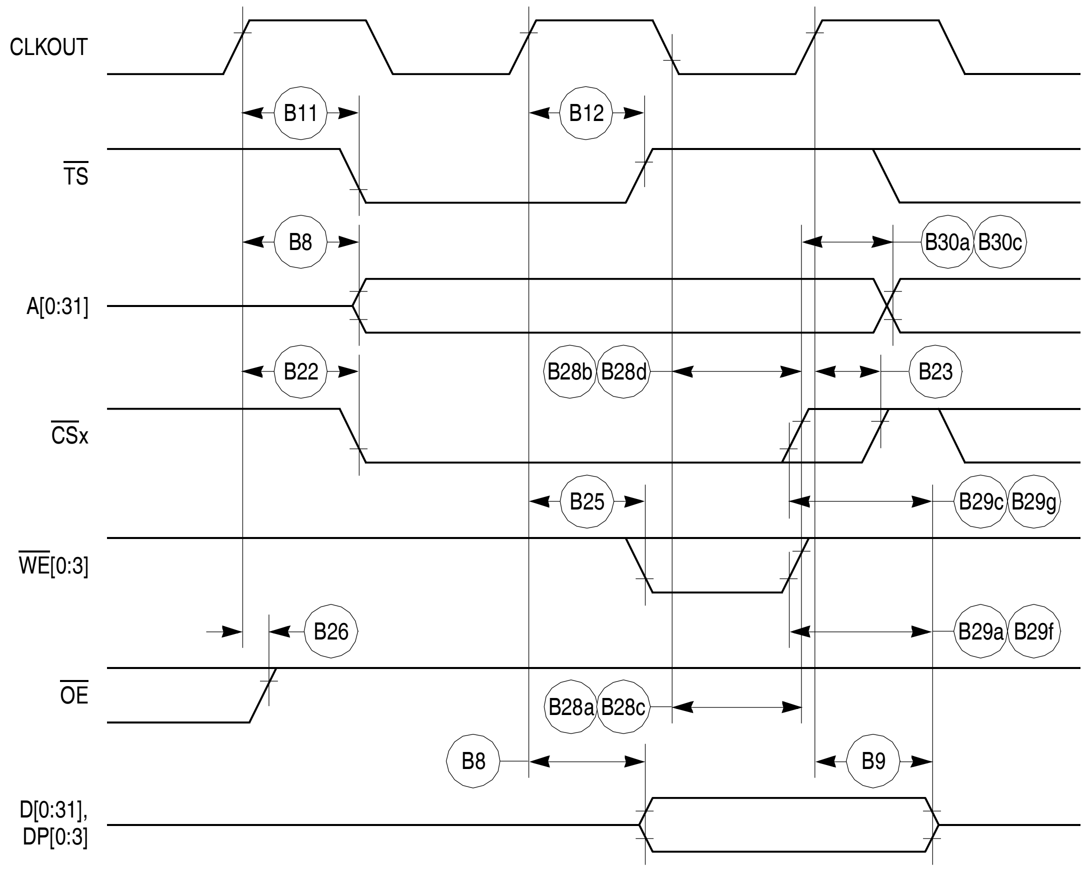


Figure 17. External Bus Write Timing (GPCM Controlled—TRLX = 0, CSNT = 1)

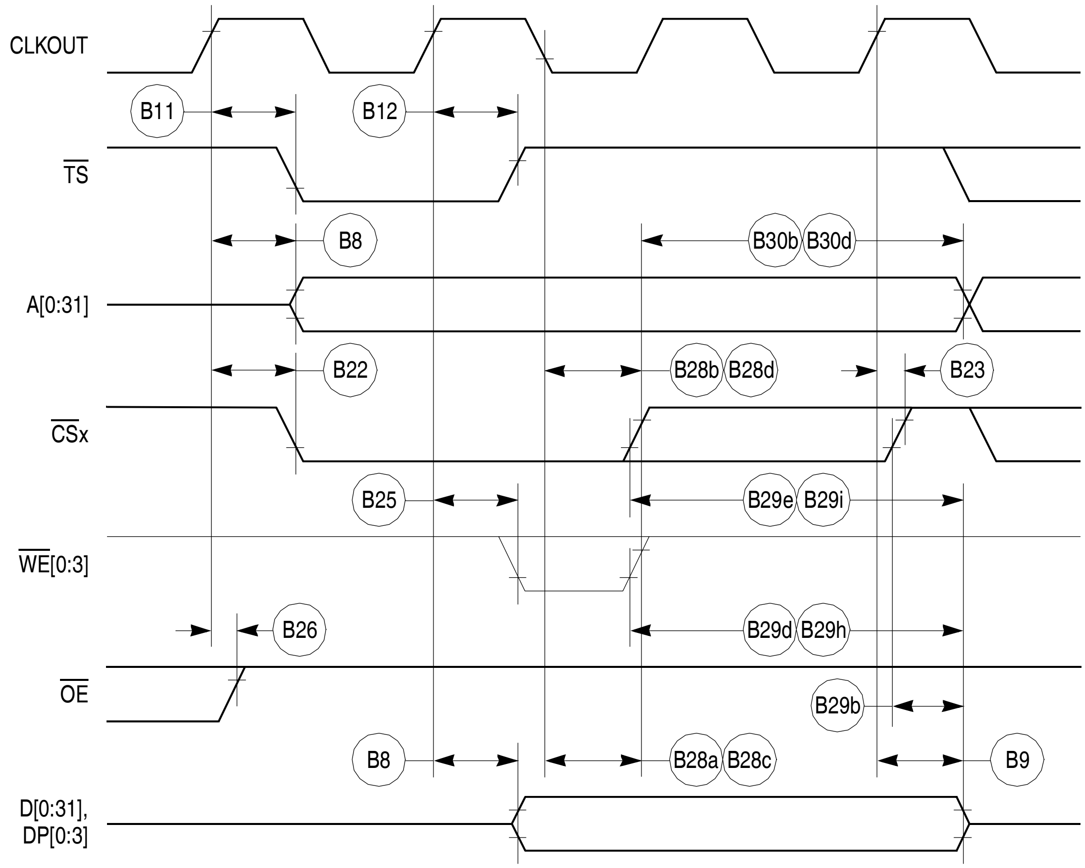


Figure 18. External Bus Write Timing (GPCM Controlled—TRLX = 1, CSNT = 1)

Figure 23 shows the timing for the asynchronous external master memory access controlled by the GPCM.

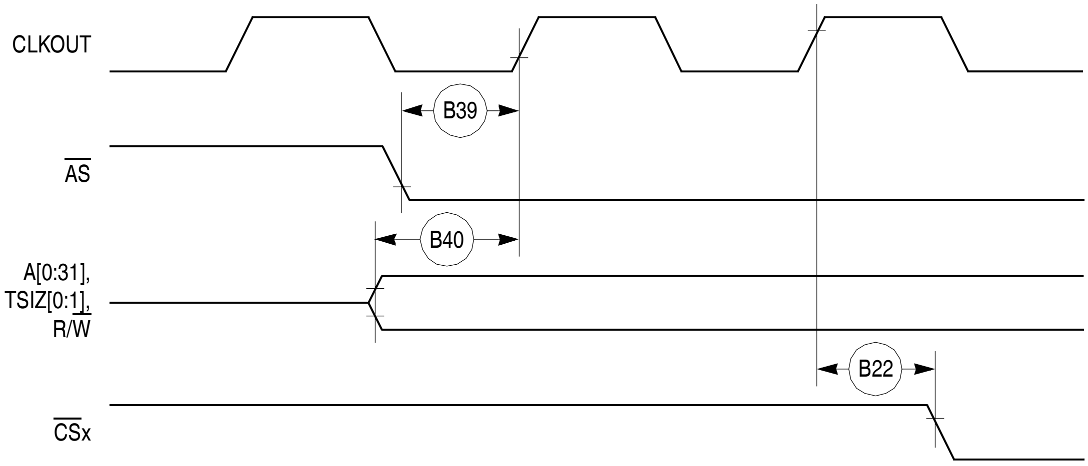


Figure 23. Asynchronous External Master Memory Access Timing (GPCM Controlled—ACS = 00)

Figure 24 shows the timing for the asynchronous external master control signals negation.

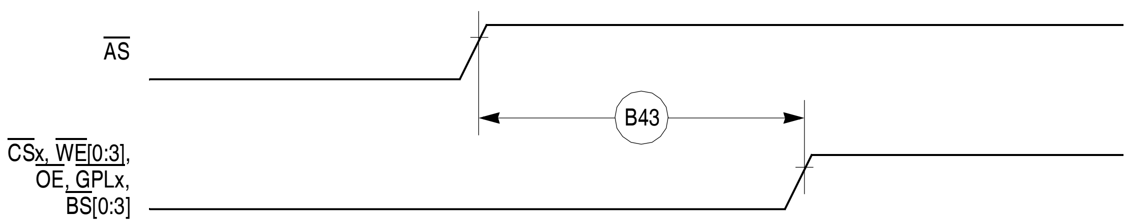


Figure 24. Asynchronous External Master—Control Signals Negation Timing

Table 10 shows the interrupt timing for the MPC866/859.

Table 10. Interrupt Timing

Num	Characteristic [1]	All Frequencies		Unit
		Min	Max	
I39	$\overline{IRQ}$x valid to CLKOUT rising edge (setup time)	6.00	—	ns
I40	$\overline{IRQ}$x hold time after CLKOUT	2.00	—	ns
I41	$\overline{IRQ}$x pulse width low	3.00	—	ns
I42	$\overline{IRQ}$x pulse width high	3.00	—	ns
I43	$\overline{IRQ}$x edge-to-edge time	$4xT_{CLOCKOUT}$	—	—

[1] The timings I39 and I40 describe the testing conditions under which the $\overline{IRQ}$ lines are tested when being defined as level sensitive. The $\overline{IRQ}$ lines are synchronized internally and do not have to be asserted or negated with reference to the CLKOUT.
The timings I41, I42, and I43 are specified to allow the correct function of the $\overline{IRQ}$ lines detection circuitry, and has no direct relation with the total system interrupt latency that the MPC866/859 is able to support.

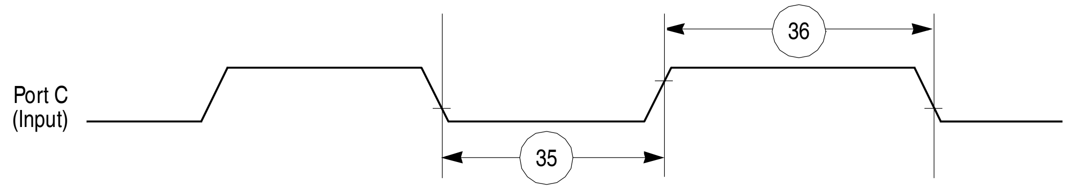


Figure 46. Port C Interrupt Detection Timing

12.3 IDMA Controller AC Electrical Specifications

Table 18 shows the IDMA controller timings as shown in Figure 47 through Figure 50.

Table 18. IDMA Controller Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
40	$\overline{\text{DREQ}}$ setup time to clock high	7	—	ns
41	$\overline{\text{DREQ}}$ hold time from clock high	3	—	ns
42	$\overline{\text{SDACK}}$ assertion delay from clock high	—	12	ns
43	$\overline{\text{SDACK}}$ negation delay from clock low	—	12	ns
44	$\overline{\text{SDACK}}$ negation delay from $\overline{\text{TA}}$ low	—	20	ns
45	$\overline{\text{SDACK}}$ negation delay from clock high	—	15	ns
46	$\overline{\text{TA}}$ assertion to falling edge of the clock setup time (applies to external $\overline{\text{TA}}$)	7	—	ns

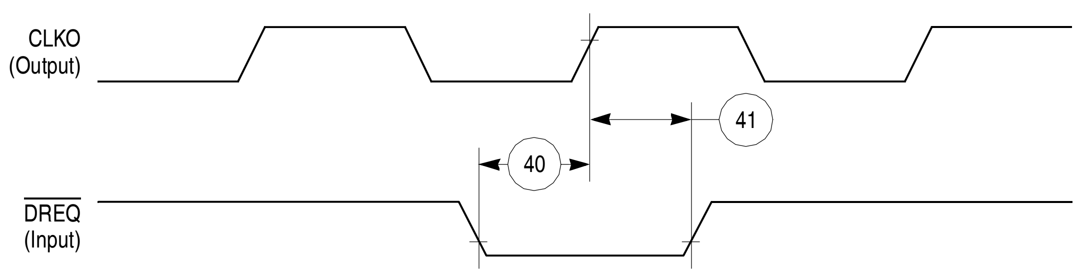


Figure 47. IDMA External Requests Timing Diagram

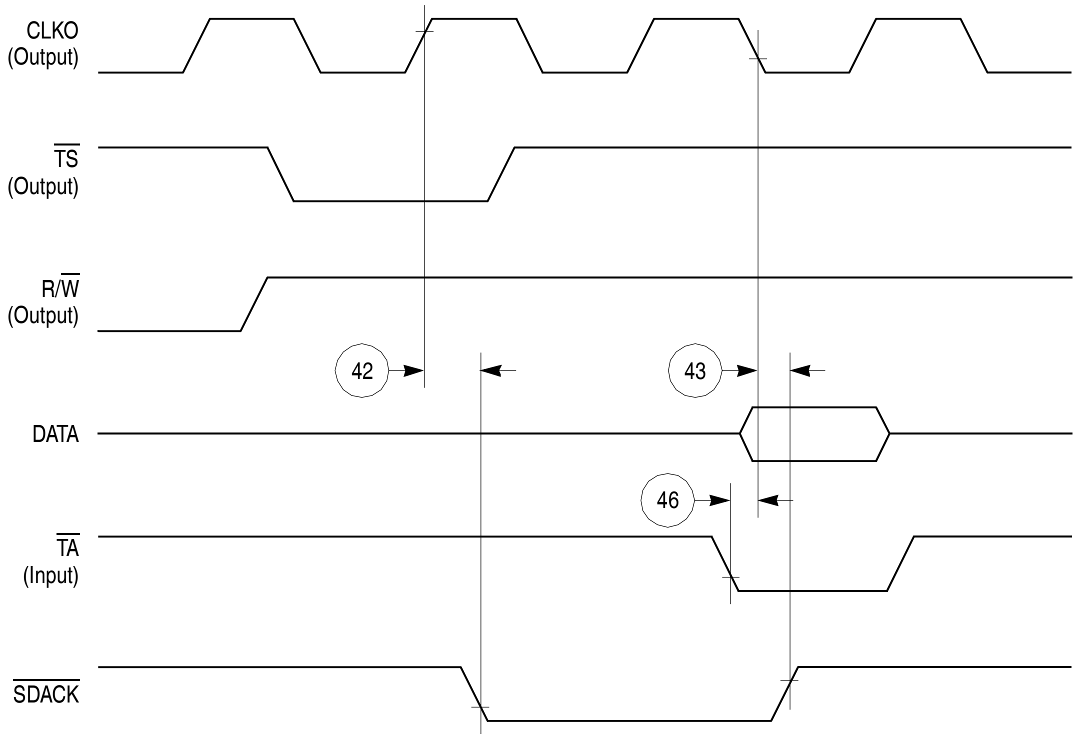


Figure 48. $\overline{\text{SDACK}}$ Timing Diagram—Peripheral Write, Externally-Generated $\overline{\text{TA}}$

Figure 49. $\overline{\text{SDACK}}$ Timing Diagram—Peripheral Write, Internally-Generated $\overline{\text{TA}}$

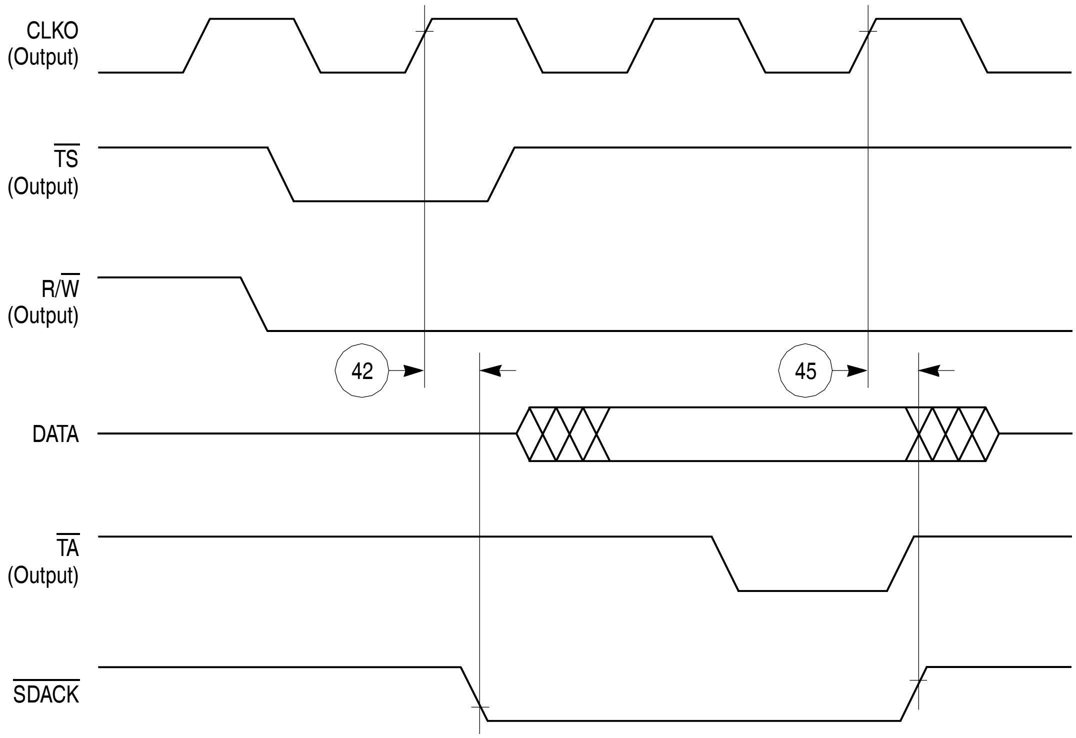


Figure 50. SDACK Timing Diagram—Peripheral Read, Internally-Generated TA

12.4 Baud Rate Generator AC Electrical Specifications

Table 19 shows the baud rate generator timings as shown in Figure 51.

Table 19. Baud Rate Generator Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
50	BRGO rise and fall time	—	10	ns
51	BRGO duty cycle	40	60	%
52	BRGO cycle	40	—	ns

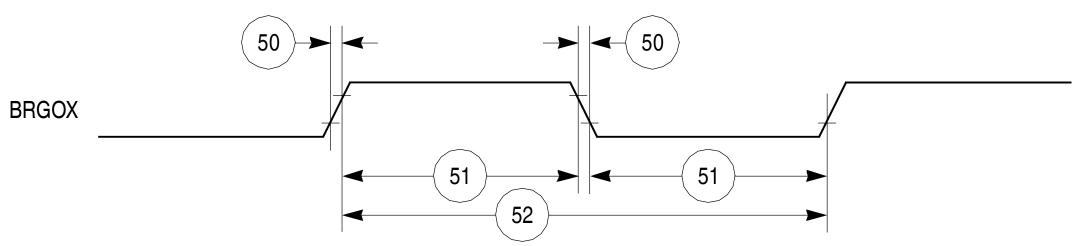


Figure 51. Baud Rate Generator Timing Diagram

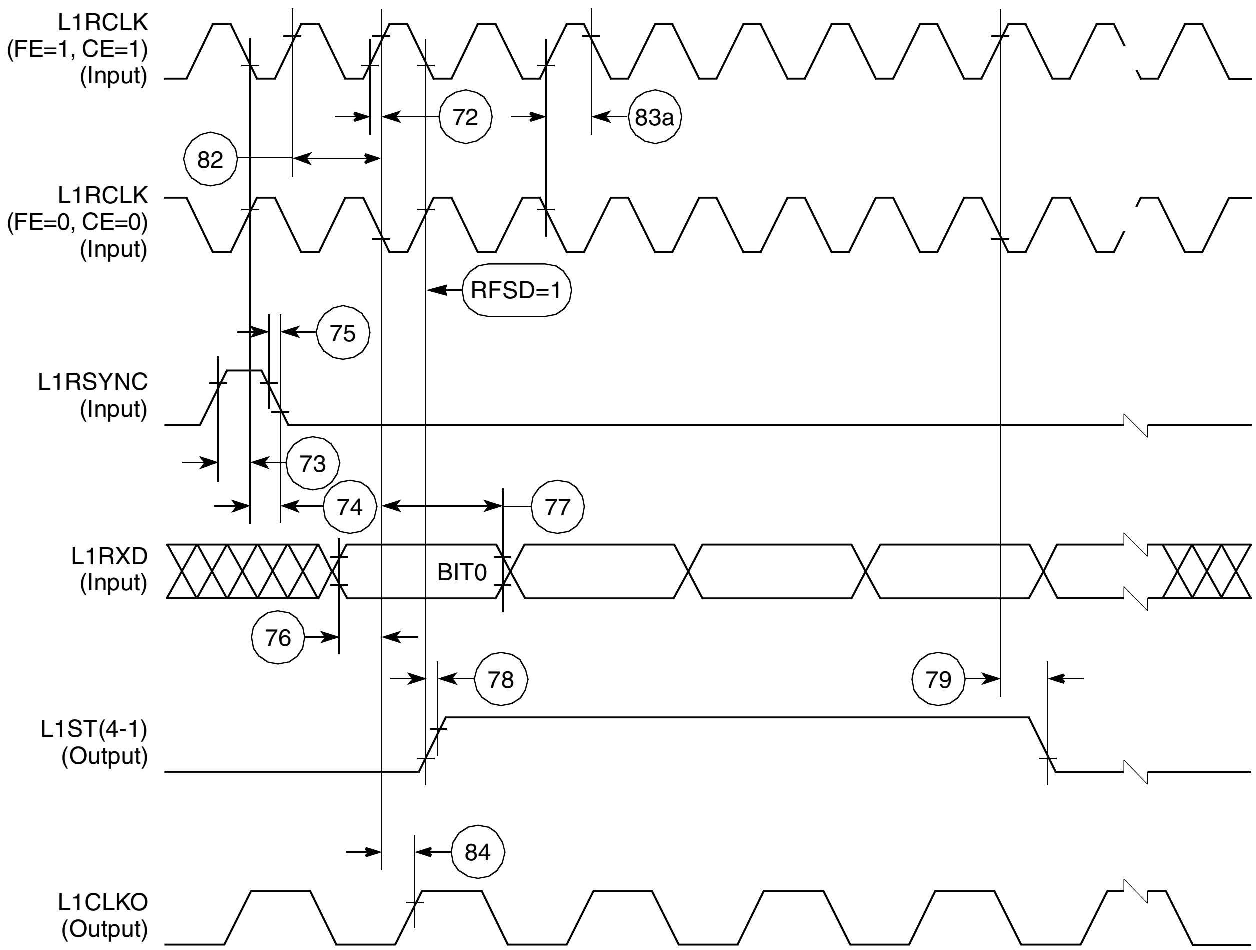
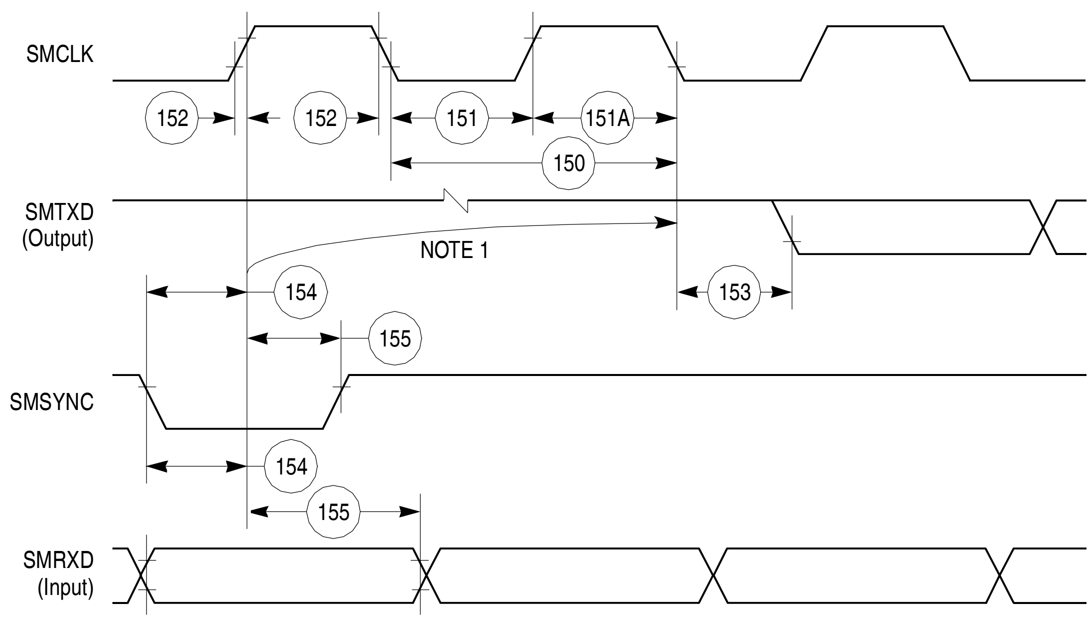


Figure 54. SI Receive Timing with Double-Speed Clocking (DSC = 1)

Table 25. SMC Transparent Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
150	SMCLK clock period [1]	100	—	ns
151	SMCLK width low	50	—	ns
151A	SMCLK width high	50	—	ns
152	SMCLK rise/fall time	—	15	ns
153	SMTXD active delay (from SMCLK falling edge)	10	50	ns
154	SMRXD/SMSYNC setup time	20	—	ns
155	RXD1/SMSYNC hold time	5	—	ns

[1] Sync CLK must be at least twice as fast as SMCLK.



NOTE:
1. This delay is equal to an integer number of character-length clocks.

Figure 66. SMC Transparent Timing Diagram

12.10SPI Master AC Electrical Specifications

Table 26 shows the SPI master timings as shown in Figure 67 and Figure 68.

Table 26. SPI Master Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
160	MASTER cycle time	4	1024	t_{cyc}
161	MASTER clock (SCK) high or low time	2	512	t_{cyc}
162	MASTER data setup time (inputs)	15	—	ns
163	Master data hold time (inputs)	0	—	ns
164	Master data valid (after SCK edge)	—	10	ns
165	Master data hold time (outputs)	0	—	ns
166	Rise time output	—	15	ns
167	Fall time output	—	15	ns

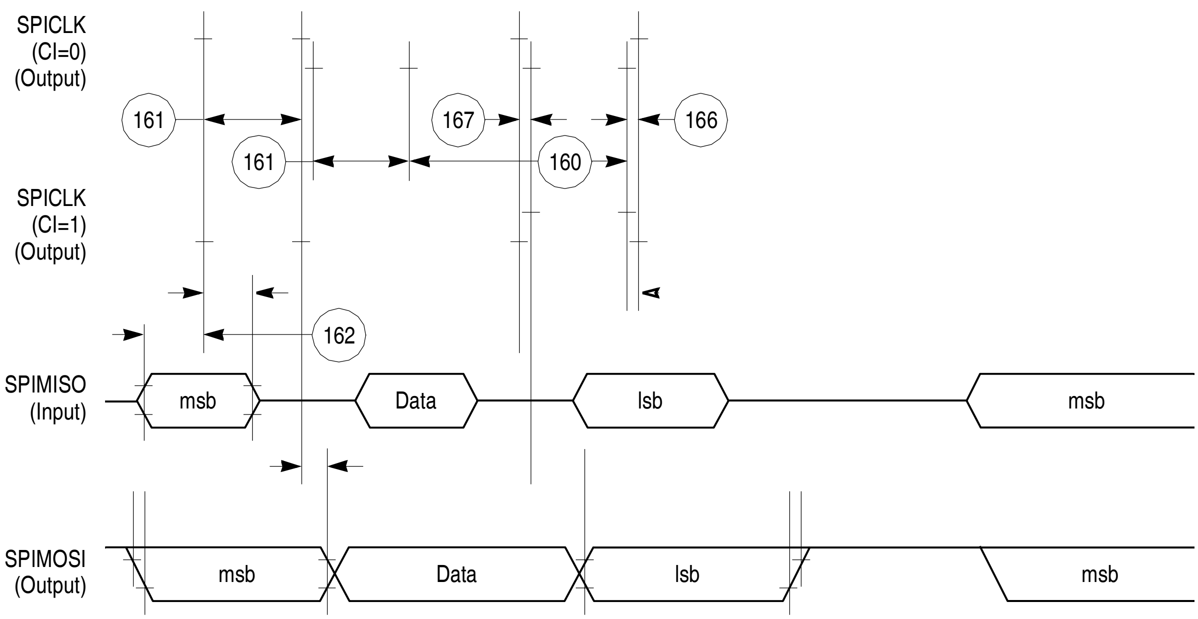


Figure 67. SPI Master (CP = 0) Timing Diagram

Table 39. Pin Assignments (continued)

Name	Pin Number	Type
PB16 $\overline{\text{L1RQa}}$ L1ST4 $\overline{\text{RTS4}}$ PHREQ0[1] RXADDR0[2]	N16	Bidirectional (Optional: Open-drain)
PB15 BRGO3 TxClav RxClav	R17	Bidirectional
PB14 RXADDR2[2] $\overline{\text{RSTRT1}}$	U18	Bidirectional
PC15 $\overline{\text{DREQ0}}$ $\overline{\text{RTS1}}$ L1ST1 RxClav TxClav	D16	Bidirectional
PC14 $\overline{\text{DREQ1}}$ $\overline{\text{RTS2}}$ L1ST2	D18	Bidirectional
PC13 $\overline{\text{L1RQb}}$ L1ST3 RTS3	E18	Bidirectional
PC12 $\overline{\text{L1RQa}}$ L1ST4 RTS4	F18	Bidirectional
PC11 $\overline{\text{CTS1}}$	J19	Bidirectional
PC10 $\overline{\text{CD1}}$ $\overline{\text{TGATE1}}$	K19	Bidirectional
PC9 $\overline{\text{CTS2}}$	L18	Bidirectional
PC8 $\overline{\text{CD2}}$ $\overline{\text{TGATE2}}$	M18	Bidirectional

Table 39. Pin Assignments (continued)

Name	Pin Number	Type
PC7 $\overline{\text{CTS3}}$ L1TSYNCB $\overline{\text{SDACK2}}$	M16	Bidirectional
PC6 $\overline{\text{CD3}}$ L1RSYNCB	R19	Bidirectional
PC5 $\overline{\text{CTS4}}$ L1TSYNCA SDACK1	T18	Bidirectional
PC4 $\overline{\text{CD4}}$ L1RSYNCA	T17	Bidirectional
PD15 L1TSYNCA MII-RXD3 UTPB0	U17	Bidirectional
PD14 L1RSYNCA MII-RXD2 UTPB1	V19	Bidirectional
PD13 L1TSYNCB MII-RXD1 UTPB2	V18	Bidirectional
PD12 L1RSYNCB MII-MDC UTPB3	R16	Bidirectional
PD11 RXD3 MII-TXERR $\overline{\text{RXENB}}$	T16	Bidirectional
PD10 TXD3 MII-RXD0 $\overline{\text{TXENB}}$	W18	Bidirectional

15.2 Mechanical Dimensions of the PBGA Package

For more information on the printed-circuit board layout of the PBGA package, including thermal via design and suggested pad layout, please refer to *Plastic Ball Grid Array Application Note* (order number: AN1231/D) available from your local Freescale sales office. Figure 79 shows the mechanical dimensions of the PBGA package.

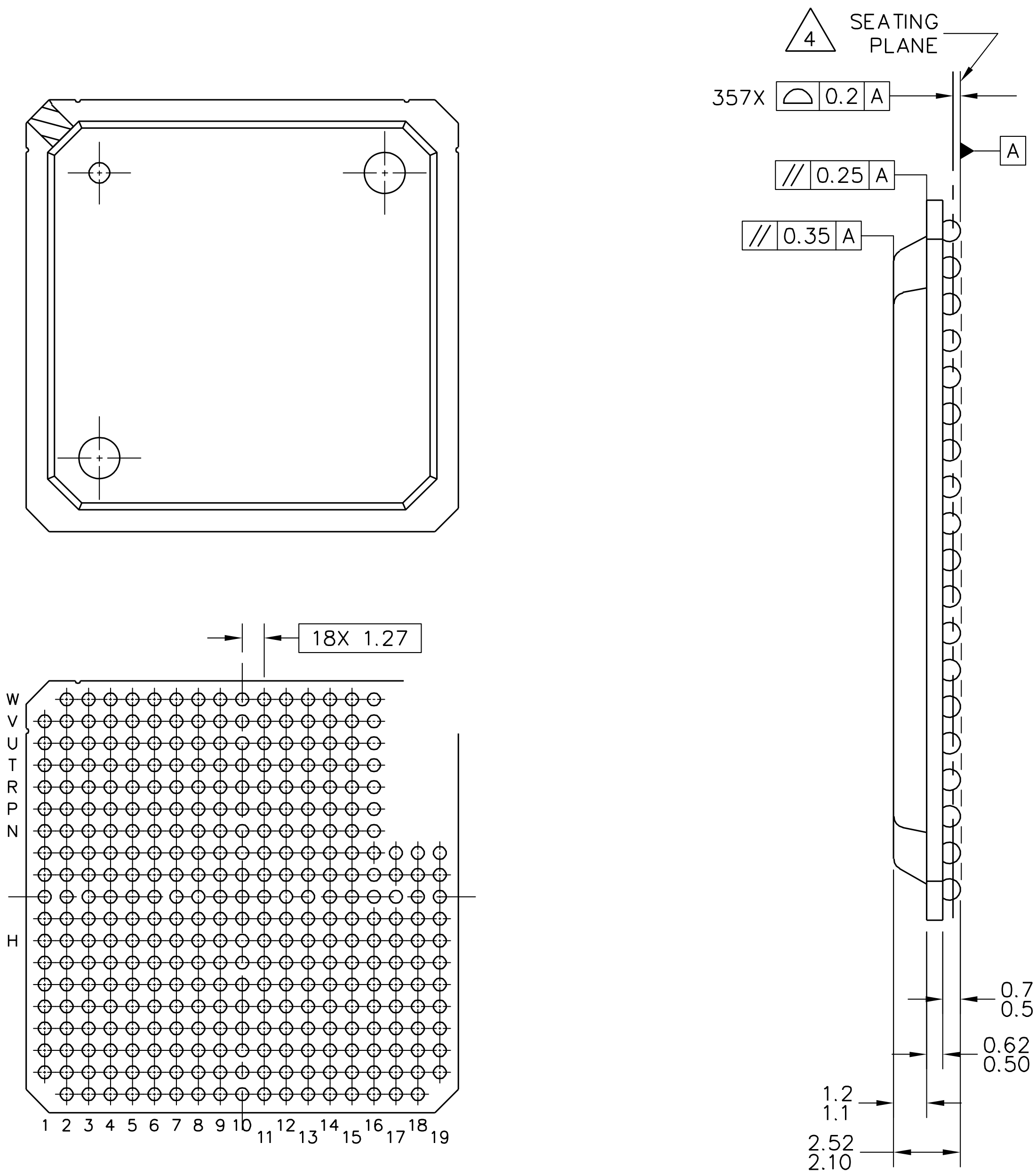


Figure 79. Mechanical Dimensions and Bottom Surface Nomenclature of the PBGA Package

16 Document Revision History

Table 40 lists significant changes between revisions of this document.

Table 40. Document Revision History

Revision Number	Date	Substantive Changes
0	5/2002	Initial revision
1	11/2002	Added the 5-V tolerant pins, new package dimensions, and other changes.
1.1	4/2003	Added the Spec. B1d and changed spec. B1a. Added the Note Solder sphere composition for MPC866XZP, MPC859DSLZP, and MPC859TZP is 62%Sn 36%Pb 2%Ag to Figure 15-79.
1.2	4/2003	Added the MPC859P.
1.3	5/2003	Changed the SPI Master Timing Specs. 162 and 164.
1.4	7-8/2003	• Added TxClav and RxClav to PB15 and PC15. Changed B28a through B28d and B29b to show that TRLX can be 0 or 1. • Added nontechnical reformatting.
1.5	3/14/2005	• Updated document template.
2	2/10/2006	• Updated orderable parts table.