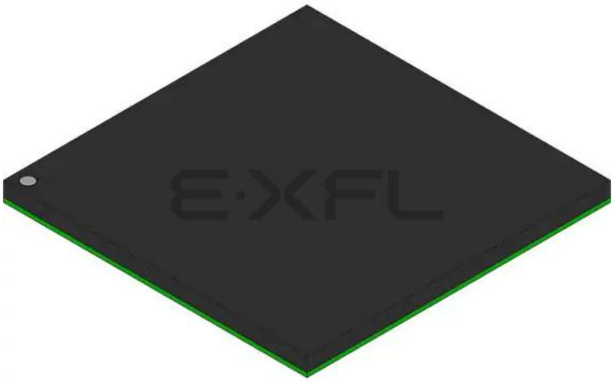
Freescale Semiconductor - MPC866TZP133A Datasheet



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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

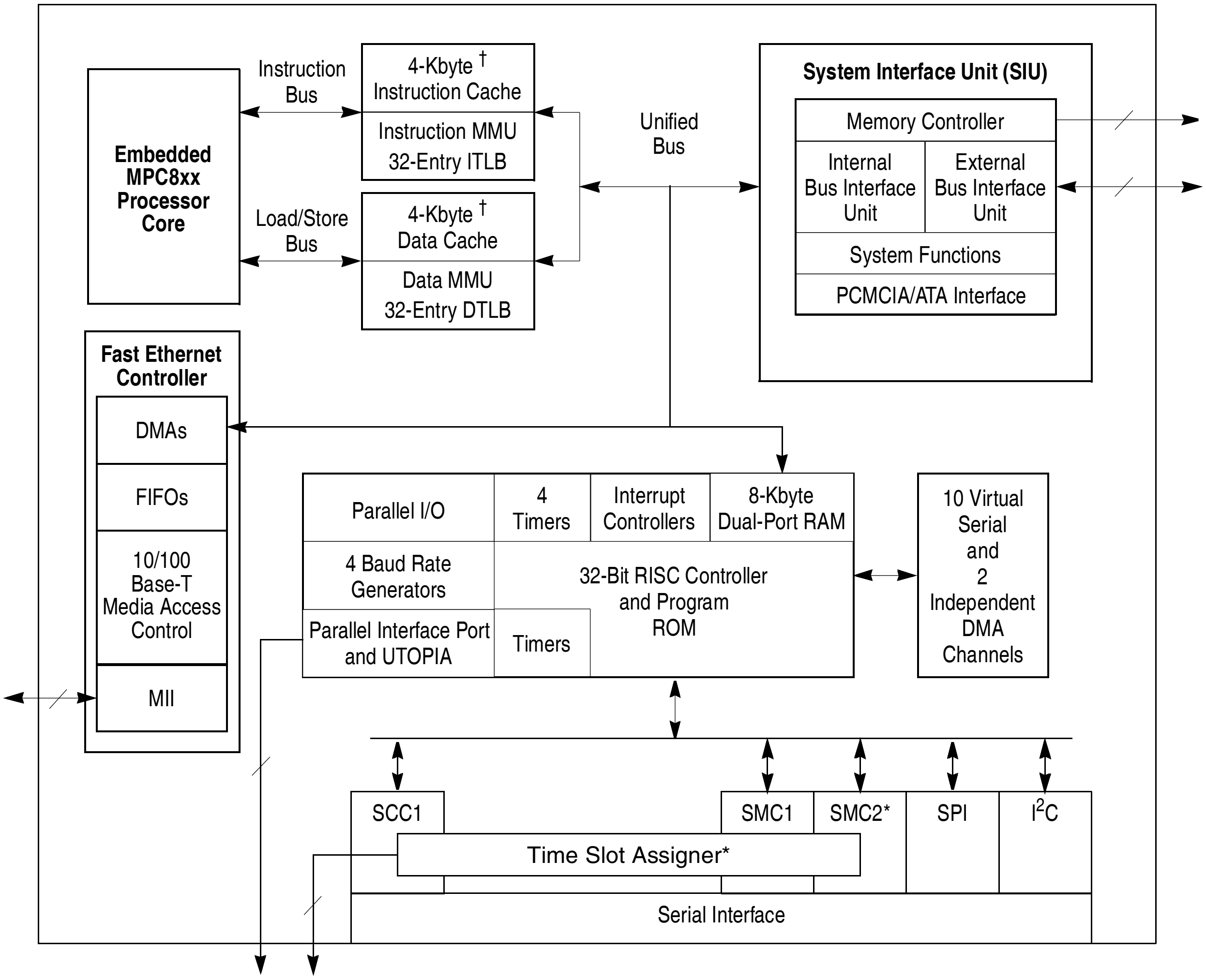
Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	MPC8xx
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	133MHz
Co-Processors/DSP	Communications; CPM
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10Mbps (4), 10/100Mbps (1)
SATA	-
USB	-
Voltage - I/O	3.3V
Operating Temperature	0°C ~ 95°C (TA)
Security Features	-
Package / Case	357-BBGA
Supplier Device Package	357-PBGA (25x25)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mpc866tzp133a

- Interrupts
  - Seven external interrupt request (IRQ) lines
  - Twelve port pins with interrupt capability
  - The MPC866P and MPC866T have 23 internal interrupt sources; the MPC859P, MPC859T, and MPC859DSL have 20 internal interrupt sources.
  - Programmable priority between SCCs (MPC866P and MPC866T)
  - Programmable highest priority request
- Communications processor module (CPM)
  - RISC controller
  - Communication-specific commands (for example, GRACEFUL STOP TRANSMIT, ENTER HUNT MODE, and RESTART TRANSMIT)
  - Supports continuous mode transmission and reception on all serial channels
  - Up to 8-Kbytes of dual-port RAM
  - MPC866P and MPC866T have 16 serial DMA (SDMA) channels; MPC859P, MPC859T, and MPC859DSL have 10 serial DMA (SDMA) channels.
  - Three parallel I/O registers with open-drain capability
- Four baud rate generators
  - Independent (can be connected to any SCC or SMC)
  - Allow changes during operation
  - Autobaud support option
- MPC866P and MPC866T have four SCCs (serial communication controller); MPC859P, MPC859T, and MPC859DSL have one SCC; and SCC1 on MPC859DSL supports Ethernet only.
  - Serial ATM capability on all SCCs
  - Optional UTOPIA port on SCC4
  - Ethernet/IEEE 802.3 optional on SCC1–4, supporting full 10-Mbps operation
  - HDLC/SDLC
  - HDLC bus (implements an HDLC-based local area network (LAN))
  - Asynchronous HDLC to support PPP (point-to-point protocol)
  - AppleTalk
  - Universal asynchronous receiver transmitter (UART)
  - Synchronous UART
  - Serial infrared (IrDA)
  - Binary synchronous communication (BISYNC)
  - Totally transparent (bit streams)
  - Totally transparent (frame based with optional cyclic redundancy check (CRC)
- Two SMCs (serial management channels) (MPC859DSL has one SMC (SMC1) for UART.)
  - UART
  - Transparent
  - General circuit interface (GCI) controller
  - Can be connected to the time-division multiplexed (TDM) channels

- One serial peripheral interface (SPI)
  - Supports master and slave modes
  - Supports multiple-master operation on the same bus
- One inter-integrated circuit (I^2C) port
  - Supports master and slave modes
  - Multiple-master environment support
- Time slot assigner (TSA) (MPC859DSL does not have TSA.)
  - Allows SCCs and SMCs to run in multiplexed and/or non-multiplexed operation
  - Supports T1, CEPT, PCM highway, ISDN basic rate, ISDN primary rate, user-defined
  - 1- or 8-bit resolution
  - Allows independent transmit and receive routing, frame synchronization, and clocking
  - Allows dynamic changes
  - On MPC866P and MPC866T, can be internally connected to six serial channels (four SCCs and two SMCs); on MPC859P and MPC859T, can be connected to three serial channels (one SCC and two SMCs).
- Parallel interface port (PIP)
  - Centronics interface support
  - Supports fast connection between compatible ports on MPC866/859 or MC68360
- PCMCIA interface
  - Master (socket) interface, compliant with PCI Local Bus Specification (Rev 2.1)
  - Supports one or two PCMCIA sockets whether ESAR functionality is enabled
  - Eight memory or I/O windows supported
- Debug interface
  - Eight comparators: four operate on instruction address, two operate on data address, and two operate on data.
  - Supports conditions: $= \neq < >$
  - Each watchpoint can generate a breakpoint internally
- Normal high and normal low power modes to conserve power
- 1.8 V core and 3.3 V I/O operation with 5-V TTL compatibility; refer to Table 6 for a listing of the 5-V tolerant pins.
- 357-pin plastic ball grid array (PBGA) package
- Operation up to 133 MHz



† The MPC859P has a 16-Kbyte instruction cache and a 8-Kbyte data cache.

* The MPC859DSL does not contain SMC2 nor the time slot assigner, and provides eight SDMA controllers.

Figure 2. MPC859P/859T/MPC859DSL Block Diagram

7.5 Experimental Determination

To determine the junction temperature of the device in the application after prototypes are available, the thermal characterization parameter (Ψ_{JT}) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D)$$

where:

Ψ_{JT} = thermal characterization parameter

T_T = thermocouple temperature on top of package

P_D = power dissipation in package

The thermal characterization parameter is measured per JESD51-2 specification published by JEDEC using a 40 gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

7.6 References

Semiconductor Equipment and Materials International(415) 964-5111
805 East Middlefield Rd.
Mountain View, CA 94043

MIL-SPEC and EIA/JESD (JEDEC) specifications800-854-7179 or
(Available from Global Engineering Documents)303-397-7956

JEDEC Specifications http://www.jedec.org

1. C.E. Triplett and B. Joiner, “An Experimental Characterization of a 272 PBGA Within an Automotive Engine Controller Module,” Proceedings of SemiTherm, San Diego, 1998, pp. 47-54.

2. B. Joiner and V. Adams, “Measurement and Simulation of Junction to Board Thermal Resistance and Its Application in Thermal Modeling,” Proceedings of SemiTherm, San Diego, 1999, pp. 212-220.

Table 9. Bus Operation Timings (continued)

Num	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
B12a	CLKOUT to $\overline{\text{TA}}$, $\overline{\text{BI}}$ negation (when driven by the memory controller or PCMCIA interface) (MAX = 0.00 x B1 + 9.00)	2.50	9.00	2.50	9.00	2.50	9.00	2.50	9.00	ns
B13	CLKOUT to $\overline{\text{TS}}$, $\overline{\text{BB}}$ High-Z (MIN = 0.25 x B1)	7.60	21.60	6.30	20.30	5.00	19.00	3.80	14.00	ns
B13a	CLKOUT to $\overline{\text{TA}}$, $\overline{\text{BI}}$ High-Z (when driven by the memory controller or PCMCIA interface) (MIN = 0.00 x B1 + 2.5)	2.50	15.00	2.50	15.00	2.50	15.00	2.50	15.00	ns
B14	CLKOUT to $\overline{\text{TEA}}$ assertion (MAX = 0.00 x B1 + 9.00)	2.50	9.00	2.50	9.00	2.50	9.00	2.50	9.00	ns
B15	CLKOUT to $\overline{\text{TEA}}$ High-Z (MIN = 0.00 x B1 + 2.50)	2.50	15.00	2.50	15.00	2.50	15.00	2.50	15.00	ns
B16	$\overline{\text{TA}}$, $\overline{\text{BI}}$ valid to CLKOUT (setup time) (MIN = 0.00 x B1 + 6.00)	6.00	—	6.00	—	6.00	—	6.00	—	ns
B16a	$\overline{\text{TEA}}$, $\overline{\text{KR}}$, $\overline{\text{RETRY}}$, $\overline{\text{CR}}$ valid to CLKOUT (setup time) (MIN = 0.00 x B1 + 4.5)	4.50	—	4.50	—	4.50	—	4.50	—	ns
B16b	$\overline{\text{BB}}$, $\overline{\text{BG}}$, $\overline{\text{BR}}$, valid to CLKOUT (setup time) [2] (4 MIN = 0.00 x B1 + 0.00)	4.00	—	4.00	—	4.00	—	4.00	—	ns
B17	CLKOUT to $\overline{\text{TA}}$, $\overline{\text{TEA}}$, $\overline{\text{BI}}$, $\overline{\text{BB}}$, $\overline{\text{BG}}$, $\overline{\text{BR}}$ valid (hold time) (MIN = 0.00 x B1 + 1.00 [3])	1.00	—	1.00	—	1.00	—	2.00	—	ns
B17a	CLKOUT to $\overline{\text{KR}}$, $\overline{\text{RETRY}}$, $\overline{\text{CR}}$ valid (hold time) (MIN = 0.00 x B1 + 2.00)	2.00	—	2.00	—	2.00	—	2.00	—	ns
B18	D(0:31), DP(0:3) valid to CLKOUT rising edge (setup time) [4] (MIN = 0.00 x B1 + 6.00)	6.00	—	6.00	—	6.00	—	6.00	—	ns
B19	CLKOUT rising edge to D(0:31), DP(0:3) valid (hold time) [4] (MIN = 0.00 x B1 + 1.00 [5])	1.00	—	1.00	—	1.00	—	2.00	—	ns
B20	D(0:31), DP(0:3) valid to CLKOUT falling edge (setup time) [6](MIN = 0.00 x B1 + 4.00)	4.00	—	4.00	—	4.00	—	4.00	—	ns
B21	CLKOUT falling edge to D(0:31), DP(0:3) valid (hold Time) [6] (MIN = 0.00 x B1 + 2.00)	2.00	—	2.00	—	2.00	—	2.00	—	ns
B22	CLKOUT rising edge to $\overline{\text{CS}}$ asserted GPCM ACS = 00 (MAX = 0.25 x B1 + 6.3)	7.60	13.80	6.30	12.50	5.00	11.30	3.80	10.00	ns
B22a	CLKOUT falling edge to $\overline{\text{CS}}$ asserted GPCM ACS = 10, TRLX = 0 (MAX = 0.00 x B1 + 8.00)	—	8.00	—	8.00	—	8.00	—	8.00	ns

Table 9. Bus Operation Timings (continued)

Num	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
B31d	CLKOUT falling edge to $\overline{\text{CS}}$ valid, as requested by control bit CST1 in the corresponding word in the UPM EBDF = 1 (MAX = 0.375 x B1 + 6.6)	13.30	18.00	11.30	16.00	9.40	14.10	7.60	12.30	ns
B32	CLKOUT falling edge to $\overline{\text{BS}}$ valid, as requested by control bit BST4 in the corresponding word in the UPM (MAX = 0.00 x B1 + 6.00)	1.50	6.00	1.50	6.00	1.50	6.00	1.50	6.00	ns
B32a	CLKOUT falling edge to $\overline{\text{BS}}$ valid, as requested by control bit BST1 in the corresponding word in the UPM, EBDF = 0 (MAX = 0.25 x B1 + 6.80)	7.60	14.30	6.30	13.00	5.00	11.80	3.80	10.50	ns
B32b	CLKOUT rising edge to $\overline{\text{BS}}$ valid, as requested by control bit BST2 in the corresponding word in the UPM (MAX = 0.00 x B1 + 8.00)	1.50	8.00	1.50	8.00	1.50	8.00	1.50	8.00	ns
B32c	CLKOUT rising edge to $\overline{\text{BS}}$ valid, as requested by control bit BST3 in the corresponding word in the UPM (MAX = 0.25 x B1 + 6.80)	7.60	14.30	6.30	13.00	5.00	11.80	3.80	10.50	ns
B32d	CLKOUT falling edge to $\overline{\text{BS}}$ valid- as requested by control bit BST1 in the corresponding word in the UPM, EBDF = 1 (MAX = 0.375 x B1 + 6.60)	13.30	18.00	11.30	16.00	9.40	14.10	7.60	12.30	ns
B33	CLKOUT falling edge to $\overline{\text{GPL}}$ valid, as requested by control bit GxT4 in the corresponding word in the UPM (MAX = 0.00 x B1 + 6.00)	1.50	6.00	1.50	6.00	1.50	6.00	1.50	6.00	ns
B33a	CLKOUT rising edge to $\overline{\text{GPL}}$ valid, as requested by control bit GxT3 in the corresponding word in the UPM (MAX = 0.25 x B1 + 6.80)	7.60	14.30	6.30	13.00	5.00	11.80	3.80	10.50	ns
B34	A(0:31), BADDR(28:30), and D(0:31) to $\overline{\text{CS}}$ valid, as requested by control bit CST4 in the corresponding word in the UPM (MIN = 0.25 x B1 - 2.00)	5.60	—	4.30	—	3.00	—	1.80	—	ns
B34a	A(0:31), BADDR(28:30), and D(0:31) to $\overline{\text{CS}}$ valid, as requested by control bit CST1 in the corresponding word in the UPM (MIN = 0.50 x B1 – 2.00)	13.20	—	10.50	—	8.00	—	5.60	—	ns
B34b	A(0:31), BADDR(28:30), and D(0:31) to $\overline{\text{CS}}$ valid, as requested by CST2 in the corresponding word in UPM (MIN = 0.75 x B1 – 2.00)	20.70	—	16.70	—	13.00	—	9.40	—	ns

Figure 6 shows the timing for the external clock.

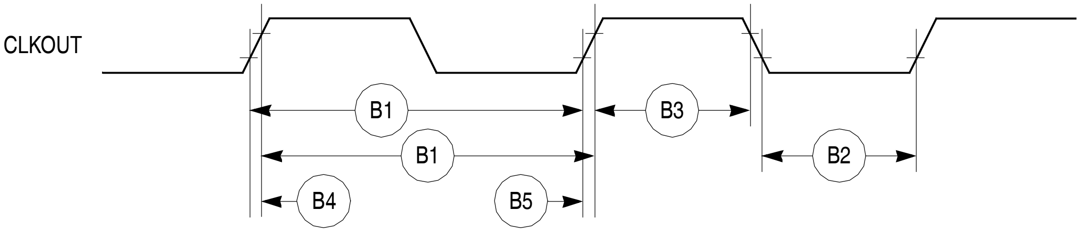


Figure 6. External Clock Timing

Figure 7 shows the timing for the synchronous output signals.

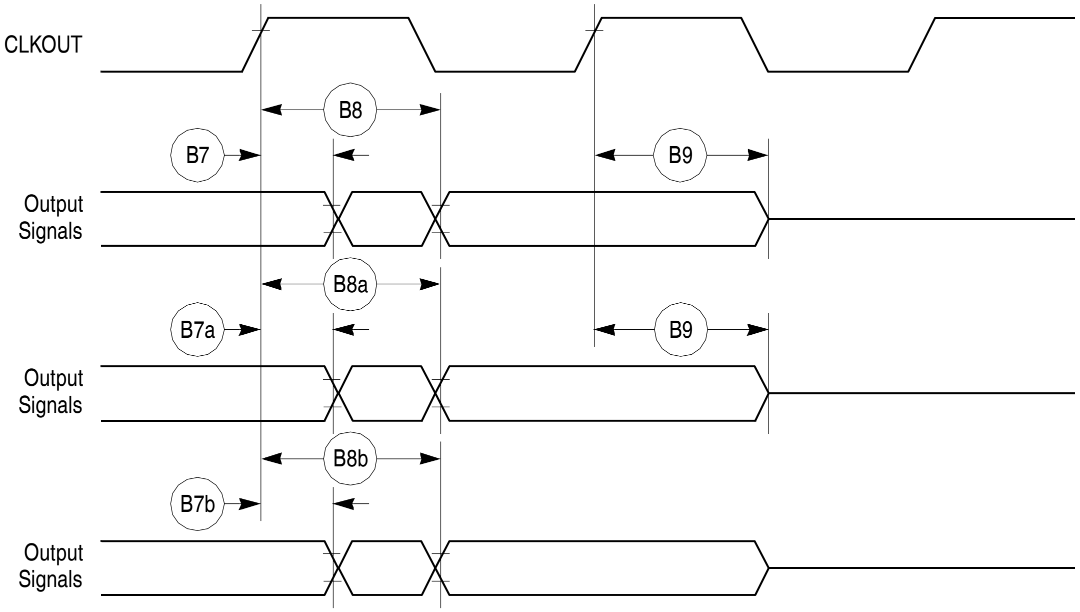


Figure 7. Synchronous Output Signals Timing

Figure 23 shows the timing for the asynchronous external master memory access controlled by the GPCM.

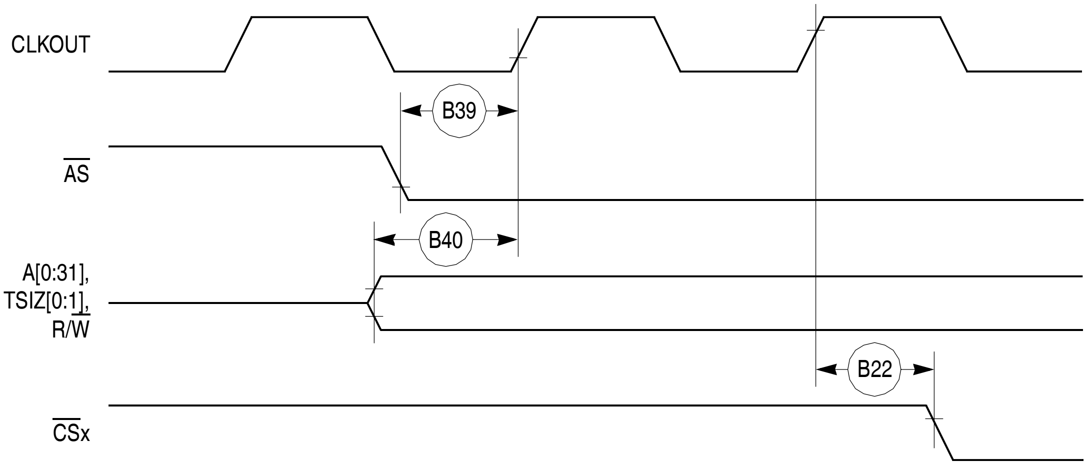


Figure 23. Asynchronous External Master Memory Access Timing (GPCM Controlled—ACS = 00)

Figure 24 shows the timing for the asynchronous external master control signals negation.

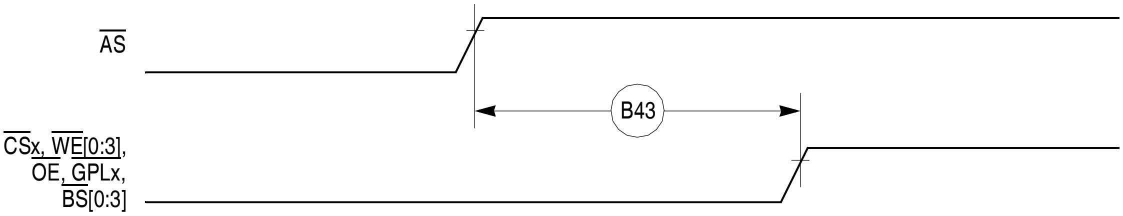


Figure 24. Asynchronous External Master—Control Signals Negation Timing

Table 10 shows the interrupt timing for the MPC866/859.

Table 10. Interrupt Timing

Num	Characteristic [1]	All Frequencies		Unit
		Min	Max	
I39	IRQx valid to CLKOUT rising edge (setup time)	6.00	—	ns
I40	IRQx hold time after CLKOUT	2.00	—	ns
I41	IRQx pulse width low	3.00	—	ns
I42	IRQx pulse width high	3.00	—	ns
I43	IRQx edge-to-edge time	4xT$_{CLOCKOUT}$	—	—

[1] The timings I39 and I40 describe the testing conditions under which the IRQ lines are tested when being defined as level sensitive. The IRQ lines are synchronized internally and do not have to be asserted or negated with reference to the CLKOUT.
The timings I41, I42, and I43 are specified to allow the correct function of the IRQ lines detection circuitry, and has no direct relation with the total system interrupt latency that the MPC866/859 is able to support.

Table 11. PCMCIA Timing (continued)

Num	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
P50	CLKOUT to $\overline{\text{PCOE}}$, $\overline{\text{IORD}}$, $\overline{\text{PCWE}}$, $\overline{\text{IOWR}}$ assert time (MAX = 0.00 x B1 + 11.00)	—	11.00	—	11.00	—	11.00	—	11.00	ns
P51	CLKOUT to $\overline{\text{PCOE}}$, $\overline{\text{IORD}}$, $\overline{\text{PCWE}}$, $\overline{\text{IOWR}}$ negate time (MAX = 0.00 x B1 + 11.00)	2.00	11.00	2.00	11.00	2.00	11.00	2.00	11.00	ns
P52	CLKOUT to ALE assert time (MAX = 0.25 x B1 + 6.30)	7.60	13.80	6.30	12.50	5.00	11.30	3.80	10.00	ns
P53	CLKOUT to ALE negate time (MAX = 0.25 x B1 + 8.00)	—	15.60	—	14.30	—	13.00	—	11.80	ns
P54	$\overline{\text{PCWE}}$, $\overline{\text{IOWR}}$ negated to D(0:31) invalid[1] (MIN = 0.25 x B1 – 2.00)	5.60	—	4.30	—	3.00	—	1.80	—	ns
P55	$\overline{\text{WAITA}}$ and $\overline{\text{WAITB}}$ valid to CLKOUT rising edge[1] (MIN = 0.00 x B1 + 8.00)	8.00	—	8.00	—	8.00	—	8.00	—	ns
P56	CLKOUT rising edge to $\overline{\text{WAITA}}$ and $\overline{\text{WAITB}}$ invalid[1] (MIN = 0.00 x B1 + 2.00)	2.00	—	2.00	—	2.00	—	2.00	—	ns

---

[1] PSST = 1. Otherwise, add PSST times cycle time.
PSHT = 0. Otherwise, add PSHT times cycle time.
These synchronous timings define when the $\overline{\text{WAITx}}$ signals are detected in order to freeze (or relieve) the PCMCIA current cycle. The $\overline{\text{WAITx}}$ assertion will be effective only if it is detected 2 cycles before the PSL timer expiration. See PCMCIA Interface in the *MPC866 PowerQUICC User's Manual*.

Figure 27 shows the PCMCIA access cycle timing for the external bus read.

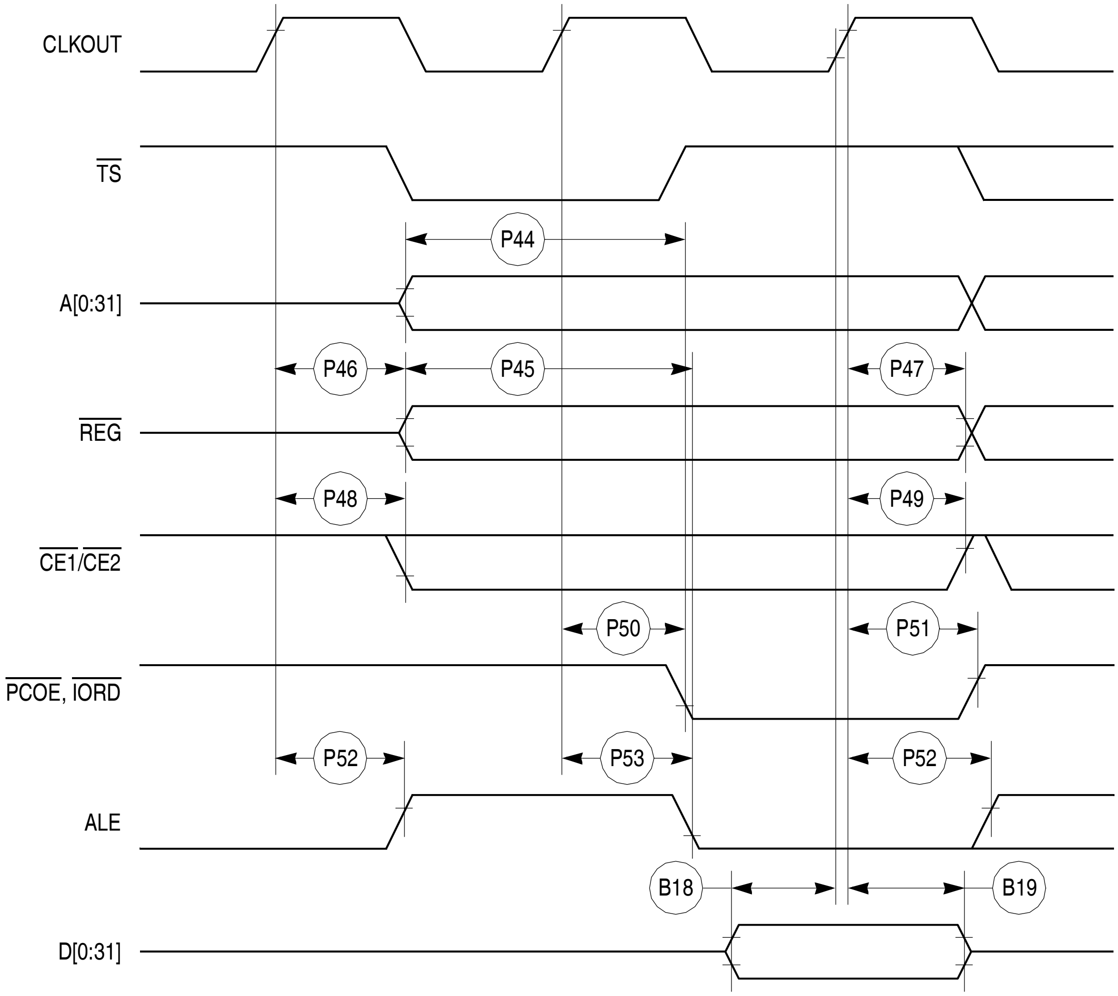


Figure 27. PCMCIA Access Cycles Timing External Bus Read

Figure 34 shows the reset timing for the data bus configuration.

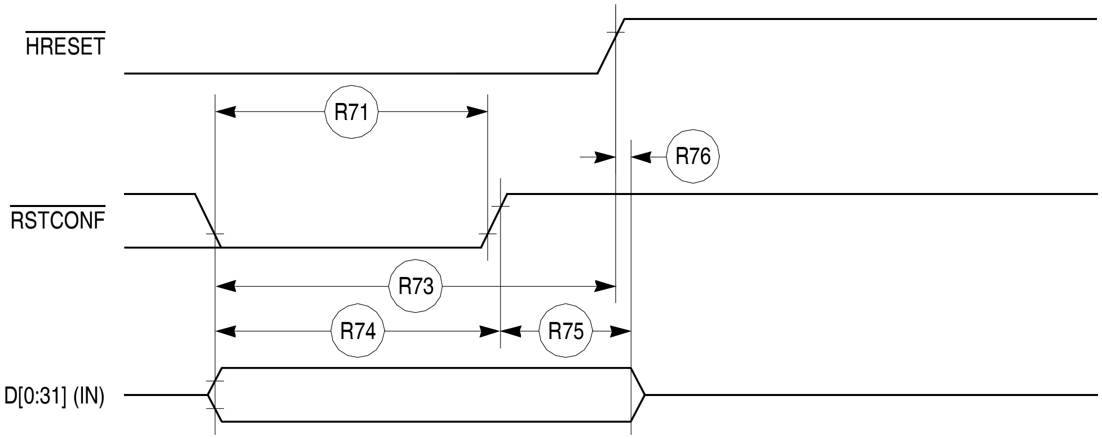


Figure 34. Reset Timing—Configuration from Data Bus

Figure 35 shows the reset timing for the data bus weak drive during configuration.

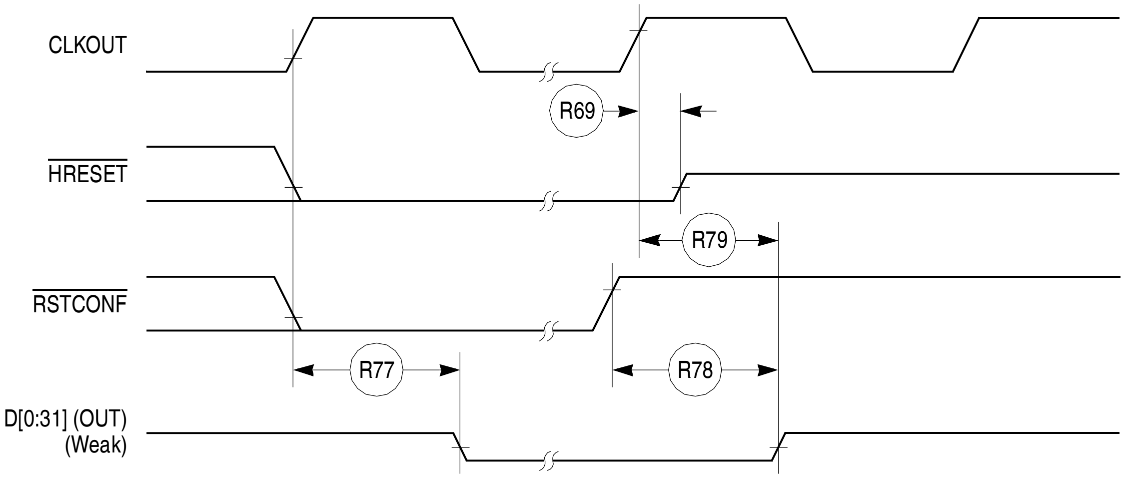


Figure 35. Reset Timing—Data Bus Weak Drive During Configuration

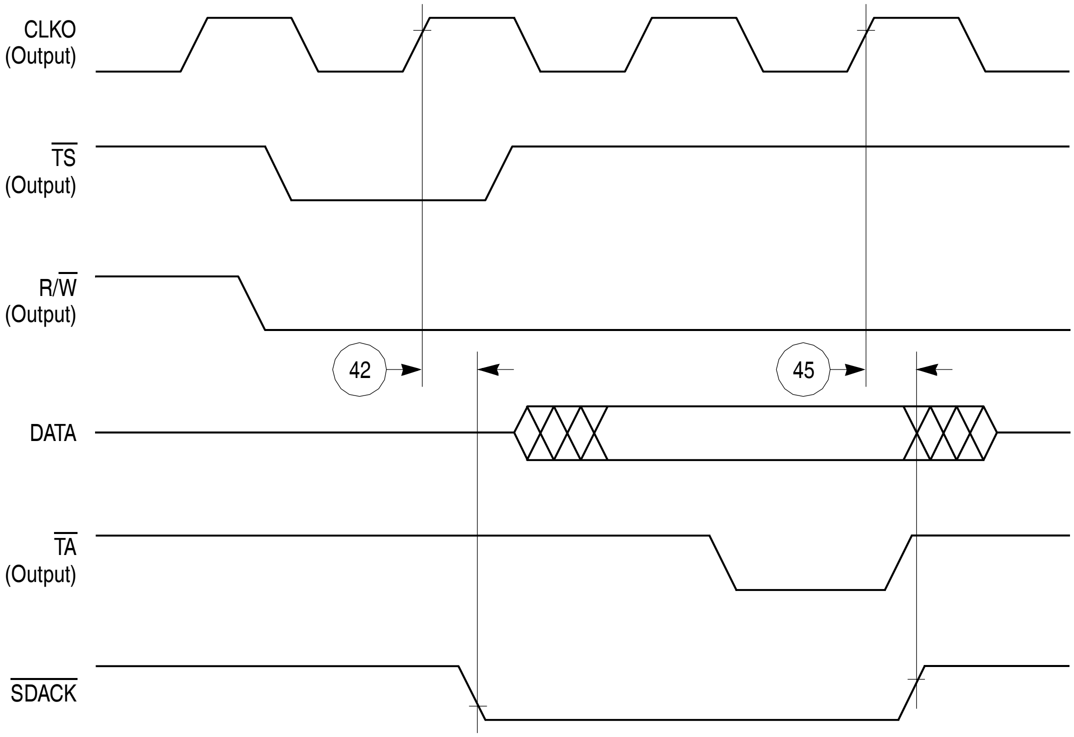


Figure 50. SDACK Timing Diagram—Peripheral Read, Internally-Generated TA

12.4 Baud Rate Generator AC Electrical Specifications

Table 19 shows the baud rate generator timings as shown in Figure 51.

Table 19. Baud Rate Generator Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
50	BRGO rise and fall time	—	10	ns
51	BRGO duty cycle	40	60	%
52	BRGO cycle	40	—	ns

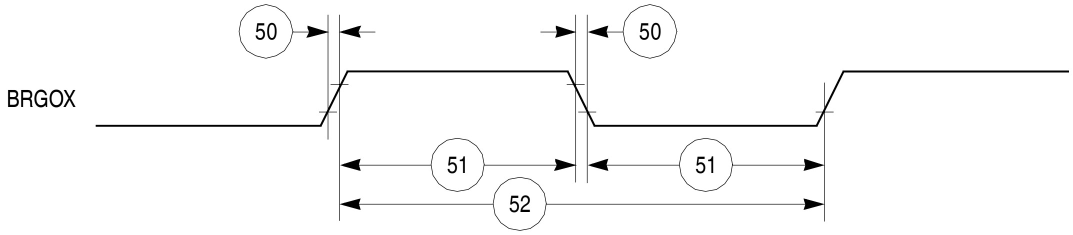


Figure 51. Baud Rate Generator Timing Diagram

Table 21. SI Timing (continued)

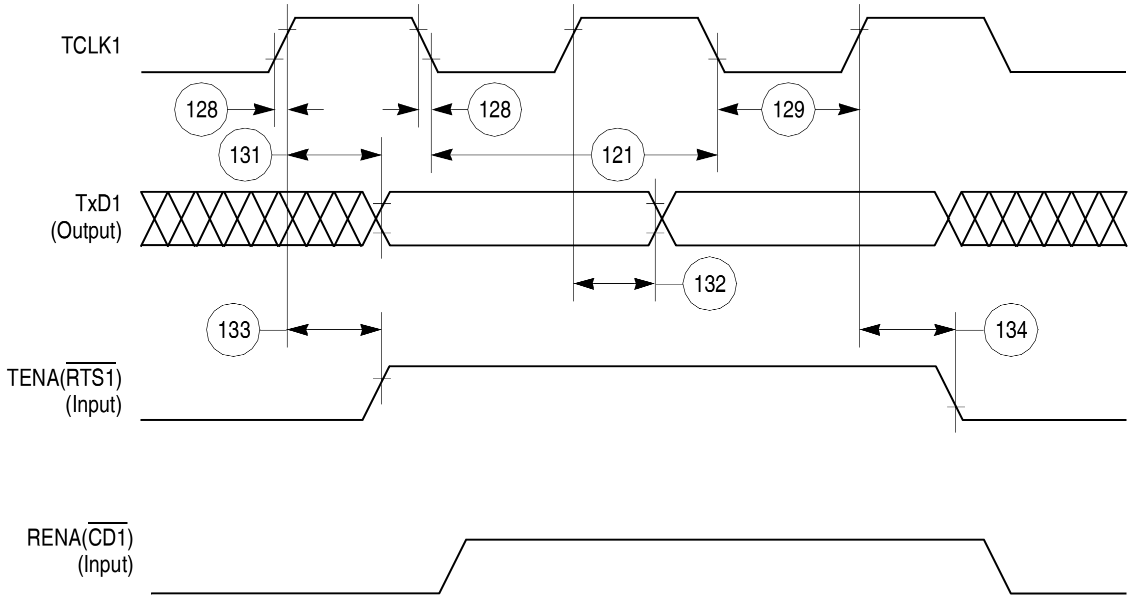
Num	Characteristic	All Frequencies		Unit
		Min	Max	
74	L1CLK edge to L1RSYNC, L1TSYNC, invalid (SYNC hold time)	35.00	—	ns
75	L1RSYNC, L1TSYNC rise/fall time	—	15.00	ns
76	L1RXD valid to L1CLK edge (L1RXD setup time)	17.00	—	ns
77	L1CLK edge to L1RXD invalid (L1RXD hold time)	13.00	—	ns
78	L1CLK edge to L1ST(1–4) valid [4]	10.00	45.00	ns
78A	L1SYNC valid to L1ST(1–4) valid	10.00	45.00	ns
79	L1CLK edge to L1ST(1–4) invalid	10.00	45.00	ns
80	L1CLK edge to L1TXD valid	10.00	55.00	ns
80A	L1TSYNC valid to L1TXD valid [4]	10.00	55.00	ns
81	L1CLK edge to L1TXD high impedance	0.00	42.00	ns
82	L1RCLK, L1TCLK frequency (DSC =1)	—	16.00 or SYNCCLK/2	MHz
83	L1RCLK, L1TCLK width low (DSC =1)	P + 10	—	ns
83a	L1RCLK, L1TCLK width high (DSC = 1)[3]	P + 10	—	ns
84	L1CLK edge to L1CLKO valid (DSC = 1)	—	30.00	ns
85	$\overline{\text{L1RQ}}$ valid before falling edge of L1TSYNC[4]	1.00	—	L1TCLK
86	L1GR setup time[2]	42.00	—	ns
87	L1GR hold time	42.00	—	ns
88	L1CLK edge to L1SYNC valid (FSD = 00) CNT = 0000, BYT = 0, DSC = 0)	—	0.00	ns

[1] The ratio SyncCLK/L1RCLK must be greater than 2.5/1.

[2] These specs are valid for IDL mode only.

[3] Where P = 1/CLKOUT. Thus, for a 25-MHz CLKO1 rate, P = 40 ns.

[4] These strobes and TxD on the first bit of the frame become valid after L1CLK edge or L1SYNC, whichever is later.



Notes:

1. Transmit clock invert (TCI) bit in GSMR is set.
2. If RENA is deasserted before TENA, or RENA is not asserted at all during transmit, then the CSL bit is set in the buffer descriptor at the end of the frame transmission.

Figure 63. Ethernet Transmit Timing Diagram

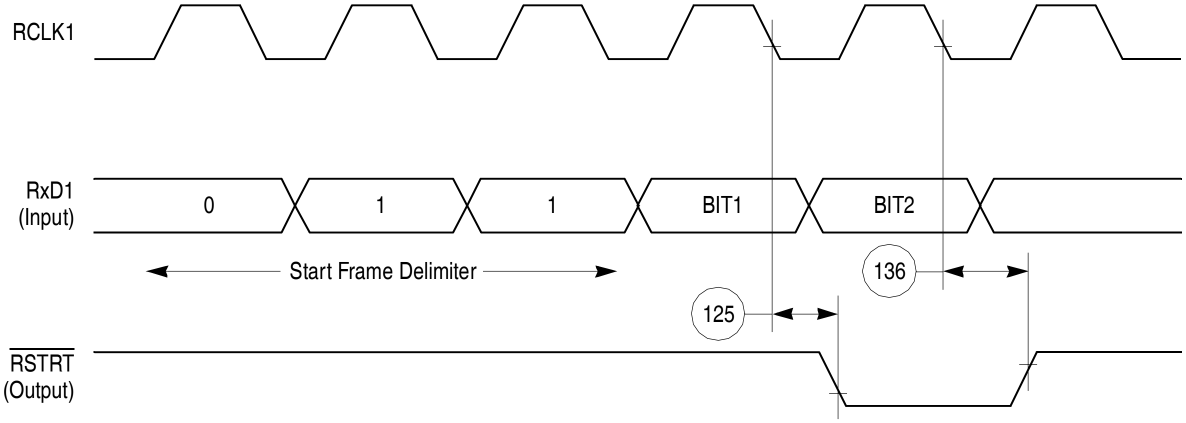


Figure 64. CAM Interface Receive Start Timing Diagram

Figure 65. CAM Interface REJECT Timing Diagram

12.9 SMC Transparent AC Electrical Specifications

Table 25 shows the SMC transparent timings as shown in Figure 66.

Table 32. UTOPIA Slave (Split Bus Mode) Electrical Specifications

Num	Signal Characteristic	Direction	Min	Max	Unit
U1	UtpClk rise/fall time (external clock option)	Input	—	4	ns
	Duty cycle		40	60	%
	Frequency		—	33	MHz
U2	UTPB, SOC, Rxclav and Txclav active delay	Output	2	16	ns
U3	UTPB_AUX, SOC_Aux, $\overline{\text{RxEnb}}$, $\overline{\text{TxEnb}}$, RxAddr, and TxAddr setup time	Input	4	—	ns
U4	UTPB_AUX, SOC_Aux, $\overline{\text{RxEnb}}$, $\overline{\text{TxEnb}}$, RxAddr, and TxAddr hold time	Input	1	—	ns

Figure 72 shows signal timings during UTOPIA receive operations.

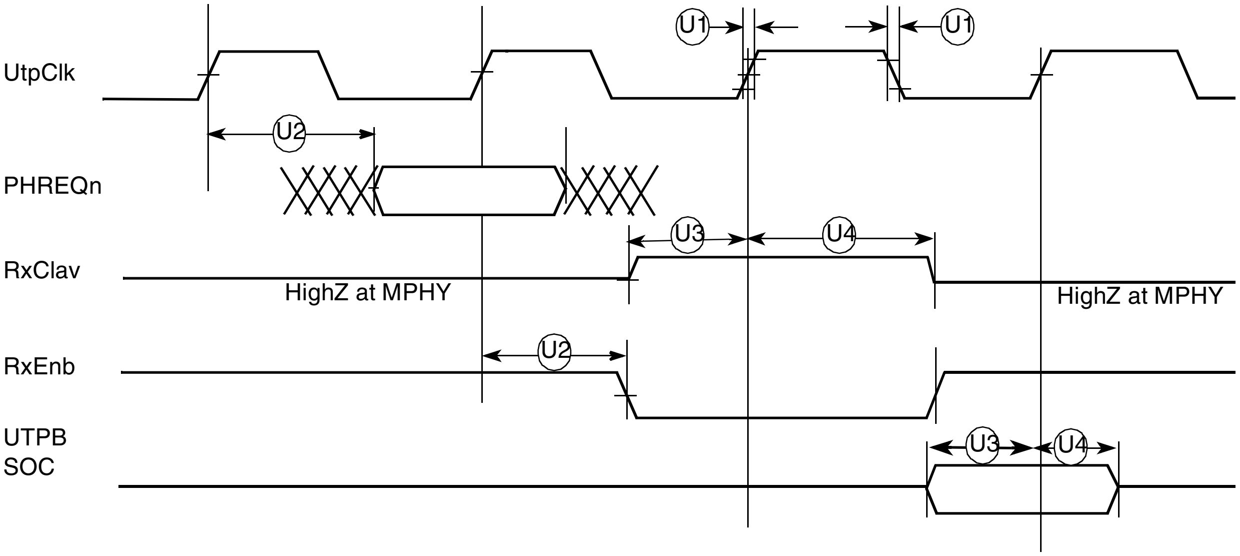


Figure 72. UTOPIA Receive Timing

Table 39. Pin Assignments (continued)

Name	Pin Number	Type
PA5 CLK3 L1TCLKA BRGO2 TIN2	N18	Bidirectional
PA4 CLK4 $\overline{\text{TOUT2}}$	P19	Bidirectional
PA3 CLK5 BRGO3 TIN3	P17	Bidirectional
PA2 CLK6 $\overline{\text{TOUT3}}$ L1RCLKB	R18	Bidirectional
PA1 CLK7 BRGO4 TIN4	T19	Bidirectional
PA0 CLK8 $\overline{\text{TOUT4}}$ L1TCLKB	U19	Bidirectional
PB31 $\overline{\text{SPISEL}}$ $\overline{\text{REJECT1}}$	C17	Bidirectional (Optional: Open-drain)
PB30 SPICLK $\overline{\text{RSTRT2}}$	C19	Bidirectional (Optional: Open-drain)
PB29 SPIMOSI	E16	Bidirectional (Optional: Open-drain)
PB28 SPIMISO BRGO4	D19	Bidirectional (Optional: Open-drain)
PB27 I2CSDA BRGO1	E19	Bidirectional (Optional: Open-drain)
PB26 I2CSCL BRGO2	F19	Bidirectional (Optional: Open-drain)

Table 39. Pin Assignments (continued)

Name	Pin Number	Type
MII_COL	H4	Input
VSSSYN1	V1	PLL analog VDD and GND
VSSSYN	U1	Power
VDDSYN	T1	Power
GND	F6, F7, F8, F9, F10, F11, F12, F13, F14, G6, G7, G8, G9, G10, G11, G12, G13, G14, H6, H7, H8, H9, H10, H11, H12, H13, H14, J6, J7, J8, J9, J10, J11, J12, J13, J14, K6, K7, K8, K9, K10, K11, K12, K13, K14, L6, L7, L8, L9, L10, L11, L12, L13, L14, M6, M7, M8, M9, M10, M11, M12, M13, M14, N6, N7, N8, N9, N10, N11, N12, N13, N14, P6, P7, P8, P9, P10, P11, P12, P13, P14	Power
VDDL	A8, M1, W8, H19, F4, F16, P4, P16, R1	Power
VDDH	E5, E6, E7, E8, E9, E10, E11, E12, E13, E14, E15, F5, F15, G5, G15, H5, H15, J5, J15, K5, K15, L5, L15, M5, M15, N5, N15, P5, P15, R5, R6, R7, R8, R9, R10, R11, R12, R13, R14, R15, T14	Power
N/C	D6, D13, D14, U2, V2, T2	No-connect

[1] Classic SAR mode only

[2] ESAR mode only

16 Document Revision History

Table 40 lists significant changes between revisions of this document.

Table 40. Document Revision History

Revision Number	Date	Substantive Changes
0	5/2002	Initial revision
1	11/2002	Added the 5-V tolerant pins, new package dimensions, and other changes.
1.1	4/2003	Added the Spec. B1d and changed spec. B1a. Added the Note Solder sphere composition for MPC866XZP, MPC859DSLZP, and MPC859TZP is 62%Sn 36%Pb 2%Ag to Figure 15-79.
1.2	4/2003	Added the MPC859P.
1.3	5/2003	Changed the SPI Master Timing Specs. 162 and 164.
1.4	7-8/2003	• Added TxClav and RxClav to PB15 and PC15. Changed B28a through B28d and B29b to show that TRLX can be 0 or 1. • Added nontechnical reformatting.
1.5	3/14/2005	• Updated document template.
2	2/10/2006	• Updated orderable parts table.

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