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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I²C, SCI, SPI
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	34
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	12K x 8
Voltage - Supply (Vcc/Vdd)	1.62V ~ 5.5V
Data Converters	A/D 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f52103bdfl-30

Table 1.1 Outline of Specifications (2 / 5)

Classification	Module/Function	Description
Low power consumption	Low power consumption facilities	• Module stop function • Four low power consumption modes Sleep mode, all-module clock stop mode, software standby mode, and deep software standby mode
	Function for lower operating power consumption	• Operating power control modes [Chip versions A and C] High-speed operating mode, middle-speed operating mode 1A, middle-speed operating mode 1B, low-speed operating mode 1, low-speed operating mode 2 [Chip version B] High-speed operating mode, middle-speed operating mode 1A, middle-speed operating mode 1B, middle-speed operating mode 2A, middle-speed operating mode 2B, low-speed operating mode 1, low-speed operating mode 2
Interrupt	Interrupt controller (ICUb)	• Interrupt vectors: 167 • External interrupts: 9 (NMI, IRQ0 to IRQ7 pins) • Non-maskable interrupts: 6 (the NMI pin, oscillation stop detection interrupt, voltage monitoring 1 interrupt, voltage monitoring 2 interrupt, WDT interrupt, and IWDT interrupt) • 16 levels specifiable for the order of priority
External bus extension		• The external address space can be divided into four areas (CS0 to CS3), each with independent control of access settings. Capacity of each area: 16 Mbytes (CS0 to CS3) A chip-select signal (CS0# to CS3#) can be output for each area. Each area is specifiable as an 8-bit or 16-bit bus space The data arrangement in each area is selectable as little or big endian (only for data). Bus format: Separate bus, multiplex bus • Wait control • Write buffer facility
DMA	DMA controller (DMACA)	• 4 channels • Three transfer modes: Normal transfer, repeat transfer, and block transfer • Activation sources: Software trigger, external interrupts, and interrupt requests from peripheral functions
	Data transfer controller (DTCa)	• Three transfer modes: Normal transfer, repeat transfer, and block transfer • Activation sources: Interrupts • Chain transfer function
I/O ports	General I/O ports	145-pin/144-pin/100-pin/80-pin/69-pin/64-pin/48-pin • I/O: 122/122/84/64/48/48/34 • Input: 1/1/1/1/1/1/1 • Pull-up resistors: 122/122/84/64/48/48/34 • Open-drain outputs: 76/76/54/44/35/35/26 • 5-V tolerance:4/4/4/4/2/2*1/2
Event link controller (ELC)		• Event signals of 59 types can be directly connected to the module • Operations of timer modules are selectable at event input • Capable of event link operation for ports B and E
Multi-function pin controller (MPC)		• Capable of selecting input/output function from multiple pins

Table 1.1 Outline of Specifications (3 / 5)

Classification	Module/Function	Description
Timers	16-bit timer pulse unit (TPUa)	• (16 bits × 6 channels) × 1 unit • Maximum of 16 pulse-input/output possible • Select from among seven or eight counter-input clock signals for each channel • Supports the input capture/output compare function • Output of PWM waveforms in up to 15 phases in PWM mode • Support for buffered operation, phase-counting mode (two-phase encoder input) and cascade-connected operation (32 bits × 2 channels) depending on the channel. • Capable of generating conversion start triggers for the A/D converters • Signals from the input capture pins are input via a digital filter • Clock frequency measuring method (Products with 144 or more pins incorporate a TPU.)
	Multi-function timer pulse unit 2 (MTU2a)	• (16 bits × 6 channels) × 1 unit • Up to 16 pulse-input/output lines and three pulse-input lines are available with six 16-bit timer channels • Select from among eight or seven counter-input clock signals for each channel (PCLK/1, PCLK/4, PCLK/16, PCLK/64, PCLK/256, PCLK/1024, MTCLKA, MTCLKB, MTCLKC, MTCLKD) other than channel 5, for which only four signals are available. • Input capture function • 21 output compare/input capture registers • Pulse output mode • Complementary PWM output mode • Reset synchronous PWM mode • Phase-counting mode • Generation of triggers for A/D converter conversion
	Port output enable 2 (POE2a)	Controls the high-impedance state of the MTU's waveform output pins
	8-bit timer (TMR)	• (8 bits × 2 channels) × 2 units • Select from among seven internal clock signals (PCLK1, PCLK/2, PCLK/8, PCLK/32, PCLK/64, PCLK/1024, PCLK/8192) and one external clock signal • Capable of output of pulse trains with desired duty cycles or of PWM signals • The 2 channels of each unit can be cascaded to create a 16-bit timer • Capable of generating baud-rate clocks for SCI5, SCI6, and SCI12
	Compare match timer (CMT)	• (16 bits × 2 channels) × 2 units • Select from among four clock signals (PCLK/8, PCLK/32, PCLK/128, PCLK/512)
	Watchdog timer (WDTA)	• 14 bits × 1 channel • Select from among six counter-input clock signals (PCLK/4, PCLK/64, PCLK/128, PCLK/512, PCLK/2048, PCLK/8192)
	Independent watchdog timer (IWDTa)	• 14 bits × 1 channel • Counter-input clock: IWDT-dedicated on-chip oscillator Frequency divided by 1, 16, 32, 64, 128, or 256
	Realtime clock (RTCb)	• Clock source: Sub-clock • Time/calendar • Interrupt sources: Alarm interrupt, periodic interrupt, and carry interrupt • Time-capture facility for three values

Table 1.2 Comparison of Functions for Different Packages

Module/Functions		RX210 Group				
		144, 145 Pins	**100 Pins**	**80 Pins**	**64, 69 Pins**	**48 Pins**
External bus	External bus width	16 bits		Not supported		
Interrupt	External interrupts	NMI, IRQ0 to IRQ7			NMI, IRQ0 to IRQ2, IRQ4 to IRQ7	NMI, IRQ0, IRQ1, IRQ4 to IRQ7
DMA	DMA controller	4 channels (DMAC0 to DMAC3)				
	Data transfer controller	Supported				
Timers	16-bit timer pulse unit	6 channels (TPU0 to TPU5)	Not supported			
	Multi-function timer pulse unit 2	6 channels (MTU0 to MTU5)				
	Port output enable 2	POE0# to POE3#, POE8#				
	8-bit timer	2 channels × 2 units				
	Compare match timer	2 channels × 2 units				
	Realtime clock	Supported				Not supported
	Watchdog timer	Supported				
	Independent watchdog timer	Supported				
Communication functions	Serial communications interface (SCIc)	12 channels (SCI0 to 11)	6 channels (SCI0, 1, 5, 6, 8, 9)		5 channels (SCI1, 5, 6, 8, 9)	4 channels (SCI1, 5, 6, 8)
	Serial communications interface (SCId)	1 channel (SCI12)				
	I^2C bus interface	1 channel				
	Serial peripheral interface	1 channel				
12-bit A/D converter		16 channels (AN000 to AN015)		14 channels (AN000 to AN013)	12 channels (AN000 to AN004, AN006, AN008 to AN013)	8 channels (AN000 to AN002, AN006, AN009 to AN012)
Temperature sensor		Supported				
D/A converter		2 channels				Not supported
CRC calculator		Supported				
Event link controller		Supported				
Comparator A		2 channels				
Comparator B		2 channels				
Packages		145-pin TFLGA 144-pin LQFP	100-pin TFLGA 100-pin LQFP	80-pin LQFP	69-pin WLBGA 64-pin TFLGA 64-pin LQFP	48-pin LQFP

Table 1.8 Pin Functions (4 / 4)

Classifications	Pin Name	I/O	Description
Analog power supply	AVCC0	Input	Analog voltage supply pin for the 12-bit A/D converter. Connect this pin to VCC if the 12-bit A/D converter is not to be used.
	AVSS0	Input	Analog ground pin for the 12-bit A/D converter. Connect this pin to VSS if the 12-bit A/D converter is not to be used.
	VREFH0	Input	Analog reference voltage supply pin for the 12-bit A/D converter. Connect this pin to VCC if the 12-bit A/D converter is not to be used.
	VREFL0	Input	Analog reference ground pin for the 12-bit A/D converter. Connect this pin to VSS if the 12-bit A/D converter is not to be used.
	VREFH	Input	Analog voltage supply pin for the D/A converter. Connect this pin to VCC if the D/A converter is not to be used.
	VREFL	Input	Analog ground pin for the D/A converter. Connect this pin to VSS if the D/A converter is not to be used.
I/O ports	P00 to P03, P05, P07	I/O	6-bit input/output pins.
	P12 to P17	I/O	6-bit input/output pins.
	P20 to P27	I/O	8-bit input/output pins.
	P30 to P37	I/O	8-bit input/output pins. (P35 input pin)
	P40 to P47	I/O	8-bit input/output pins.
	P50 to P56	I/O	7-bit input/output pins.
	P60 to P67	I/O	8-bit input/output pins.
	P70 to P77	I/O	8-bit input/output pins.
	P80 to P83, P86, P87	I/O	6-bit input/output pins.
	P90 to P93	I/O	4-bit input/output pins.
	PA0 to PA7	I/O	8-bit input/output pins.
	PB0 to PB7	I/O	8-bit input/output pins.
	PC0 to PC7	I/O	8-bit input/output pins.
	PD0 to PD7	I/O	8-bit input/output pins.
	PE0 to PE7	I/O	8-bit input/output pins.
	PF5	I/O	1-bit input/output pin.
	PH0 to PH3	I/O	4-bit input/output pins.
	PJ1, PJ3, PJ5	I/O	3-bit input/output pins.
	PK2 to PK5	I/O	4-bit input/output pins.
	PL0, PL1	I/O	2-bit input/output pins.

Table 1.9 List of Pins and Pin Functions (145-Pin TFLGA) (4 / 4)

Pin No.	Power Supply, Clock, System Control	I/O Port	External Bus	Timers (MTU, TMR, POE)	Communications (SCIc, SCId, RSPI, RIIC)	Others
M11		PC0	A16	MTIOC3C/TCLKC	CTS5#/RTS5#/SS5#/ SSLA1	
M12		PC1	A17	MTIOC3A/TCLKD	SCK5/SSLA2	
M13		PL1				
N1		P21		MTIOC1B/TMCI0/ TIOCA3	RXD0/SMISO0/SSCL0	
N2		P20		MTIOC1A/TMRI0/ TIOCB3	TXD0/SMOSI0/SSDA0	
N3		P87		TIOCA2		
N4		P14		MTIOC3A/MTCLKA/ TMRI2/TIOCB5/TCLKA	CTS1#/RTS1#/SS1#	IRQ4
N5		PH2		TMRI0		IRQ1
N6		PH1		TMO0		IRQ0
N7		P55	WAIT#	MTIOC4D/TMO3		
N8	VSS					
N9		PC7	A23/CS0#	MTIOC3A/TMO2/ MTCLKB	TXD8/SMOSI8/SSDA8/ MISOA	CACREF
N10		P82		MTIOC4A	TXD10/SMOSI10/SSDA10	
N11		PC3	A19	MTIOC4D/TCLKB	TXD5/SMOSI5/SSDA5	
N12		P75			SCK11	
N13		P74			CTS11#/RTS11#/SS11#	

Note: • Pin names to which –DS is appended are for pins that can be used to trigger release from deep software standby mode.
Note: • Leave the NC pin open.

Table 1.10 List of Pins and Pin Functions (144-Pin LQFP) (2 / 4)

Pin No.	Power Supply, Clock, System Control	I/O Port	External Bus	Timers (MTU, TMR, POE)	Communications (SCIc, SCId, RSPI, RIIC)	Others
40		P16		MTIOC3C/MTIOC3D/ TMO2/TIOCB1/TCLKC	TXD1/SMOSI1/SSDA1/ MOSIA/SCL-DS/RXD3/ SMISO3/SSCL3	IRQ6/RTCOUT/ ADTRG0#
41		P86		TIOCA0		
42		P15		MTIOC0B/MTCLKB/ TMCI2/TIOCB2/TCLKB	RXD1/SMISO1/SSCL1/ SCK3	IRQ5
43		P14		MTIOC3A/MTCLKA/ TMRI2/TIOCB5/TCLKA	CTS1#/RTS1#/SS1#	IRQ4
44		P13		MTIOC0B/TMO3/ TIOCA5	SDA/TXD2/SMOSI2/ SSDA2	IRQ3
45		P12		TMCI1	SCL/RXD2/SMISO2/ SSCL2	IRQ2
46		PH3		TMCI0		
47		PH2		TMRI0		IRQ1
48		PH1		TMO0		IRQ0
49		PH0				CACREF
50		P56		MTIOC3C/TIOCA1		
51		P55	WAIT#	MTIOC4D/TMO3		
52		P54	ALE	MTIOC4B/TMCI1	CTS2#/RTS2#/SS2#	
53	BCLK	P53				
54		P52	RD#		RXD2/SMISO2/SSCL2	
55		P51	WR1#/BC1#/WAIT#		SCK2	
56		P50	WR0#/WR#		TXD2/SMOSI2/SSDA2	
57	VSS					
58		P83		MTIOC4C	CTS10#/RTS10#	
59	VCC					
60		PC7	A23/CS0#	MTIOC3A/TMO2/ MTCLKB	TXD8/SMOSI8/SSDA8/ MISOA	CACREF
61		PC6	A22/CS1#	MTIOC3C/MTCLKA/ TMCI2	RXD8/SMISO8/SSCL8/ MOSIA	
62		PC5	A21/CS2#/WAIT#	MTIOC3B/MTCLKD/ TMRI2	SCK8/RSPCKA	
63		P82		MTIOC4A	TXD10/SMOSI10/SSDA10	
64		P81		MTIOC3D	RXD10/SMISO10/SSCL10	
65		P80		MTIOC3B	SCK10	
66		PC4	A20/CS3#	MTIOC3D/MTCLKC/ TMCI1/POE0#	SCK5/CTS8#/RTS8#/ SS8#/SSLA0	
67		PC3	A19	MTIOC4D/TCLKB	TXD5/SMOSI5/SSDA5	
68		P77			TXD11/SMOSI11/SSDA11	
69		P76			RXD11/SMISO11/SSCL11	
70		PC2	A18	MTIOC4B/TCLKA	RXD5/SMISO5/SSCL5/ ISSLA3	
71		P75			SCK11	
72		P74			CTS11#/RTS11#/SS11#	
73		PC1	A17	MTIOC3A/TCLKD	SCK5/SSLA2	
74		PL1				
75		PC0	A16	MTIOC3C/TCLKC	CTS5#/RTS5#/SS5#/ SSLA1	
76		PL0				
77		P73				
78		PB7	A15	MTIOC3B/TIOCB5	TXD9/SMOSI9/SSDA9	
79		PB6	A14	MTIOC3D/TIOCA5	RXD9/SMISO9/SSCL9	
80		PB5	A13	MTIOC2A/MTIOC1B/ TMRI1/POE1#/TIOCB4	SCK9	

- Longword-size I/O registers

```
MOV.L  #SFR_ADDR, R1
MOV.L  #SFR_DATA, [R1]
CMP    [R1].L, R1
;; Next process
```

If multiple registers are written to and a subsequent instruction should be executed after the write operations are entirely completed, only read the I/O register that was last written to and execute the operation using the value; it is not necessary to read or execute operation for all the registers that were written to.

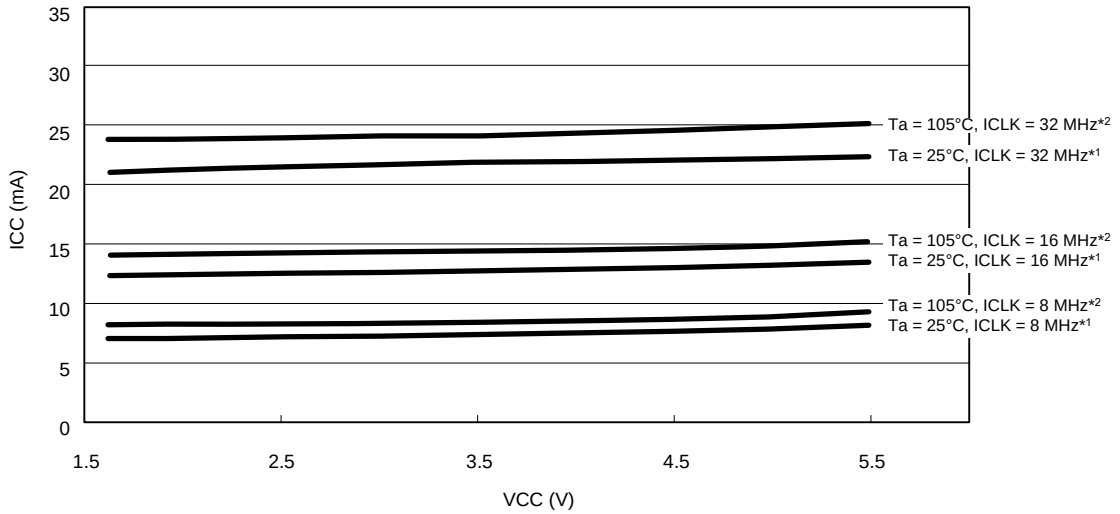
(3) Number of Access Cycles to I/O Registers

For numbers of clock cycles for access to I/O registers, see Table 4.1, List of I/O Registers (Address Order).
The number of access cycles to I/O registers is obtained by following equation.*1

Number of access cycles to I/O registers = Number of bus cycles for internal main bus 1 +
Number of divided clock synchronization cycles +
Number of bus cycles for internal peripheral bus 1 to 6

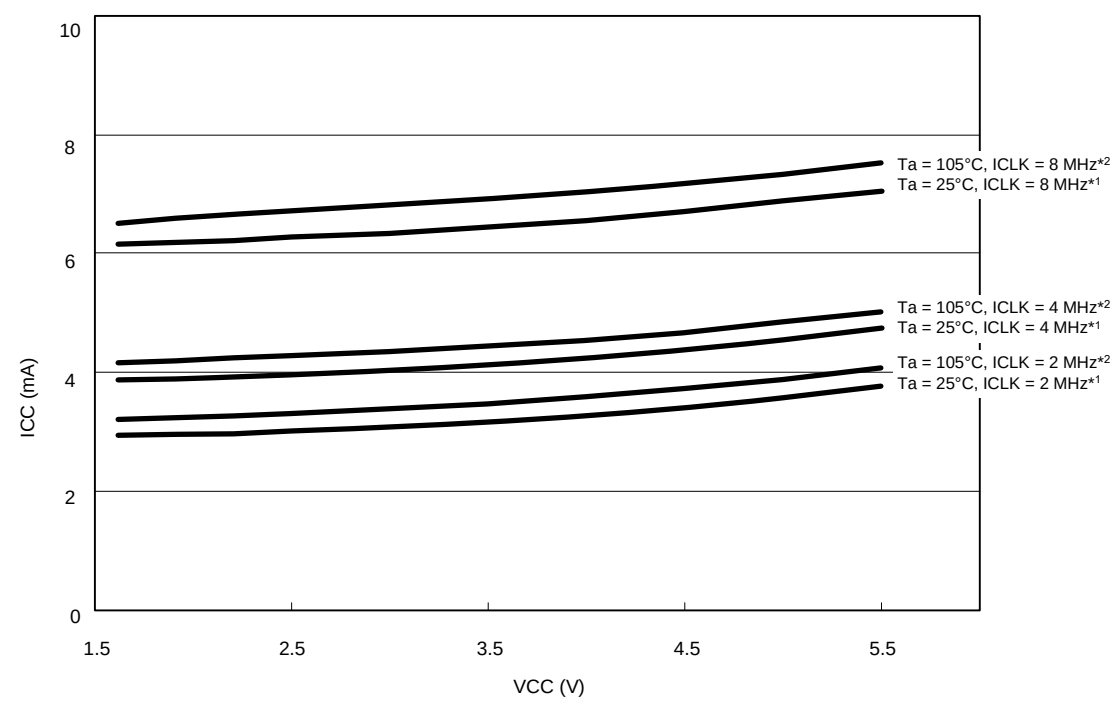
The number of bus cycles of internal peripheral bus 1 to 6 differs according to the register to be accessed.
When peripheral functions connected to internal peripheral bus 2 to 6 or registers for the external bus control unit (except for bus error related registers) are accessed, the number of divided clock synchronization cycles is added.
The number of divided clock synchronization cycles differs depending on the frequency ratio between ICLK and PCLK (or FCLK, BCLK) or bus access timing.
In the peripheral function unit, when the frequency ratio of ICLK is equal to or greater than that of PCLK (or FCLK), the sum of the number of bus cycles for internal main bus 1 and the number of the divided clock synchronization cycles will be one cycle of PCLK (or FCLK) at a maximum. Therefore, one PCLK (or FCLK) has been added to the number of access cycles shown in Table 4.1.
When the frequency ratio of ICLK is lower than that of PCLK (or FCLK), the subsequent bus access is started from the ICLK cycle following the completion of the access to the peripheral functions. Therefore, the access cycles are described on an ICLK basis.
In the external bus control unit, the sum of the number of bus cycles for internal main bus 1 and the number of divided clock synchronization cycles will be one cycle of BCLK at a maximum. Therefore, one BCLK is added to the number of access cycles shown in Table 4.1.

Note 1. This applies to the number of cycles when the access from the CPU does not conflict with the instruction fetching to the external memory or bus access from the different bus master (DMAC or DTC).



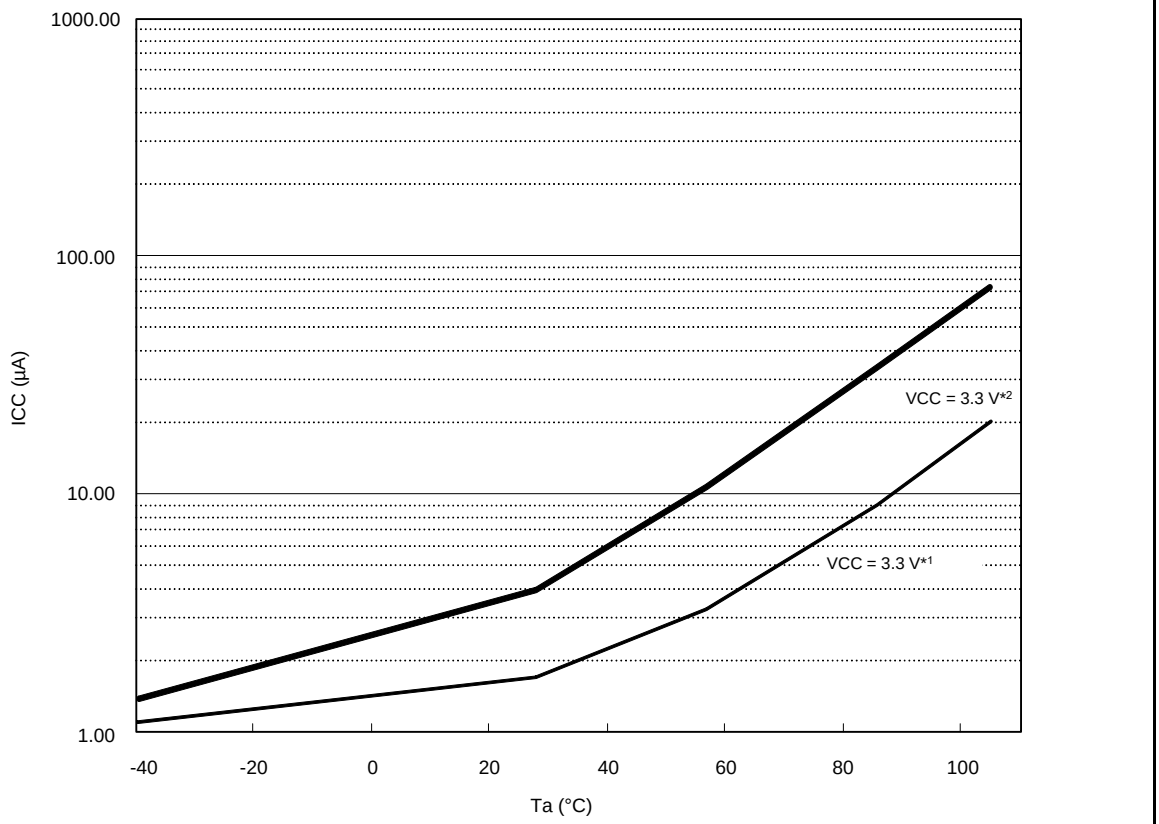
Note 1. All peripheral operation is normal. This does not include BGO operation.
Average value of the tested middle samples during product evaluation
Note 2. All peripheral operation is maximum. This does not include BGO operation.
Average value of the tested upper-limit samples during product evaluation.

Figure 5.37 Voltage Dependency in Middle-Speed Operating Modes 2A and 2B (Reference Data) for Chip Version B with 512 Kbytes or Less of Flash Memory and 144 and 145 Pins



Note 1. All peripheral operation is normal.
Average value of the tested middle samples during product evaluation.
Note 2. All peripheral operation is maximum.
Average value of the tested upper-limit samples during product evaluation.

Figure 5.38 Voltage Dependency in Low-Speed Operating Mode 1 (Reference Data) for Chip Version B with 512 Kbytes or Less of Flash Memory and 144 and 145 Pins



Note 1. Average value of the tested middle samples during product evaluation
Note 2. Average value of the tested upper-limit samples during product evaluation.

Figure 5.41 Temperature Dependency in Software Standby Mode (SOFTCUT[2:0] Bits = 110b) (Reference Data) for Chip Version B with 512 Kbytes or Less of Flash Memory and 144 and 145 Pins

Table 5.44 Clock Timing

Conditions: VCC = AVCC0 = 1.62 to 5.5 V, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
EXTAL external clock input cycle time		t_{EXcyc}	50	—	—	ns	Figure 5.60
EXTAL external clock input high pulse width		t_{EXH}	20	—	—	ns	
EXTAL external clock input low pulse width		t_{EXL}	20	—	—	ns	
EXTAL external clock rising time		t_{EXr}	—	—	5	ns	
EXTAL external clock falling time		t_{EXf}	—	—	5	ns	
EXTAL external clock input wait time*1		t_{EXWT}	1	—	—	ms	
Main clock oscillator oscillation frequency*2		f_{MAIN}	1	—	20	MHz	
Main clock oscillation stabilization time (crystal)*2		$t_{MAINOSC}$	—	3	—	ms	Figure 5.61
Main clock oscillation stabilization time (ceramic resonator)*2		$t_{MAINOSC}$	—	50		µs	
Main clock oscillation stabilization wait time (crystal)*2		$t_{MAINOSCWT}$	—	6	—	ms	
Main clock oscillation stabilization wait time (ceramic resonator)*2		$t_{MAINOSCWT}$	—	100		µs	
LOCO clock cycle time		t_{cyc}	7.27	8	8.89	µs	
LOCO clock oscillation frequency*6		f_{LOCO}	112.5	125	137.5	kHz	
LOCO clock oscillation stabilization wait time		t_{LOCOWT}	—	—	20	µs	Figure 5.62
HOCO clock oscillation frequency*7		f_{HOCO}	31.680	32	32.320	MHz	Ta = 0 to 50°C
			36.495	36.864	37.233		
			39.600	40	40.400		
			49.500	50	50.500		
			31.520	32	32.480		Ta = -40 to 105°C
			36.311	36.864	37.417		
			39.400	40	40.600		
			49.250	50	50.750		
HOCO clock oscillation stabilization time 1		t_{HOCO1}	—	—	300	µs	Figure 5.63
HOCO clock oscillation stabilization time 2		t_{HOCO2}	—	—	175	µs	Figure 5.64
HOCO clock oscillation stabilization wait time		t_{HOCOWT}	—	—	350	µs	Figure 5.64
HOCO clock power supply stabilization time		t_{HOCOP}	—	—	350	µs	Figure 5.65
PLL input frequency		f_{PLLIN}	4	—	12.5	MHz	
PLL circuit oscillation frequency		f_{PLL}	50	—	100	MHz	
PLL clock oscillation stabilization time	PLL operation started after main clock oscillation has settled	t_{PLL1}	—	—	500	µs	Figure 5.66
PLL clock oscillation stabilization wait time		t_{PLLWT1}	1.5	—	—	ms	
PLL clock oscillation stabilization time*4	PLL operation started before main clock oscillation has settled	t_{PLL2}	—	3.5*3	—	ms	Figure 5.67
PLL clock oscillation stabilization wait time*4		t_{PLLWT2}	—	7	—	ms	
PLL clock power supply stabilization time (for chip version B only)		t_{PLLPW}	—	—	30	µs	Figure 5.68
Sub-clock oscillator oscillation frequency		f_{SUB}	—	32.768	—	kHz	
Sub-clock oscillation stabilization time*5		t_{SUBOSC}	2	—	—	s	Figure 5.69
Sub-clock oscillation stabilization wait time*5		$t_{SUBOSCWT}$	4	—	—	s	

Note 1. The time interval from the time P36 and P37 are configured for input and the main clock oscillator stopping bit (MOSCCR.MOSTP) is set to 0 (operating) until the clock becomes available.

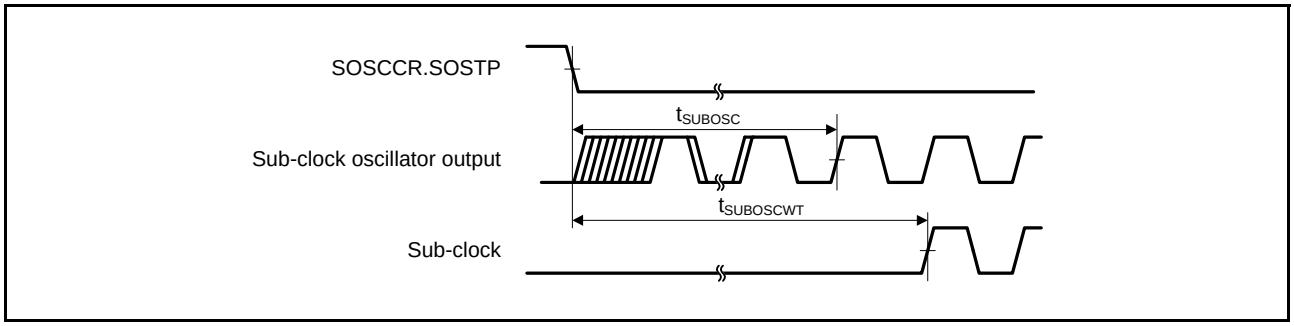


Figure 5.69 Sub-clock Oscillation Start Timing

Item				Symbol	Min.	Max.	Unit*1	Test Conditions
RSPI	MOSI and MISO rise/fall time	Output		t_{Dr}, t_{Df}	—	20	ns	C = 30 pF Figure 5.92 to Figure 5.97
		Input			—	1	μs	
	SSL rise/fall time	Output		t_{SSLr}, t_{SSLf}	—	20	ns	
		Input			—	1	μs	
	Slave access time		2.7 V ≤ VCC ≤ 5.5 V	t_{SA}	—	6	t_{Pcyc}	C = 30 pF Figure 5.96 and Figure 5.97
			1.8 V ≤ VCC < 2.7 V		—	7		
			1.62 V ≤ VCC < 1.8 V		—	7		
	Slave output release time		2.7 V ≤ VCC ≤ 5.5 V	t_{REL}	—	5	t_{Pcyc}	
			1.8 V ≤ VCC < 2.7 V		—	6		
			1.62 V ≤ VCC < 1.8 V		—	6		

Note 1. t_{Pcyc}: PCLK cycle

[768 Kbytes/1 Mbyte of flash memory or 144/145 pins]

Table 5.57 Timing of On-Chip Peripheral Modules (3)

Conditions: VCC = AVCC0 = 1.62 to 5.5 V, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +105°C
When high-drive output is selected by the drive capacity register

Item				Symbol	Min.	Max.	Unit*1	Test Conditions
RSPI	RSPCK clock cycle	Master		t_{SPcyc}	2	4096	t_{Pcyc}	C = 30pF Figure 5.91
		Slave			8	4096		
	RSPCK clock high pulse width	Master	2.7 V ≤ VCC ≤ 5.5 V	t_{SPCKWH}	$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2 - 3$	—	ns	
			1.8 V ≤ VCC < 2.7 V		$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2 - 3$	—		
			1.62 V ≤ VCC < 1.8 V		$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2 - 10$	—		
		Slave			$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2$	—		
	RSPCK clock low pulse width	Master	2.7 V ≤ VCC ≤ 5.5 V	t_{SPCKWL}	$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2 - 3$	—	ns	
			1.8 V ≤ VCC < 2.7 V		$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2 - 3$	—		
			1.62 V ≤ VCC < 1.8 V		$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2 - 10$	—		
		Slave			$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2$	—		
	RSPCK clock rise/fall time	Output	2.7 V ≤ VCC ≤ 5.5 V	t_{SPCKr}, t_{SPCKf}	—	10	ns	
			1.8 V ≤ VCC < 2.7 V		—	15		
			1.62 V ≤ VCC < 1.8 V		—	20		
		Input			—	1	μs	

Differential nonlinearity error (DNL)

Differential nonlinearity error is the difference between 1-LSB width based on the ideal A/D conversion characteristics and the width of the actually output code.

Offset error

Offset error is the difference between a transition point of the ideal first output code and the actual first output code.

Full-scale error

Full-scale error is the difference between a transition point of the ideal last output code and the actual last output code.

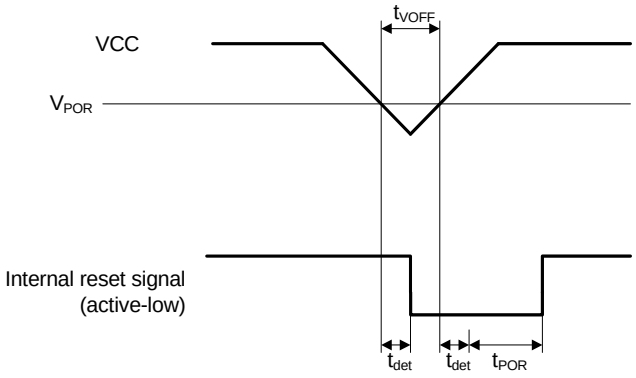
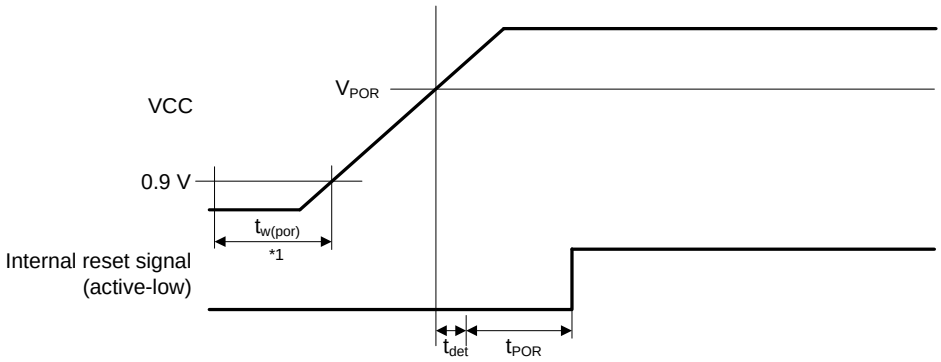


Figure 5.103 Voltage Detection Reset Timing



Note 1. $t_{w(por)}$ is the time required for a power-on reset to be enabled while the external power VCC is being held below the valid voltage (0.9 V).
When VCC turns on, maintain $t_{w(por)}$ for 1 ms or more.

Figure 5.104 Power-on Reset Timing

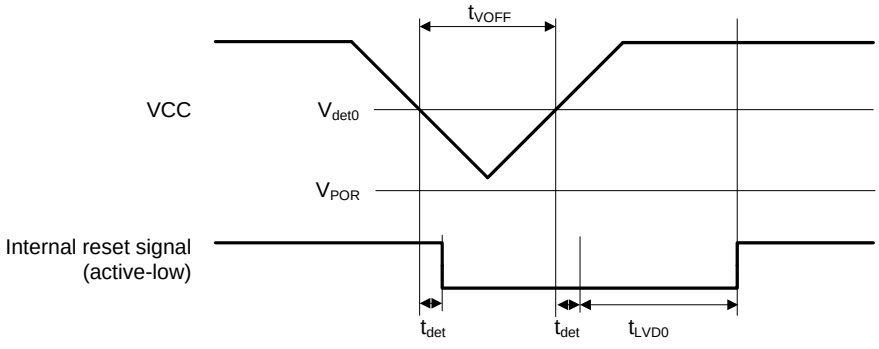


Figure 5.105 Voltage Detection Circuit Timing (V_{det0})

[Chip version B]

Table 5.79 ROM (Flash Memory for Code Storage) Characteristics (6) : middle-speed operating modes 1B and 2B

Conditions: VCC = AVCC0 = 1.62 to 3.6 V, VREFH = VREFH0 = AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V
Temperature range for the programming/erasure operation: T_a = –40 to +105°C

Item		Symbol	FCLK = 4 MHz			FCLK = 32 MHz*1			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Programming time when N_{PEC} ≤ 100 times	2 bytes	t_{P2}	—	0.25	5.0	—	0.21	2.8	ms
	8 bytes	t_{P8}	—	0.25	5.3	—	0.21	3.0	
	128 bytes	t_{P128}	—	0.92	14.0	—	0.65	8.3	
Programming time when N_{PEC} > 100 times	2 bytes	t_{P2}	—	0.31	6.2	—	0.26	3.5	ms
	8 bytes	t_{P8}	—	0.31	6.6	—	0.26	3.7	
	128 bytes	t_{P128}	—	1.09	17.5	—	0.77	10.0	
Erasure time when N_{PEC} ≤ 100 times	2 Kbytes	t_{E2K}	—	21.0	113.7	—	18.5	46	ms
Erasure time when N_{PEC} > 100 times	2 Kbytes	t_{E2K}	—	25.6	220.6	—	22.5	90 (1000 times ≥ N_{PEC} > 100 times), 98 (10000 times ≥ N_{PEC} > 1000 times)	ms
Suspend delay time during programming (in programming/erasure priority mode)		t_{SPD}	—	—	1.7	—	—	1.6	ms
First suspend delay time during programming (in suspend priority mode)		t_{SPSD1}	—	—	220	—	—	120	µs
Second suspend delay time during programming (in suspend priority mode)		t_{SPSD2}	—	—	1.7	—	—	1.6	ms
Suspend delay time during erasing (in programming/erasure priority mode)		t_{SED}	—	—	1.7	—	—	1.6	ms
First suspend delay time during erasing (in suspend priority mode)		t_{SESD1}	—	—	220	—	—	120	µs
Second suspend delay time during erasing (in suspend priority mode)		t_{SESD2}	—	—	1.7	—	—	1.6	ms
FCU reset time		t_{FCUR}	20 µs or longer and FCLK × 6 or greater	—	—	20 µs or longer and FCLK × 6 or greater	—	—	µs

Note 1. The operating frequency is 20 MHz (max.) when the voltage is in the range from 1.62 V to less than 1.8 V.

[Chip version B]

Table 5.84 E2 DataFlash Characteristics (5)
: high-speed operating mode, middle-speed operating modes 1A and 2A

Conditions: VCC = AVCC0 = 2.7 to 5.5 V, VREFH = VREFH0 = AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V
Temperature range for the programming/erasure operation: T_a = –40 to +105°C

Item		Symbol	FCLK = 4 MHz			FCLK = 32 MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Programming time when N_{DPEC} ≤ 100 times	2 bytes	t_{DP2}	—	0.19	4.4	—	0.13	2.0	ms
	8 bytes	t_{DP8}	—	0.24	5.1	—	0.13	2.2	
Programming time when N_{DPEC} > 100 times	2 bytes	t_{DP2}	—	0.25	6.4	—	0.17	3.0	ms
	8 bytes	t_{DP8}	—	0.32	7.5	—	0.18	3.2	
Erasure time when N_{DPEC} ≤ 100 times	128 bytes	t_{DE128}	—	3.3	27.1	—	2.5	8	ms
Erasure time when N_{DPEC} > 100 times	128 bytes	t_{DE128}	—	4.0	45.1	—	3.0	12	ms
Blank check time	2 bytes	t_{DBC2}	—	—	98	—	—	35	µs
	2 Kbytes	t_{DBC2K}	—	—	16	—	—	2.5	ms
Suspend delay time during programming (in programming/erasure priority mode)		t_{DSPD}	—	—	0.9	—	—	0.8	ms
First suspend delay time during programming (in suspend priority mode)		t_{DSPSD1}	—	—	220	—	—	120	µs
Second suspend delay time during programming (in suspend priority mode)		t_{DSPSD2}	—	—	0.9	—	—	0.8	ms
Suspend delay time during erasing (in programming/erasure priority mode)		t_{DSED}	—	—	0.9	—	—	0.8	ms
First suspend delay time during erasing (in suspend priority mode)		t_{DSESD1}	—	—	220	—	—	120	µs
Second suspend delay time during erasing (in suspend priority mode)		t_{DSESD2}	—	—	0.9	—	—	0.8	ms

[Chip version B]

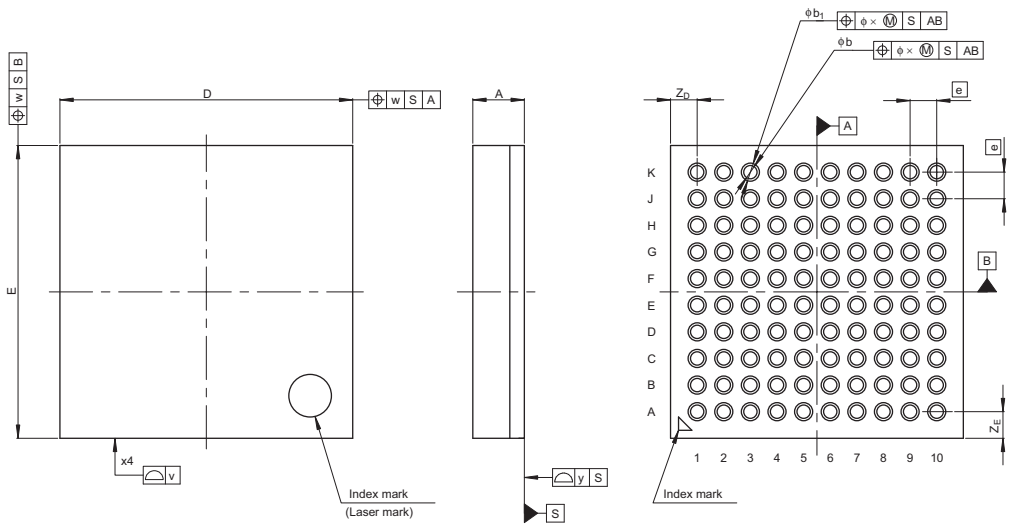
Table 5.85 E2 DataFlash Characteristics (6)
: middle-speed operating modes 1B and 2B

Conditions: VCC = AVCC0 = 1.62 to 3.6 V, VREFH = VREFH0 = AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V
Temperature range for the programming/erasure operation: T_a = –40 to +105°C

Item		Symbol	FCLK = 4 MHz			FCLK = 32 MHz*1			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Programming time when N_{DPEC} ≤ 100 times	2 bytes	t_{DP2}	—	0.28	5.1	—	0.20	2.8	ms
	8 bytes	t_{DP8}	—	0.32	6.0	—	0.22	3.2	
Programming time when N_{DPEC} > 100 times	2 bytes	t_{DP2}	—	0.36	7.6	—	0.25	4.2	ms
	8 bytes	t_{DP8}	—	0.40	8.8	—	0.28	4.5	
Erasure time when N_{DPEC} ≤ 100 times	128 bytes	t_{DE128}	—	4.8	32.4	—	4.1	12	ms
Erasure time when N_{DPEC} > 100 times	128 bytes	t_{DE128}	—	5.8	51.4	—	4.9	17	ms
Blank check time	2 bytes	t_{DBC2}	—	—	110	—	—	40	µs
	2 Kbytes	t_{DBC2K}	—	—	16.3	—	—	2.6	ms
Suspend delay time during programming (in programming/erasure priority mode)		t_{DSPD}	—	—	1.7	—	—	1.6	ms
First suspend delay time during programming (in suspend priority mode)		t_{DSPSD1}	—	—	220	—	—	120	µs
Second suspend delay time during programming (in suspend priority mode)		t_{DSPSD2}	—	—	1.7	—	—	1.6	ms
Suspend delay time during erasing (in programming/erasure priority mode)		t_{DSED}	—	—	1.7	—	—	1.6	ms
First suspend delay time during erasing (in suspend priority mode)		t_{DSESD1}	—	—	220	—	—	120	µs
Second suspend delay time during erasing (in suspend priority mode)		t_{DSESD2}	—	—	1.7	—	—	1.6	ms

Note 1. The operating frequency is 20 MHz (max.) when the voltage is in the range from 1.62 V to less than 1.8 V.

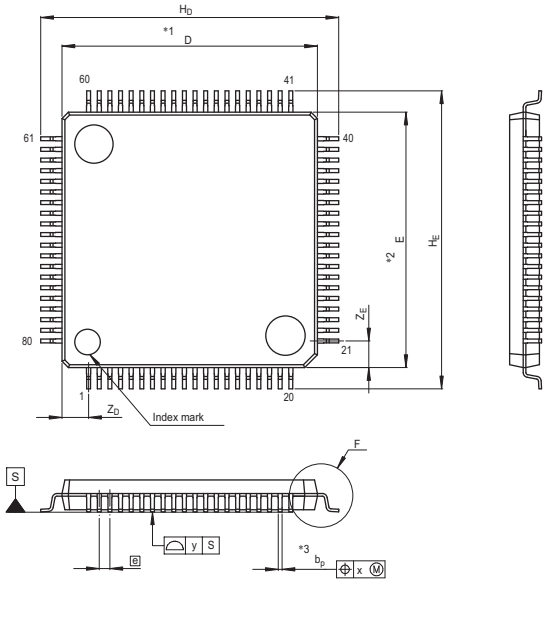
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-TFLGA100-5.5x5.5-0.50	PTLG0100KA-A	100F0M	0.1g



Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	5.5	—
E	—	5.5	—
v	—	—	0.15
w	—	—	0.20
A	—	—	1.05
e	—	0.5	—
b	0.21	0.25	0.29
b_1	0.29	0.34	0.39
x	—	—	0.08
y	—	—	0.08
Z_D	—	0.5	—
Z_E	—	0.5	—

Figure D 100-Pin TFLGA (PTLG0100KA-A)

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LFQFP80-12x12-0.50	PLQP0080KB-A	80P6Q-A	0.5g



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	11.9	12.0	12.1
E	11.9	12.0	12.1
A_2	—	1.4	—
H_D	13.8	14.0	14.2
H_E	13.8	14.0	14.2
A	—	—	1.7
A_1	0	0.1	0.2
b_p	0.15	0.20	0.25
b_1	—	0.18	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	10°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
Z_D	—	1.25	—
Z_E	—	1.25	—
L	0.3	0.5	0.7
L_1	—	1.0	—

Figure H 80-Pin LQFP (PLQP0080KB-A)

Rev.	Date	Description	
		Page	Summary
1.30	Jan 22, 2013	11	Table 1.6 List of Products Chip Version C: D Version (Ta = -40 to +85°C), Table 1.7 List of Products Chip Version C: G Version (Ta = -40 to +105°C), changed
		12	Figure 1.1 How to Read the Product Part No., Memory Capacity, and Package Type, changed
		13	Figure 1.2 Block Diagram, changed
		14 to 17	Table 1.8 Pin Functions, changed
		18	Figure 1.3 Pin Assignments of the 145-Pin TFLGA (Upper Perspective View), added
		19	Figure 1.4 Pin Assignments of the 144-Pin LQFP, added
		25 to 28	Table 1.9 List of Pins and Pin Functions (145-Pin TFLGA), changed
		29 to 32	Table 1.10 List of Pins and Pin Functions (144-Pin LQFP), changed
		3. Address Space	
		48	Figure 3.1 Memory Map in Each Operating Mode, changed
		4. I/O Registers	
		52 to 81	Table 4.1 List of I/O Registers (Address Order, changed
		5. Electrical Characteristics	
		83	Table 5.2 DC Characteristics (1), Table 5.3 DC Characteristics (2), changed
		84 to 122	Table 5.6 DC Characteristics (5) to Table 5.20 DC Characteristics (19), changed Figure 5.1 Voltage Dependency in High-Speed .... for Chip Version A to Figure 5.34 Temperature Dependency in .... and 100 to 145 pins, changed
		158	Table 5.55 Timing of On-Chip Peripheral Modules (1), changed
		159	[512 Kbytes or less of flash memory and 48 to 100 pins] Table 5.56 Timing of On-Chip Peripheral Modules (2), added
		160, 161	[768 Kbytes/1 Mbyte of flash memory or 145/145 pins] Table 5.57 Timing of On-Chip Peripheral Modules (3), added
		162	Table 5.58 Timing of On-Chip Peripheral Modules (4), changed
		165	Figure 5.75 MTU/TPU Input/Output Timing, Figure 5.76 MTU/TPU Clock Input Timing, changed
		166	Figure 5.79 SCK Clock Input Timing, Figure 5.80 SCI Input/Output Timing: Clock Synchronous Mode, changed
		167	Figure 5.82 RSPI Clock Timing and Simple SPI Clock Timing, changed
		168	Figure 5.83 RSPI Timing (Master, CPHA = 0) .... and Simple SPI Timing (Master, CKPH = 1), Figure 5.84 RSPI Timing (Master, CPHA = 0) (Bit Rate: PCLKB Set to Divided by 2), changed
		169	Figure 5.85 RSPI Timing (Master, CPHA = 1) .... and Simple SPI Timing (Master, CKPH = 0), Figure 5.86 RSPI Timing (Master, CPHA = 1) (Bit Rate: PCLKB Set to Divided by 2), changed
		170	Figure 5.87 RSPI Timing (Slave, CPHA = 0) and Simple SPI Timing (Slave, CKPH = 1), Figure 5.88 RSPI Timing (Slave, CPHA = 1) and Simple SPI Timing (Slave, CKPH = 0), changed
		173	Table 5.64 A/D Conversion Characteristics (2), changed
		175	Figure 5.91 Illustration of A/D Converter Characteristic Terms, Absolute accuracy, changed
		184	Table 5.74 ROM (Flash Memory for Code Storage) Characteristics (1), changed
		189	Table 5.80 E2 DataFlash Characteristics (1), Table 5.81 E2 DataFlash Characteristics (2), changed
		Appendix 1. Package Dimensions	
		195	Figure A 145-Pin TFLGA (PTLG0145KA-A), added
		196	Figure B 144-Pin LQFP (PLQP0144KA-A), added
1.40	Feb 19, 2013	1. Overview	
		2 to 6	Table 1.1 Outline of Specifications, changed Note 2, added
		9	Table 1.4 List of Products Chip Version B: D Version (Ta = -40 to +85°C), changed
		10	Table 1.5 List of Products Chip Version B: G Version (Ta = -40 to +105°C), changed Note, added
		11	Table 1.6 List of Products Chip Version C: D Version (Ta = -40 to +85°C): Note 1, Table 1.7 List of Products Chip Version C: G Version (Ta = -40 to +105°C): Note 1 deleted, Note added
		12	Figure 1.1 How to Read the Product Part No., Memory Capacity, and Package Type, changed
		4. I/O Registers	
		58	Table 5.1 List of I/O Registers (Address Order), changed
		5. Electrical Characteristics	
		83	Table 5.4 DC Characteristics (3), changed
		88	Table 5.8 DC Characteristics (7), changed