Renesas Electronics America Inc - R5F52103BDFM#30 Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I²C, SCI, SPI
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	48
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	12K x 8
Voltage - Supply (Vcc/Vdd)	1.62V ~ 5.5V
Data Converters	A/D 12x12b; D/A 2x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LFQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f52103bdfm-30

Table 1.1 Outline of Specifications (5 / 5)

Classification	Module/Function	Description
Packages	Chip version A	100-pin TFLGA (PTLG0100JA-A) 7 × 7 mm, 0.65-mm pitch 100-pin LQFP (PLQP0100KB-A) 14 × 14 mm, 0.5-mm pitch 80-pin LQFP (PLQP0080KB-A) 12 × 12 mm, 0.5-mm pitch 64-pin LQFP (PLQP0064KB-A) 10 × 10 mm, 0.5-mm pitch
	Chip version B	145-pin TFLGA (PTLG0145KA-A) 7 × 7 mm, 0.5-mm pitch 100-pin TFLGA (PTLG0100JA-A) 7 × 7 mm, 0.65-mm pitch 100-pin TFLGA (PTLG0100KA-A) 5.5 × 5.5 mm, 0.5-mm pitch 64-pin TFLGA (PTLG0064JA-A) 6 × 6 mm, 0.65-mm pitch 144-pin LQFP (PLQP0144KA-A) 20 × 20 mm, 0.5-mm pitch 100-pin LQFP (PLQP0100KB-A) 14 × 14 mm, 0.5-mm pitch 80-pin LQFP (PLQP0080KB-A) 12 × 12 mm, 0.5-mm pitch 80-pin LQFP (PLQP0080JA-A) 14 × 14 mm, 0.65-mm pitch 64-pin LQFP (PLQP0064KB-A) 10 × 10 mm, 0.5-mm pitch 64-pin LQFP (PLQP0064GA-A) 14 × 14 mm, 0.8-mm pitch 48-pin LQFP (PLQP0048KB-A) 7 × 7 mm, 0.5-mm pitch 69-pin WLBGA (SWBG0069LA-A) 3.91 × 4.26mm, 0.40-mm pitch
	Chip version C	100-pin TFLGA (PTLG0100JA-A) 7 × 7 mm, 0.65-mm pitch 100-pin LQFP (PLQP0100KB-A) 14 × 14 mm, 0.5-mm pitch 80-pin LQFP (PLQP0080KB-A) 12 × 12 mm, 0.5-mm pitch 80-pin LQFP (PLQP0080JA-A) 14 × 14 mm, 0.65-mm pitch 64-pin LQFP (PLQP0064KB-A) 10 × 10 mm, 0.5-mm pitch 64-pin LQFP (PLQP0064GA-A) 14 × 14 mm, 0.8-mm pitch
On-chip debugging system		E1 emulator (FINE interface)

Note 1. In chip version A of the part numbers below, port P17 is not 5 V tolerant. Therefore there is only one port in these products.
R5F52108ADFM, R5F52107ADFM, R5F52106ADFM, and R5F52105ADFM

Note 2. Please contact Renesas Electronics sales office for derating of operation under Ta = +85°C to +105°C. Derating is the systematic reduction of load for the sake of improved reliability.

Table 1.5 List of Products Chip Version B: G Version (Ta = –40 to +105°C)

Group	Part No.	Orderable Part No.	Package	ROM Capacity	RAM Capacity	E2 DataFlash	Operating Frequency (Max.)	Operating Temperature
RX210	R5F5210BBGFB	R5F5210BBGFB#30	PLQP0144KA-A	1 Mbytes	96 Kbytes	8 Kbytes	50 MHz	–40 to +105°C
	R5F5210BBGFP	R5F5210BBGFP#30	PLQP0100KB-A					
	R5F5210ABGFB	R5F5210ABGFB#30	PLQP0144KA-A	768 Kbytes				
	R5F5210ABGFP	R5F5210ABGFP#30	PLQP0100KB-A					
	R5F52108BGFB	R5F52108BGFB#30	PLQP0144KA-A	512 Kbytes	64 Kbytes			
	R5F52107BGFB	R5F52107BGFB#30	PLQP0144KA-A	384 Kbytes				
	R5F52106BGFB	R5F52106BGFB#30	PLQP0144KA-A	256 Kbytes	32 Kbytes			
	R5F52106BGFP	R5F52106BGFP#30	PLQP0100KB-A					
	R5F52106BGFN	R5F52106BGFN#30	PLQP0080KB-A					
	R5F52106BGFM	R5F52106BGFM#30	PLQP0064KB-A					
	R5F52106BGFL	R5F52106BGFL#30	PLQP0048KB-A					
	R5F52106BGFF	R5F52106BGFF#V0	PTLG0100JA-A					
	R5F52106BGFK	R5F52106BGFK#30	PLQP0064GA-A					
	R5F52105BGFB	R5F52105BGFB#30	PLQP0144KA-A	128 Kbytes	20 Kbytes			
	R5F52105BGFP	R5F52105BGFP#30	PLQP0100KB-A					
	R5F52105BGFN	R5F52105BGFN#30	PLQP0080KB-A					
	R5F52105BGFM	R5F52105BGFM#30	PLQP0064KB-A					
	R5F52105BGFL	R5F52105BGFL#30	PLQP0048KB-A					
	R5F52105BGFF	R5F52105BGFF#V0	PLQP0080JA-A					
	R5F52105BGFK	R5F52105BGFK#30	PLQP0064GA-A					
	R5F52104BGFM	R5F52104BGFM#30	PLQP0064KB-A	96 Kbytes	16 Kbytes			
	R5F52104BGFL	R5F52104BGFL#30	PLQP0048KB-A					
	R5F52104BGFF	R5F52104BGFF#V0	PLQP0080JA-A					
	R5F52103BGFM	R5F52103BGFM#30	PLQP0064KB-A	64 Kbytes	12 Kbytes			
	R5F52103BGFL	R5F52103BGFL#30	PLQP0048KB-A					
	R5F52103BGFF	R5F52103BGFF#V0	PLQP0080JA-A					

Note: • Please contact Renesas Electronics sales office for derating of operation under Ta = +85°C to +105°C. Derating is the systematic reduction of load for the sake of improved reliability.

Note: • Orderable part numbers are current as of when this manual was published. Please make sure to refer to the relevant product page on the Renesas website for the latest part numbers.

Table 1.8 Pin Functions (4 / 4)

Classifications	Pin Name	I/O	Description
Analog power supply	AVCC0	Input	Analog voltage supply pin for the 12-bit A/D converter. Connect this pin to VCC if the 12-bit A/D converter is not to be used.
	AVSS0	Input	Analog ground pin for the 12-bit A/D converter. Connect this pin to VSS if the 12-bit A/D converter is not to be used.
	VREFH0	Input	Analog reference voltage supply pin for the 12-bit A/D converter. Connect this pin to VCC if the 12-bit A/D converter is not to be used.
	VREFL0	Input	Analog reference ground pin for the 12-bit A/D converter. Connect this pin to VSS if the 12-bit A/D converter is not to be used.
	VREFH	Input	Analog voltage supply pin for the D/A converter. Connect this pin to VCC if the D/A converter is not to be used.
	VREFL	Input	Analog ground pin for the D/A converter. Connect this pin to VSS if the D/A converter is not to be used.
I/O ports	P00 to P03, P05, P07	I/O	6-bit input/output pins.
	P12 to P17	I/O	6-bit input/output pins.
	P20 to P27	I/O	8-bit input/output pins.
	P30 to P37	I/O	8-bit input/output pins. (P35 input pin)
	P40 to P47	I/O	8-bit input/output pins.
	P50 to P56	I/O	7-bit input/output pins.
	P60 to P67	I/O	8-bit input/output pins.
	P70 to P77	I/O	8-bit input/output pins.
	P80 to P83, P86, P87	I/O	6-bit input/output pins.
	P90 to P93	I/O	4-bit input/output pins.
	PA0 to PA7	I/O	8-bit input/output pins.
	PB0 to PB7	I/O	8-bit input/output pins.
	PC0 to PC7	I/O	8-bit input/output pins.
	PD0 to PD7	I/O	8-bit input/output pins.
	PE0 to PE7	I/O	8-bit input/output pins.
	PF5	I/O	1-bit input/output pin.
	PH0 to PH3	I/O	4-bit input/output pins.
	PJ1, PJ3, PJ5	I/O	3-bit input/output pins.
	PK2 to PK5	I/O	4-bit input/output pins.
	PL0, PL1	I/O	2-bit input/output pins.

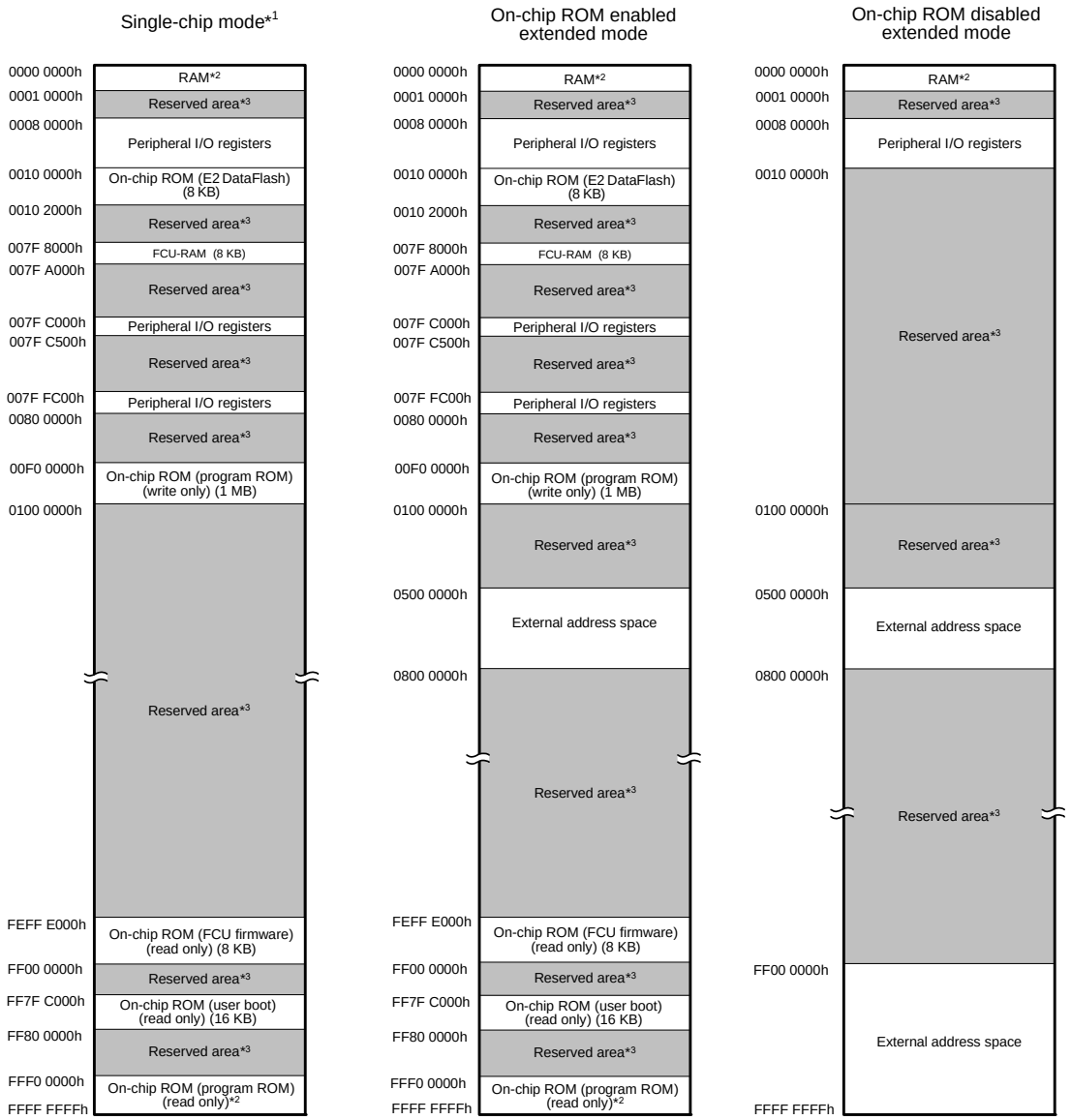
Table 1.12 List of Pins and Pin Functions (100-Pin LQFP) (2 / 3)

Pin No.	Power Supply, Clock, System Control	I/O Port	External Bus	Timers (MTU, TMR, POE)	Communications (SCIc, SCId, RSPI, RIIC)	Others
42		P52	RD#			
43		P51	WR1#/BC1#/WAIT#			
44		P50	WR0#/WR#			
45		PC7	A23/CS0#	MTIOC3A/TMO2/ MTCLKB	TXD8/SMOSI8/SSDA8/ MISOA	CACREF
46		PC6	A22/CS1#	MTIOC3C/MTCLKA/ TMCI2	RXD8/SMISO8/SSCL8/ MOSIA	
47		PC5	A21/CS2#/WAIT#	MTIOC3B/MTCLKD/ TMRI2	SCK8/RSPCKA	
48		PC4	A20/CS3#	MTIOC3D/MTCLKC/ TMCI1/POE0#	SCK5/CTS8#/RTS8#/ SS8#/SSLA0	
49		PC3	A19	MTIOC4D	TXD5/SMOSI5/SSDA5	
50		PC2	A18	MTIOC4B	RXD5/SMISO5/SSCL5/ SSLA3	
51		PC1	A17	MTIOC3A	SCK5/SSLA2	
52		PC0	A16	MTIOC3C	CTS5#/RTS5#/SS5#/ SSLA1	
53		PB7	A15	MTIOC3B	TXD9/SMOSI9/SSDA9	
54		PB6	A14	MTIOC3D	RXD9/SMISO9/SSCL9	
55		PB5	A13	MTIOC2A/MTIOC1B/ TMRI1/POE1#	SCK9	
56		PB4	A12		CTS9#/RTS9#/SS9#	
57		PB3	A11	MTIOC0A/MTIOC4A/ TMO0/POE3#	SCK6	
58		PB2	A10		CTS6#/RTS6#/SS6#	
59		PB1	A9	MTIOC0C/MTIOC4C/ TMCI0	TXD6/SMOSI6/SSDA6	IRQ4-DS
60	VCC					
61		PB0	A8	MTIC5W	RXD6/SMISO6/SSCL6/ RSPCKA	
62	VSS					
63		PA7	A7		MISOA	
64		PA6	A6	MTIC5V/MTCLKB/ TMCI3/POE2#	CTS5#/RTS5#/SS5#/ MOSIA	
65		PA5	A5		RSPCKA	
66		PA4	A4	MTIC5U/MTCLKA/ TMRI0	TXD5/SMOSI5/SSDA5/ SSLA0	IRQ5-DS/CVREFB1
67		PA3	A3	MTIOC0D/MTCLKD	RXD5/SMISO5/SSCL5	IRQ6-DS/CMPB1
68		PA2	A2		RXD5/SMISO5/SSCL5/ SSLA3	
69		PA1	A1	MTIOC0B/MTCLKC	SCK5/SSLA2	CVREFA
70		PA0	A0/BC0#	MTIOC4A	SSLA1	CACREF
71		PE7	D15[A15/D15]			IRQ7/AN015
72		PE6	D14[A14/D14]			IRQ6/AN014
73		PE5	D13[A13/D13]	MTIOC4C/MTIOC2B		IRQ5/AN013
74		PE4	D12[A12/D12]	MTIOC4D/MTIOC1A		AN012/CMPA2
75		PE3	D11[A11/D11]	MTIOC4B/POE8#	CTS12#/RTS12#/SS12#	AN011/CMPA1
76		PE2	D10[A10/D10]	MTIOC4A	RXD12/RXDX12/ SMISO12/SSCL12	IRQ7-DS/AN010/ CVREFB0
77		PE1	D9[A9/D9]	MTIOC4C	TXD12/TXDX12/SIOX12/ SMOSI12/SSDA12	AN009/CMPB0
78		PE0	D8[A8/D8]		SCK12	AN008
79		PD7	D7[A7/D7]	MTIC5U/POE0#		IRQ7

Table 1.16 List of Pins and Pin Functions (64-Pin LQFP) (2 / 2)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (MTU, TMR, POE)	Communication (SCIc, SCId, RSPI, RIIC)	Others
44		PA1	MTIOC0B/MTCLKC	SCK5/SSLA2	CVREFA
45		PA0	MTIOC4A	SSLA1	CACREF
46		PE5	MTIOC4C/MTIOC2B		IRQ5/AN013
47		PE4	MTIOC4D/MTIOC1A		AN012/CMPA2
48		PE3	MTIOC4B/POE8#	CTS12#/RTS12#/SS12#	AN011/CMPA1
49		PE2	MTIOC4A	RXD12/RXDX12/SMISO12/ SSCL12	IRQ7-DS/AN010/ CVREFB0
50		PE1	MTIOC4C	TXD12/TXDX12/SIOX12/ SMOSI12/SSDA12	AN009/CMPB0
51		PE0		SCK12	AN008
52	VREFL				
53		P46			AN006
54	VREFH				
55		P44			AN004
56		P43			AN003
57		P42			AN002
58		P41			AN001
59	VREFL0				
60		P40			AN000
61	VREFH0				
62	AVCC0				
63		P05			DA1
64	AVSS0				

Note: • Pin names to which –DS is appended are for pins that can be used to trigger release from deep software standby mode.



Note 1. The address space in boot mode and user boot mode is the same as the address space in single-chip mode.
Note 2. The capacity of ROM/RAM differs depending on the products.

ROM (bytes)		RAM (bytes)	
Capacity	**Address**	**Capacity**	**Address**
1 M	FFF0 0000h to FFFF FFFFh	96 K	0000 0000h to 0001 7FFFh
768 K	FFF4 0000h to FFFF FFFFh		
512 K	FFF8 0000h to FFFF FFFFh	64 K	0000 0000h to 0000 FFFFh
384 K	FFFA 0000h to FFFF FFFFh		
256 K	FFFC 0000h to FFFF FFFFh	32 K	0000 0000h to 0000 7FFFh
128 K	FFFE 0000h to FFFF FFFFh	20 K	0000 0000h to 0000 4FFFh
96 K	FFFE 8000h to FFFF FFFFh	16 K	0000 0000h to 0000 3FFFh
64 K	FFFF 0000h to FFFF FFFFh	12 K	0000 0000h to 0000 2FFFh

Note:•See Table 1.3 to Table 1.7 List of Products, for the product type name.

Note 3. Reserved areas should not be accessed.

Figure 3.1 Memory Map in Each Operating Mode

Table 4.1 List of I/O Registers (Address Order) (2 / 29)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles ICLK ≥ PCLK	Number of Access Cycles ICLK < PCLK
0008 201Dh	DMAC0	DMA software start register	DMREQ	8	8	2 ICLK	
0008 201Eh	DMAC0	DMA status register	DMSTS	8	8	2 ICLK	
0008 201Fh	DMAC0	DMA activation source flag control register	DMCSL	8	8	2 ICLK	
0008 2040h	DMAC1	DMA source address register	DMSAR	32	32	2 ICLK	
0008 2044h	DMAC1	DMA destination address register	DMDAR	32	32	2 ICLK	
0008 2048h	DMAC1	DMA transfer count register	DMCRA	32	32	2 ICLK	
0008 204Ch	DMAC1	DMA block transfer count register	DMCRB	16	16	2 ICLK	
0008 2050h	DMAC1	DMA transfer mode register	DMTMD	16	16	2 ICLK	
0008 2053h	DMAC1	DMA interrupt setting register	DMINT	8	8	2 ICLK	
0008 2054h	DMAC1	DMA address mode register	DMAMD	16	16	2 ICLK	
0008 205Ch	DMAC1	DMA transfer enable register	DMCNT	8	8	2 ICLK	
0008 205Dh	DMAC1	DMA software start register	DMREQ	8	8	2 ICLK	
0008 205Eh	DMAC1	DMA status register	DMSTS	8	8	2 ICLK	
0008 205Fh	DMAC1	DMA activation source flag control register	DMCSL	8	8	2 ICLK	
0008 2080h	DMAC2	DMA source address register	DMSAR	32	32	2 ICLK	
0008 2084h	DMAC2	DMA destination address register	DMDAR	32	32	2 ICLK	
0008 2088h	DMAC2	DMA transfer count register	DMCRA	32	32	2 ICLK	
0008 208Ch	DMAC2	DMA block transfer count register	DMCRB	16	16	2 ICLK	
0008 2090h	DMAC2	DMA transfer mode register	DMTMD	16	16	2 ICLK	
0008 2093h	DMAC2	DMA interrupt setting register	DMINT	8	8	2 ICLK	
0008 2094h	DMAC2	DMA address mode register	DMAMD	16	16	2 ICLK	
0008 209Ch	DMAC2	DMA transfer enable register	DMCNT	8	8	2 ICLK	
0008 209Dh	DMAC2	DMA software start register	DMREQ	8	8	2 ICLK	
0008 209Eh	DMAC2	DMA status register	DMSTS	8	8	2 ICLK	
0008 209Fh	DMAC2	DMA activation source flag control register	DMCSL	8	8	2 ICLK	
0008 20C0h	DMAC3	DMA source address register	DMSAR	32	32	2 ICLK	
0008 20C4h	DMAC3	DMA destination address register	DMDAR	32	32	2 ICLK	
0008 20C8h	DMAC3	DMA transfer count register	DMCRA	32	32	2 ICLK	
0008 20CCh	DMAC3	DMA block transfer count register	DMCRB	16	16	2 ICLK	
0008 20D0h	DMAC3	DMA transfer mode register	DMTMD	16	16	2 ICLK	
0008 20D3h	DMAC3	DMA interrupt setting register	DMINT	8	8	2 ICLK	
0008 20D4h	DMAC3	DMA address mode register	DMAMD	16	16	2 ICLK	
0008 20DCh	DMAC3	DMA transfer enable register	DMCNT	8	8	2 ICLK	
0008 20DDh	DMAC3	DMA software start register	DMREQ	8	8	2 ICLK	
0008 20DEh	DMAC3	DMA status register	DMSTS	8	8	2 ICLK	
0008 20DFh	DMAC3	DMA activation source flag control register	DMCSL	8	8	2 ICLK	
0008 2200h	DMAC	DMA module activation register	DMAST	8	8	2 ICLK	
0008 2400h	DTC	DTC control register	DTCCR	8	8	2 ICLK	
0008 2404h	DTC	DTC vector base register	DTCVBR	32	32	2 ICLK	
0008 2408h	DTC	DTC address mode register	DTCADMOD	8	8	2 ICLK	
0008 240Ch	DTC	DTC module start register	DTCST	8	8	2 ICLK	
0008 240Eh	DTC	DTC status register	DTCSTS	16	16	2 ICLK	
0008 3002h	BSC	CS0 mode register	CS0MOD	16	16	1, 2 BCLK	
0008 3004h	BSC	CS0 wait control register 1	CS0WCR1	32	32	1, 2 BCLK	
0008 3008h	BSC	CS0 wait control register 2	CS0WCR2	32	32	1, 2 BCLK	
0008 3012h	BSC	CS1 mode register	CS1MOD	16	16	1, 2 BCLK	
0008 3014h	BSC	CS1 wait control register 1	CS1WCR1	32	32	1, 2 BCLK	
0008 3018h	BSC	CS1 wait control register 2	CS1WCR2	32	32	1, 2 BCLK	
0008 3022h	BSC	CS2 mode register	CS2MOD	16	16	1, 2 BCLK	
0008 3024h	BSC	CS2 wait control register 1	CS2WCR1	32	32	1, 2 BCLK	
0008 3028h	BSC	CS2 wait control register 2	CS2WCR2	32	32	1, 2 BCLK	

Table 4.1 List of I/O Registers (Address Order) (3 / 29)

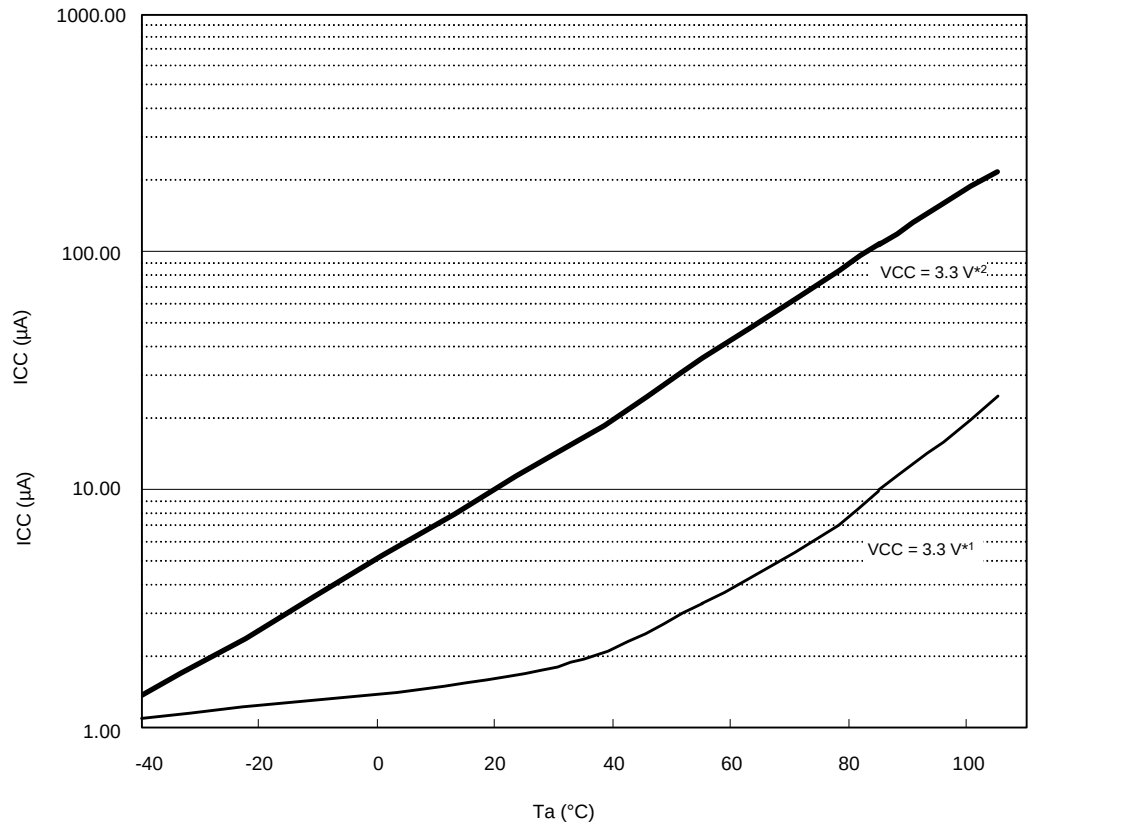
Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles ICLK ≥ PCLK	Number of Access Cycles ICLK < PCLK
0008 3032h	BSC	CS3 mode register	CS3MOD	16	16	1, 2 BCLK	
0008 3034h	BSC	CS3 wait control register 1	CS3WCR1	32	32	1, 2 BCLK	
0008 3038h	BSC	CS3 wait control register 2	CS3WCR2	32	32	1, 2 BCLK	
0008 3802h	BSC	CS0 control register	CS0CR	16	16	1, 2 BCLK	
0008 380Ah	BSC	CS0 recovery cycle register	CS0REC	16	16	1, 2 BCLK	
0008 3812h	BSC	CS1 control register	CS1CR	16	16	1, 2 BCLK	
0008 381Ah	BSC	CS1 recovery cycle register	CS1REC	16	16	1, 2 BCLK	
0008 3822h	BSC	CS2 control register	CS2CR	16	16	1, 2 BCLK	
0008 382Ah	BSC	CS2 recovery cycle register	CS2REC	16	16	1, 2 BCLK	
0008 3832h	BSC	CS3 control register	CS3CR	16	16	1, 2 BCLK	
0008 383Ah	BSC	CS3 recovery cycle register	CS3REC	16	16	1, 2 BCLK	
0008 3880h	BSC	CS recovery cycle insertion enable register	CSRECEN	16	16	1, 2 BCLK	
0008 7010h	ICU	Interrupt request register 016	IR016	8	8	2 ICLK	
0008 7015h	ICU	Interrupt request register 021	IR021	8	8	2 ICLK	
0008 7017h	ICU	Interrupt request register 023	IR023	8	8	2 ICLK	
0008 701Bh	ICU	Interrupt request register 027	IR027	8	8	2 ICLK	
0008 701Ch	ICU	Interrupt request register 028	IR028	8	8	2 ICLK	
0008 701Dh	ICU	Interrupt request register 029	IR029	8	8	2 ICLK	
0008 701Eh	ICU	Interrupt request register 030	IR030	8	8	2 ICLK	
0008 701Fh	ICU	Interrupt request register 031	IR031	8	8	2 ICLK	
0008 7020h	ICU	Interrupt request register 032	IR032	8	8	2 ICLK	
0008 7021h	ICU	Interrupt request register 033	IR033	8	8	2 ICLK	
0008 7022h	ICU	Interrupt request register 034	IR034	8	8	2 ICLK	
0008 702Ch	ICU	Interrupt request register 044	IR044	8	8	2 ICLK	
0008 702Dh	ICU	Interrupt request register 045	IR045	8	8	2 ICLK	
0008 702Eh	ICU	Interrupt request register 046	IR046	8	8	2 ICLK	
0008 702Fh	ICU	Interrupt request register 047	IR047	8	8	2 ICLK	
0008 7039h	ICU	Interrupt request register 057	IR057	8	8	2 ICLK	
0008 703Ah	ICU	Interrupt request register 058	IR058	8	8	2 ICLK	
0008 703Bh	ICU	Interrupt request register 059	IR059	8	8	2 ICLK	
0008 703Fh	ICU	Interrupt request register 063	IR063	8	8	2 ICLK	
0008 7040h	ICU	Interrupt request register 064	IR064	8	8	2 ICLK	
0008 7041h	ICU	Interrupt request register 065	IR065	8	8	2 ICLK	
0008 7042h	ICU	Interrupt request register 066	IR066	8	8	2 ICLK	
0008 7043h	ICU	Interrupt request register 067	IR067	8	8	2 ICLK	
0008 7044h	ICU	Interrupt request register 068	IR068	8	8	2 ICLK	
0008 7045h	ICU	Interrupt request register 069	IR069	8	8	2 ICLK	
0008 7046h	ICU	Interrupt request register 070	IR070	8	8	2 ICLK	
0008 7047h	ICU	Interrupt request register 071	IR071	8	8	2 ICLK	
0008 7058h	ICU	Interrupt request register 088	IR088	8	8	2 ICLK	
0008 7059h	ICU	Interrupt request register 089	IR089	8	8	2 ICLK	
0008 705Ch	ICU	Interrupt request register 092	IR092	8	8	2 ICLK	
0008 705Dh	ICU	Interrupt request register 093	IR093	8	8	2 ICLK	
0008 7066h	ICU	Interrupt request register 102	IR102	8	8	2 ICLK	
0008 7067h	ICU	Interrupt request register 103	IR103	8	8	2 ICLK	
0008 706Ah	ICU	Interrupt request register 106	IR106	8	8	2 ICLK	
0008 706Bh	ICU	Interrupt request register 107	IR107	8	8	2 ICLK	
0008 7072h	ICU	Interrupt request register 114	IR114	8	8	2 ICLK	
0008 7073h	ICU	Interrupt request register 115	IR115	8	8	2 ICLK	
0008 7074h	ICU	Interrupt request register 116	IR116	8	8	2 ICLK	
0008 7075h	ICU	Interrupt request register 117	IR117	8	8	2 ICLK	

Table 4.1 List of I/O Registers (Address Order) (4 / 29)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles ICLK ≥ PCLK	Number of Access Cycles ICLK < PCLK
0008 7076h	ICU	Interrupt request register 118	IR118	8	8		2 ICLK
0008 7077h	ICU	Interrupt request register 119	IR119	8	8		2 ICLK
0008 7078h	ICU	Interrupt request register 120	IR120	8	8		2 ICLK
0008 7079h	ICU	Interrupt request register 121	IR121	8	8		2 ICLK
0008 707Ah	ICU	Interrupt request register 122	IR122	8	8		2 ICLK
0008 707Bh	ICU	Interrupt request register 123	IR123	8	8		2 ICLK
0008 707Ch	ICU	Interrupt request register 124	IR124	8	8		2 ICLK
0008 707Dh	ICU	Interrupt request register 125	IR125	8	8		2 ICLK
0008 707Eh	ICU	Interrupt request register 126	IR126	8	8		2 ICLK
0008 707Fh	ICU	Interrupt request register 127	IR127	8	8		2 ICLK
0008 7080h	ICU	Interrupt request register 128	IR128	8	8		2 ICLK
0008 7081h	ICU	Interrupt request register 129	IR129	8	8		2 ICLK
0008 7082h	ICU	Interrupt request register 130	IR130	8	8		2 ICLK
0008 7083h	ICU	Interrupt request register 131	IR131	8	8		2 ICLK
0008 7084h	ICU	Interrupt request register 132	IR132	8	8		2 ICLK
0008 7085h	ICU	Interrupt request register 133	IR133	8	8		2 ICLK
0008 7086h	ICU	Interrupt request register 134	IR134	8	8		2 ICLK
0008 7087h	ICU	Interrupt request register 135	IR135	8	8		2 ICLK
0008 7088h	ICU	Interrupt request register 136	IR136	8	8		2 ICLK
0008 7089h	ICU	Interrupt request register 137	IR137	8	8		2 ICLK
0008 708Ah	ICU	Interrupt request register 138	IR138	8	8		2 ICLK
0008 708Bh	ICU	Interrupt request register 139	IR139	8	8		2 ICLK
0008 708Ch	ICU	Interrupt request register 140	IR140	8	8		2 ICLK
0008 708Dh	ICU	Interrupt request register 141	IR141	8	8		2 ICLK
0008 708Eh	ICU	Interrupt request register 142	IR142	8	8		2 ICLK
0008 708Fh	ICU	Interrupt request register 143	IR143	8	8		2 ICLK
0008 7090h	ICU	Interrupt request register 144	IR144	8	8		2 ICLK
0008 7091h	ICU	Interrupt request register 145	IR145	8	8		2 ICLK
0008 7092h	ICU	Interrupt request register 146	IR146	8	8		2 ICLK
0008 7093h	ICU	Interrupt request register 147	IR147	8	8		2 ICLK
0008 7094h	ICU	Interrupt request register 148	IR148	8	8		2 ICLK
0008 7095h	ICU	Interrupt request register 149	IR149	8	8		2 ICLK
0008 7096h	ICU	Interrupt request register 150	IR150	8	8		2 ICLK
0008 7097h	ICU	Interrupt request register 151	IR151	8	8		2 ICLK
0008 7098h	ICU	Interrupt request register 152	IR152	8	8		2 ICLK
0008 7099h	ICU	Interrupt request register 153	IR153	8	8		2 ICLK
0008 709Ah	ICU	Interrupt request register 154	IR154	8	8		2 ICLK
0008 709Bh	ICU	Interrupt request register 155	IR155	8	8		2 ICLK
0008 709Ch	ICU	Interrupt request register 156	IR156	8	8		2 ICLK
0008 709Dh	ICU	Interrupt request register 157	IR157	8	8		2 ICLK
0008 709Eh	ICU	Interrupt request register 158	IR158	8	8		2 ICLK
0008 709Fh	ICU	Interrupt request register 159	IR159	8	8		2 ICLK
0008 70A0h	ICU	Interrupt request register 160	IR160	8	8		2 ICLK
0008 70A1h	ICU	Interrupt request register 161	IR161	8	8		2 ICLK
0008 70A2h	ICU	Interrupt request register 162	IR162	8	8		2 ICLK
0008 70A3h	ICU	Interrupt request register 163	IR163	8	8		2 ICLK
0008 70A4h	ICU	Interrupt request register 164	IR164	8	8		2 ICLK
0008 70A5h	ICU	Interrupt request register 165	IR165	8	8		2 ICLK
0008 70A6h	ICU	Interrupt request register 166	IR166	8	8		2 ICLK
0008 70A7h	ICU	Interrupt request register 167	IR167	8	8		2 ICLK
0008 70AAh	ICU	Interrupt request register 170	IR170	8	8		2 ICLK

Table 4.1 List of I/O Registers (Address Order) (28 / 29)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles: ICLK ≥ PCLK	Number of Access Cycles: ICLK < PCLK
0008 C1B0h	MPC	PE0 pin function control register	PE0PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C1B1h	MPC	PE1 pin function control register	PE1PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C1B2h	MPC	PE2 pin function control register	PE2PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C1B3h	MPC	PE3 pin function control register	PE3PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C1B4h	MPC	PE4 pin function control register	PE4PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C1B5h	MPC	PE5 pin function control register	PE5PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C1B6h	MPC	PE6 pin function control register	PE6PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C1B7h	MPC	PE7 pin function control register	PE7PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C1BDh	MPC	PF5 pin function control register	PF5PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C1C8h	MPC	PH0 pin function control register	PH0PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C1C9h	MPC	PH1 pin function control register	PH1PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C1CAh	MPC	PH2 pin function control register	PH2PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C1CBh	MPC	PH3 pin function control register	PH3PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C1D1h	MPC	PJ1 pin function control register	PJ1PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C1D3h	MPC	PJ3 pin function control register	PJ3PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C1DAh	MPC	PK2 pin function control register	PK2PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C1DBh	MPC	PK3 pin function control register	PK3PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C1DCh	MPC	PK4 pin function control register	PK4PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C1DDh	MPC	PK5 pin function control register	PK5PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C280h	SYSTEM	Deep standby control register	DPSBYCR	8	8	4, 5 PCLKB	2, 3 ICLK
0008 C282h	SYSTEM	Deep standby interrupt enable register 0	DPSIER0	8	8	4, 5 PCLKB	2, 3 ICLK
0008 C284h	SYSTEM	Deep standby interrupt enable register 2	DPSIER2	8	8	4, 5 PCLKB	2, 3 ICLK
0008 C286h	SYSTEM	Deep standby interrupt flag register 0	DPSIFR0	8	8	4, 5 PCLKB	2, 3 ICLK
0008 C288h	SYSTEM	Deep standby interrupt flag register 2	DPSIFR2	8	8	4, 5 PCLKB	2, 3 ICLK
0008 C28Ah	SYSTEM	Deep standby interrupt edge register 0	DPSIEGR0	8	8	4, 5 PCLKB	2, 3 ICLK
0008 C28Ch	SYSTEM	Deep standby interrupt edge register 2	DPSIEGR2	8	8	4, 5 PCLKB	2, 3 ICLK
0008 C28Fh	SYSTEM	Flash HOCO software standby control register	FHSSBYCR	8	8	4, 5 PCLKB	2, 3 ICLK
0008 C290h	SYSTEM	Reset status register 0	RSTSR0	8	8	4, 5 PCLKB	2, 3 ICLK
0008 C291h	SYSTEM	Reset status register 1	RSTSR1	8	8	4, 5 PCLKB	2, 3 ICLK
0008 C293h	SYSTEM	Main clock oscillator forced oscillation control register	MOFCR	8	8	4, 5 PCLKB	2, 3 ICLK
0008 C294h	SYSTEM	High-speed clock oscillator power supply control register	HOCOPCR	8	8	4, 5 PCLKB	2, 3 ICLK
0008 C295h	SYSTEM	PLL power control register	PLLPCR	8	8	4, 5 PCLKB	2, 3 ICLK
0008 C296h	FLASH	Flash write erase protection register	FWEPROR	8	8	4, 5 PCLKB	2, 3 ICLK
0008 C297h	SYSTEM	Voltage monitoring circuit/comparator A control register	LVCMPCR	8	8	4, 5 PCLKB	2, 3 ICLK
0008 C298h	SYSTEM	Voltage detection level select register	LVDLVLR	8	8	4, 5 PCLKB	2, 3 ICLK
0008 C29Ah	SYSTEM	Voltage monitoring 1 circuit/comparator A1 control register 0	LVD1CR0	8	8	4, 5 PCLKB	2, 3 ICLK
0008 C29Bh	SYSTEM	Voltage monitoring 2 circuit/comparator A2 control register 0	LVD2CR0	8	8	4, 5 PCLKB	2, 3 ICLK
0008 C2A0h to 0008 C2BFh	SYSTEM	Deep standby backup register 0 to 31	DPSBKR0 to DPSBKR31	8	8	4, 5 PCLKB	2, 3 ICLK
0008 C400h	RTC	64-Hz counter	R64CNT	8	8	2, 3 PCLKB	2 ICLK
0008 C402h	RTC	Second counter	RSECCNT	8	8	2, 3 PCLKB	2 ICLK
0008 C404h	RTC	Minute counter	RMINCNT	8	8	2, 3 PCLKB	2 ICLK
0008 C406h	RTC	Hour counter	RHRCNT	8	8	2, 3 PCLKB	2 ICLK
0008 C408h	RTC	Day-of-week counter	RWKCNT	8	8	2, 3 PCLKB	2 ICLK
0008 C40Ah	RTC	Date counter	RDAYCNT	8	8	2, 3 PCLKB	2 ICLK
0008 C40Ch	RTC	Month counter	RMONCNT	8	8	2, 3 PCLKB	2 ICLK
0008 C40Eh	RTC	Year counter	RYRCNT	16	16	2, 3 PCLKB	2 ICLK
0008 C410h	RTC	Second alarm register	RSECAR	8	8	2, 3 PCLKB	2 ICLK
0008 C412h	RTC	Minute alarm register	RMINAR	8	8	2, 3 PCLKB	2 ICLK
0008 C414h	RTC	Hour alarm register	RHRAR	8	8	2, 3 PCLKB	2 ICLK
0008 C416h	RTC	Day-of-week alarm register	RWKAR	8	8	2, 3 PCLKB	2 ICLK
0008 C418h	RTC	Date alarm register	RDAYAR	8	8	2, 3 PCLKB	2 ICLK



Note 1. Average value of the tested middle samples during product evaluation.
Note 2. Average value of the tested upper-limit samples during product evaluation.

Figure 5.32 Temperature Dependency in Software Standby Mode (SOFTCUT[2:0] Bits = 110b) (Reference Data) for Chip Version B with 768 Kbytes/1 Mbyte of Flash Memory and 100 to 145 Pins

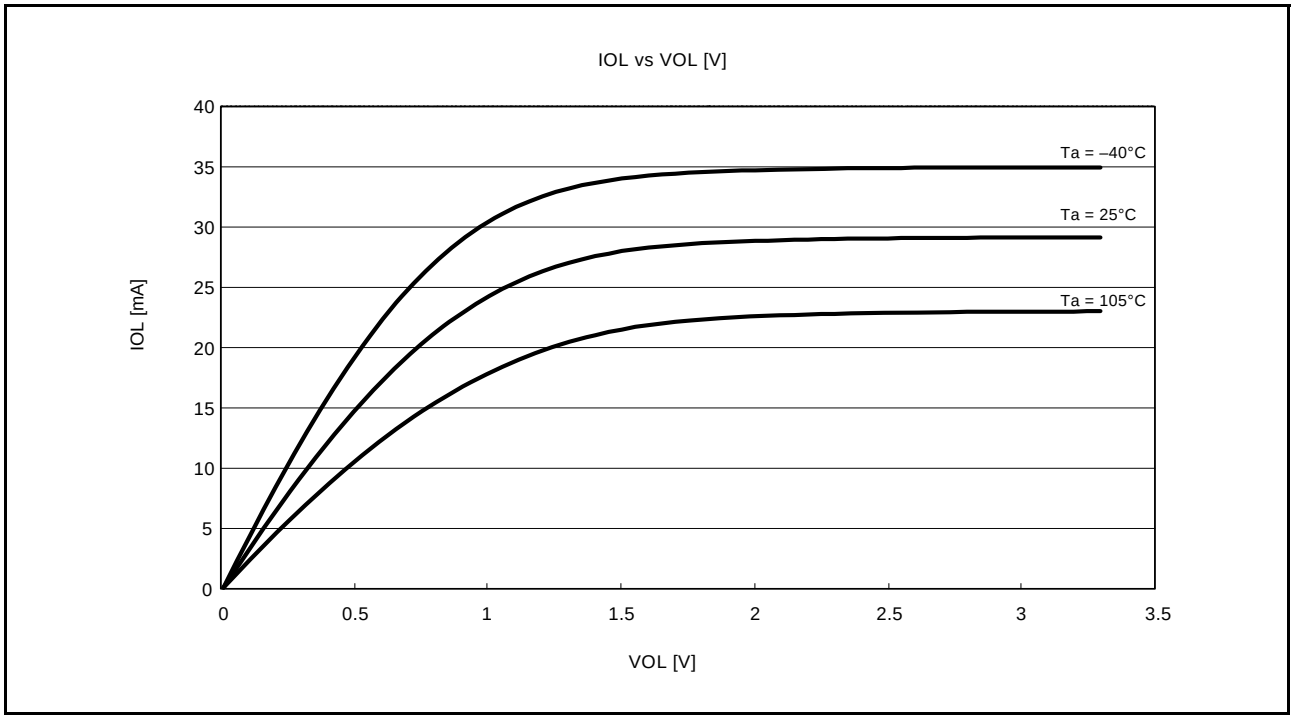


Figure 5.57 VOL and IOL Temperature Characteristics of RIIC Output Pin at VCC = 3.3 V (Reference Data)

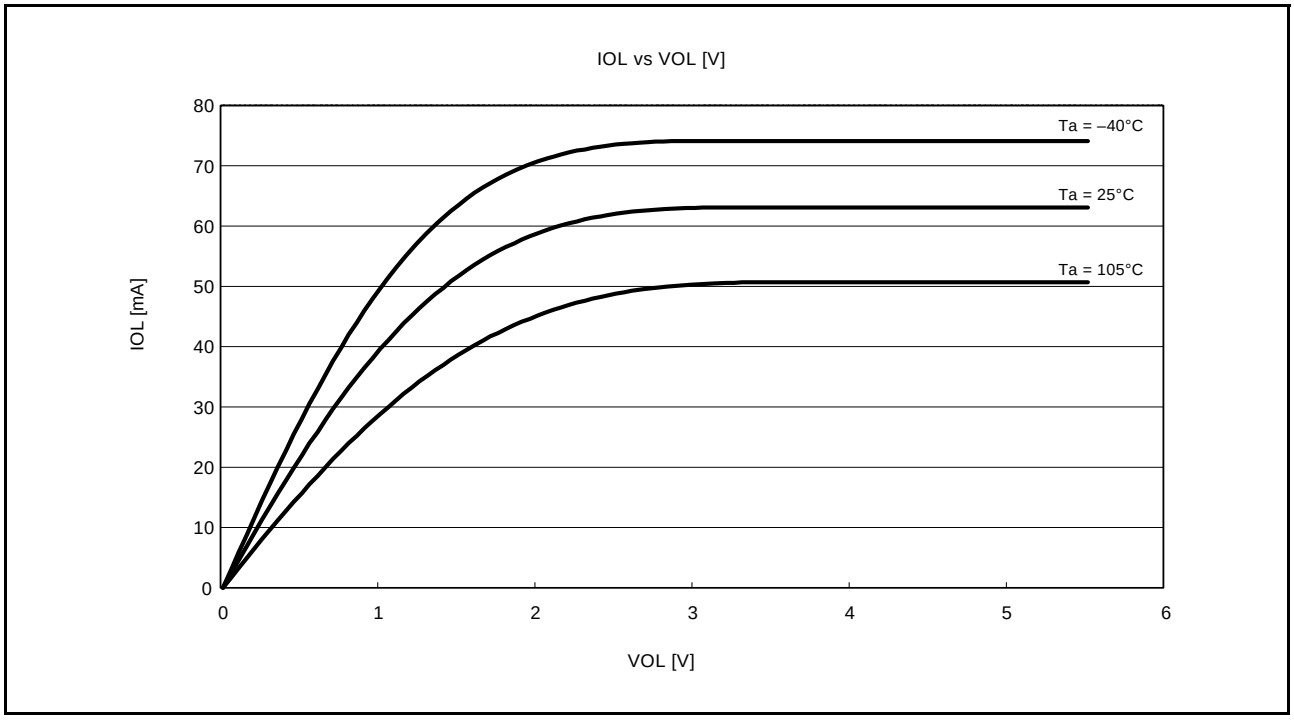


Figure 5.58 VOL and IOL Temperature Characteristics of RIIC Output Pin at VCC = 5.5 V (Reference Data)

5.3.1 Clock Timing

Table 5.41 BCLK Timing (1)

Conditions: VCC = AVCC0 = 2.7 to 5.5 V, VSS = AVSS0 = VREFL = VREFL0 = 0 V,
fBCLK = up to 25 MHz (BCLK pin output frequency = up to 12.5 MHz), T_a = –40 to +105°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
BCLK pin output cycle time	t_{Bcyc}	80	—	—	ns	Figure 5.59
BCLK pin output high pulse width*1	t_{CH}	20	—	—	ns	
BCLK pin output low pulse width*1	t_{CL}	20	—	—	ns	
BCLK pin output rising time	t_{Cr}	—	—	15	ns	
BCLK pin output falling time	t_{Cf}	—	—	15	ns	

Note 1. When the EXTAL external clock input is used with divided by 1 (SCKCR.BCK[3:0] bits = 0000b and BCKCR.BCLKDIV bit = 0) to output from the BCLK pin, the above should be satisfied with a duty cycle of 45 to 55%.

Table 5.42 BCLK Timing (2)

Conditions: VCC = AVCC0 = 1.8 to 2.7 V, VSS = AVSS0 = VREFL = VREFL0 = 0 V,
fBCLK = up to 16 MHz (BCLK pin output frequency= up to 8 MHz), T_a = –40 to +105°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
BCLK pin output cycle time	t_{Bcyc}	125	—	—	ns	Figure 5.59
BCLK pin output high pulse width*1	t_{CH}	30	—	—	ns	
BCLK pin output low pulse width*1	t_{CL}	30	—	—	ns	
BCLK pin output rising time	t_{Cr}	—	—	25	ns	
BCLK pin output falling time	t_{Cf}	—	—	25	ns	

Note 1. When the EXTAL external clock input is used with divided by 1 (SCKCR.BCK[3:0] bits = 0000b and BCKCR.BCLKDIV bit = 0) to output from the BCLK pin, the above should be satisfied with a duty cycle of 45 to 55%.

Table 5.43 BCLK Timing (3)

Conditions: VCC = AVCC0 = 1.62 to 1.8 V, VSS = AVSS0 = VREFL=VREFL0 = 0 V,
fBCLK = up to 12 MHz (BCLK pin output frequency = up to 6 MHz), T_a = –40 to +105°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
BCLK pin output cycle time	t_{Bcyc}	166.6	—	—	ns	Figure 5.59
BCLK pin output high pulse width*1	t_{CH}	42	—	—	ns	
BCLK pin output low pulse width*1	t_{CL}	42	—	—	ns	
BCLK pin output rising time	t_{Cr}	—	—	35	ns	
BCLK pin output falling time	t_{Cf}	—	—	35	ns	

Note: • Set high driving ability for the output port pin to be used for the BCLK pin function.
Note 1. When the EXTAL external clock input is used with divided by 1 (SCKCR.BCK[3:0] bits = 0000b and BCKCR.BCLKDIV bit = 0) to output from the BCLK pin, the above should be satisfied with a duty cycle of 45 to 55%.

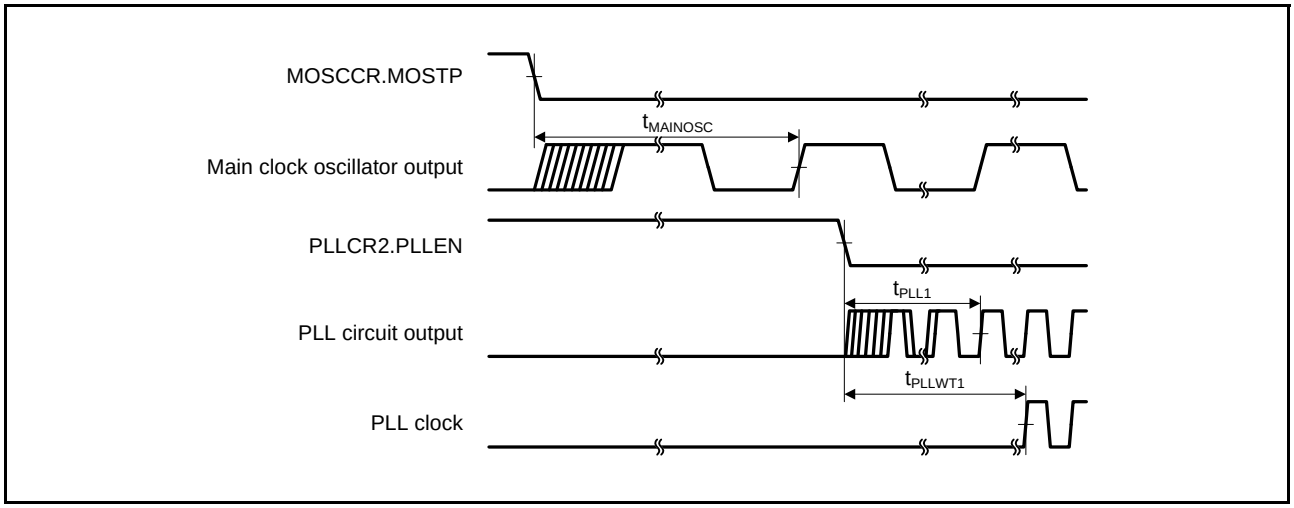


Figure 5.66 PLL Clock Oscillation Start Timing (PLL is Operated after Main Clock Oscillation Has Settled)

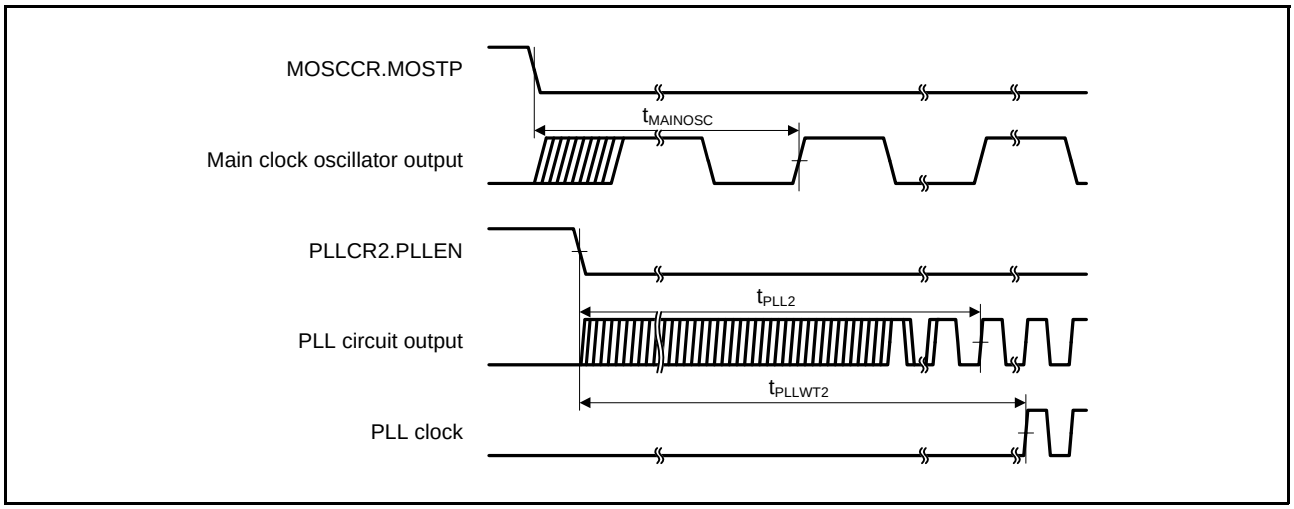


Figure 5.67 PLL Clock Oscillation Start Timing (PLL is Operated before Main Clock Oscillation Has Settled)

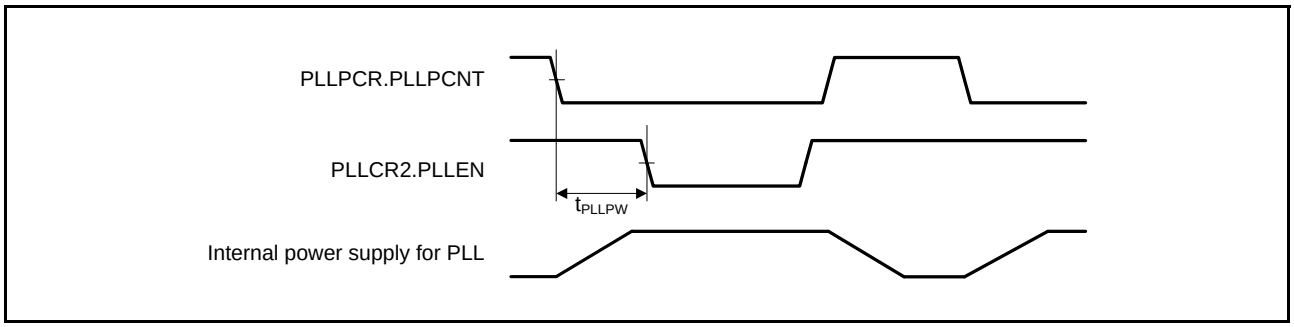


Figure 5.68 PLL Power Control Timing

5.3.6 Timing of On-Chip Peripheral Modules

Table 5.55 Timing of On-Chip Peripheral Modules (1)

Conditions: VCC = AVCC0 = 1.62 to 5.5 V, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +105°C
When high-drive output is selected by the drive capacity register

Item				Symbol	Min.	Max.	Unit	Test Conditions
I/O ports	Input data pulse width			t_{PRW}	1.5	—	t_{Pcyc}	Figure 5.83
MTU/ TPU	Input capture input pulse width		Single-edge setting	t_{TICW}	1.5	—	t_{Pcyc}	Figure 5.84
			Both-edge setting		2.5	—		
	Timer clock pulse width		Single-edge setting	t_{TCKWH}, t_{TCKWL}	1.5	—	t_{Pcyc}	Figure 5.85
			Both-edge setting		2.5	—		
			Phase counting mode		2.5	—		
POE	POE# input pulse width			t_{POEW}	1.5	—	t_{Pcyc}	Figure 5.86
8-bit timer	Timer clock pulse width		Single-edge setting	t_{TMCWH}, t_{TMCWL}	1.5	—	t_{Pcyc}	Figure 5.87
			Both-edge setting		2.5	—		
SCI	Input clock cycle		Asynchronous	t_{Scyc}	4	—	t_{Pcyc}	Figure 5.88
			Clock synchronous		6	—		
	Input clock pulse width			t_{SCKW}	0.4	0.6	t_{Scyc}	
	Input clock rise time			t_{SCKr}	—	20	ns	
	Input clock fall time			t_{SCKf}	—	20	ns	
	Output clock cycle		Asynchronous	t_{Scyc}	16	—	t_{Pcyc}	C = 30 pF Figure 5.89
			Clock synchronous		4	—		
	Output clock pulse width		2.7 V ≤ VCC ≤ 5.5 V	t_{SCKW}	0.4	0.6	t_{Scyc}	
			1.8 V ≤ VCC < 2.7 V		0.35	0.65		
			1.62 V ≤ VCC < 1.8 V		0.35	0.65		
	Output clock rise time			t_{SCKr}	—	20	ns	
	Output clock fall time			t_{SCKf}	—	20	ns	
	Transmit data delay time (master)	Clock synchronous		t_{TXD}	—	40	ns	
	Transmit data delay time (slave)	Clock synchronous	2.7 V ≤ VCC ≤ 5.5 V		—	65	ns	
			1.8 V ≤ VCC < 2.7 V		—	85	ns	
			1.62 V ≤ VCC < 1.8 V		—	95	ns	
	Receive data setup time (master)	Clock synchronous	2.7 V ≤ VCC ≤ 5.5 V	t_{RXS}	65	—	ns	
			1.8 V ≤ VCC < 2.7 V		75	—	ns	
			1.62 V ≤ VCC < 1.8 V		80	—	ns	
	Receive data setup time (slave)	Clock synchronous			40	—	ns	
	Receive data hold time	Clock synchronous		t_{RXH}	40	—	ns	
A/D converter	Trigger input pulse width			t_{TRGW}	1.5	—	t_{Pcyc}	Figure 5.90
CAC	CACREF input pulse width		$t_{Pcyc} \le t_{cac}$*2	t_{CACREF}	4.5 t_{cac} + 3 t_{Pcyc}	—	ns	
			$t_{Pcyc} > t_{cac}$*2		5 t_{cac} + 6.5 t_{Pcyc}			

Note 1. t_{Pcyc}: PCLK cycle
Note 2. t_{cac}: CAC count clock source cycle

[512 Kbytes or less of flash memory and 48 to 100 pins]

Table 5.56 Timing of On-Chip Peripheral Modules (2)

Conditions: VCC = AVCC0 = 1.62 to 5.5 V, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +105°C
When high-drive output is selected by the drive capacity register

Item				Symbol	Min.	Max.	Unit*1	Test Conditions
RSPI	RSPCK clock cycle	Master		t_{SPcyc}	2	4096	t_{Pcyc}	C = 30 pF Figure 5.91
					125	—	ns	
		Slave			8	4096	t_{Pcyc}	
	RSPCK clock high pulse width	Master	2.7 V ≤ VCC ≤ 5.5 V	t_{SPCKWH}	$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2 - 3$	—	ns	
			1.8 V ≤ VCC < 2.7 V		$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2 - 3$	—		
			1.62 V ≤ VCC < 1.8 V		$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2 - 10$	—		
		Slave			$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2$	—		
	RSPCK clock low pulse width	Master	2.7 V ≤ VCC ≤ 5.5 V	t_{SPCKWL}	$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2 - 3$	—	ns	
			1.8 V ≤ VCC < 2.7 V		$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2 - 3$	—		
			1.62 V ≤ VCC < 1.8 V		$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2 - 10$	—		
		Slave			$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2$	—		
	RSPCK clock rise/fall time	Output	2.7 V ≤ VCC ≤ 5.5 V	t_{SPCKr}, t_{SPCKf}	—	10	ns	
			1.8 V ≤ VCC < 2.7 V		—	15		
			1.62 V ≤ VCC < 1.8 V		—	20		
		Input			—	1	µs	
	Data input setup time	Master	2.7 V ≤ VCC ≤ 5.5 V	t_{SU}	50	—	ns	C = 30 pF Figure 5.92 to Figure 5.97
			1.8 V ≤ VCC < 2.7 V		65	—		
			1.62 V ≤ VCC < 1.8 V		75	—		
		Slave			$25 - t_{Pcyc}$	—		
	Data input hold time	Master		t_H	t_{Pcyc}	—	ns	
		Slave			$20 + 2 \times t_{Pcyc}$	—		
	SSL setup time	Master		t_{LEAD}	1	8	t_{SPcyc}	
		Slave			4	—	t_{Pcyc}	
	SSL hold time	Master		t_{LAG}	1	8	t_{SPcyc}	
		Slave			4	—	t_{Pcyc}	
	Data output delay time	Master	2.7 V ≤ VCC ≤ 5.5 V	t_{OD}	—	50	ns	
			1.8 V ≤ VCC < 2.7 V		—	55		
			1.62 V ≤ VCC < 1.8 V		—	60		
		Slave	2.7 V ≤ VCC ≤ 5.5 V		—	$3 \times t_{Pcyc} + 65$		
			1.8 V ≤ VCC < 2.7 V		—	$3 \times t_{Pcyc} + 85$		
			1.62 V ≤ VCC < 1.8 V		—	$3 \times t_{Pcyc} + 95$		
	Data output hold time	Master		t_{OH}	0	—	ns	
		Slave			0	—		
	Successive transmission delay time	Master		t_{TD}	$t_{SPcyc} + 2 \times t_{Pcyc}$	$8 \times t_{SPcyc} + 2 \times t_{Pcyc}$	ns	
		Slave			$4 \times t_{Pcyc}$	—		

Item				Symbol	Min.	Max.	Unit*1	Test Conditions
RSPI	Data input setup time	Master	2.7 V ≤ VCC ≤ 5.5 V	t_{SU}	10	—	ns	C = 30pF Figure 5.92 to Figure 5.97
			1.8 V ≤ VCC < 2.7 V		25	—		
			1.62 V ≤ VCC < 1.8 V		30	—		
		Slave			25 – t_{Pcyc}	—		
	Data input hold time	Master	PCLKB set to a division ratio other than divided by 2	t_H	t_{Pcyc}	—	ns	
			PCLKB set to divided by 2*2	t_{HF}	0	—		
		Slave		t_H	20 + 2 × t_{Pcyc}	—		
	SSL setup time	Master		t_{LEAD}	1	8	t_{SPcyc}	
		Slave			4	—	t_{Pcyc}	
	SSL hold time	Master		t_{LAG}	1	8	t_{SPcyc}	
		Slave			4	—	t_{Pcyc}	
	Data output delay time	Master	2.7 V ≤ VCC ≤ 5.5 V	t_{OD}	—	14	ns	
			1.8 V ≤ VCC < 2.7 V		—	20		
			1.62 V ≤ VCC < 1.8 V		—	25		
		Slave	2.7 V ≤ VCC ≤ 5.5 V		—	3 × t_{Pcyc} + 65		
			1.8 V ≤ VCC < 2.7 V		—	3 × tPcyc +85		
			1.62 V ≤ VCC < 1.8 V		—	3 × tPcyc +95		
	Data output hold time	Master		t_{OH}	0	—	ns	
		Slave			0	—		
	Successive transmission delay time	Master		t_{TD}	t_{SPcyc} + 2 × t_{Pcyc}	8 × t_{SPcyc} + 2 × t_{Pcyc}	ns	
		Slave			4 × t_{Pcyc}	—		
	MOSI and MISO rise/fall time	Output	2.7 V ≤ VCC ≤ 5.5 V	t_{Dr}, t_{Df}	—	10	ns	
			1.8 V ≤ VCC < 2.7 V		—	15		
			1.62 V ≤ VCC < 1.8 V		—	20		
		Input			—	1	µs	
	SSL rise/fall time	Output	2.7 V ≤ VCC ≤ 5.5 V	t_{SSLr}, t_{SSLf}	—	10	ns	
			1.8 V ≤ VCC < 2.7 V		—	15		
			1.62 V ≤ VCC < 1.8 V		—	20		
		Input			—	1	µs	
	Slave access time		2.7 V ≤ VCC ≤ 5.5 V	t_{SA}	—	6	t_{Pcyc}	C = 30pF Figure 5.96 and Figure 5.97
			1.8 V ≤ VCC < 2.7 V		—	7		
			1.62 V ≤ VCC < 1.8 V		—	7		
	Slave output release time		2.7 V ≤ VCC ≤ 5.5 V	t_{REL}	—	5	t_{Pcyc}	
			1.8 V ≤ VCC < 2.7 V		—	6		
			1.62 V ≤ VCC < 1.8 V		—	6		

Note 1. t_{Pcyc}: PCLK cycle
Note 2. Divided by 2 can be set only in packages with 768 Kbytes/1 Mbyte of flash memory or 144/145 pins.

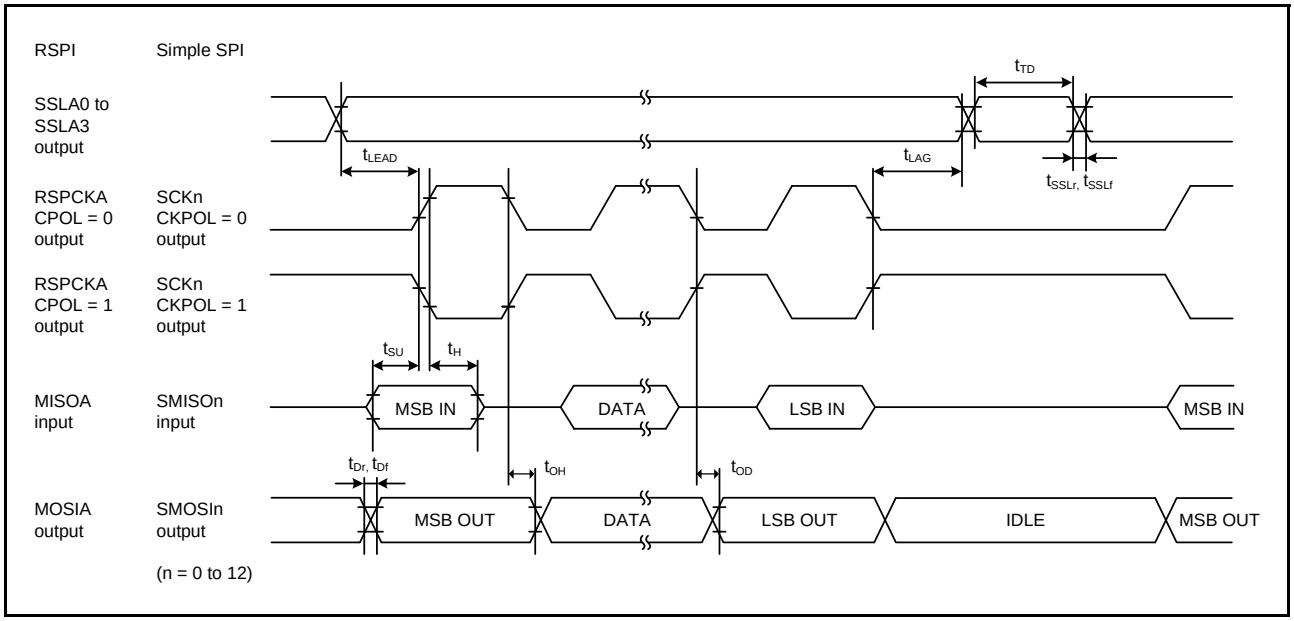


Figure 5.92 RSPI Timing (Master, CPHA = 0) (Bit Rate: PCLKB Set to Division Ratio Other Than Divided by 2) and Simple SPI Timing (Master, CKPH = 1)

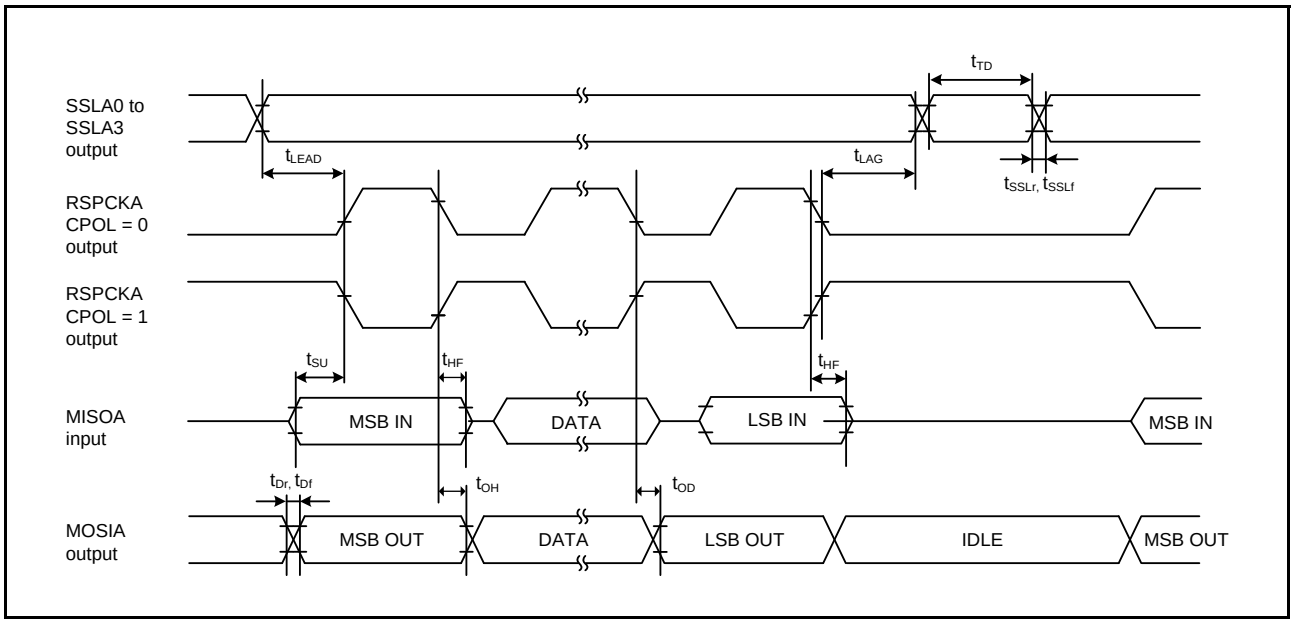
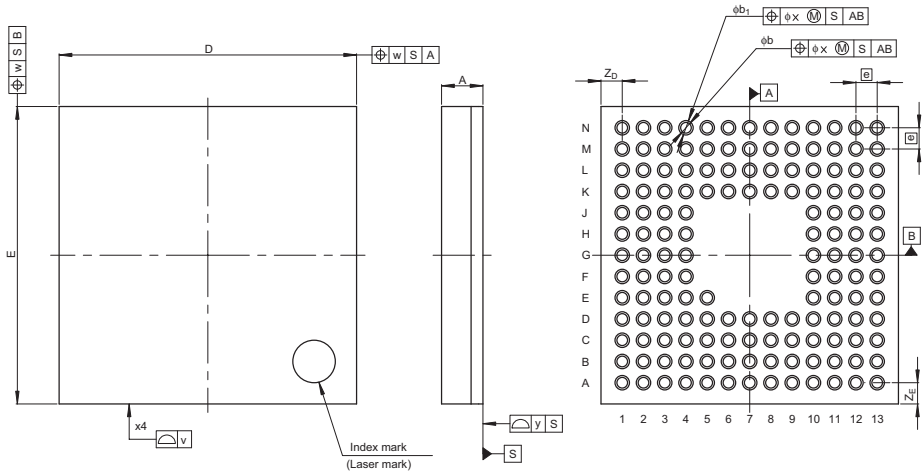


Figure 5.93 RSPI Timing (Master, CPHA = 0) (Bit Rate: PCLKB Set to Divided by 2)

Appendix 1. Package Dimensions

Information on the latest version of the package dimensions or mountings has been displayed in “Packages” on Renesas Electronics Corporation website.

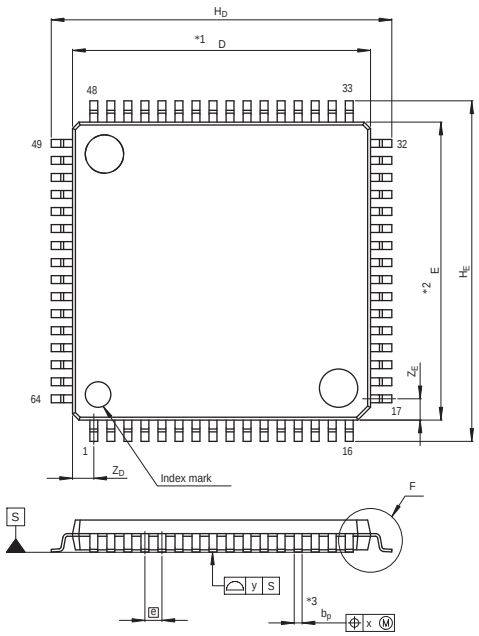
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-TFLGA145-7x7-0.50	PTLG0145KA-A	145F0G	0.1g

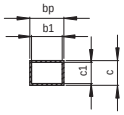


Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	7.0	—
E	—	7.0	—
v	—	—	0.15
w	—	—	0.20
A	—	—	1.05
e	—	0.5	—
b	0.21	0.25	0.29
b_1	0.29	0.34	0.39
x	—	—	0.08
y	—	—	0.08
Z_D	—	0.5	—
Z_E	—	0.5	—

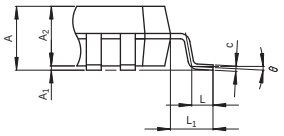
Figure A 145-Pin TFLGA (PTLG0145KA-A)

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP64-14x14-0.80	PLQP0064GA-A	64P6U-A/ —	0.7g





Terminal cross section



Detail F

NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	13.9	14.0	14.1
E	13.9	14.0	14.1
A_2	—	1.4	—
H_D	15.8	16.0	16.2
H_E	15.8	16.0	16.2
A	—	—	1.7
A_1	0	0.1	0.2
b_p	0.32	0.37	0.42
b_1	—	0.35	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.8	—
x	—	—	0.20
y	—	—	0.10
Z_D	—	1.0	—
Z_E	—	1.0	—
L	0.3	0.5	0.7
L_1	—	1.0	—

Figure K 64-Pin LQFP (PLQP0064GA-A)