Renesas Electronics America Inc - R5F52104BDFF#V0 Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I²C, SCI, SPI
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	64
Program Memory Size	96KB (96K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.62V ~ 5.5V
Data Converters	A/D 14x12b; D/A 2x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f52104bdff-v0

Table 1.1 Outline of Specifications (2 / 5)

Classification	Module/Function	Description
Low power consumption	Low power consumption facilities	• Module stop function • Four low power consumption modes Sleep mode, all-module clock stop mode, software standby mode, and deep software standby mode
	Function for lower operating power consumption	• Operating power control modes [Chip versions A and C] High-speed operating mode, middle-speed operating mode 1A, middle-speed operating mode 1B, low-speed operating mode 1, low-speed operating mode 2 [Chip version B] High-speed operating mode, middle-speed operating mode 1A, middle-speed operating mode 1B, middle-speed operating mode 2A, middle-speed operating mode 2B, low-speed operating mode 1, low-speed operating mode 2
Interrupt	Interrupt controller (ICUb)	• Interrupt vectors: 167 • External interrupts: 9 (NMI, IRQ0 to IRQ7 pins) • Non-maskable interrupts: 6 (the NMI pin, oscillation stop detection interrupt, voltage monitoring 1 interrupt, voltage monitoring 2 interrupt, WDT interrupt, and IWDT interrupt) • 16 levels specifiable for the order of priority
External bus extension		• The external address space can be divided into four areas (CS0 to CS3), each with independent control of access settings. Capacity of each area: 16 Mbytes (CS0 to CS3) A chip-select signal (CS0# to CS3#) can be output for each area. Each area is specifiable as an 8-bit or 16-bit bus space The data arrangement in each area is selectable as little or big endian (only for data). Bus format: Separate bus, multiplex bus • Wait control • Write buffer facility
DMA	DMA controller (DMACA)	• 4 channels • Three transfer modes: Normal transfer, repeat transfer, and block transfer • Activation sources: Software trigger, external interrupts, and interrupt requests from peripheral functions
	Data transfer controller (DTCa)	• Three transfer modes: Normal transfer, repeat transfer, and block transfer • Activation sources: Interrupts • Chain transfer function
I/O ports	General I/O ports	145-pin/144-pin/100-pin/80-pin/69-pin/64-pin/48-pin • I/O: 122/122/84/64/48/48/34 • Input: 1/1/1/1/1/1/1 • Pull-up resistors: 122/122/84/64/48/48/34 • Open-drain outputs: 76/76/54/44/35/35/26 • 5-V tolerance:4/4/4/4/2/2*1/2
Event link controller (ELC)		• Event signals of 59 types can be directly connected to the module • Operations of timer modules are selectable at event input • Capable of event link operation for ports B and E
Multi-function pin controller (MPC)		• Capable of selecting input/output function from multiple pins

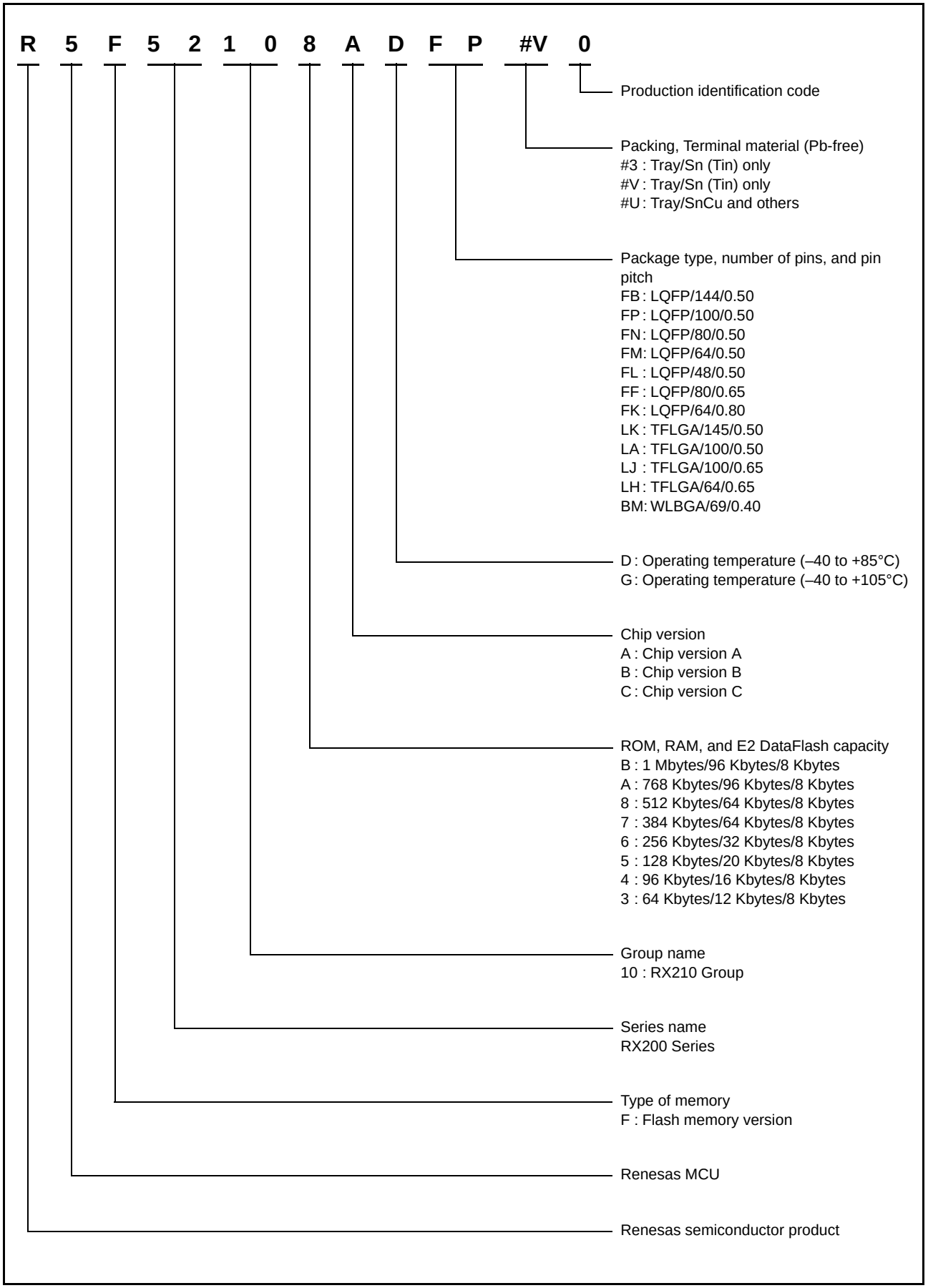


Figure 1.1 How to Read the Product Part No., Memory Capacity, and Package Type

Table 1.9 List of Pins and Pin Functions (145-Pin TFLGA) (4 / 4)

Pin No.	Power Supply, Clock, System Control	I/O Port	External Bus	Timers (MTU, TMR, POE)	Communications (SCIc, SCId, RSPI, RIIC)	Others
M11		PC0	A16	MTIOC3C/TCLKC	CTS5#/RTS5#/SS5#/ SSLA1	
M12		PC1	A17	MTIOC3A/TCLKD	SCK5/SSLA2	
M13		PL1				
N1		P21		MTIOC1B/TMCI0/ TIOCA3	RXD0/SMISO0/SSCL0	
N2		P20		MTIOC1A/TMRI0/ TIOCB3	TXD0/SMOSI0/SSDA0	
N3		P87		TIOCA2		
N4		P14		MTIOC3A/MTCLKA/ TMRI2/TIOCB5/TCLKA	CTS1#/RTS1#/SS1#	IRQ4
N5		PH2		TMRI0		IRQ1
N6		PH1		TMO0		IRQ0
N7		P55	WAIT#	MTIOC4D/TMO3		
N8	VSS					
N9		PC7	A23/CS0#	MTIOC3A/TMO2/ MTCLKB	TXD8/SMOSI8/SSDA8/ MISOA	CACREF
N10		P82		MTIOC4A	TXD10/SMOSI10/SSDA10	
N11		PC3	A19	MTIOC4D/TCLKB	TXD5/SMOSI5/SSDA5	
N12		P75			SCK11	
N13		P74			CTS11#/RTS11#/SS11#	

Note: • Pin names to which –DS is appended are for pins that can be used to trigger release from deep software standby mode.
Note: • Leave the NC pin open.

Table 1.11 List of Pins and Pin Functions (100-Pin TFLGA) (2 / 3)

Pin No.	Power Supply, Clock, System Control	I/O Port	External Bus	Timers (MTU, TMR, POE)	Communications (SCIc, SCId, RSPI, RIIC)	Others
E6		PA2	A2		RXD5/SMISO5/SSCL5/ SSLA3	
E7		PA6	A6	MTIC5V/MTCLKB/ TMCI3/POE2#	CTS5#/RTS5#/SS5#/ MOSIA	
E8		PA4	A4	MTIC5U/MTCLKA/ TMRI0	TXD5/SMOSI5/SSDA5/ SSLA0	IRQ5-DS/CVREFB1
E9		PA5	A5		RSPCKA	
E10		PA3	A3	MTIOC0D/MTCLKD	RXD5/SMISO5/SSCL5	IRQ6-DS/CMPB1
F1	EXTAL	P36				
F2	VCC					
F3		P35				NMI
F4		P32		MTIOC0C/TMO3	TXD6/SMOSI6/SSDA6	IRQ2-DS/RTCOUT/ RTCIC2
F5		P12		TMCI1	SCL	IRQ2
F6		PB3	A11	MTIOC0A/MTIOC4A/ TMO0/POE3#	SCK6	
F7		PB2	A10		CTS6#/RTS6#/SS6#	
F8		PB0	A8	MTIC5W	RXD6/SMISO6/SSCL6/ RSPCKA	
F9		PA7	A7		MISOA	
F10	VSS					
G1		P33		MTIOC0D/TMRI3/ POE3#	RXD6/SMISO6/SSCL6	IRQ3-DS
G2		P31		MTIOC4D/TMCI2	CTS1#/RTS1#/SS1#	IRQ1-DS/RTCIC1
G3		P30		MTIOC4B/TMRI3/ POE8#	RXD1/SMISO1/SSCL1	IRQ0-DS/RTCIC0
G4		P27	CS3#	MTIOC2B/TMCI3	SCK1	
G5	BCLK	P53				
G6		P52	RD#			
G7		PB5	A13	MTIOC2A/MTIOC1B/ TMRI1/POE1#	SCK9	
G8		PB4	A12		CTS9#/RTS9#/SS9#	
G9		PB1	A9	MTIOC0C/MTIOC4C/ TMCI0	TXD6/SMOSI6/SSDA6	IRQ4-DS
G10	VCC					
H1		P26	CS2#	MTIOC2A/TMO1	TXD1/SMOSI1/SSDA1	
H2		P25	CS1#	MTIOC4C/MTCLKB		ADTRG0#
H3		P16		MTIOC3C/MTIOC3D/ TMO2	TXD1/SMOSI1/SSDA1/ MOSIA/SCL-DS	IRQ6/RTCOUT/ ADTRG0#
H4		P15		MTIOC0B/MTCLKB/ TMCI2	RXD1/SMISO1/SSCL1	IRQ5
H5		P55	WAIT#	MTIOC4D/TMO3		
H6		P54	ALE	MTIOC4B/TMCI1		
H7		PC7	A23/CS0#	MTIOC3A/TMO2/ MTCLKB	TXD8/SMOSI8/SSDA8/ MISOA	CACREF
H8		PC6	A22/CS1#	MTIOC3C/MTCLKA/ TMCI2	RXD8/SMISO8/SSCL8/ MOSIA	
H9		PB6	A14	MTIOC3D	RXD9/SMISO9/SSCL9	
H10		PB7	A15	MTIOC3B	TXD9/SMOSI9/SSDA9	
J1		P24	CS0#	MTIOC4A/MTCLKA/ TMRI1		
J2		P21		MTIOC1B/TMCI0	RXD0/SMISO0/SSCL0	
J3		P17		MTIOC3A/MTIOC3B/ TMO1/POE8#	SCK1/MISOA/ SDA-DS	IRQ7

Table 1.12 List of Pins and Pin Functions (100-Pin LQFP) (1 / 3)

Pin No.	Power Supply, Clock, System Control	I/O Port	External Bus	Timers (MTU, TMR, POE)	Communications (SCIc, SCId, RSPI, RIIC)	Others
1	VREFH					
2		P03				DA0
3	VREFL					
4		PJ3		MTIOC3C	CTS6#/RTS6#/SS6#	
5	VCL					
6		PJ1		MTIOC3A		
7	MD					FINED
8	XCIN					
9	XCOUT					
10	RES#					
11	XTAL	P37				
12	VSS					
13	EXTAL	P36				
14	VCC					
15		P35				NMI
16		P34		MTIOC0A/TMCI3/ POE2#	SCK6	IRQ4
17		P33		MTIOC0D/TMRI3/ POE3#	RXD6/SMISO6/SSCL6	IRQ3-DS
18		P32		MTIOC0C/TMO3	TXD6/SMOSI6/SSDA6	IRQ2-DS/RTCOUT/ RTCIC2
19		P31		MTIOC4D/TMCI2	CTS1#/RTS1#/SS1#	IRQ1-DS/RTCIC1
20		P30		MTIOC4B/TMRI3/ POE8#	RXD1/SMISO1/SSCL1	IRQ0-DS/RTCIC0
21		P27	CS3#	MTIOC2B/TMCI3	SCK1	
22		P26	CS2#	MTIOC2A/TMO1	TXD1/SMOSI1/SSDA1	
23		P25	CS1#	MTIOC4C/MTCLKB		ADTRG0#
24		P24	CS0#	MTIOC4A/MTCLKA/ TMRI1		
25		P23		MTIOC3D/MTCLKD	CTS0#/RTS0#/SS0#	
26		P22		MTIOC3B/MTCLKC/ TMO0	SCK0	
27		P21		MTIOC1B/TMCI0	RXD0/SMISO0/SSCL0	
28		P20		MTIOC1A/TMRI0	TXD0/SMOSI0/SSDA0	
29		P17		MTIOC3A/MTIOC3B/ TMO1/POE8#	SCK1/MISOA/ SDA-DS	IRQ7
30		P16		MTIOC3C/MTIOC3D/ TMO2	TXD1/SMOSI1/SSDA1/ MOSIA/SCL-DS	IRQ6/RTCOUT/ ADTRG0#
31		P15		MTIOC0B/MTCLKB/ TMCI2	RXD1/SMISO1/SSCL1	IRQ5
32		P14		MTIOC3A/MTCLKA/ TMRI2	CTS1#/RTS1#/SS1#	IRQ4
33		P13		MTIOC0B/TMO3	SDA	IRQ3
34		P12		TMCI1	SCL	IRQ2
35		PH3		TMCI0		
36		PH2		TMRI0		IRQ1
37		PH1		TMO0		IRQ0
38		PH0				CACREF
39		P55	WAIT#	MTIOC4D/TMO3		
40		P54	ALE	MTIOC4B/TMCI1		
41	BCLK	P53				

2.1 General-Purpose Registers (R0 to R15)

This CPU has sixteen general-purpose registers (R0 to R15). R1 to R15 can be used as data registers or address registers. R0, a general-purpose register, also functions as the stack pointer (SP). The stack pointer is switched to operate as the interrupt stack pointer (ISP) or user stack pointer (USP) by the value of the stack pointer select bit (U) in the processor status word (PSW).

2.2 Control Registers

(1) Interrupt Stack Pointer (ISP)/User Stack Pointer (USP)

The stack pointer (SP) can be either of two types, the interrupt stack pointer (ISP) or the user stack pointer (USP). Whether the stack pointer operates as the ISP or USP depends on the value of the stack pointer select bit (U) in the processor status word (PSW).
Set the ISP or USP to a multiple of four, as this reduces the numbers of cycles required to execute interrupt sequences and instructions entailing stack manipulation.

(2) Interrupt Table Register (INTB)

The interrupt table register (INTB) specifies the address where the relocatable vector table starts.

(3) Program Counter (PC)

The program counter (PC) indicates the address of the instruction being executed.

(4) Processor Status Word (PSW)

The processor status word (PSW) indicates the results of instruction execution or the state of the CPU.

(5) Backup PC (BPC)

The backup PC (BPC) is provided to speed up response to interrupts.
After a fast interrupt has been generated, the contents of the program counter (PC) are saved in the BPC register.

(6) Backup PSW (BPSW)

The backup PSW (BPSW) is provided to speed up response to interrupts.
After a fast interrupt has been generated, the contents of the processor status word (PSW) are saved in the BPSW. The allocation of bits in the BPSW corresponds to that in the PSW.

(7) Fast Interrupt Vector Register (FINTV)

The fast interrupt vector register (FINTV) is provided to speed up response to interrupts.
The FINTV register specifies a branch destination address when a fast interrupt has been generated.

2.3 Register Associated with DSP Instructions

(1) Accumulator (ACC)

The accumulator (ACC) is a 64-bit register used for DSP instructions. The accumulator is also used for the multiply and multiply-and-accumulate instructions; EMUL, EMULU, MUL, and RMPA, in which case the prior value in the accumulator is modified by execution of the instruction.
Use the MVTACHI and MVTACLO instructions for writing to the accumulator. The MVTACHI and MVTACLO instructions write data to the higher-order 32 bits (bits 63 to 32) and the lower-order 32 bits (bits 31 to 0), respectively.
Use the MVFACHI and MVFACMI instructions for reading data from the accumulator. The MVFACHI and MVFACMI instructions read data from the higher-order 32 bits (bits 63 to 32) and the middle 32 bits (bits 47 to 16), respectively.

[Chip version B with 256 Kbytes or less of flash memory and 48 to 100 pins]

Table 5.12 DC Characteristics (11)

Conditions: VCC = AVCC0 = 2.7 to 5.5 V, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +105°C

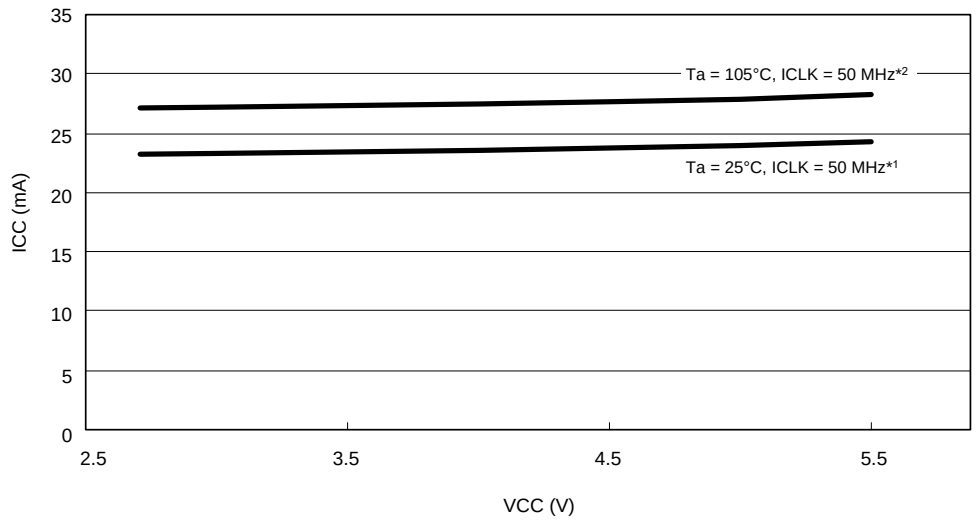
Item					Symbol	Typ.	Max.	Unit	Test Conditions
Supply current*1	High-speed operating mode	Normal operating mode	No peripheral operation*2	ICLK = 50 MHz	I_{CC}	7.2	—	mA	
			All peripheral operation: Normal*3	ICLK = 50 MHz		23.5	—		
			All peripheral operation: Max.*3	ICLK = 50 MHz		—	45		
		Sleep mode	No peripheral operation	ICLK = 50 MHz		4.3	—		
			All peripheral operation: Normal	ICLK = 50 MHz		12	—		
		All-module clock stop mode		ICLK = 50 MHz		3.7	—		
		Increase during BGO operation*4				20	—		

Note 1. Supply current values do not include output charge/discharge current from all pins. The values apply when internal pull-up MOSs are in the off state.

Note 2. Clock supply to the peripheral functions is stopped. This does not include BGO operation. The clock source is PLL and the VCO oscillation frequency is 100 MHz. BCLK, FCLK, and PCLK are set to divided by 64.

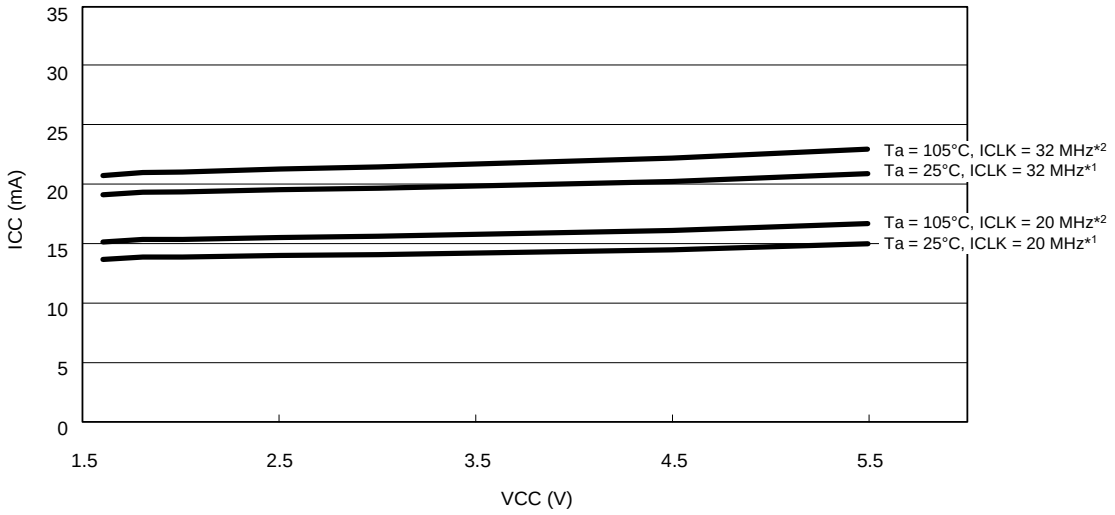
Note 3. Clocks are supplied to the peripheral functions. This does not include BGO operation. The clock source is PLL and the VCO oscillation frequency is 100 MHz. BCLK, FCLK, and PCLK are ICLK divided by 2.

Note 4. This is the increase if data is programmed to or erasing from the ROM or E2 DataFlash during program execution.



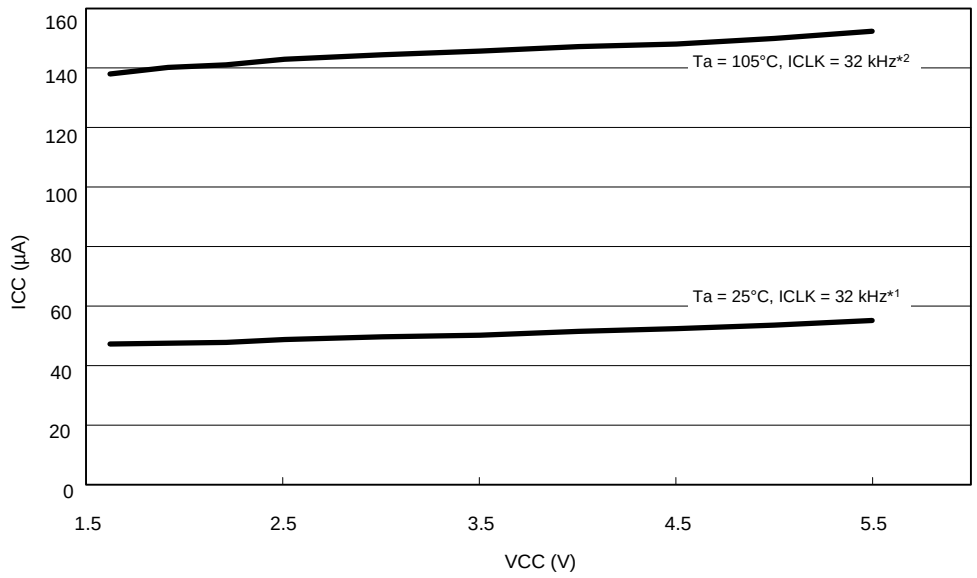
Note 1. All peripheral operation is normal. This does not include BGO operation.
Average value of the tested middle samples during product evaluation.
Note 2. All peripheral operation is maximum. This does not include BGO operation.
Average value of the tested upper-limit samples during product evaluation.

Figure 5.17 Voltage Dependency in High-Speed Operating Mode (Reference Data) for Chip Version B with 256 Kbytes or Less of Flash Memory and 48 to 100 Pins



Note 1. All peripheral operation is normal. This does not include BGO operation.
Average value of the tested middle samples during product evaluation.
Note 2. All peripheral operation is maximum. This does not include BGO operation.
Average value of the tested upper-limit samples during product evaluation.

Figure 5.18 Voltage Dependency in Middle-Speed Operating Modes 1A and 1B (Reference Data) for Chip Version B with 256 Kbytes or Less of Flash Memory and 48 to 100 Pins



Note 1. All peripheral operation is normal.
Average value of the tested middle samples during product evaluation.
Note 2. All peripheral operation is maximum.
Average value of the tested upper-limit samples during product evaluation.

Figure 5.21 Voltage Dependency in Low-Speed Operating Mode 2 (Reference Data) for Chip Version B with 256 Kbytes or Less of Flash Memory and 48 to 100 Pins

[Chip version B with 768 Kbytes/1 Mbyte of flash memory and 100 to 145 pins]

Table 5.16 DC Characteristics (15)

Conditions: VCC = AVCC0 = 1.62 to 5.5 V, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +105°C

Item					Symbol	Typ.	Max.	Unit	Test Conditions
Supply current*1	Middle-speed operating modes 1A and 1B	Normal operating mode	No peripheral operation	ICLK = 32 MHz*2	I_{CC}	5.6	—	mA	
				ICLK = 20 MHz*3		4.6	—		
			All peripheral operation: Normal	ICLK = 32 MHz*4		25.5	—		
				ICLK = 20 MHz*5		17.6	—		
			All peripheral operation: Max.	ICLK = 32 MHz*4		—	35		
				ICLK = 20 MHz*5		—	—		
		Sleep mode	No peripheral operation	ICLK = 32 MHz		3.4	—		
				ICLK = 20 MHz		3.3	—		
			All peripheral operation: Normal	ICLK = 32 MHz		13.4	—		
				ICLK = 20 MHz		10.2	—		
		All-module clock stop mode		ICLK = 32 MHz		3	—		
				ICLK = 20 MHz		3	—		
		Increase during BGO operation*6	Middle-speed operating mode 1A			23	—		
			Middle-speed operating mode 1B			20	—		
	Middle-speed operating modes 2A and 2B	Normal operating mode	No peripheral operation*2	ICLK = 32 MHz		5.1	—		
				ICLK = 16 MHz		3.5	—		
				ICLK = 8 MHz		2.7	—		
			All peripheral operation: Normal*4	ICLK = 32 MHz		25	—		
				ICLK = 16 MHz		14	—		
				ICLK = 8 MHz		8.5	—		
			All peripheral operation: Max.*4	ICLK = 32 MHz		—	34		
				ICLK = 16 MHz		—	—		
				ICLK = 8 MHz		—	—		
		Sleep mode	No peripheral operation	ICLK = 32 MHz		2.9	—		
				ICLK = 16 MHz		2.5	—		
				ICLK = 8 MHz		2.2	—		
			All peripheral operation: Normal	ICLK = 32 MHz		13	—		
				ICLK = 16 MHz		8.2	—		
				ICLK = 8 MHz		5.8	—		
		All-module clock stop mode		ICLK = 32 MHz		2.5	—		
				ICLK = 16 MHz		2.2	—		
				ICLK = 8 MHz		2.1	—		
		Increase during BGO operation*6	Middle-speed operating mode 1A			23	—		
			Middle-speed operating mode 1B			20	—		

[Chip version B with 512 Kbytes or less of flash memory and 144 and 145 pins]

Table 5.18 DC Characteristics (17)

Conditions: VCC = AVCC0 = 2.7 to 5.5 V, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +105°C

Item					Symbol	Typ.	Max.	Unit	Test Conditions
Supply current*1	High-speed operating mode	Normal operating mode	No peripheral operation*2	ICLK = 50 MHz	I_{CC}	7.2	—	mA	
			All peripheral operation: Normal*3	ICLK = 50 MHz		25.9	—		
			All peripheral operation: Max.*3	ICLK = 50 MHz		—	45		
		Sleep mode	No peripheral operation	ICLK = 50 MHz		4.3	—		
			All peripheral operation: Normal	ICLK = 50 MHz		13	—		
		All-module clock stop mode				3.7	—		
		Increase during BGO operation*4				21	—		

Note 1. Supply current values do not include output charge/discharge current from all pins. The values apply when internal pull-up MOSs are in the off state.

Note 2. Clock supply to the peripheral functions is stopped. This does not include BGO operation. The clock source is PLL and the VCO oscillation frequency is 100 MHz. BCLK, FCLK, and PCLK are set to divided by 64.

Note 3. Clocks are supplied to the peripheral functions. This does not include BGO operation. The clock source is PLL and the VCO oscillation frequency is 100 MHz. BCLK, FCLK, and PCLK are ICLK divided by 2.

Note 4. This is the increase if data is programmed to or erasing from the ROM or E2 DataFlash during program execution.

[Chip version B with 512 Kbytes or less of flash memory and 144 and 145 pins]

Table 5.19 DC Characteristics (18)

Conditions: VCC = AVCC0 = 1.62 to 5.5 V, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +105°C

Item					Symbol	Typ.	Max.	Unit	Test Conditions
Supply current*1	Middle-speed operating modes 1A and 1B	Normal operating mode	No peripheral operation	ICLK = 32 MHz*2	I_{CC}	5.3	—	mA	
				ICLK = 20 MHz*3		4.6	—		
			All peripheral operation: Normal	ICLK = 32 MHz*4		22.3	—		
				ICLK = 20 MHz*5		15.6	—		
			All peripheral operation: Max.	ICLK = 32 MHz*4		—	35		
				ICLK = 20 MHz*5		—	—		
		Sleep mode	No peripheral operation	ICLK = 32 MHz		3.4	—		
				ICLK = 20 MHz		3.3	—		
			All peripheral operation: Normal	ICLK = 32 MHz		12.8	—		
				ICLK = 20 MHz		9.8	—		
		All-module clock stop mode		ICLK = 32 MHz		3	—		
				ICLK = 20 MHz		3	—		
		Increase during BGO operation*6	Middle-speed operating mode 1A			21	—		
			Middle-speed operating mode 1B			19	—		
	Middle-speed operating modes 2A and 2B	Normal operating mode	No peripheral operation*2	ICLK = 32 MHz		4.7	—		
				ICLK = 16 MHz		3.4	—		
				ICLK = 8 MHz		2.7	—		
			All peripheral operation: Normal*4	ICLK = 32 MHz*3		21.7	—		
				ICLK = 16 MHz*3		12.3	—		
				ICLK = 8 MHz		7.6	—		
			All peripheral operation: Max.*4	ICLK = 32 MHz*3		—	34		
				ICLK = 16 MHz*3		—	—		
				ICLK = 8 MHz		—	—		
		Sleep mode	No peripheral operation	ICLK = 32 MHz		2.9	—		
				ICLK = 16 MHz		2.5	—		
				ICLK = 8 MHz		2.2	—		
			All peripheral operation: Normal	ICLK = 32 MHz		12.3	—		
				ICLK = 16 MHz		7.8	—		
				ICLK = 8 MHz		5.6	—		
		All-module clock stop mode		ICLK = 32 MHz		2.5	—		
				ICLK = 16 MHz		2.2	—		
				ICLK = 8 MHz		2.1	—		
		Increase during BGO operation*6	Middle-speed operating mode 1A			21	—		
			Middle-speed operating mode 1B			19	—		

5.3.3 Timing of Recovery from Low Power Consumption Modes

[Chip versions A and C]

Table 5.46 Timing of Recovery from Low Power Consumption Modes

Conditions: VCC = AVCC0 = 1.62 to 5.5 V, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +105°C

Item			Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Recovery time after cancellation of software standby mode (flash memory, HOCO power supplied) (SOFTCUT[2:0] bits = 000b)*1	Crystal resonator connected to main clock oscillator*2	Main clock oscillator operating	t_{SBYMC}	—	3	—	ms	Figure 5.72
		Main clock oscillator and PLL circuit operating	t_{SBYPC}	—	3.5	—	ms	
	External clock input to main clock oscillator	Main clock oscillator operating	t_{SBYEX}	10	—	—	µs	
		Main clock oscillator and PLL circuit operating	t_{SBYPE}	0.5	—	—	ms	
	Sub-clock oscillator operating		t_{SBYSC}	2*3	—	—	s	
	HOCO clock oscillator operating		t_{SBYHO}	—	—	500	µs	
	LOCO clock oscillator operating		t_{SBYLO}	—	—	90	µs	
Recovery time after cancellation of software standby mode (flash memory power supplied, HOCO power not supplied) (SOFTCUT[2:0] bits = 110b)*1	Crystal resonator connected to main clock oscillator*2	Main clock oscillator operating	t_{SBYMC}	—	3	—	ms	Figure 5.72
		Main clock oscillator and PLL circuit operating	t_{SBYPC}	—	3.5	—	ms	
	External clock input to main clock oscillator	Main clock oscillator operating	t_{SBYEX}	40	—	—	µs	
		Main clock oscillator and PLL circuit operating	t_{SBYPE}	0.5	—	—	ms	
	Sub-clock oscillator operating		t_{SBYSC}	2*3	—	—	s	
	HOCO clock oscillator operating		t_{SBYHO}	—	—	1.2	ms	
	LOCO clock oscillator operating		t_{SBYLO}	—	—	90	µs	
Recovery time after cancellation of software standby mode (flash memory, HOCO power not supplied) (SOFTCUT[2:0] bits = 111b)*1	Crystal resonator connected to main clock oscillator*2	Main clock oscillator operating	t_{SBYMC}	—	3	—	ms	Figure 5.72
		Main clock oscillator and PLL circuit operating	t_{SBYPC}	—	3.5	—	ms	
	External clock input to main clock oscillator	Main clock oscillator operating	t_{SBYEX}	100	—	—	µs	
		Main clock oscillator and PLL circuit operating	t_{SBYPE}	0.5	—	—	ms	
	Sub-clock oscillator operating		t_{SBYSC}	2*4	—	—	s	
	HOCO clock oscillator operating		t_{SBYHO}	—	—	1.2	ms	
	LOCO clock oscillator operating		t_{SBYLO}	—	—	10	ms	
Recovery time after cancellation of deep software standby mode			t_{DSBY}	—	—	8	ms	Figure 5.73
Wait time after cancellation of deep software standby mode			t_{DSBYWT}	—	—	0.8	ms	

Note 1. The recovery time varies depending on the state of each oscillator when the WAIT instruction is executed. The recovery time when multiple oscillators are operating varies depending on the operating state of the oscillators that are not selected as the system clock source, and depends on the time set in the wait control registers corresponding to the oscillators.
Note 2. The indicated value is measured for an 8 MHz crystal resonator.
Note 3. When RCR3.RTCEN = 1, the time will be the time set in the SOSCWTCR register minus 2 s.
Note 4. When RCR3.RTCEN = 1, the time will be the time set in the SOSCWTCR register minus 2 s and plus 31.25 ms.

Table 5.52 Bus Timing (Multiplexed Bus) (1)

Conditions: VCC = AVCC0 = 2.7 to 5.5 V, VSS = AVSS0 = VREFL = VREFL0 = 0 V,
fBCLK ≤ 25 MHz (BCLK pin output frequency ≤ 12.5 MHz), T_a = –40 to +105°C, V_{OH} = VCC × 0.5,
V_{OL} = VCC × 0.5, I_{OH} = –1.0 mA, I_{OL} = 1.0 mA, C_L = 30 pF
When normal output is selected by the drive capacity register

Item	Symbol	Min.	Typ.	Max.	Unit
Address delay time	t_{AD}	—	60	ns	Figure 5.81 and Figure 5.82
Byte control delay time	t_{BCD}	—	60	ns	
CS# delay time	t_{CSD}	—	60	ns	
RD# delay time	t_{RSD}	—	60	ns	
ALE delay time	t_{ALED}	—	60	ns	
Read data setup time	t_{RDS}	40	—	ns	
Read data hold time	t_{RDH}	0	—	ns	
WR# delay time	t_{WRD}	—	60	ns	
Write data delay time	t_{WDD}	—	60	ns	
Write data hold time	t_{WDH}	0	—	ns	
WAIT# setup time	t_{WTS}	40	—	ns	Figure 5.80
WAIT# hold time	t_{WTH}	0	—	ns	

Table 5.53 Bus Timing (Multiplexed Bus) (2)

Conditions: VCC = AVCC0 = 1.8 to 2.7 V, VSS = AVSS0 = VREFL = VREFL0 = 0 V,
fBCLK ≤ 16 MHz (BCLK pin output frequency ≤ 8 MHz), T_a = –40 to +105°C, V_{OH} = VCC × 0.5,
V_{OL} = VCC × 0.5, I_{OH} = –1.0 mA, I_{OL} = 1.0 mA, C_L = 30 pF
When normal output is selected by the drive capacity register

Item	Symbol	Min.	Typ.	Max.	Unit
Address delay time	t_{AD}	—	90	ns	Figure 5.81 and Figure 5.82
Byte control delay time	t_{BCD}	—	90	ns	
CS# delay time	t_{CSD}	—	90	ns	
RD# delay time	t_{RSD}	—	90	ns	
ALE delay time	t_{ALED}	—	90	ns	
Read data setup time	t_{RDS}	60	—	ns	
Read data hold time	t_{RDH}	0	—	ns	
WR# delay time	t_{WRD}	—	90	ns	
Write data delay time	t_{WDD}	—	90	ns	
Write data hold time	t_{WDH}	0	—	ns	
WAIT# setup time	t_{WTS}	60	—	ns	Figure 5.80
WAIT# hold time	t_{WTH}	0	—	ns	

Table 5.60 Timing of On-Chip Peripheral Modules (6)

Conditions: VCC = AVCC0 = 2.7 to 5.5 V, VSS = AVSS0 = VREFL = VREFL0 = 0 V, fPCLKB = up to 32 MHz,
T_a = –40 to +105°C
When high-drive output is selected by the drive capacity register

Item		Symbol	Min.*1	Max.	Unit	Test Conditions
Simple IIC (Standard mode)	SDA input rise time	t_{Sr}	—	1000	ns	Figure 5.98
	SDA input fall time	t_{Sf}	—	300	ns	
	SDA input spike pulse removal time	t_{SP}	0	$4 \times t_{pcyc}$*2	ns	
	Data input setup time	t_{SDAS}	250	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	
Simple IIC (Fast mode)	SCL, SDA input rise time	t_{Sr}	$20 + 0.1C_b$	300	ns	Figure 5.98
	SCL, SDA input fall time	t_{Sf}	$20 + 0.1C_b$	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	$4 \times t_{pcyc}$*2	ns	
	Data input setup time	t_{SDAS}	100	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	

Note: • t_{Pcyc}: PCLK cycle
Note 1. C_b indicates the total capacity of the bus line.
Note 2. This applies when the SMR.CKS[1:0] bits = 00b and the SNFR.NFCS[2:0] bits = 010b while the SNFR.NFE bit = 1 and the digital filter is enabled.

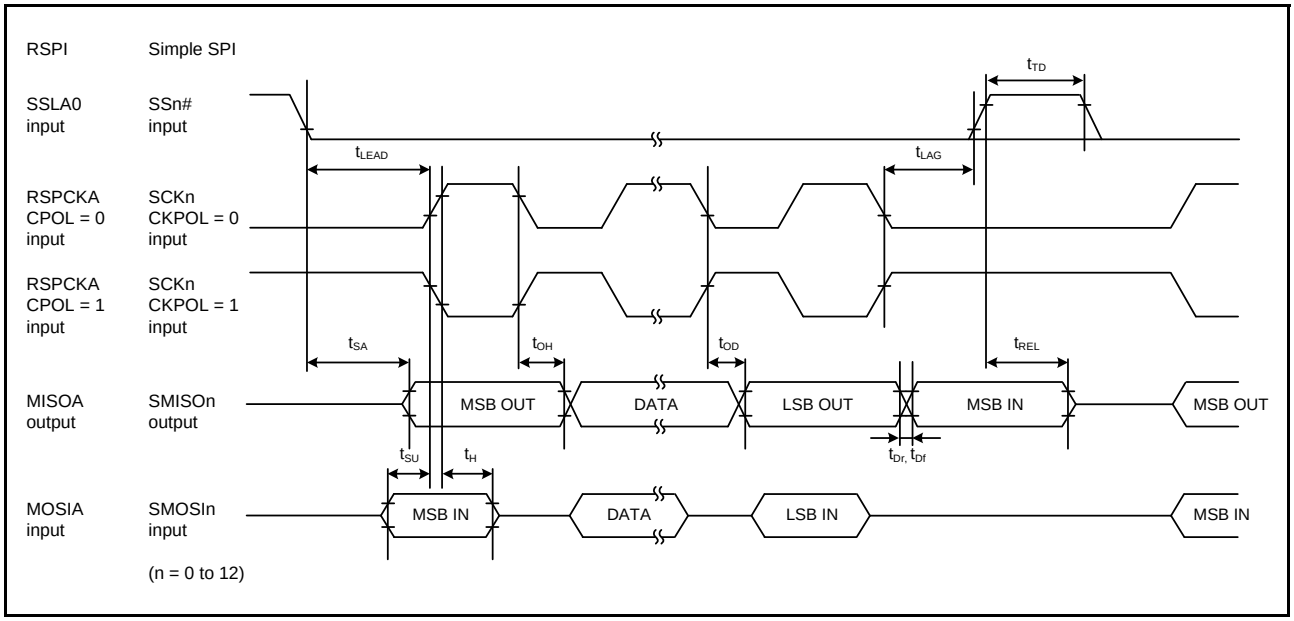


Figure 5.96 RSPI Timing (Slave, CPHA = 0) and Simple SPI Timing (Slave, CKPH = 1)

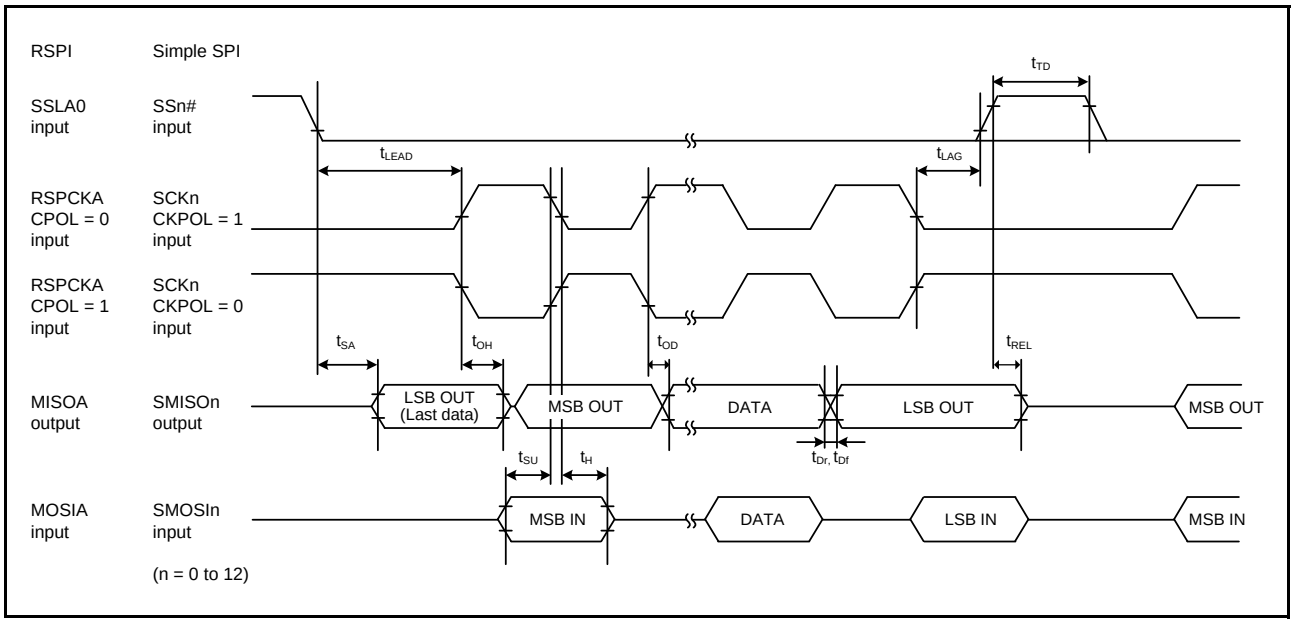


Figure 5.97 RSPI Timing (Slave, CPHA = 1) and Simple SPI Timing (Slave, CKPH = 0)

5.4 A/D Conversion Characteristics

Table 5.61 A/D Conversion Characteristics (1)

Conditions: VCC = AVCC0 = 2.7 to 5.5 V, VREFH0 ≥ 2.7 V, AVCC0-0.9 V ≤ VREFH0 ≤ AVCC0*3,
VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +105°C

Item		Min.	Typ.	Max.	Unit	Test Conditions
A/D conversion clock frequency (fPCLKD)		1	—	50	MHz	
Resolution		—	—	12	Bit	
Conversion time*1 (Operation at fPCLKD = 50 MHz)	Permissible signal source impedance (Max.) = 0.5 kΩ	1.0 (0.4)*2	—	—	µs	Sampling in 20 states
	Permissible signal source impedance (Max.) = 1 kΩ	1.1 (0.5)*2	—	—		Sampling in 25 states
	Permissible signal source impedance (Max.) = 5 kΩ	1.5 (0.9)*2	—	—		Sampling in 45 states
Analog input capacitance		—	—	30	pF	
Offset error		—	±0.5	±4.5	LSB	High-precision channel
				±7.5		Normal-precision channel
Full-scale error		—	±0.75	±4.5	LSB	High-precision channel
				±7.5		Normal-precision channel
Quantization error		—	±0.5	—	LSB	
Absolute accuracy		—	±1.25	±5.0	LSB	High-precision channel
		—	±1.25	±8.0	LSB	Normal-precision channel
DNL differential nonlinearity error		—	±1.0	—	LSB	
INL integral nonlinearity error		—	±1.0	±3.0	LSB	

Note: • PCLKD must be set to 40 MHz or lower when HOCO is to be selected as the A/D conversion clock. The characteristics apply when no pin functions other than A/D converter input are used. Absolute accuracy includes quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.

Note: • When using the channel-dedicated sample-and-hold circuit, use the AN000 to AN002 analog input voltage (V_{AN}) that satisfies all the following conditions: 0.25 V ≤ V_{AN} ≤ AVCC0 - 0.25 V, V_{AN} ≤ VREFH0, and AVCC0 ≥ 2.7 V.

Note 1. The conversion time is the sum of the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.

Note 2. The value in parentheses indicates the sampling time.

Note 3. When using the temperature sensor, use it when AVCC0 = VREFH0.

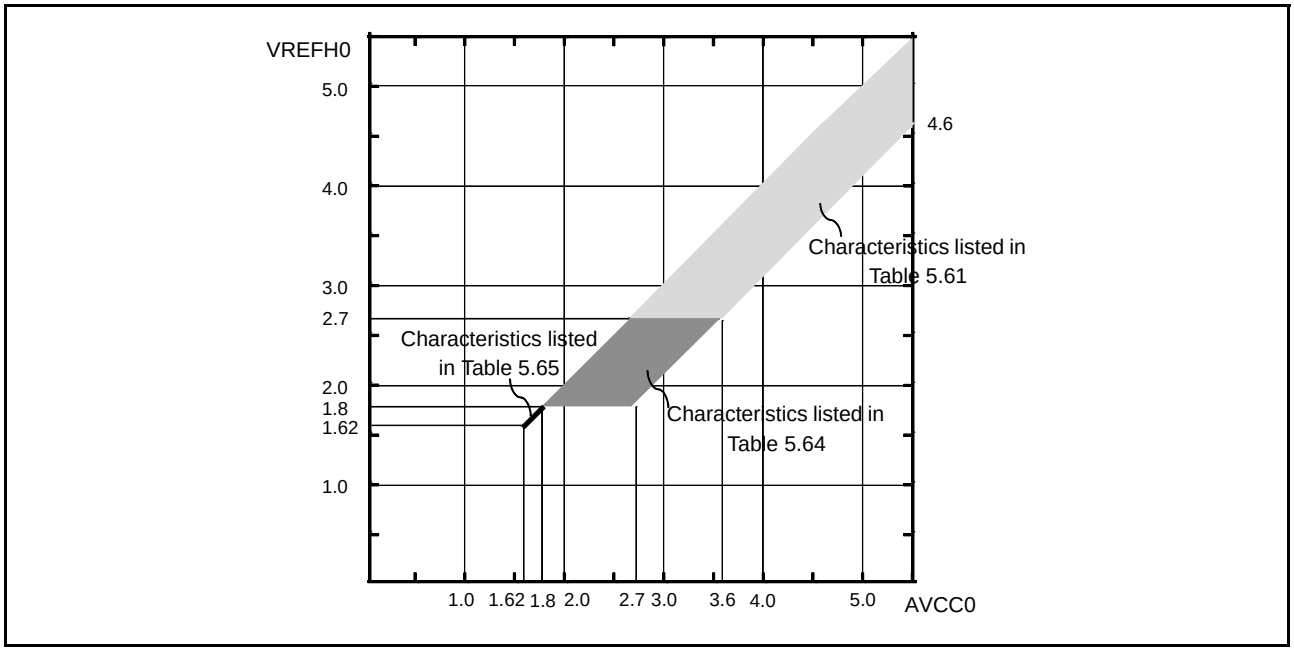


Figure 5.99 AVCC0 to VREFH0 Voltage Range

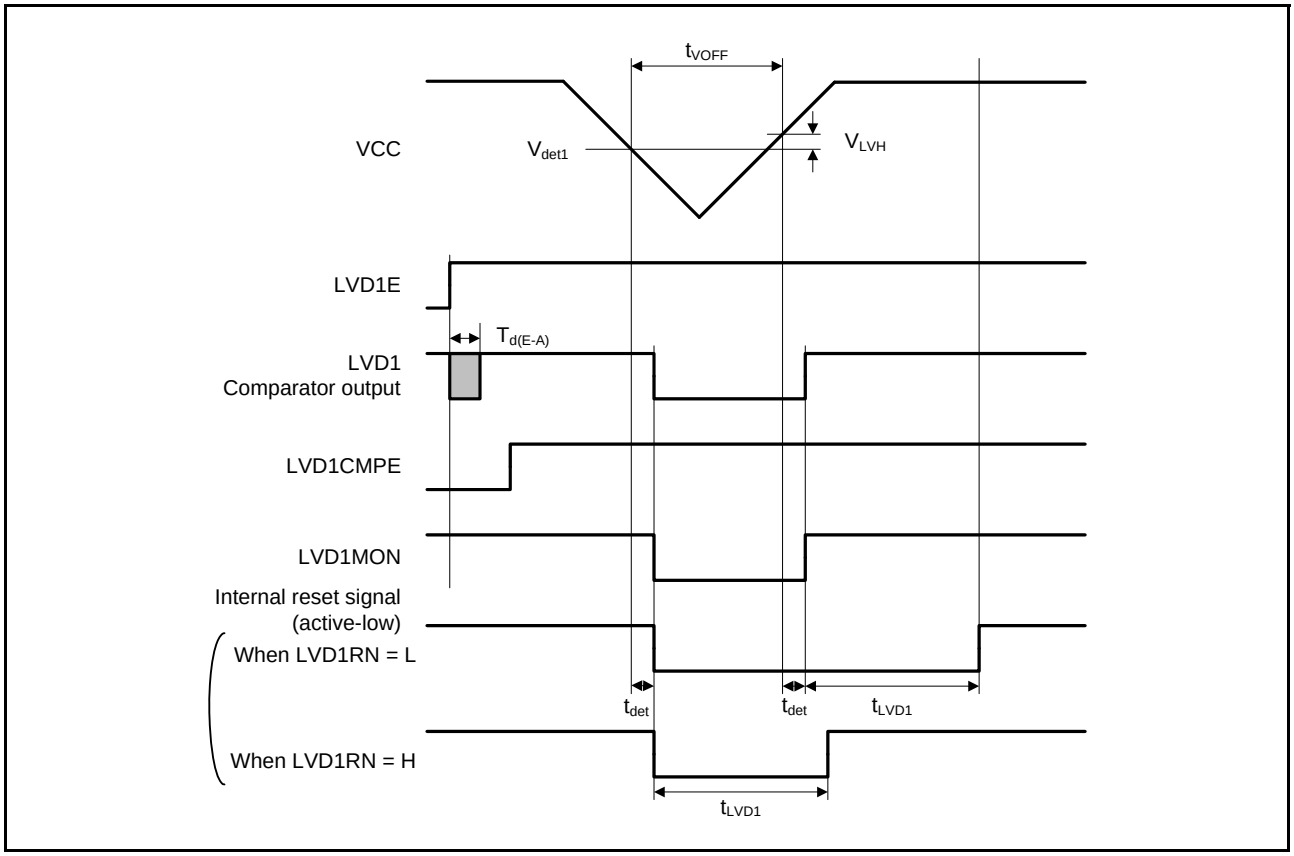


Figure 5.106 Voltage Detection Circuit Timing (V_{det1})

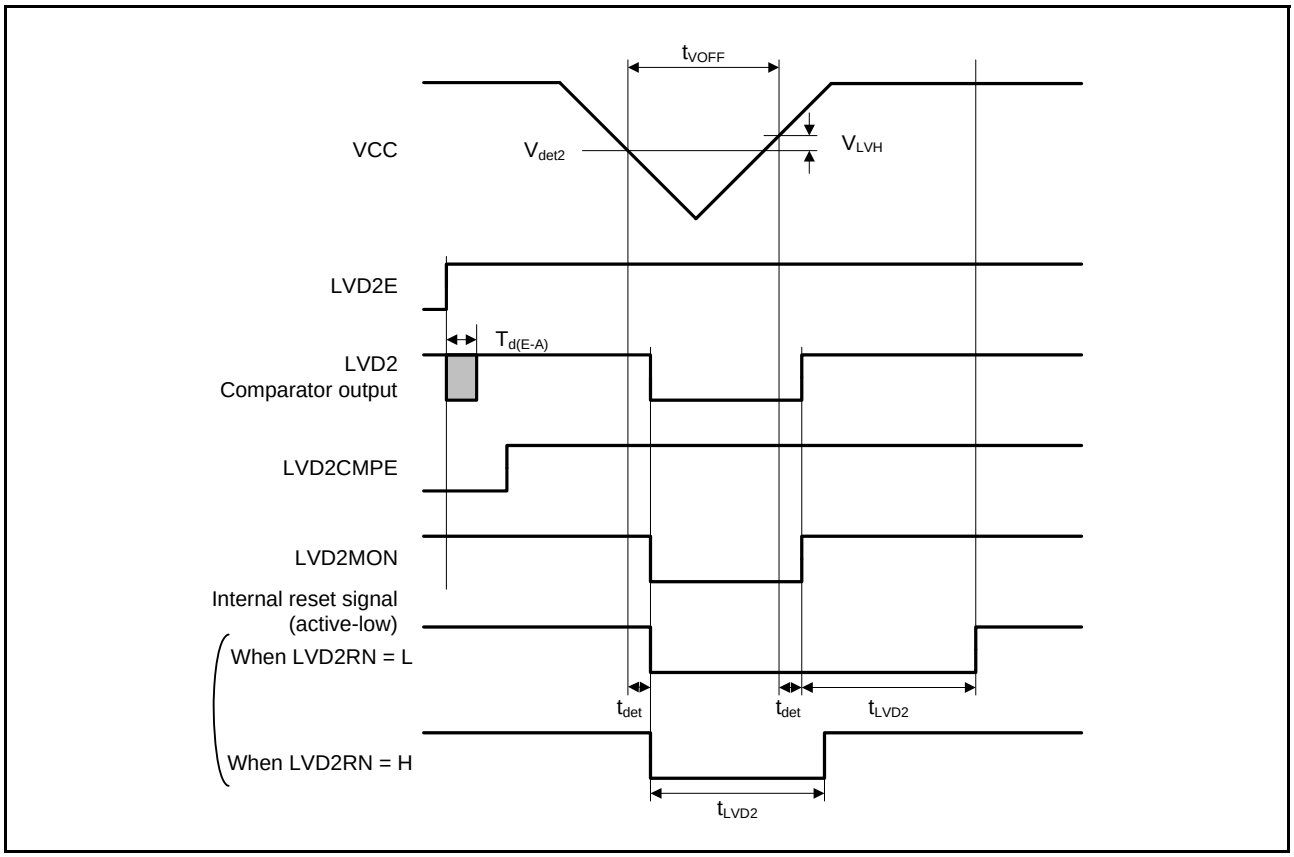


Figure 5.107 Voltage Detection Circuit Timing (V_{det2})

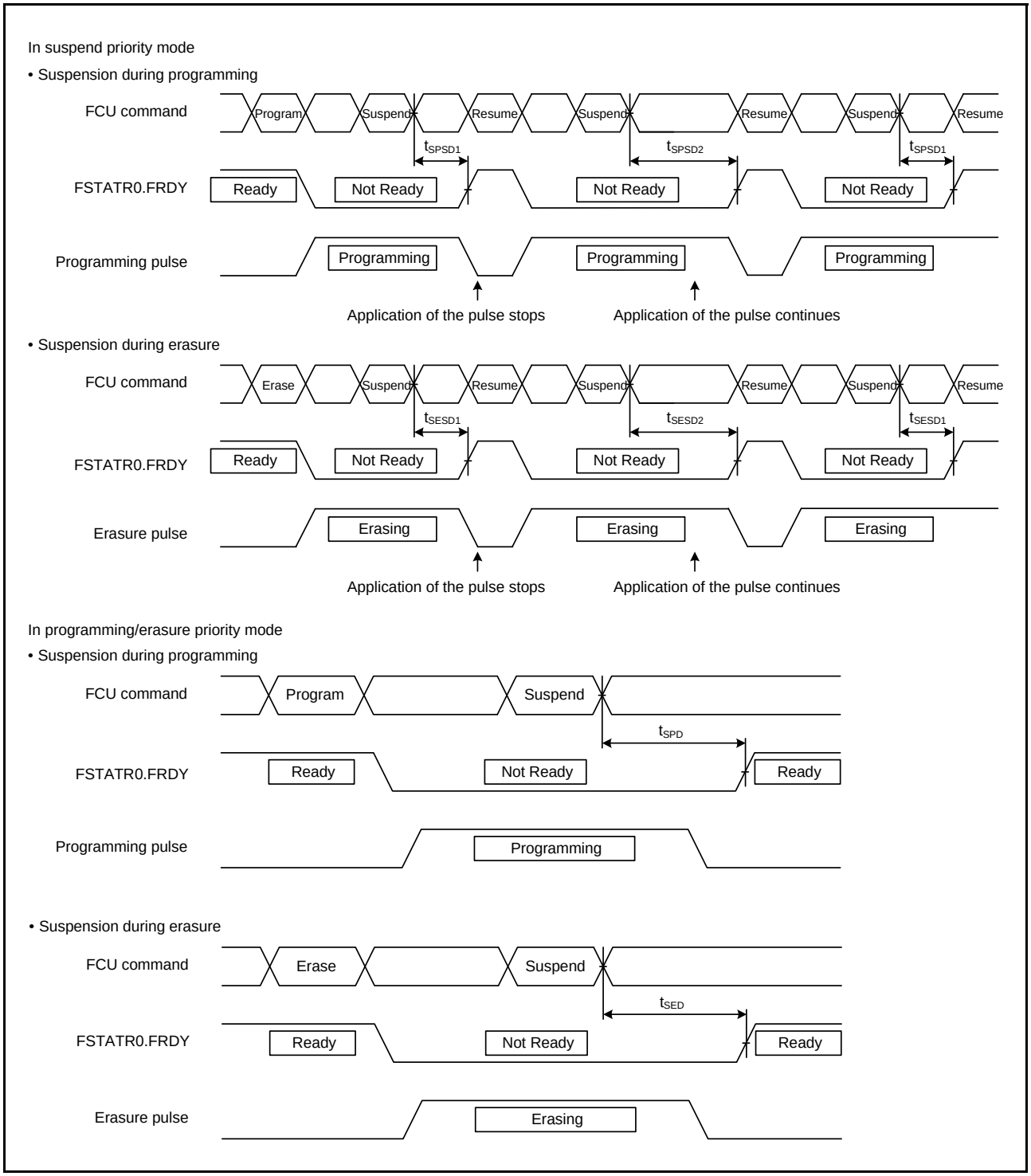


Figure 5.109 Flash Memory Program/Erase Suspend Timing

Rev.	Date	Description	
		Page	Summary
1.40	Feb 19, 2013	96	Table 5.11 DC Characteristics (10), changed
		105	Table 5.14 DC Characteristics (13), changed
		114	Table 5.17 DC Characteristics (16), changed
		115	Figure 5.31 Voltage Dependency in Software Standby Mode (SOFTCUT[2:0] Bits = 110b) (Reference Data) for Chip Version B with 768 Kbytes/1 Mbyte of Flash Memory and 100 to 145 Pins, changed
		116	Figure 5.32 Temperature Dependency in Software Standby Mode (SOFTCUT[2:0] Bits = 110b) (Reference Data) for Chip Version B with 768 Kbytes/1 Mbyte of Flash Memory and 100 to 145 Pins, changed
		118	Table 5.18 DC Characteristics (17), changed
		119, 120	Table 5.19 DC Characteristics (18), changed
		121 to 123	Figure 5.35 Voltage Dependency in High-Speed Operating Mode (Reference Data) for Chip Version B with 512 Kbytes or Less of Flash Memory and 144 and 145 Pins to Figure 5.39 Voltage Dependency in Low-Speed Operating Mode 2 (Reference Data) for Chip Version B with 512 Kbytes or Less of Flash Memory and 144 and 145 Pins, added
		124	Table 5.20 DC Characteristics (19), changed
		125 to 127	Figure 5.40 Voltage Dependency in Software Standby Mode (SOFTCUT[2:0] Bits = 110b) (Reference Data) for Chip Version B with 512 Kbytes or Less of Flash Memory and 144 and 145 Pins to Figure 5.43 Temperature Dependency in Deep Software Standby Mode (DEEPCUT1 Bit = 1) (Reference Data) for Chip Version B with 512 Kbytes or Less of Flash Memory and 144 and 145 Pins, added
		128	Table 5.22 DC Characteristics (21), changed, Note 2 added
		144	Table 5.44 Clock Timing: Note 5, changed
		154	Table 5.49 Bus Timing (1), Table 5.50 Bus Timing (2), changed
		155	Table 5.51 Bus Timing (3), changed
		160	Table 5.52 Bus Timing (Multiplexed Bus) (1), Table 5.53 Bus Timing (Multiplexed Bus) (2), changed
		161	Table 5.54 Bus Timing (Multiplexed Bus) (3), changed
		164	Table 5.56 Timing of On-Chip Peripheral Modules (2), changed
		166	Table 5.57 Timing of On-Chip Peripheral Modules (3), changed
		177	Table 5.61 A/D Conversion Characteristics (1), Note 3, deleted Figure 5.99 AVCC to AVREFH Voltage Range, added
		179	Table 5.64 A/D Conversion Characteristics (2), Note 3, Table 5.65 A/D Conversion Characteristics (3), Note 3, deleted
		186	Table 5.72 Power-on Reset Circuit and Voltage Detection Circuit Characteristics (2), changed
1.50	Oct 18, 2013	All	69-Pin WLBGA package products, added
		Features	
		1	SWBG0069LA-A 3.91 × 4.26mm, 0.40-mm pitch, ■ Applications, added
		1. Overview	
		2	1.1 Outline of Specifications, changed
		2 to 6	Table 1.1 Outline of Specifications, Note 2, changed
		7	Table 1.2 Comparison of Functions for Different Packages, changed
		8	Table 1.3 List of Products Chip Version A: D Version (Ta = -40 to +85°C), changed, Note, added
		9	Table 1.4 List of Products Chip Version B: D Version (Ta = -40 to +85°C), Note 1, changed, Note added
		10	Table 1.5 List of Products Chip Version B: G Version (Ta = -40 to +105°C), Note, changed, Note 1, deleted
		11	Table 1.6 List of Products Chip Version C: D Version (Ta = -40 to +85°C), Table 1.7 List of Products Chip Version C: G Version (Ta = -40 to +105°C), Note, changed
		12	Figure 1.1 How to Read the Product Part No., Memory Capacity, and Package Type, changed
		23	Figure 1.8 Pin Assignments of the 69-Pin WLBGA, added
		43, 44	Table 1.14 List of Pins and Pin Functions (69-Pin WLBGA), added
		5. Electrical Characteristics	
		134	Table 5.21 DC Characteristics (20) Note, added
		149, 150	Table 5.44 Clock Timing Note 6, Note 7, added
		183	Table 5.61 A/D Conversion Characteristics (1) Note, changed, Note 4, deleted
		184	Table 5.62 Channel Classification for A/D Converter, changed
		185	Table 5.64 A/D Conversion Characteristics (2) Note, changed
		Appendix 1. Package Dimensions	
		211	Figure E 69-Pin WLBGA (SWBG0069LA-A), added