Renesas Electronics America Inc - R5F52105BDFB#30 Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	EBI/EMI, I²C, SCI, SPI
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	122
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	20K x 8
Voltage - Supply (Vcc/Vdd)	1.62V ~ 5.5V
Data Converters	A/D 16x12b; D/A 2x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LFQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f52105bdfb-30

Table 1.1 Outline of Specifications (5 / 5)

Classification	Module/Function	Description
Packages	Chip version A	100-pin TFLGA (PTLG0100JA-A) 7 × 7 mm, 0.65-mm pitch 100-pin LQFP (PLQP0100KB-A) 14 × 14 mm, 0.5-mm pitch 80-pin LQFP (PLQP0080KB-A) 12 × 12 mm, 0.5-mm pitch 64-pin LQFP (PLQP0064KB-A) 10 × 10 mm, 0.5-mm pitch
	Chip version B	145-pin TFLGA (PTLG0145KA-A) 7 × 7 mm, 0.5-mm pitch 100-pin TFLGA (PTLG0100JA-A) 7 × 7 mm, 0.65-mm pitch 100-pin TFLGA (PTLG0100KA-A) 5.5 × 5.5 mm, 0.5-mm pitch 64-pin TFLGA (PTLG0064JA-A) 6 × 6 mm, 0.65-mm pitch 144-pin LQFP (PLQP0144KA-A) 20 × 20 mm, 0.5-mm pitch 100-pin LQFP (PLQP0100KB-A) 14 × 14 mm, 0.5-mm pitch 80-pin LQFP (PLQP0080KB-A) 12 × 12 mm, 0.5-mm pitch 80-pin LQFP (PLQP0080JA-A) 14 × 14 mm, 0.65-mm pitch 64-pin LQFP (PLQP0064KB-A) 10 × 10 mm, 0.5-mm pitch 64-pin LQFP (PLQP0064GA-A) 14 × 14 mm, 0.8-mm pitch 48-pin LQFP (PLQP0048KB-A) 7 × 7 mm, 0.5-mm pitch 69-pin WLBGA (SWBG0069LA-A) 3.91 × 4.26mm, 0.40-mm pitch
	Chip version C	100-pin TFLGA (PTLG0100JA-A) 7 × 7 mm, 0.65-mm pitch 100-pin LQFP (PLQP0100KB-A) 14 × 14 mm, 0.5-mm pitch 80-pin LQFP (PLQP0080KB-A) 12 × 12 mm, 0.5-mm pitch 80-pin LQFP (PLQP0080JA-A) 14 × 14 mm, 0.65-mm pitch 64-pin LQFP (PLQP0064KB-A) 10 × 10 mm, 0.5-mm pitch 64-pin LQFP (PLQP0064GA-A) 14 × 14 mm, 0.8-mm pitch
On-chip debugging system		E1 emulator (FINE interface)

Note 1. In chip version A of the part numbers below, port P17 is not 5 V tolerant. Therefore there is only one port in these products.
R5F52108ADFM, R5F52107ADFM, R5F52106ADFM, and R5F52105ADFM

Note 2. Please contact Renesas Electronics sales office for derating of operation under Ta = +85°C to +105°C. Derating is the systematic reduction of load for the sake of improved reliability.

Table 1.8 Pin Functions (2 / 4)

Classifications	Pin Name	I/O	Description
16-bit timer pulse unit	TIOCA0, TIOCB0 TIOCC0, TIOCD0	I/O	The TGRA0 to TGRD0 input capture input/output compare output/ PWM output pins.
	TIOCA1, TIOCB1	I/O	The TGRA1 and TGRB1 input capture input/output compare output/ PWM output pins.
	TIOCA2, TIOCB2	I/O	The TGRA2 and TGRB2 input capture input/output compare output/ PWM output pins.
	TIOCA3, TIOCB3 TIOCC3, TIOCD3	I/O	The TGRA3 to TGRD3 input capture input/output compare output/ PWM output pins.
	TIOCA4, TIOCB4	I/O	The TGRA4 and TGRB4 input capture input/output compare output/ PWM output pins.
	TIOCA5, TIOCB5	I/O	The TGRA5 and TGRB5 input capture input/output compare output/ PWM output pins.
	TCLKA, TCLKB TCLKC, TCLKD	Input	Input pins for external clock signals.
Multi-function timer pulse unit 2	MTIOC0A, MTIOC0B MTIOC0C, MTIOC0D	I/O	The TGRA0 to TGRD0 input capture input/output compare output/ PWM output pins.
	MTIOC1A, MTIOC1B	I/O	The TGRA1 and TGRB1 input capture input/output compare output/ PWM output pins.
	MTIOC2A, MTIOC2B	I/O	The TGRA2 and TGRB2 input capture input/output compare output/ PWM output pins.
	MTIOC3A, MTIOC3B MTIOC3C, MTIOC3D	I/O	The TGRA3 to TGRD3 input capture input/output compare output/ PWM output pins.
	MTIOC4A, MTIOC4B MTIOC4C, MTIOC4D	I/O	The TGRA4 to TGRD4 input capture input/output compare output/ PWM output pins.
	MTIC5U, MTIC5V, MTIC5W	Input	The TGRU5, TGRV5, and TGRW5 input capture input/external pulse input pins.
	MTCLKA, MTCLKB, MTCLKC, MTCLKD	Input	Input pins for the external clock.
Port output enable 2	POE0# to POE3#, POE8#	Input	Input pins for request signals to place the MTU pins in the high impedance state.
8-bit timer	TMO0 to TMO3	Output	Compare match output pins.
	TMCI0 to TMCI3	Input	Input pins for external clocks to be input to the counter.
	TMRI0 to TMRI3	Input	Input pins for the counter reset.
Realtime clock	RTCOUT	Output	Output pin for 1-Hz clock.
	RTCIC0 to RTCIC2	Input	Time capture event input pins.
Serial communications interface (SCIc)	• Asynchronous mode/clock synchronous mode		
	SCK0 to SCK11	I/O	Input/output pins for the clock
	RXD0 to RXD11	Input	Input pins for received data
	TXD0 to TXD11	Output	Output pins for transmitted data
	CTS0# to CTS11#	Input	Input pins for controlling the start of transmission and reception
	RTS0# to RTS11#	Output	Output pins for controlling the start of transmission and reception
	• Simple I^2C mode		
	SSCL0 to SSCL11	I/O	Input/output pins for the I^2C clock
	SSDA0 to SSDA11	I/O	Input/output pins for the I^2C data
	• Simple SPI mode		
	SCK0 to SCK11	I/O	Input/output pins for the clock
	SMISO0 to SMISO11	I/O	Input/output pins for slave transmission of data
	SMOSI0 to SMOSI11	I/O	Input/output pins for master transmission of data
	SS0# to SS11#	Input	Chip-select input pins

Table 1.11 List of Pins and Pin Functions (100-Pin TFLGA) (2 / 3)

Pin No.	Power Supply, Clock, System Control	I/O Port	External Bus	Timers (MTU, TMR, POE)	Communications (SCIc, SCId, RSPI, RIIC)	Others
E6		PA2	A2		RXD5/SMISO5/SSCL5/ SSLA3	
E7		PA6	A6	MTIC5V/MTCLKB/ TMCI3/POE2#	CTS5#/RTS5#/SS5#/ MOSIA	
E8		PA4	A4	MTIC5U/MTCLKA/ TMRI0	TXD5/SMOSI5/SSDA5/ SSLA0	IRQ5-DS/CVREFB1
E9		PA5	A5		RSPCKA	
E10		PA3	A3	MTIOC0D/MTCLKD	RXD5/SMISO5/SSCL5	IRQ6-DS/CMPB1
F1	EXTAL	P36				
F2	VCC					
F3		P35				NMI
F4		P32		MTIOC0C/TMO3	TXD6/SMOSI6/SSDA6	IRQ2-DS/RTCOUT/ RTCIC2
F5		P12		TMCI1	SCL	IRQ2
F6		PB3	A11	MTIOC0A/MTIOC4A/ TMO0/POE3#	SCK6	
F7		PB2	A10		CTS6#/RTS6#/SS6#	
F8		PB0	A8	MTIC5W	RXD6/SMISO6/SSCL6/ RSPCKA	
F9		PA7	A7		MISOA	
F10	VSS					
G1		P33		MTIOC0D/TMRI3/ POE3#	RXD6/SMISO6/SSCL6	IRQ3-DS
G2		P31		MTIOC4D/TMCI2	CTS1#/RTS1#/SS1#	IRQ1-DS/RTCIC1
G3		P30		MTIOC4B/TMRI3/ POE8#	RXD1/SMISO1/SSCL1	IRQ0-DS/RTCIC0
G4		P27	CS3#	MTIOC2B/TMCI3	SCK1	
G5	BCLK	P53				
G6		P52	RD#			
G7		PB5	A13	MTIOC2A/MTIOC1B/ TMRI1/POE1#	SCK9	
G8		PB4	A12		CTS9#/RTS9#/SS9#	
G9		PB1	A9	MTIOC0C/MTIOC4C/ TMCI0	TXD6/SMOSI6/SSDA6	IRQ4-DS
G10	VCC					
H1		P26	CS2#	MTIOC2A/TMO1	TXD1/SMOSI1/SSDA1	
H2		P25	CS1#	MTIOC4C/MTCLKB		ADTRG0#
H3		P16		MTIOC3C/MTIOC3D/ TMO2	TXD1/SMOSI1/SSDA1/ MOSIA/SCL-DS	IRQ6/RTCOUT/ ADTRG0#
H4		P15		MTIOC0B/MTCLKB/ TMCI2	RXD1/SMISO1/SSCL1	IRQ5
H5		P55	WAIT#	MTIOC4D/TMO3		
H6		P54	ALE	MTIOC4B/TMCI1		
H7		PC7	A23/CS0#	MTIOC3A/TMO2/ MTCLKB	TXD8/SMOSI8/SSDA8/ MISOA	CACREF
H8		PC6	A22/CS1#	MTIOC3C/MTCLKA/ TMCI2	RXD8/SMISO8/SSCL8/ MOSIA	
H9		PB6	A14	MTIOC3D	RXD9/SMISO9/SSCL9	
H10		PB7	A15	MTIOC3B	TXD9/SMOSI9/SSDA9	
J1		P24	CS0#	MTIOC4A/MTCLKA/ TMRI1		
J2		P21		MTIOC1B/TMCI0	RXD0/SMISO0/SSCL0	
J3		P17		MTIOC3A/MTIOC3B/ TMO1/POE8#	SCK1/MISOA/ SDA-DS	IRQ7

Table 1.12 List of Pins and Pin Functions (100-Pin LQFP) (1 / 3)

Pin No.	Power Supply, Clock, System Control	I/O Port	External Bus	Timers (MTU, TMR, POE)	Communications (SCIc, SCId, RSPI, RIIC)	Others
1	VREFH					
2		P03				DA0
3	VREFL					
4		PJ3		MTIOC3C	CTS6#/RTS6#/SS6#	
5	VCL					
6		PJ1		MTIOC3A		
7	MD					FINED
8	XCIN					
9	XCOUT					
10	RES#					
11	XTAL	P37				
12	VSS					
13	EXTAL	P36				
14	VCC					
15		P35				NMI
16		P34		MTIOC0A/TMCI3/ POE2#	SCK6	IRQ4
17		P33		MTIOC0D/TMRI3/ POE3#	RXD6/SMISO6/SSCL6	IRQ3-DS
18		P32		MTIOC0C/TMO3	TXD6/SMOSI6/SSDA6	IRQ2-DS/RTCOUT/ RTCIC2
19		P31		MTIOC4D/TMCI2	CTS1#/RTS1#/SS1#	IRQ1-DS/RTCIC1
20		P30		MTIOC4B/TMRI3/ POE8#	RXD1/SMISO1/SSCL1	IRQ0-DS/RTCIC0
21		P27	CS3#	MTIOC2B/TMCI3	SCK1	
22		P26	CS2#	MTIOC2A/TMO1	TXD1/SMOSI1/SSDA1	
23		P25	CS1#	MTIOC4C/MTCLKB		ADTRG0#
24		P24	CS0#	MTIOC4A/MTCLKA/ TMRI1		
25		P23		MTIOC3D/MTCLKD	CTS0#/RTS0#/SS0#	
26		P22		MTIOC3B/MTCLKC/ TMO0	SCK0	
27		P21		MTIOC1B/TMCI0	RXD0/SMISO0/SSCL0	
28		P20		MTIOC1A/TMRI0	TXD0/SMOSI0/SSDA0	
29		P17		MTIOC3A/MTIOC3B/ TMO1/POE8#	SCK1/MISOA/ SDA-DS	IRQ7
30		P16		MTIOC3C/MTIOC3D/ TMO2	TXD1/SMOSI1/SSDA1/ MOSIA/SCL-DS	IRQ6/RTCOUT/ ADTRG0#
31		P15		MTIOC0B/MTCLKB/ TMCI2	RXD1/SMISO1/SSCL1	IRQ5
32		P14		MTIOC3A/MTCLKA/ TMRI2	CTS1#/RTS1#/SS1#	IRQ4
33		P13		MTIOC0B/TMO3	SDA	IRQ3
34		P12		TMCI1	SCL	IRQ2
35		PH3		TMCI0		
36		PH2		TMRI0		IRQ1
37		PH1		TMO0		IRQ0
38		PH0				CACREF
39		P55	WAIT#	MTIOC4D/TMO3		
40		P54	ALE	MTIOC4B/TMCI1		
41	BCLK	P53				

2.1 General-Purpose Registers (R0 to R15)

This CPU has sixteen general-purpose registers (R0 to R15). R1 to R15 can be used as data registers or address registers. R0, a general-purpose register, also functions as the stack pointer (SP). The stack pointer is switched to operate as the interrupt stack pointer (ISP) or user stack pointer (USP) by the value of the stack pointer select bit (U) in the processor status word (PSW).

2.2 Control Registers

(1) Interrupt Stack Pointer (ISP)/User Stack Pointer (USP)

The stack pointer (SP) can be either of two types, the interrupt stack pointer (ISP) or the user stack pointer (USP). Whether the stack pointer operates as the ISP or USP depends on the value of the stack pointer select bit (U) in the processor status word (PSW).
Set the ISP or USP to a multiple of four, as this reduces the numbers of cycles required to execute interrupt sequences and instructions entailing stack manipulation.

(2) Interrupt Table Register (INTB)

The interrupt table register (INTB) specifies the address where the relocatable vector table starts.

(3) Program Counter (PC)

The program counter (PC) indicates the address of the instruction being executed.

(4) Processor Status Word (PSW)

The processor status word (PSW) indicates the results of instruction execution or the state of the CPU.

(5) Backup PC (BPC)

The backup PC (BPC) is provided to speed up response to interrupts.
After a fast interrupt has been generated, the contents of the program counter (PC) are saved in the BPC register.

(6) Backup PSW (BPSW)

The backup PSW (BPSW) is provided to speed up response to interrupts.
After a fast interrupt has been generated, the contents of the processor status word (PSW) are saved in the BPSW. The allocation of bits in the BPSW corresponds to that in the PSW.

(7) Fast Interrupt Vector Register (FINTV)

The fast interrupt vector register (FINTV) is provided to speed up response to interrupts.
The FINTV register specifies a branch destination address when a fast interrupt has been generated.

2.3 Register Associated with DSP Instructions

(1) Accumulator (ACC)

The accumulator (ACC) is a 64-bit register used for DSP instructions. The accumulator is also used for the multiply and multiply-and-accumulate instructions; EMUL, EMULU, MUL, and RMPA, in which case the prior value in the accumulator is modified by execution of the instruction.
Use the MVTACHI and MVTACLO instructions for writing to the accumulator. The MVTACHI and MVTACLO instructions write data to the higher-order 32 bits (bits 63 to 32) and the lower-order 32 bits (bits 31 to 0), respectively.
Use the MVFACHI and MVFACMI instructions for reading data from the accumulator. The MVFACHI and MVFACMI instructions read data from the higher-order 32 bits (bits 63 to 32) and the middle 32 bits (bits 47 to 16), respectively.

Table 4.1 List of I/O Registers (Address Order) (6 / 29)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles ICLK ≥ PCLK	Number of Access Cycles ICLK < PCLK
0008 70E4h	ICU	Interrupt request register 228	IR228	8	8		2 ICLK
0008 70E5h	ICU	Interrupt request register 229	IR229	8	8		2 ICLK
0008 70E6h	ICU	Interrupt request register 230	IR230	8	8		2 ICLK
0008 70E7h	ICU	Interrupt request register 231	IR231	8	8		2 ICLK
0008 70E8h	ICU	Interrupt request register 232	IR232	8	8		2 ICLK
0008 70E9h	ICU	Interrupt request register 233	IR233	8	8		2 ICLK
0008 70EAh	ICU	Interrupt request register 234	IR234	8	8		2 ICLK
0008 70EBh	ICU	Interrupt request register 235	IR235	8	8		2 ICLK
0008 70ECh	ICU	Interrupt request register 236	IR236	8	8		2 ICLK
0008 70EDh	ICU	Interrupt request register 237	IR237	8	8		2 ICLK
0008 70EEh	ICU	Interrupt request register 238	IR238	8	8		2 ICLK
0008 70EFh	ICU	Interrupt request register 239	IR239	8	8		2 ICLK
0008 70F0h	ICU	Interrupt request register 240	IR240	8	8		2 ICLK
0008 70F1h	ICU	Interrupt request register 241	IR241	8	8		2 ICLK
0008 70F2h	ICU	Interrupt request register 242	IR242	8	8		2 ICLK
0008 70F3h	ICU	Interrupt request register 243	IR243	8	8		2 ICLK
0008 70F4h	ICU	Interrupt request register 244	IR244	8	8		2 ICLK
0008 70F5h	ICU	Interrupt request register 245	IR245	8	8		2 ICLK
0008 70F6h	ICU	Interrupt request register 246	IR246	8	8		2 ICLK
0008 70F7h	ICU	Interrupt request register 247	IR247	8	8		2 ICLK
0008 70F8h	ICU	Interrupt request register 248	IR248	8	8		2 ICLK
0008 70F9h	ICU	Interrupt request register 249	IR249	8	8		2 ICLK
0008 70FAh	ICU	Interrupt request register 250	IR250	8	8		2 ICLK
0008 70FBh	ICU	Interrupt request register 251	IR251	8	8		2 ICLK
0008 70FCh	ICU	Interrupt request register 252	IR252	8	8		2 ICLK
0008 70FDh	ICU	Interrupt request register 253	IR253	8	8		2 ICLK
0008 711Bh	ICU	DTC activation enable register 027	DTCER027	8	8		2 ICLK
0008 711Ch	ICU	DTC activation enable register 028	DTCER028	8	8		2 ICLK
0008 711Dh	ICU	DTC activation enable register 029	DTCER029	8	8		2 ICLK
0008 711Eh	ICU	DTC activation enable register 030	DTCER030	8	8		2 ICLK
0008 711Fh	ICU	DTC activation enable register 031	DTCER031	8	8		2 ICLK
0008 712Dh	ICU	DTC activation enable register 045	DTCER045	8	8		2 ICLK
0008 712Eh	ICU	DTC activation enable register 046	DTCER046	8	8		2 ICLK
0008 713Ah	ICU	DTC activation enable register 058	DTCER058	8	8		2 ICLK
0008 713Bh	ICU	DTC activation enable register 059	DTCER059	8	8		2 ICLK
0008 7140h	ICU	DTC activation enable register 064	DTCER064	8	8		2 ICLK
0008 7141h	ICU	DTC activation enable register 065	DTCER065	8	8		2 ICLK
0008 7142h	ICU	DTC activation enable register 066	DTCER066	8	8		2 ICLK
0008 7143h	ICU	DTC activation enable register 067	DTCER067	8	8		2 ICLK
0008 7144h	ICU	DTC activation enable register 068	DTCER068	8	8		2 ICLK
0008 7145h	ICU	DTC activation enable register 069	DTCER069	8	8		2 ICLK
0008 7146h	ICU	DTC activation enable register 070	DTCER070	8	8		2 ICLK
0008 7147h	ICU	DTC activation enable register 071	DTCER071	8	8		2 ICLK
0008 7166h	ICU	DTC activation enable register 102	DTCER102	8	8		2 ICLK
0008 7167h	ICU	DTC activation enable register 103	DTCER103	8	8		2 ICLK
0008 716Ah	ICU	DTC activation enable register 106	DTCER106	8	8		2 ICLK
0008 716Bh	ICU	DTC activation enable register 107	DTCER107	8	8		2 ICLK
0008 7172h	ICU	DTC activation enable register 114	DTCER114	8	8		2 ICLK
0008 7173h	ICU	DTC activation enable register 115	DTCER115	8	8		2 ICLK
0008 7174h	ICU	DTC activation enable register 116	DTCER116	8	8		2 ICLK
0008 7175h	ICU	DTC activation enable register 117	DTCER117	8	8		2 ICLK

Table 4.1 List of I/O Registers (Address Order) (12 / 29)

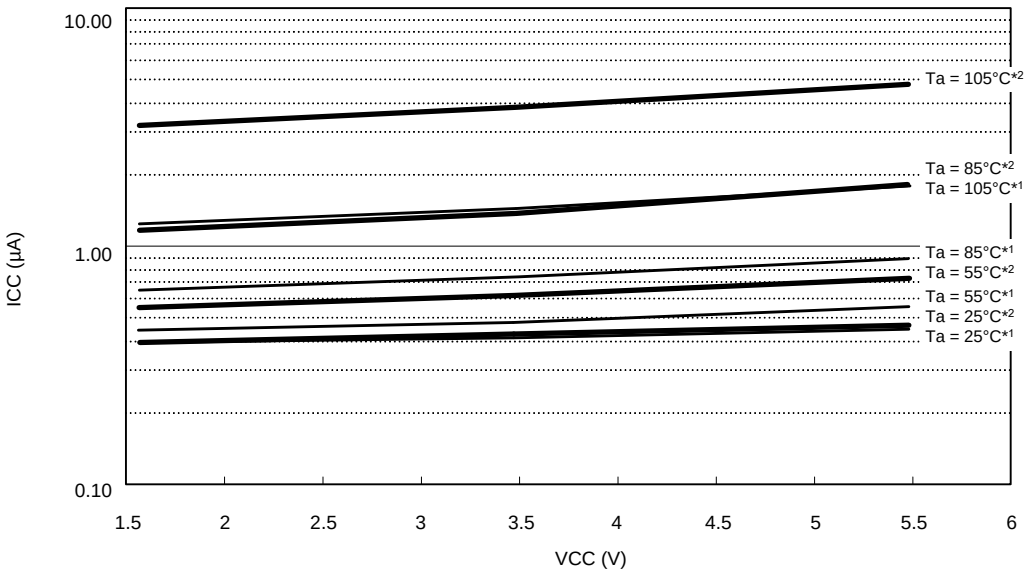
Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles: ICLK ≥ PCLK	Number of Access Cycles: ICLK < PCLK
0008 8122h	TPU1	Timer I/O control register	TIOR	8	8	2, 3 PCLKB	2 ICLK
0008 8124h	TPU1	Timer interrupt enable register	TIER	8	8	2, 3 PCLKB	2 ICLK
0008 8125h	TPU1	Timer status register	TSR	8	8	2, 3 PCLKB	2 ICLK
0008 8126h	TPU1	Timer counter	TCNT	16	16	2, 3 PCLKB	2 ICLK
0008 8128h	TPU1	Timer general register A	TGRA	16	16	2, 3 PCLKB	2 ICLK
0008 812Ah	TPU1	Timer general register B	TGRB	16	16	2, 3 PCLKB	2 ICLK
0008 8130h	TPU2	Timer control register	TCR	8	8	2, 3 PCLKB	2 ICLK
0008 8131h	TPU2	Timer mode register	TMDR	8	8	2, 3 PCLKB	2 ICLK
0008 8132h	TPU2	Timer I/O control register	TIOR	8	8	2, 3 PCLKB	2 ICLK
0008 8134h	TPU2	Timer interrupt enable register	TIER	8	8	2, 3 PCLKB	2 ICLK
0008 8135h	TPU2	Timer status register	TSR	8	8	2, 3 PCLKB	2 ICLK
0008 8136h	TPU2	Timer counter	TCNT	16	16	2, 3 PCLKB	2 ICLK
0008 8138h	TPU2	Timer general register A	TGRA	16	16	2, 3 PCLKB	2 ICLK
0008 813Ah	TPU2	Timer general register B	TGRB	16	16	2, 3 PCLKB	2 ICLK
0008 8140h	TPU3	Timer control register	TCR	8	8	2, 3 PCLKB	2 ICLK
0008 8141h	TPU3	Timer mode register	TMDR	8	8	2, 3 PCLKB	2 ICLK
0008 8142h	TPU3	Timer I/O control register H	TIORH	8	8	2, 3 PCLKB	2 ICLK
0008 8143h	TPU3	Timer I/O control register L	TIORL	8	8	2, 3 PCLKB	2 ICLK
0008 8144h	TPU3	Timer interrupt enable register	TIER	8	8	2, 3 PCLKB	2 ICLK
0008 8145h	TPU3	Timer status register	TSR	8	8	2, 3 PCLKB	2 ICLK
0008 8146h	TPU3	Timer counter	TCNT	16	16	2, 3 PCLKB	2 ICLK
0008 8148h	TPU3	Timer general register A	TGRA	16	16	2, 3 PCLKB	2 ICLK
0008 814Ah	TPU3	Timer general register B	TGRB	16	16	2, 3 PCLKB	2 ICLK
0008 814Ch	TPU3	Timer general register C	TGRC	16	16	2, 3 PCLKB	2 ICLK
0008 814Eh	TPU3	Timer general register D	TGRD	16	16	2, 3 PCLKB	2 ICLK
0008 8150h	TPU4	Timer control register	TCR	8	8	2, 3 PCLKB	2 ICLK
0008 8151h	TPU4	Timer mode register	TMDR	8	8	2, 3 PCLKB	2 ICLK
0008 8152h	TPU4	Timer I/O control register	TIOR	8	8	2, 3 PCLKB	2 ICLK
0008 8154h	TPU4	Timer interrupt enable register	TIER	8	8	2, 3 PCLKB	2 ICLK
0008 8155h	TPU4	Timer status register	TSR	8	8	2, 3 PCLKB	2 ICLK
0008 8156h	TPU4	Timer counter	TCNT	16	16	2, 3 PCLKB	2 ICLK
0008 8158h	TPU4	Timer general register A	TGRA	16	16	2, 3 PCLKB	2 ICLK
0008 815Ah	TPU4	Timer general register B	TGRB	16	16	2, 3 PCLKB	2 ICLK
0008 8160h	TPU5	Timer control register	TCR	8	8	2, 3 PCLKB	2 ICLK
0008 8161h	TPU5	Timer mode register	TMDR	8	8	2, 3 PCLKB	2 ICLK
0008 8162h	TPU5	Timer I/O control register	TIOR	8	8	2, 3 PCLKB	2 ICLK
0008 8164h	TPU5	Timer interrupt enable register	TIER	8	8	2, 3 PCLKB	2 ICLK
0008 8165h	TPU5	Timer status register	TSR	8	8	2, 3 PCLKB	2 ICLK
0008 8166h	TPU5	Timer counter	TCNT	16	16	2, 3 PCLKB	2 ICLK
0008 8168h	TPU5	Timer general register A	TGRA	16	16	2, 3 PCLKB	2 ICLK
0008 816Ah	TPU5	Timer general register B	TGRB	16	16	2, 3 PCLKB	2 ICLK
0008 8200h	TMR0	Timer control register	TCR	8	8	2, 3 PCLKB	2 ICLK
0008 8201h	TMR1	Timer counter control register	TCR	8	8	2, 3 PCLKB	2 ICLK
0008 8202h	TMR0	Timer control/status register	TCSR	8	8	2, 3 PCLKB	2 ICLK
0008 8203h	TMR1	Timer control/status register	TCSR	8	8	2, 3 PCLKB	2 ICLK
0008 8204h	TMR0	Time constant register A	TCORA	8	8	2, 3 PCLKB	2 ICLK
0008 8205h	TMR1	Time constant register A	TCORA	8	8*1	2, 3 PCLKB	2 ICLK
0008 8206h	TMR0	Time constant register B	TCORB	8	8	2, 3 PCLKB	2 ICLK
0008 8207h	TMR1	Time constant register B	TCORB	8	8*1	2, 3 PCLKB	2 ICLK
0008 8208h	TMR0	Timer counter	TCNT	8	8	2, 3 PCLKB	2 ICLK
0008 8209h	TMR1	Timer counter	TCNT	8	8*1	2, 3 PCLKB	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (21 / 29)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles: ICLK ≥ PCLK	Number of Access Cycles: ICLK < PCLK
0008 B11Dh	ELC	Event link setting register 28	ELSR28	8	8	2, 3 PCLKB	2 ICLK
0008 B11Eh	ELC	Event link setting register 29	ELSR29	8	8	2, 3 PCLKB	2 ICLK
0008 B11Fh	ELC	Event link option setting register A	ELOPA	8	8	2, 3 PCLKB	2 ICLK
0008 B120h	ELC	Event link option setting register B	ELOPB	8	8	2, 3 PCLKB	2 ICLK
0008 B121h	ELC	Event link option setting register C	ELOPC	8	8	2, 3 PCLKB	2 ICLK
0008 B122h	ELC	Event link option setting register D	ELOPD	8	8	2, 3 PCLKB	2 ICLK
0008 B123h	ELC	Port group setting register 1	PGR1	8	8	2, 3 PCLKB	2 ICLK
0008 B124h	ELC	Port group setting register 2	PGR2	8	8	2, 3 PCLKB	2 ICLK
0008 B125h	ELC	Port group control register 1	PGC1	8	8	2, 3 PCLKB	2 ICLK
0008 B126h	ELC	Port group control register 2	PGC2	8	8	2, 3 PCLKB	2 ICLK
0008 B127h	ELC	Port buffer register 1	PDBF1	8	8	2, 3 PCLKB	2 ICLK
0008 B128h	ELC	Port buffer register 2	PDBF2	8	8	2, 3 PCLKB	2 ICLK
0008 B129h	ELC	Event link port setting register 0	PEL0	8	8	2, 3 PCLKB	2 ICLK
0008 B12Ah	ELC	Event link port setting register 1	PEL1	8	8	2, 3 PCLKB	2 ICLK
0008 B12Bh	ELC	Event link port setting register 2	PEL2	8	8	2, 3 PCLKB	2 ICLK
0008 B12Ch	ELC	Event link port setting register 3	PEL3	8	8	2, 3 PCLKB	2 ICLK
0008 B12Dh	ELC	Event link software event generation register	ELSEGR	8	8	2, 3 PCLKB	2 ICLK
0008 B300h	SCI12	Serial mode register	SMR	8	8	2, 3 PCLKB	2 ICLK
0008 B301h	SCI12	Bit rate register	BRR	8	8	2, 3 PCLKB	2 ICLK
0008 B302h	SCI12	Serial control register	SCR	8	8	2, 3 PCLKB	2 ICLK
0008 B303h	SCI12	Transmit data register	TDR	8	8	2, 3 PCLKB	2 ICLK
0008 B304h	SCI12	Serial status register	SSR	8	8	2, 3 PCLKB	2 ICLK
0008 B305h	SCI12	Receive data register	RDR	8	8	2, 3 PCLKB	2 ICLK
0008 B306h	SCI12	Smart card mode register	SCMR	8	8	2, 3 PCLKB	2 ICLK
0008 B307h	SCI12	Serial extended mode register	SEMR	8	8	2, 3 PCLKB	2 ICLK
0008 B308h	SCI12	Noise filter setting register	SNFR	8	8	2, 3 PCLKB	2 ICLK
0008 B309h	SCI12	I^2C mode register 1	SIMR1	8	8	2, 3 PCLKB	2 ICLK
0008 B30Ah	SCI12	I^2C mode register 2	SIMR2	8	8	2, 3 PCLKB	2 ICLK
0008 B30Bh	SCI12	I^2C mode register 3	SIMR3	8	8	2, 3 PCLKB	2 ICLK
0008 B30Ch	SCI12	I^2C status register	SISR	8	8	2, 3 PCLKB	2 ICLK
0008 B30Dh	SCI12	SPI mode register	SPMR	8	8	2, 3 PCLKB	2 ICLK
0008 B320h	SCI12	Extended serial mode enable register	ESMER	8	8	2, 3 PCLKB	2 ICLK
0008 B321h	SCI12	Control register 0	CR0	8	8	2, 3 PCLKB	2 ICLK
0008 B322h	SCI12	Control register 1	CR1	8	8	2, 3 PCLKB	2 ICLK
0008 B323h	SCI12	Control register 2	CR2	8	8	2, 3 PCLKB	2 ICLK
0008 B324h	SCI12	Control register 3	CR3	8	8	2, 3 PCLKB	2 ICLK
0008 B325h	SCI12	Port control register	PCR	8	8	2, 3 PCLKB	2 ICLK
0008 B326h	SCI12	Interrupt control register	ICR	8	8	2, 3 PCLKB	2 ICLK
0008 B327h	SCI12	Status register	STR	8	8	2, 3 PCLKB	2 ICLK
0008 B328h	SCI12	Status clear register	STCR	8	8	2, 3 PCLKB	2 ICLK
0008 B329h	SCI12	Control Field 0 data register	CF0DR	8	8	2, 3 PCLKB	2 ICLK
0008 B32Ah	SCI12	Control Field 0 compare enable register	CF0CR	8	8	2, 3 PCLKB	2 ICLK
0008 B32Bh	SCI12	Control Field 0 receive data register	CF0RR	8	8	2, 3 PCLKB	2 ICLK
0008 B32Ch	SCI12	Primary control field 1 data register	PCF1DR	8	8	2, 3 PCLKB	2 ICLK
0008 B32Dh	SCI12	Secondary control field 1 data register	SCF1DR	8	8	2, 3 PCLKB	2 ICLK
0008 B32Eh	SCI12	Control field 1 compare enable register	CF1CR	8	8	2, 3 PCLKB	2 ICLK
0008 B32Fh	SCI12	Control field 1 receive data register	CF1RR	8	8	2, 3 PCLKB	2 ICLK
0008 B330h	SCI12	Timer control register	TCR	8	8	2, 3 PCLKB	2 ICLK
0008 B331h	SCI12	Timer mode register	TMR	8	8	2, 3 PCLKB	2 ICLK
0008 B332h	SCI12	Timer prescaler register	TPRE	8	8	2, 3 PCLKB	2 ICLK
0008 B333h	SCI12	Timer count register	TCNT	8	8	2, 3 PCLKB	2 ICLK

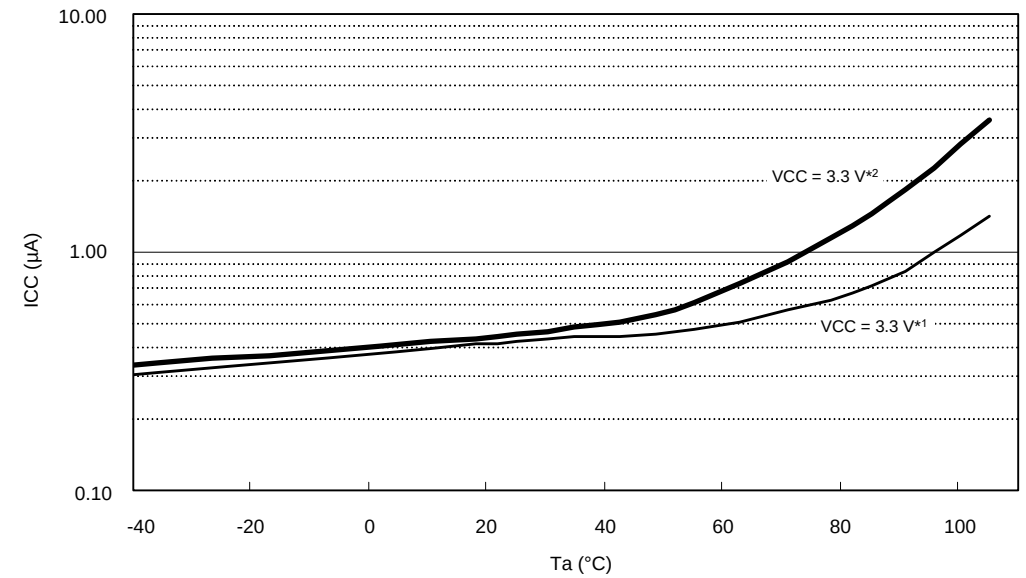
Item					Symbol	Typ.	Max.	Unit	Test Conditions
Supply current*1	Low-speed operating mode 1	Normal operating mode	No peripheral operation*7	ICLK = 8 MHz	I_{CC}	2.1	—	mA	
				ICLK = 4 MHz		1.7	—		
				ICLK = 2 MHz		1.5	—		
			All peripheral operation: Normal*8	ICLK = 8 MHz		7.3	—		
				ICLK = 4 MHz		4.5	—		
				ICLK = 2 MHz		3.1	—		
			All peripheral operation: Max.*7	ICLK = 8 MHz		—	12		
				ICLK = 4 MHz		—	—		
				ICLK = 2 MHz		—	—		
		Sleep mode	No peripheral operation	ICLK = 8 MHz		1.5	—		
				ICLK = 4 MHz		1.4	—		
				ICLK = 2 MHz		1.3	—		
			All peripheral operation: Normal	ICLK = 8 MHz		4.1	—		
				ICLK = 4 MHz		3.0	—		
				ICLK = 2 MHz		2.3	—		
		All-module clock stop mode		ICLK = 8 MHz		1.4	—		
				ICLK = 4 MHz		1.3	—		
				ICLK = 2 MHz		1.2	—		
	Low-speed operating mode 2	Normal operating mode	No peripheral operation*9	ICLK = 32 kHz		0.022	—		
			All peripheral operation: Normal*10	ICLK = 32 kHz		0.06	—		
			All peripheral operation: Max.*10	ICLK = 32 kHz		—	3*11		
		Sleep mode	No peripheral operation	ICLK = 32 kHz		0.017	—		
			All peripheral operation: Normal	ICLK = 32 kHz		0.036	—		
		All-module clock stop mode				0.017	—		

Note 1. Supply current values do not include output charge/discharge current from all pins. The values apply when internal pull-up MOSs are in the off state.
Note 2. Clock supply to the peripheral functions is stopped. This does not include BGO operation. The clock source is PLL and the VCO oscillation frequency is 64 MHz. BCLK, FCLK, and PCLK are set to divided by 64.
Note 3. Clock supply to the peripheral functions is stopped. This does not include BGO operation. The clock source is HOCO and the oscillation frequency is 40 MHz. BCLK, FCLK, and PCLK are set to divided by 64.
Note 4. Clocks are supplied to the peripheral functions. This does not include BGO operation. The clock source is PLL and the VCO oscillation frequency is 64 MHz. BCLK, FCLK, and PCLK are ICLK divided by 1.
Note 5. Clocks are supplied to the peripheral functions. This does not include BGO operation. The clock source is HOCO and the oscillation frequency is 40 MHz. BCLK, FCLK, and PCLK are ICLK divided by 1.
Note 6. This is the increase if data is programmed to or erasing from the ROM or E2 DataFlash during program execution.
Note 7. Clock supply to the peripheral functions is stopped. This does not include BGO operation. The clock source is HOCO and the oscillation frequency is 32 MHz. BCLK, FCLK, and PCLK are set to divided by 64.
Note 8. Clocks are supplied to the peripheral functions. This does not include BGO operation. The clock source is HOCO and the oscillation frequency is 32 MHz. BCLK, FCLK, and PCLK are ICLK divided by 1.
Note 9. Clock supply to the peripheral functions is stopped. This does not include BGO operation. The clock source is the sub oscillation circuit. BCLK, FCLK, and PCLK are set to divided by 64.
Note 10. Clocks are supplied to the peripheral functions. This does not include BGO operation. The clock source is the sub oscillation circuit. BCLK, FCLK, and PCLK are ICLK divided by 1.
Note 11. Value when the main clock continues oscillating at 12.5 MHz.



Note 1. Average value of the tested middle samples during product evaluation.
Note 2. Average value of the tested upper-limit samples during product evaluation.

Figure 5.42 Voltage Dependency in Deep Software Standby Mode (DEEPCUT1 Bit = 1) (Reference Data) for Chip Version B with 512 Kbytes or Less of Flash Memory and 144 and 145 Pins



Note 1. Average value of the tested middle samples during product evaluation.
Note 2. Average value of the tested upper-limit samples during product evaluation.

Figure 5.43 Temperature Dependency in Deep Software Standby Mode (DEEPCUT1 Bit = 1) (Reference Data) for Chip Version B with 512 Kbytes or Less of Flash Memory and 144 and 145 Pins

Table 5.21 DC Characteristics (20)

Conditions: VCC = AVCC0 = 1.62 to 5.5 V, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +105°C

Item	Symbol	Typ.	Max.	Unit	Test Conditions
Permissible total consumption power*1	Pd	—	350	mW	Ta = –40 to 85°C
		—	150		85°C < Ta ≤ 105°C

Note: • Please contact Renesas Electronics sales office for derating of operation under Ta = +85°C to +105°C. Derating is the systematic reduction of load for the sake of improved reliability.
Note 1. Total power dissipated by the entire chip (including output currents)

Table 5.22 DC Characteristics (21)

Conditions: VCC = AVCC0 = 1.62 to 5.5 V, VREFH = 1.8 to AVCC0, VREFH0 = 1.62 to AVCC0,
VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Analog power supply current	During A/D conversion	I_{AVCC0}	—	1.0	3.2	mA	
	Temperature sensor operating, waiting for A/D conversion		—	60	200	µA	
	During D/A conversion (per channel)	I_{VREFH}*1	—	0.25	0.75	mA	
	Waiting for A/D, D/A conversion (all units)*2	—	—	0.2	5.0	µA	
Reference power supply current	During A/D conversion	I_{VREFH0}	—	0.1	0.2	mA	
	Waiting for A/D conversion		—	0.2	0.4	µA	

Note: • The values for A/D conversion apply when the sample and hold circuit is not in use.
Note 1. The reference power supply current is included in the power supply current value for D/A conversion.
Note 2. The value is the total value of I_{AVCC0} and I_{VREFH}.

Table 5.23 DC Characteristics (22)

Conditions: VCC = AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +105°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
RAM standby voltage	V_{RAM}	1.62	—	—	V	

Table 5.24 DC Characteristics (23)

Conditions: VCC = AVCC0 = 0 to 5.5 V, VREFH = VREFH0 = 0 to AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V,
T_a = –40 to +105°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
VCC rising gradient	SrVCC	0.02	—	20	ms/V	At cold start

[Chip versions B and C]

Table 5.31 Output Values of Voltage (4)

Conditions: VCC = AVCC0 = 2.7 to 4.0 V, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +105°C

Item			Symbol	Min.	Max.	Unit	Test Conditions
Output low	All output pins (other than RIIC)	Normal output mode	V_{OL}	—	0.5	V	I_{OL} = 1.0 mA
		High-drive output mode		—	0.5		I_{OL} = 2.0 mA
	RIIC pins			—	0.4		I_{OL} = 3.0 mA
				—	0.6		I_{OL} = 6.0 mA
Output high	All output pins	Normal output mode	V_{OH}	VCC – 0.5	—	V	I_{OH} = –1.0 mA
		High-drive output mode		VCC – 0.5	—		I_{OH} = –2.0 mA

[Chip versions B and C]

Table 5.32 Output Values of Voltage (5)

Conditions: VCC = AVCC0 = 4.0 to 5.5 V, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +105°C

Item			Symbol	Min.	Max.	Unit	Test Conditions
Output low	All output pins (other than RIIC)	Normal output mode	V_{OL}	—	0.8	V	I_{OL} = 2.0 mA
		High-drive output mode		—	0.8		I_{OL} = 4.0 mA
	RIIC pins			—	0.4		I_{OL} = 3.0 mA
				—	0.6		I_{OL} = 6.0 mA
Output high	All output pins	Normal output mode	V_{OH}	VCC – 0.8	—	V	I_{OH} = –2.0 mA
		High-drive output mode		VCC – 0.8	—		I_{OH} = –4.0 mA

5.2.1 Standard I/O Pin Output Characteristics (1)

Figure 5.45 to Figure 5.49 show the characteristics when normal output is selected by the drive capacity control register.

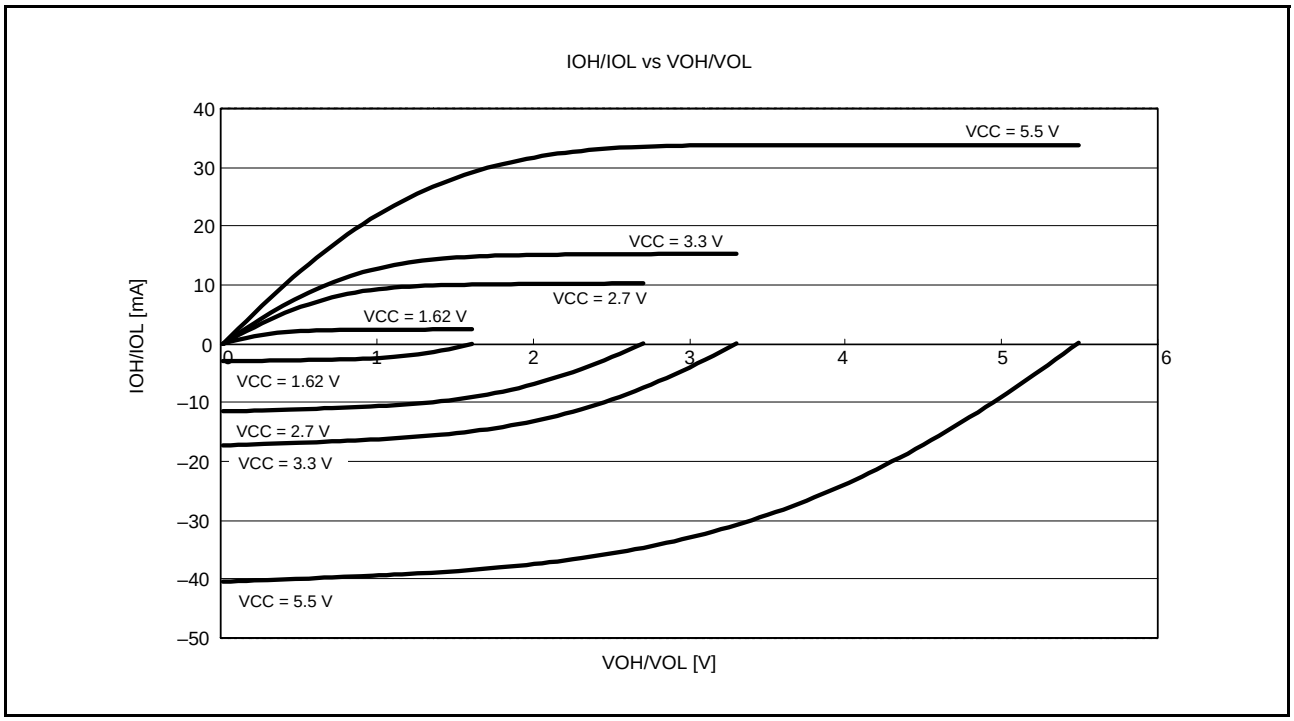


Figure 5.45 VOH/VOL and IOH/IOL Voltage Characteristics at Ta = 25°C when Normal Output is Selected (Reference Data)

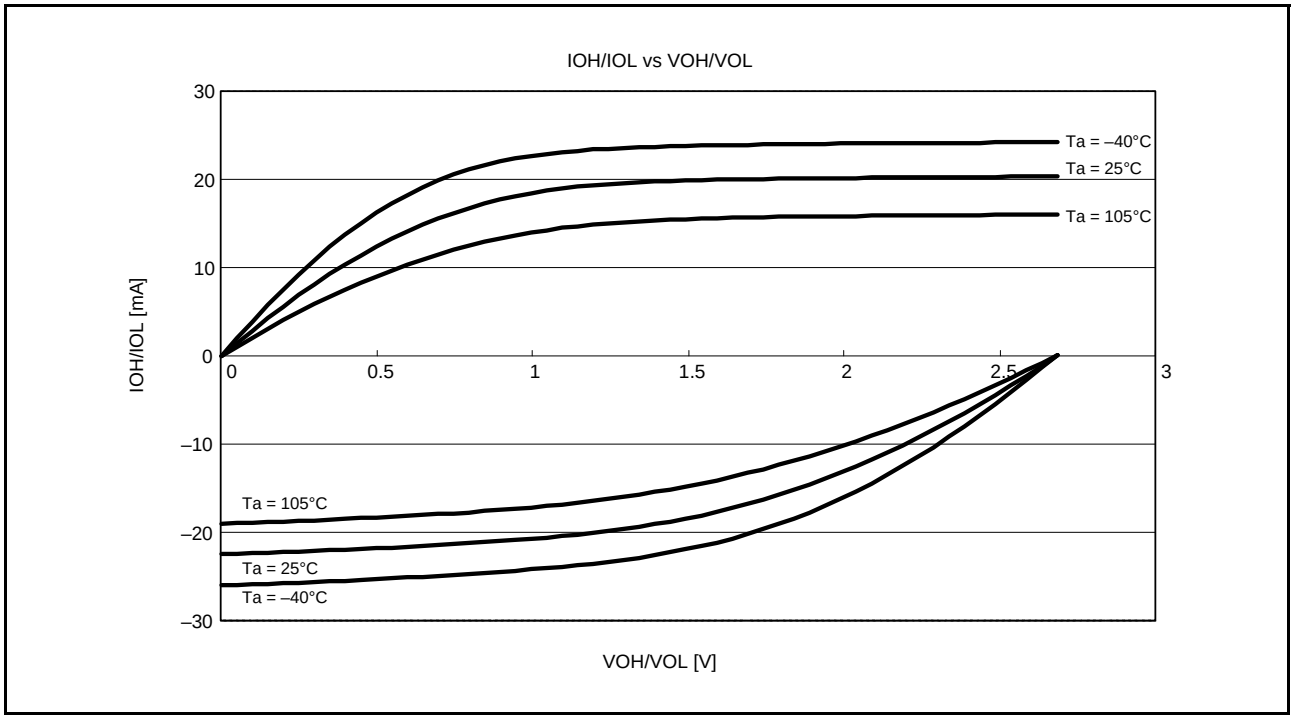


Figure 5.52 VOH/VOL and IOH/IOL Temperature Characteristics at VCC = 2.7 V when High-Drive Output is Selected (Reference Data)

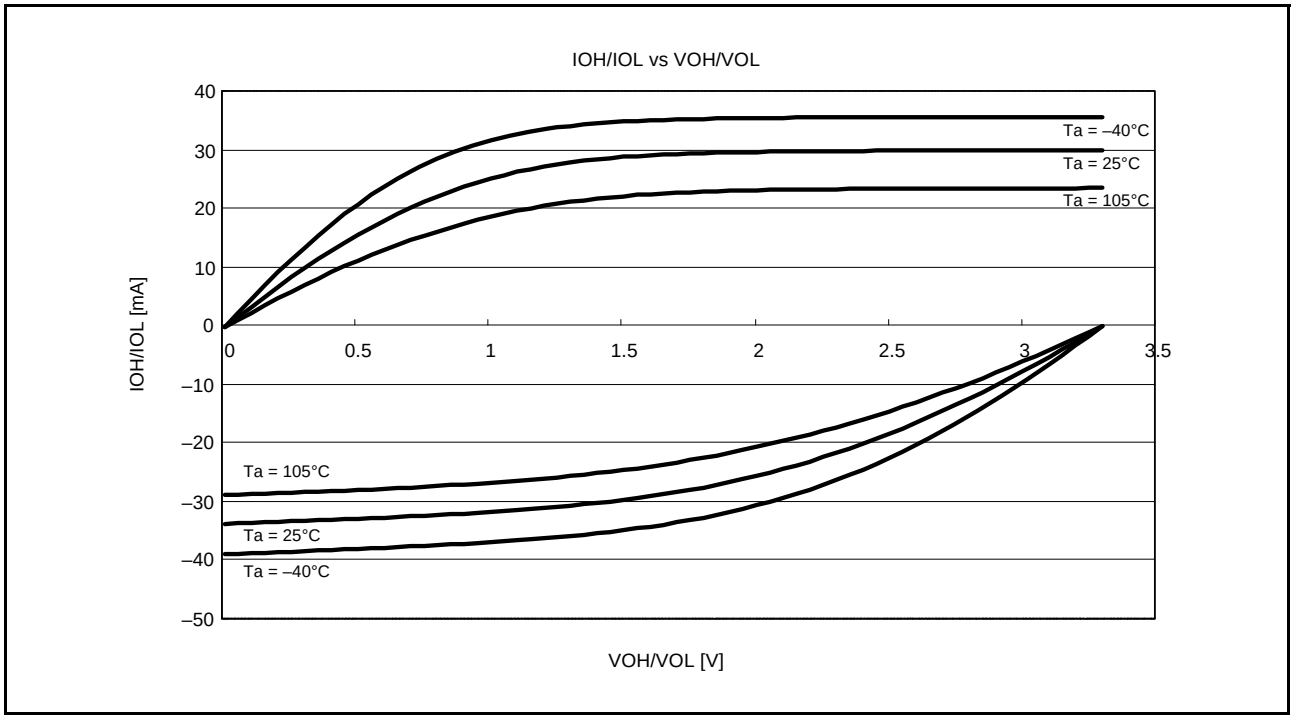


Figure 5.53 VOH/VOL and IOH/IOL Temperature Characteristics at VCC = 3.3 V when High-Drive Output is Selected (Reference Data)

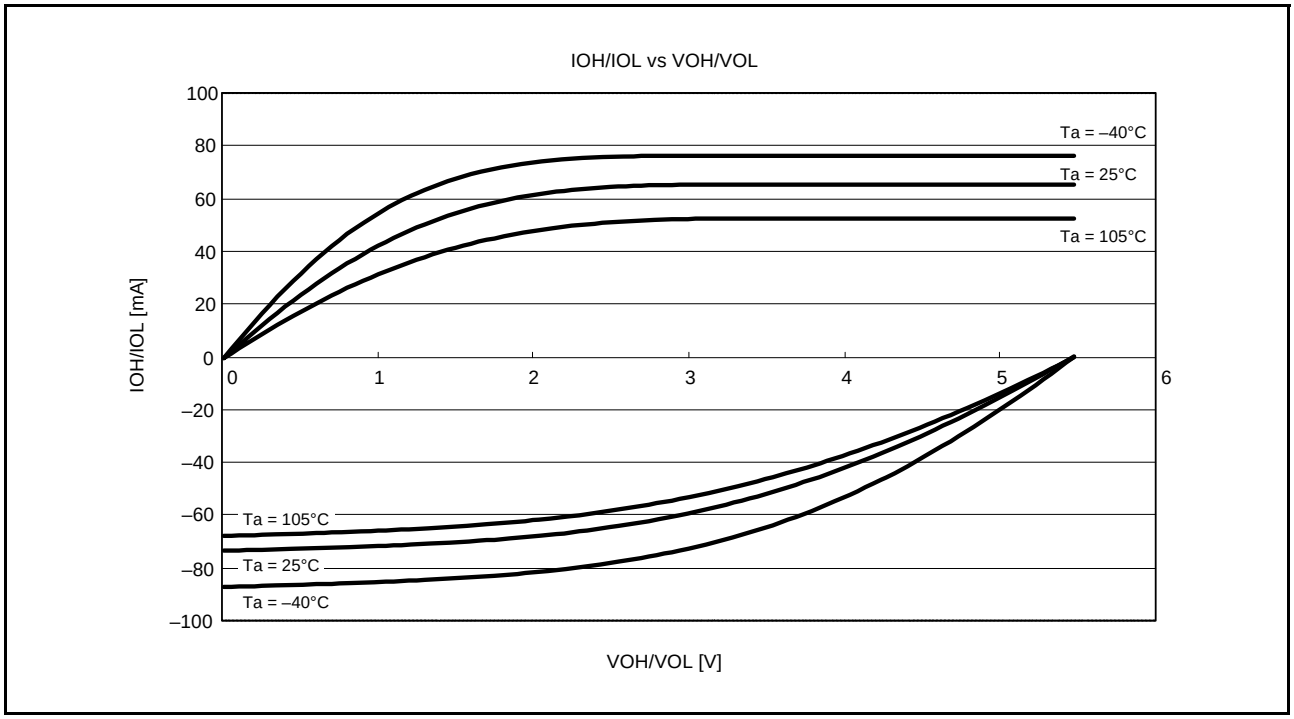


Figure 5.54 VOH/VOL and IOH/IOL Temperature Characteristics at VCC = 5.5 V when High-Drive Output is Selected (Reference Data)

5.3.3 Timing of Recovery from Low Power Consumption Modes

[Chip versions A and C]

Table 5.46 Timing of Recovery from Low Power Consumption Modes

Conditions: VCC = AVCC0 = 1.62 to 5.5 V, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +105°C

Item			Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Recovery time after cancellation of software standby mode (flash memory, HOCO power supplied) (SOFTCUT[2:0] bits = 000b)*1	Crystal resonator connected to main clock oscillator*2	Main clock oscillator operating	t_{SBYMC}	—	3	—	ms	Figure 5.72
		Main clock oscillator and PLL circuit operating	t_{SBYPC}	—	3.5	—	ms	
	External clock input to main clock oscillator	Main clock oscillator operating	t_{SBYEX}	10	—	—	µs	
		Main clock oscillator and PLL circuit operating	t_{SBYPE}	0.5	—	—	ms	
	Sub-clock oscillator operating		t_{SBYSC}	2*3	—	—	s	
	HOCO clock oscillator operating		t_{SBYHO}	—	—	500	µs	
	LOCO clock oscillator operating		t_{SBYLO}	—	—	90	µs	
Recovery time after cancellation of software standby mode (flash memory power supplied, HOCO power not supplied) (SOFTCUT[2:0] bits = 110b)*1	Crystal resonator connected to main clock oscillator*2	Main clock oscillator operating	t_{SBYMC}	—	3	—	ms	Figure 5.72
		Main clock oscillator and PLL circuit operating	t_{SBYPC}	—	3.5	—	ms	
	External clock input to main clock oscillator	Main clock oscillator operating	t_{SBYEX}	40	—	—	µs	
		Main clock oscillator and PLL circuit operating	t_{SBYPE}	0.5	—	—	ms	
	Sub-clock oscillator operating		t_{SBYSC}	2*3	—	—	s	
	HOCO clock oscillator operating		t_{SBYHO}	—	—	1.2	ms	
	LOCO clock oscillator operating		t_{SBYLO}	—	—	90	µs	
Recovery time after cancellation of software standby mode (flash memory, HOCO power not supplied) (SOFTCUT[2:0] bits = 111b)*1	Crystal resonator connected to main clock oscillator*2	Main clock oscillator operating	t_{SBYMC}	—	3	—	ms	Figure 5.72
		Main clock oscillator and PLL circuit operating	t_{SBYPC}	—	3.5	—	ms	
	External clock input to main clock oscillator	Main clock oscillator operating	t_{SBYEX}	100	—	—	µs	
		Main clock oscillator and PLL circuit operating	t_{SBYPE}	0.5	—	—	ms	
	Sub-clock oscillator operating		t_{SBYSC}	2*4	—	—	s	
	HOCO clock oscillator operating		t_{SBYHO}	—	—	1.2	ms	
	LOCO clock oscillator operating		t_{SBYLO}	—	—	10	ms	
Recovery time after cancellation of deep software standby mode			t_{DSBY}	—	—	8	ms	Figure 5.73
Wait time after cancellation of deep software standby mode			t_{DSBYWT}	—	—	0.8	ms	

Note 1. The recovery time varies depending on the state of each oscillator when the WAIT instruction is executed. The recovery time when multiple oscillators are operating varies depending on the operating state of the oscillators that are not selected as the system clock source, and depends on the time set in the wait control registers corresponding to the oscillators.
Note 2. The indicated value is measured for an 8 MHz crystal resonator.
Note 3. When RCR3.RTCEN = 1, the time will be the time set in the SOSCWTCR register minus 2 s.
Note 4. When RCR3.RTCEN = 1, the time will be the time set in the SOSCWTCR register minus 2 s and plus 31.25 ms.

Table 5.59 Timing of On-Chip Peripheral Modules (5)

Conditions: VCC = AVCC0 = 2.7 to 5.5 V, VSS = AVSS0 = VREFL = VREFL0 = 0 V, fPCLKB = up to 32 MHz,
T_a = –40 to +105°C

Item		Symbol	Min.*1,*2	Max.	Unit	Test Conditions
RIIC (Standard mode, SMBus)	SCL input cycle time	t_{SCL}	6 (12) × t_{IICcyc} + 1300	—	ns	Figure 5.98
	SCL input high pulse width	t_{SCLH}	3 (6) × t_{IICcyc} + 300	—	ns	
	SCL input low pulse width	t_{SCLL}	3 (6) × t_{IICcyc} + 300	—	ns	
	SCL, SDA input rise time	t_{Sr}	—	1000	ns	
	SCL, SDA input fall time	t_{Sf}	—	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	1 (4) × t_{IICcyc}	ns	
	SDA input bus free time	t_{BUF}	3 (6) × t_{IICcyc} + 300	—	ns	
	Start condition input hold time	t_{STAH}	t_{IICcyc} + 300	—	ns	
	Restart condition input setup time	t_{STAS}	1000	—	ns	
	Stop condition input setup time	t_{STOS}	1000	—	ns	
	Data input setup time	t_{SDAS}	t_{IICcyc} + 50	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	
RIIC (Fast mode)	SCL input cycle time	t_{SCL}	6 (12) × t_{IICcyc} + 600	—	ns	Figure 5.98
	SCL input high pulse width	t_{SCLH}	3 (6) × t_{IICcyc} + 300	—	ns	
	SCL input low pulse width	t_{SCLL}	3 (6) × t_{IICcyc} + 300	—	ns	
	SCL, SDA input rise time	t_{Sr}	20 + 0.1C_b	300	ns	
	SCL, SDA input fall time	t_{Sf}	20 + 0.1C_b	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	1 (4) × t_{IICcyc}	ns	
	SDA input bus free time	t_{BUF}	3 (6) × t_{IICcyc} + 300	—	ns	
	Start condition input hold time	t_{STAH}	t_{IICcyc} + 300	—	ns	
	Restart condition input setup time	t_{STAS}	300	—	ns	
	Stop condition input setup time	t_{STOS}	300	—	ns	
	Data input setup time	t_{SDAS}	t_{IICcyc} + 50	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	

Note: • t_{IICcyc}: RIIC internal reference count clock (IICφ) cycle
Note 1. The value in parentheses is used when the ICMR3.NF[1:0] bits are set to 11b while a digital filter is enabled with the ICFER.NFE bits = 1.
Note 2. C_b indicates the total capacity of the bus line.

[Chip versions A and C]

Table 5.77 ROM (Flash Memory for Code Storage) Characteristics (4) : middle-speed operating mode 1B

Conditions: VCC = AVCC0 = 1.62 to 3.6 V, VREFH = VREFH0 = AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V
Temperature range for the programming/erasure operation: T_a = –40 to +105°C

Item		Symbol	FCLK = 4 MHz			FCLK = 32 MHz*1			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Programming time when N_{PEC} ≤ 100 times	2 bytes	t_{P2}	—	0.69	6.0	—	0.30	3.5	ms
	8 bytes	t_{P8}	—	0.69	6.0	—	0.30	3.5	
	128 bytes	t_{P128}	—	1.76	14.2	—	0.85	8.3	
Programming time when N_{PEC} > 100 times	2 bytes	t_{P2}	—	0.81	7.1	—	0.35	4.2	ms
	8 bytes	t_{P8}	—	0.81	7.6	—	0.35	4.5	
	128 bytes	t_{P128}	—	1.99	17.5	—	0.96	10	
Erasure time when N_{PEC} ≤ 100 times	2 Kbytes	t_{E2K}	—	24.5	113.7	—	19.0	46	ms
Erasure time when N_{PEC} > 100 times	2 Kbytes	t_{E2K}	—	29.8	225.8	—	23.2	90 (1000 times ≥ N_{PEC} > 100 times), 98 (10000 times ≥ N_{PEC} > 1000 times)	ms
Suspend delay time during programming (in programming/erasure priority mode)		t_{SPD}	—	—	1.7	—	—	1.6	ms
First suspend delay time during programming (in suspend priority mode)		t_{SPSD1}	—	—	220	—	—	120	µs
Second suspend delay time during programming (in suspend priority mode)		t_{SPSD2}	—	—	1.7	—	—	1.6	ms
Suspend delay time during erasing (in programming/erasure priority mode)		t_{SED}	—	—	1.7	—	—	1.6	ms
First suspend delay time during erasing (in suspend priority mode)		t_{SESD1}	—	—	220	—	—	120	µs
Second suspend delay time during erasing (in suspend priority mode)		t_{SESD2}	—	—	1.7	—	—	1.6	ms
FCU reset time		t_{FCUR}	20 µs or longer and FCLK × 6 or greater	—	—	20 µs or longer and FCLK × 6 or greater	—	—	µs

Note 1. The operating frequency is 20 MHz (max.) when the voltage is in the range from 1.62 V to less than 1.8 V.

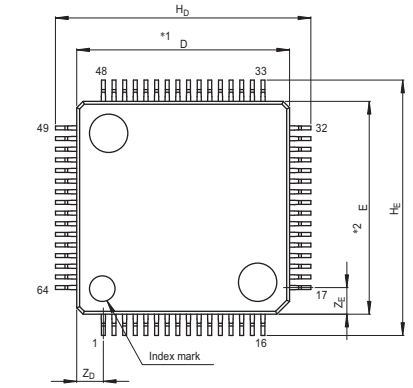
[Chip version B]

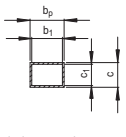
Table 5.78 ROM (Flash Memory for Code Storage) Characteristics (5) : middle-speed operating modes 1A and 2A

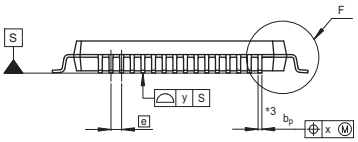
Conditions: VCC = AVCC0 = 2.7 to 5.5 V, VREFH = VREFH0 = AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V
Temperature range for the programming/erasure operation: T_a = –40 to +105°C

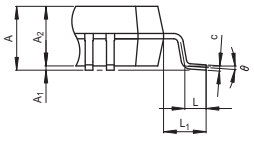
Item		Symbol	FCLK = 4 MHz			FCLK = 32 MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Programming time when N_{PEC} ≤ 100 times	2 bytes	t_{P2}	—	0.19	4.3	—	0.12	2.0	ms
	8 bytes	t_{P8}	—	0.19	4.4	—	0.12	2.0	
	128 bytes	t_{P128}	—	0.67	10.7	—	0.41	4.8	
Programming time when N_{PEC} > 100 times	2 bytes	t_{P2}	—	0.23	5.3	—	0.15	2.5	ms
	8 bytes	t_{P8}	—	0.23	5.4	—	0.15	2.5	
	128 bytes	t_{P128}	—	0.80	13.2	—	0.48	6.0	
Erasure time when N_{PEC} ≤ 100 times	2 Kbytes	t_{E2K}	—	13.0	92.9	—	10.5	29	ms
Erasure time when N_{PEC} > 100 times	2 Kbytes	t_{E2K}	—	15.9	176.9	—	12.8	60	ms
Suspend delay time during programming (in programming/erasure priority mode)		t_{SPD}	—	—	0.9	—	—	0.8	ms
First suspend delay time during programming (in suspend priority mode)		t_{SPSD1}	—	—	220	—	—	120	µs
Second suspend delay time during programming (in suspend priority mode)		t_{SPSD2}	—	—	0.9	—	—	0.8	ms
Suspend delay time during erasing (in programming/erasure priority mode)		t_{SED}	—	—	0.9	—	—	0.8	ms
First suspend delay time during erasing (in suspend priority mode)		t_{SESD1}	—	—	220	—	—	120	µs
Second suspend delay time during erasing (in suspend priority mode)		t_{SESD2}	—	—	0.9	—	—	0.8	ms
FCU reset time		t_{FCUR}	20 µs or longer and FCLK × 6 or greater	—	—	20 µs or longer and FCLK × 6 or greater	—	—	µs

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LFQFP64-10x10-0.50	PLQP0064KB-A	64P6Q-A / FP-64K / FP-64KV	0.3g









NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	9.9	10.0	10.1
E	9.9	10.0	10.1
A_2	—	1.4	—
H_D	11.8	12.0	12.2
H_E	11.8	12.0	12.2
A	—	—	1.7
A_1	0.05	0.1	0.15
b_p	0.15	0.20	0.25
b_1	—	0.18	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
Z_D	—	1.25	—
Z_E	—	1.25	—
L	0.35	0.5	0.65
L_1	—	1.0	—

Figure J 64-Pin LQFP (PLQP0064KB-A)

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

   — The characteristics of an MPU or MCU in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.