Renesas Electronics America Inc - R5F52105BDFN#30 Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I²C, SCI, SPI
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	64
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	20K x 8
Voltage - Supply (Vcc/Vdd)	1.62V ~ 5.5V
Data Converters	A/D 14x12b; D/A 2x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f52105bdfn-30

1.5 Pin Assignments

Figure 1.3 to Figure 1.11 show the pin assignments. Table 1.9 to Table 1.17 show the lists of pins and pin functions.

	A	B	C	D	E	F	G	H	J	K	L	M	N	
13	PE3	PE4	PK4	PE6	P67	PA2	PA4	PA7	PB1	PB5	PL0	PL1	P74	13
12	PE1	PE2	P70	PE5	P65	PA1	VCC	PB0	PB2	PB6	P73	PC1	P75	12
11	P62	P61	PE0	PK5	P66	VSS	PA6	P71	PB4	PB7	PC2	PC0	PC3	11
10	PK3	PK2	P63	PE7	PA0	PA3	PA5	P72	PB3	P76	PC4	P77	P82	10
9	PD6	PD4	PD7	P64						P80	PC5	P81	PC7	9
8	PD2	PD0	PD3	P60						VCC	P83	PC6	VSS	8
7	P92	P91	PD1	PD5						P51	P52	P50	P55	7
6	P90	P47	VSS	P93						P53	P56	PH0	PH1	6
5	P45	P43	P46	VCC	P44					P54	P13	PH3	PH2	5
4	P42	VREFL0	P41	P01	NC	PJ1	NC	P35	P30	P15	P24	P12	P14	4
3	P40	P05	VREFH0	P03	PJ5	PJ3	MD	VSS	P32	P31	P16	P86	P87	3
2	P07	AVCC0	P02	PF5	VCL	XCOUT	RES#	VCC	P33	P26	P23	P17	P20	2
1	AVSS0	VREFH	VREFL	P00	VSS	XCIN	XTAL	EXTAL	P34	P27	P25	P22	P21	1
	A	B	C	D	E	F	G	H	J	K	L	M	N	

RX210 Group
PTLG0145KA-A
(145-pin TFLGA)
(Upper perspective view)

Note: • This figure indicates the power supply pins and I/O port pins. For the pin configuration, see the table “List of Pins and Pin Functions (145-Pin TFLGA)”.
Note: • For the position of A1 pin in the package, see “Package Dimensions”.

Figure 1.3 Pin Assignments of the 145-Pin TFLGA (Upper Perspective View)

Table 1.10 List of Pins and Pin Functions (144-Pin LQFP) (2 / 4)

Pin No.	Power Supply, Clock, System Control	I/O Port	External Bus	Timers (MTU, TMR, POE)	Communications (SCIc, SCId, RSPI, RIIC)	Others
40		P16		MTIOC3C/MTIOC3D/ TMO2/TIOCB1/TCLKC	TXD1/SMOSI1/SSDA1/ MOSIA/SCL-DS/RXD3/ SMISO3/SSCL3	IRQ6/RTCOUT/ ADTRG0#
41		P86		TIOCA0		
42		P15		MTIOC0B/MTCLKB/ TMCI2/TIOCB2/TCLKB	RXD1/SMISO1/SSCL1/ SCK3	IRQ5
43		P14		MTIOC3A/MTCLKA/ TMRI2/TIOCB5/TCLKA	CTS1#/RTS1#/SS1#	IRQ4
44		P13		MTIOC0B/TMO3/ TIOCA5	SDA/TXD2/SMOSI2/ SSDA2	IRQ3
45		P12		TMCI1	SCL/RXD2/SMISO2/ SSCL2	IRQ2
46		PH3		TMCI0		
47		PH2		TMRI0		IRQ1
48		PH1		TMO0		IRQ0
49		PH0				CACREF
50		P56		MTIOC3C/TIOCA1		
51		P55	WAIT#	MTIOC4D/TMO3		
52		P54	ALE	MTIOC4B/TMCI1	CTS2#/RTS2#/SS2#	
53	BCLK	P53				
54		P52	RD#		RXD2/SMISO2/SSCL2	
55		P51	WR1#/BC1#/WAIT#		SCK2	
56		P50	WR0#/WR#		TXD2/SMOSI2/SSDA2	
57	VSS					
58		P83		MTIOC4C	CTS10#/RTS10#	
59	VCC					
60		PC7	A23/CS0#	MTIOC3A/TMO2/ MTCLKB	TXD8/SMOSI8/SSDA8/ MISOA	CACREF
61		PC6	A22/CS1#	MTIOC3C/MTCLKA/ TMCI2	RXD8/SMISO8/SSCL8/ MOSIA	
62		PC5	A21/CS2#/WAIT#	MTIOC3B/MTCLKD/ TMRI2	SCK8/RSPCKA	
63		P82		MTIOC4A	TXD10/SMOSI10/SSDA10	
64		P81		MTIOC3D	RXD10/SMISO10/SSCL10	
65		P80		MTIOC3B	SCK10	
66		PC4	A20/CS3#	MTIOC3D/MTCLKC/ TMCI1/POE0#	SCK5/CTS8#/RTS8#/ SS8#/SSLA0	
67		PC3	A19	MTIOC4D/TCLKB	TXD5/SMOSI5/SSDA5	
68		P77			TXD11/SMOSI11/SSDA11	
69		P76			RXD11/SMISO11/SSCL11	
70		PC2	A18	MTIOC4B/TCLKA	RXD5/SMISO5/SSCL5/ ISSLA3	
71		P75			SCK11	
72		P74			CTS11#/RTS11#/SS11#	
73		PC1	A17	MTIOC3A/TCLKD	SCK5/SSLA2	
74		PL1				
75		PC0	A16	MTIOC3C/TCLKC	CTS5#/RTS5#/SS5#/ SSLA1	
76		PL0				
77		P73				
78		PB7	A15	MTIOC3B/TIOCB5	TXD9/SMOSI9/SSDA9	
79		PB6	A14	MTIOC3D/TIOCA5	RXD9/SMISO9/SSCL9	
80		PB5	A13	MTIOC2A/MTIOC1B/ TMRI1/POE1#/TIOCB4	SCK9	

Table 1.14 List of Pins and Pin Functions (69-Pin WLBGA) (1 / 2)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (MTU, TMR, POE)	Communications (SCIc, SCId, RSPI, RIIC)	Others
A1	NC				
A2		PE2	MTIOC4A	RXD12/RXDX12/SMISO12/ SSCL12	IRQ7-DS/AN010/ CVREFB0
A3	VREFL				
A4	VREFH				
A5		P43			AN003
A6	VREFL0				
A7	AVCC0				
A8	AVSS0				
A9	AVSS0				
B1		PE5	MTIOC4C/MTIOC2B		IRQ5/AN013
B2		PE4	MTIOC4D/MTIOC1A		AN012/CMPA2
B3		PE3	MTIOC4B/POE8#	CTS12#/RTS12#/SS12#	AN011/CMPA1
B4		P46			AN006
B5		P44			AN004
B6		P41			AN001
B7	VREFH0				
B8		P05			DA1
B9	VCL				
C1		PA3	MTIOC0D/MTCLKD	RXD5/SMISO5/SSCL5	IRQ6-DS/CMPB1
C2		PA4	MTIC5U/MTCLKA/TMRI0	TXD5/SMOSI5/SSDA5/SSLA0	IRQ5-DS/CVREFB1
C3		PA0	MTIOC4A	SSLA1	CACREF
C4		PE1	MTIOC4C	TXD12/TXDX12/SIOX12/ SMOSI12/SSDA12	AN009/CMPB0
C5		PE0		SCK12	AN008
C6		P42			AN002
C7		P40			AN000
C8		P03			DA0
C9	XCIN				
D1		PA6	MTIC5V/MTCLKB/TMCI3/ POE2#	CTS5#/RTS5#/SS5#/MOSIA	
D2		PB0	MTIC5W	RXD6/SMISO6/SSCL6/ RSPCKA	
D3		PA1	MTIOC0B/MTCLKC	SCK5/SSLA2	CVREFA
D7	MD				FINED
D8	RES#				
D9	XCOUT				
E1	VSS				
E2		PB1	MTIOC0C/MTIOC4C/TMCI0	TXD6/SMOSI6/SSDA6	IRQ4-DS
E8	XTAL	P37			
E9	VSS				
F1	VCC				
F2		PB3	MTIOC0A/MTIOC4A/TMO0/ POE3#	SCK6	
F7		P31	MTIOC4D/TMCI2	CTS1#/RTS1#/SS1#	IRQ1-DS/RTCIC1
F8	EXTAL	P36			
F9	VCC				
G1		PB5	MTIOC2A/MTIOC1B/TMRI1/ POE1#	SCK9	
G2		PB6	MTIOC3D	RXD9/SMISO9/SSCL9	

Table 1.17 List of Pins and Pin Functions (48-Pin LQFP) (1 / 2)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (MTU, TMR, POE)	Communication (SCIc, SCId, RSPI, RIIC)	Others
1	VCL				
2	MD				FINED
3	RES#				
4	XTAL	P37			
5	VSS				
6	EXTAL	P36			
7	VCC				
8		P35			NMI
9		P31	MTIOC4D/TMCI2	CTS1#/RTS1#/SS1#	IRQ1-DS
10		P30	MTIOC4B/TMRI3/POE8#	RXD1/SMISO1/SSCL1	IRQ0-DS
11		P27	MTIOC2B/TMCI3	SCK1	
12		P26	MTIOC2A/TMO1	TXD1/SMOSI1/SSDA1	
13		P17	MTIOC3A/MTIOC3B/TMO1/ POE8#	SCK1/MISOA/SDA-DS	IRQ7
14		P16	MTIOC3C/MTIOC3D/TMO2	TXD1/SMOSI1/SSDA1/MOSIA/ SCL-DS	IRQ6/ADTRG0#
15		P15	MTIOC0B/MTCLKB/TMCI2	RXD1/SMISO1/SSCL1	IRQ5
16		P14	MTIOC3A/MTCLKA/TMRI2	CTS1#/RTS1#/SS1#	IRQ4
17		PH3	TMCI0		
18		PH2	TMRI0		IRQ1
19		PH1	TMO0		IRQ0
20		PH0			CACREF
21		PC7	MTIOC3A/TMO2/MTCLKB	TXD8/SMOSI8/SSDA8/MISOA	CACREF
22		PC6	MTIOC3C/MTCLKA/TMCI2	RXD8/SMISO8/SSCL8/MOSIA	
23		PC5	MTIOC3B/MTCLKD/TMRI2	SCK8/RSPCKA	
24		PC4	MTIOC3D/MTCLKC/TMCI1/ POE0#	SCK5/CTS8#/RTS8#/SS8#/ SSLA0	
25		PB5	MTIOC2A/MTIOC1B/TMRI1/ POE1#		
26		PB3	MTIOC0A/MTIOC4A/TMO0/ POE3#	SCK6	
27		PB1	MTIOC0C/MTIOC4C/TMCI0	TXD6/SMOSI6/SSDA6	IRQ4-DS
28	VCC				
29		PB0	MTIC5W	RXD6/SMISO6/SSCL6/RSPCKA	
30	VSS				
31		PA6	MTIC5V/MTCLKB/TMCI3/ POE2#	CTS5#/RTS5#/SS5#/MOSIA	
32		PA4	MTIC5U/MTCLKA/TMRI0	TXD5/SMOSI5/SSDA5/SSLA0	IRQ5-DS/CVREFB1
33		PA3	MTIOC0D/MTCLKD	RXD5/SMISO5/SSCL5	IRQ6-DS/CMPB1
34		PA1	MTIOC0B/MTCLKC	SCK5/SSLA2	CVREFA
35		PE4	MTIOC4D/MTIOC1A		AN012/CMPA2
36		PE3	MTIOC4B/POE8#	CTS12#/RTS12#	AN011/CMPA1
37		PE2	MTIOC4A	RXD12/RXDX12/SSCL12	IRQ7-DS/AN010/ CVREFB0
38		PE1	MTIOC4C	TXD12/TXDX12/SIOX12/ SSDA12	AN009/CMPB0
39	VREFL				
40		P46			AN006
41	VREFH				
42		P42			AN002
43		P41			AN001

- Longword-size I/O registers

```
MOV.L  #SFR_ADDR, R1
MOV.L  #SFR_DATA, [R1]
CMP    [R1].L, R1
;; Next process
```

If multiple registers are written to and a subsequent instruction should be executed after the write operations are entirely completed, only read the I/O register that was last written to and execute the operation using the value; it is not necessary to read or execute operation for all the registers that were written to.

(3) Number of Access Cycles to I/O Registers

For numbers of clock cycles for access to I/O registers, see Table 4.1, List of I/O Registers (Address Order).
The number of access cycles to I/O registers is obtained by following equation.*1

Number of access cycles to I/O registers = Number of bus cycles for internal main bus 1 +
Number of divided clock synchronization cycles +
Number of bus cycles for internal peripheral bus 1 to 6

The number of bus cycles of internal peripheral bus 1 to 6 differs according to the register to be accessed.
When peripheral functions connected to internal peripheral bus 2 to 6 or registers for the external bus control unit (except for bus error related registers) are accessed, the number of divided clock synchronization cycles is added.
The number of divided clock synchronization cycles differs depending on the frequency ratio between ICLK and PCLK (or FCLK, BCLK) or bus access timing.
In the peripheral function unit, when the frequency ratio of ICLK is equal to or greater than that of PCLK (or FCLK), the sum of the number of bus cycles for internal main bus 1 and the number of the divided clock synchronization cycles will be one cycle of PCLK (or FCLK) at a maximum. Therefore, one PCLK (or FCLK) has been added to the number of access cycles shown in Table 4.1.
When the frequency ratio of ICLK is lower than that of PCLK (or FCLK), the subsequent bus access is started from the ICLK cycle following the completion of the access to the peripheral functions. Therefore, the access cycles are described on an ICLK basis.
In the external bus control unit, the sum of the number of bus cycles for internal main bus 1 and the number of divided clock synchronization cycles will be one cycle of BCLK at a maximum. Therefore, one BCLK is added to the number of access cycles shown in Table 4.1.

Note 1. This applies to the number of cycles when the access from the CPU does not conflict with the instruction fetching to the external memory or bus access from the different bus master (DMAC or DTC).

Table 4.1 List of I/O Registers (Address Order) (8 / 29)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles	
						ICLK ≥ PCLK	ICLK < PCLK
0008 71D0h	ICU	DTC activation enable register 208	DTCER208	8	8	2 ICLK	
0008 71D3h	ICU	DTC activation enable register 211	DTCER211	8	8	2 ICLK	
0008 71D4h	ICU	DTC activation enable register 212	DTCER212	8	8	2 ICLK	
0008 71D7h	ICU	DTC activation enable register 215	DTCER215	8	8	2 ICLK	
0008 71D8h	ICU	DTC activation enable register 216	DTCER216	8	8	2 ICLK	
0008 71DBh	ICU	DTC activation enable register 219	DTCER219	8	8	2 ICLK	
0008 71DCh	ICU	DTC activation enable register 220	DTCER220	8	8	2 ICLK	
0008 71DFh	ICU	DTC activation enable register 223	DTCER223	8	8	2 ICLK	
0008 71E0h	ICU	DTC activation enable register 224	DTCER224	8	8	2 ICLK	
0008 71E3h	ICU	DTC activation enable register 227	DTCER227	8	8	2 ICLK	
0008 71E4h	ICU	DTC activation enable register 228	DTCER228	8	8	2 ICLK	
0008 71E7h	ICU	DTC activation enable register 231	DTCER231	8	8	2 ICLK	
0008 71E8h	ICU	DTC activation enable register 232	DTCER232	8	8	2 ICLK	
0008 71EBh	ICU	DTC activation enable register 235	DTCER235	8	8	2 ICLK	
0008 71ECh	ICU	DTC activation enable register 236	DTCER236	8	8	2 ICLK	
0008 71EFh	ICU	DTC activation enable register 239	DTCER239	8	8	2 ICLK	
0008 71F0h	ICU	DTC activation enable register 240	DTCER240	8	8	2 ICLK	
0008 71F7h	ICU	DTC activation enable register 247	DTCER247	8	8	2 ICLK	
0008 71F8h	ICU	DTC activation enable register 248	DTCER248	8	8	2 ICLK	
0008 71FBh	ICU	DTC activation enable register 251	DTCER251	8	8	2 ICLK	
0008 71FCh	ICU	DTC activation enable register 252	DTCER252	8	8	2 ICLK	
0008 7202h	ICU	Interrupt request enable register 02	IER02	8	8	2 ICLK	
0008 7203h	ICU	Interrupt request enable register 03	IER03	8	8	2 ICLK	
0008 7204h	ICU	Interrupt request enable register 04	IER04	8	8	2 ICLK	
0008 7205h	ICU	Interrupt request enable register 05	IER05	8	8	2 ICLK	
0008 7207h	ICU	Interrupt request enable register 07	IER07	8	8	2 ICLK	
0008 7208h	ICU	Interrupt request enable register 08	IER08	8	8	2 ICLK	
0008 720Bh	ICU	Interrupt request enable register 0B	IER0B	8	8	2 ICLK	
0008 720Ch	ICU	Interrupt request enable register 0C	IER0C	8	8	2 ICLK	
0008 720Dh	ICU	Interrupt request enable register 0D	IER0D	8	8	2 ICLK	
0008 720Eh	ICU	Interrupt request enable register 0E	IER0E	8	8	2 ICLK	
0008 720Fh	ICU	Interrupt request enable register 0F	IER0F	8	8	2 ICLK	
0008 7210h	ICU	Interrupt request enable register 10	IER10	8	8	2 ICLK	
0008 7211h	ICU	Interrupt request enable register 11	IER11	8	8	2 ICLK	
0008 7212h	ICU	Interrupt request enable register 12	IER12	8	8	2 ICLK	
0008 7213h	ICU	Interrupt request enable register 13	IER13	8	8	2 ICLK	
0008 7214h	ICU	Interrupt request enable register 14	IER14	8	8	2 ICLK	
0008 7215h	ICU	Interrupt request enable register 15	IER15	8	8	2 ICLK	
0008 7216h	ICU	Interrupt request enable register 16	IER16	8	8	2 ICLK	
0008 7217h	ICU	Interrupt request enable register 17	IER17	8	8	2 ICLK	
0008 7218h	ICU	Interrupt request enable register 18	IER18	8	8	2 ICLK	
0008 7219h	ICU	Interrupt request enable register 19	IER19	8	8	2 ICLK	
0008 721Ah	ICU	Interrupt request enable register 1A	IER1A	8	8	2 ICLK	
0008 721Bh	ICU	Interrupt request enable register 1B	IER1B	8	8	2 ICLK	
0008 721Ch	ICU	Interrupt request enable register 1C	IER1C	8	8	2 ICLK	
0008 721Dh	ICU	Interrupt request enable register 1D	IER1D	8	8	2 ICLK	
0008 721Eh	ICU	Interrupt request enable register 1E	IER1E	8	8	2 ICLK	
0008 721Fh	ICU	Interrupt request enable register 1F	IER1F	8	8	2 ICLK	
0008 72E0h	ICU	Software interrupt activation register	SWINTR	8	8	2 ICLK	
0008 72F0h	ICU	Fast interrupt set register	FIR	16	16	2 ICLK	
0008 7300h	ICU	Interrupt source priority register 000	IPR000	8	8	2 ICLK	

Table 4.1 List of I/O Registers (Address Order) (9 / 29)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles ICLK ≥ PCLK	Number of Access Cycles ICLK < PCLK
0008 7301h	ICU	Interrupt source priority register 001	IPR001	8	8	2 ICLK	
0008 7302h	ICU	Interrupt source priority register 002	IPR002	8	8	2 ICLK	
0008 7303h	ICU	Interrupt source priority register 003	IPR003	8	8	2 ICLK	
0008 7304h	ICU	Interrupt source priority register 004	IPR004	8	8	2 ICLK	
0008 7305h	ICU	Interrupt source priority register 005	IPR005	8	8	2 ICLK	
0008 7306h	ICU	Interrupt source priority register 006	IPR006	8	8	2 ICLK	
0008 7307h	ICU	Interrupt source priority register 007	IPR007	8	8	2 ICLK	
0008 7320h	ICU	Interrupt source priority register 032	IPR032	8	8	2 ICLK	
0008 7321h	ICU	Interrupt source priority register 033	IPR033	8	8	2 ICLK	
0008 7322h	ICU	Interrupt source priority register 034	IPR034	8	8	2 ICLK	
0008 732Ch	ICU	Interrupt source priority register 044	IPR044	8	8	2 ICLK	
0008 7339h	ICU	Interrupt source priority register 057	IPR057	8	8	2 ICLK	
0008 733Ah	ICU	Interrupt source priority register 058	IPR058	8	8	2 ICLK	
0008 733Bh	ICU	Interrupt source priority register 059	IPR059	8	8	2 ICLK	
0008 733Fh	ICU	Interrupt source priority register 063	IPR063	8	8	2 ICLK	
0008 7340h	ICU	Interrupt source priority register 064	IPR064	8	8	2 ICLK	
0008 7341h	ICU	Interrupt source priority register 065	IPR065	8	8	2 ICLK	
0008 7342h	ICU	Interrupt source priority register 066	IPR066	8	8	2 ICLK	
0008 7343h	ICU	Interrupt source priority register 067	IPR067	8	8	2 ICLK	
0008 7344h	ICU	Interrupt source priority register 068	IPR068	8	8	2 ICLK	
0008 7345h	ICU	Interrupt source priority register 069	IPR069	8	8	2 ICLK	
0008 7346h	ICU	Interrupt source priority register 070	IPR070	8	8	2 ICLK	
0008 7347h	ICU	Interrupt source priority register 071	IPR071	8	8	2 ICLK	
0008 7358h	ICU	Interrupt source priority register 088	IPR088	8	8	2 ICLK	
0008 7359h	ICU	Interrupt source priority register 089	IPR089	8	8	2 ICLK	
0008 735Ch	ICU	Interrupt source priority register 092	IPR092	8	8	2 ICLK	
0008 735Dh	ICU	Interrupt source priority register 093	IPR093	8	8	2 ICLK	
0008 7366h	ICU	Interrupt source priority register 102	IPR102	8	8	2 ICLK	
0008 7367h	ICU	Interrupt source priority register 103	IPR103	8	8	2 ICLK	
0008 736Ah	ICU	Interrupt source priority register 106	IPR106	8	8	2 ICLK	
0008 736Bh	ICU	Interrupt source priority register 107	IPR107	8	8	2 ICLK	
0008 7372h	ICU	Interrupt source priority register 114	IPR114	8	8	2 ICLK	
0008 7376h	ICU	Interrupt source priority register 118	IPR118	8	8	2 ICLK	
0008 7379h	ICU	Interrupt source priority register 121	IPR121	8	8	2 ICLK	
0008 737Bh	ICU	Interrupt source priority register 123	IPR123	8	8	2 ICLK	
0008 737Dh	ICU	Interrupt source priority register 125	IPR125	8	8	2 ICLK	
0008 737Fh	ICU	Interrupt source priority register 127	IPR127	8	8	2 ICLK	
0008 7381h	ICU	Interrupt source priority register 129	IPR129	8	8	2 ICLK	
0008 7385h	ICU	Interrupt source priority register 133	IPR133	8	8	2 ICLK	
0008 7386h	ICU	Interrupt source priority register 134	IPR134	8	8	2 ICLK	
0008 738Ah	ICU	Interrupt source priority register 138	IPR138	8	8	2 ICLK	
0008 738Bh	ICU	Interrupt source priority register 139	IPR139	8	8	2 ICLK	
0008 738Eh	ICU	Interrupt source priority register 142	IPR142	8	8	2 ICLK	
0008 7392h	ICU	Interrupt source priority register 146	IPR146	8	8	2 ICLK	
0008 7393h	ICU	Interrupt source priority register 147	IPR147	8	8	2 ICLK	
0008 7395h	ICU	Interrupt source priority register 149	IPR149	8	8	2 ICLK	
0008 7397h	ICU	Interrupt source priority register 151	IPR151	8	8	2 ICLK	
0008 7399h	ICU	Interrupt source priority register 153	IPR153	8	8	2 ICLK	
0008 739Bh	ICU	Interrupt source priority register 155	IPR155	8	8	2 ICLK	
0008 739Fh	ICU	Interrupt source priority register 159	IPR159	8	8	2 ICLK	
0008 73A0h	ICU	Interrupt source priority register 160	IPR160	8	8	2 ICLK	

Table 5.4 DC Characteristics (3)

Conditions: VCC = AVCC0 = 1.62 to 5.5 V, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Input leakage current	RES#, MD pin, P35/NMI	$\lvert I_{in} \rvert$	—	—	1.0	µA	V_{in} = 0 V, VCC
Three-state leakage current (off-state)	Port 4	$\lvert I_{TSI} \rvert$	—	—	1.0	µA	V_{in} = 0 V, VCC
	Other pins except for ports for 5 V tolerant and port 4		—	—	0.2		
	Ports for 5 V tolerant		—	—	1.0		V_{in} = 0 V, 5.8 V
Input capacitance	All input pins (except for ports 12, 13, 16, 17, 4, A1, A3, A4, and E)	C_{in}	—	—	15	pF	V_{in} = 0 V, f = 1 MHz, T_a = 25°C
	Ports 12, 13, 16, 17, 4, A1, A3, A4, and E		—	—	30		

Table 5.5 DC Characteristics (4)

Conditions: VCC = AVCC0 = 1.62 to 5.5 V, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +105°C

Item		Symbol	VCC						Unit	Test Conditions
			1.62 to 2.7 V		2.7 to 4.0 V		4.0 to 5.5 V			
			Min.	Max.	Min.	Max.	Min.	Max.		
Input pull-up MOS current	All ports (except for port 35)	I_p	–150	–5	–200	–10	–400	–50	µA	V_{in} = 0 V

[Chip version A]

Table 5.6 DC Characteristics (5)

Conditions: VCC = AVCC0 = 2.7 to 5.5 V, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +105°C

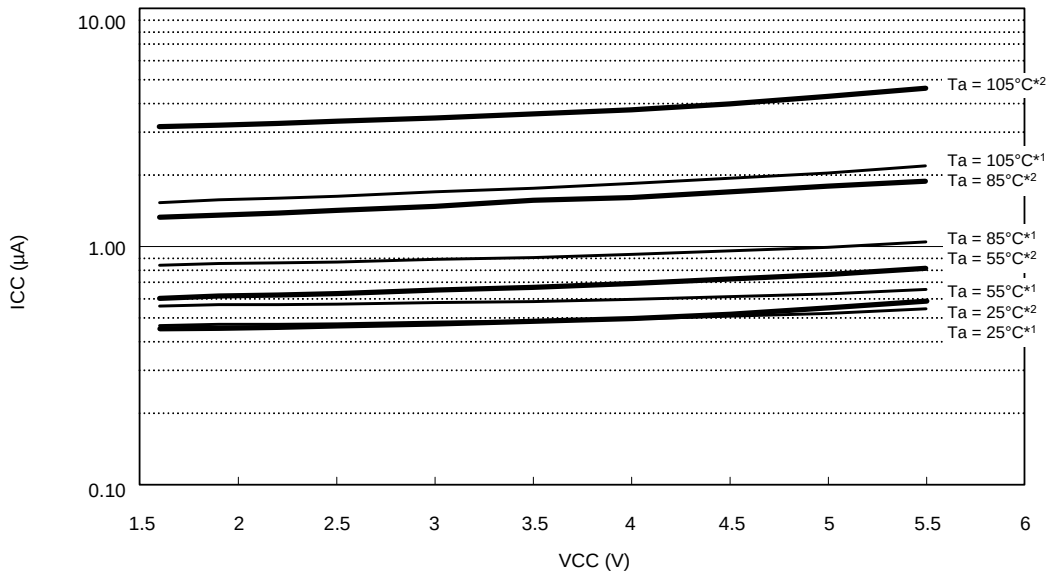
Item					Symbol	Typ.	Max.	Unit	Test Conditions
Supply current*1	High-speed operating mode	Normal operating mode	No peripheral operation*2	ICLK = 50 MHz	I_{CC}	10	—	mA	
			All peripheral operation: Normal*3	ICLK = 50 MHz		31.5	—		
			All peripheral operation: Max.*3	ICLK = 50 MHz		—	55		
		Sleep mode	No peripheral operation	ICLK = 50 MHz		7.5	—		
			All peripheral operation: Normal	ICLK = 50 MHz		17.5	—		
		All-module clock stop mode		ICLK = 50 MHz		6.7	—		
		Increase during BGO operation*4				25	—		

Note 1. Supply current values do not include output charge/discharge current from all pins. The values apply when internal pull-up MOSs are in the off state.

Note 2. Clock supply to the peripheral functions is stopped. This does not include BGO operation. The clock source is PLL and the VCO oscillation frequency is 100 MHz. BCLK, FCLK, and PCLK are set to divided by 64.

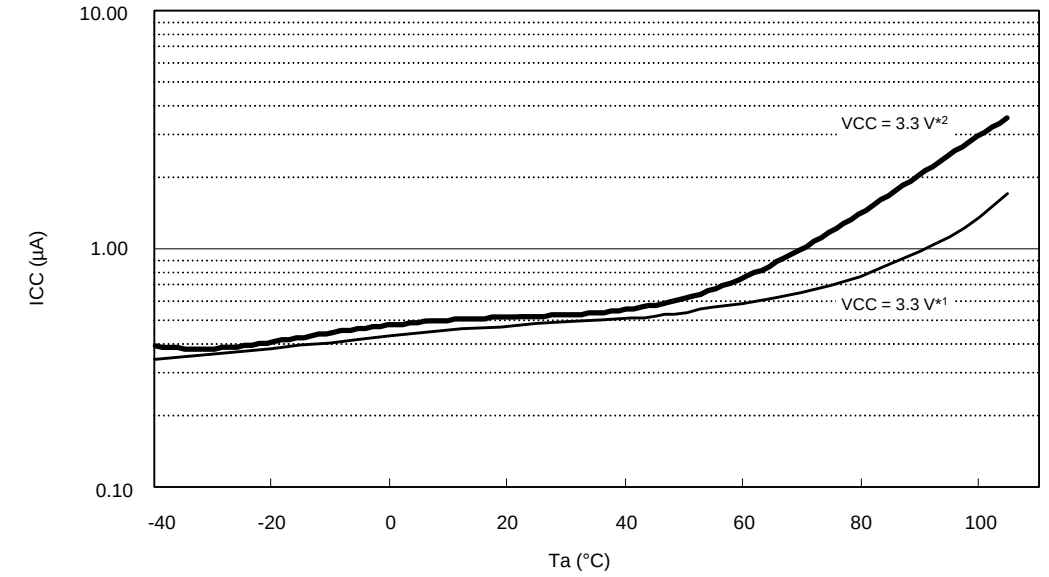
Note 3. Clocks are supplied to the peripheral functions. This does not include BGO operation. The clock source is PLL and the VCO oscillation frequency is 100 MHz. BCLK, FCLK, and PCLK are ICLK divided by 2.

Note 4. This is the increase if data is programmed to or erasing from the ROM or E2 DataFlash during program execution.



Note 1. Average value of the tested middle samples during product evaluation.
Note 2. Average value of the tested upper-limit samples during product evaluation.

Figure 5.15 Voltage Dependency in Deep Software Standby Mode (DEEPCUT1 Bit = 1) (Reference Data) for Chip Version C

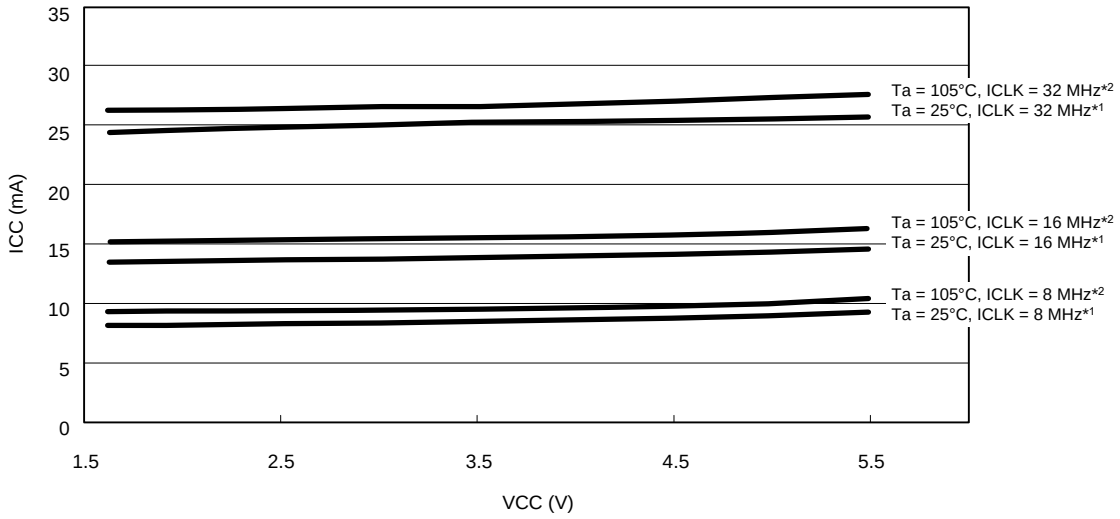


Note 1. Average value of the tested middle samples during product evaluation
Note 2. Average value of the tested upper-limit samples during product evaluation.

Figure 5.16 Temperature Dependency in Deep Software Standby Mode (DEEPCUT1 Bit = 1) (Reference Data) for Chip Version C

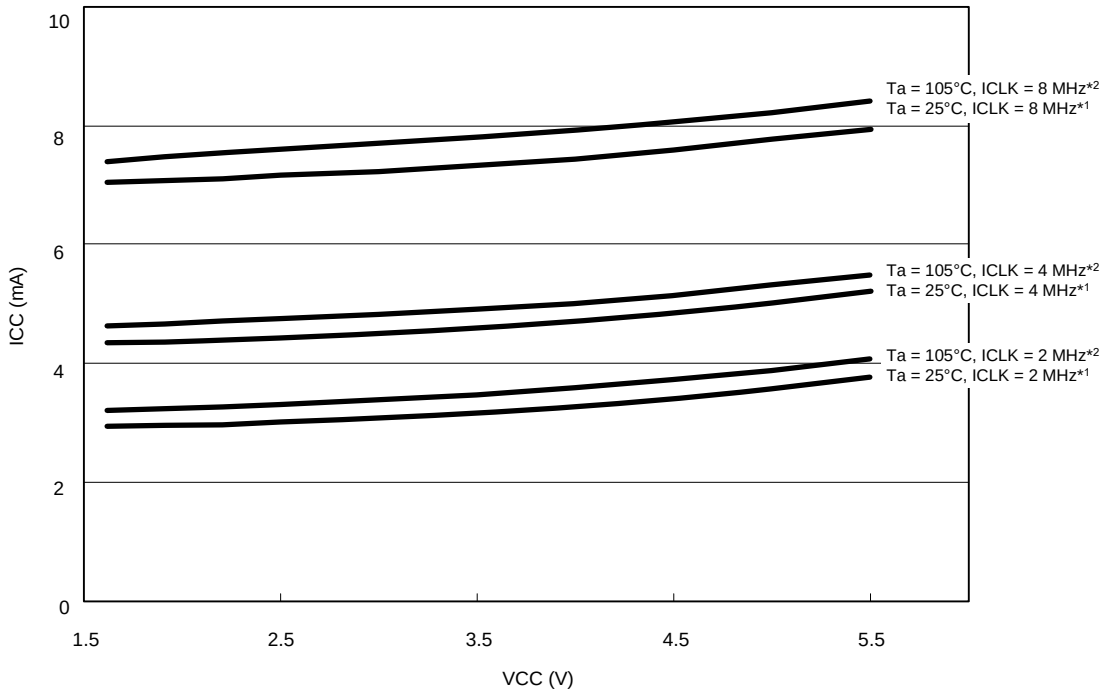
Item					Symbol	Typ.	Max.	Unit	Test Conditions
Supply current*1	Low-speed operating mode 1	Normal operating mode	No peripheral operation*7	ICLK = 8 MHz	I_{CC}	2.1	—	mA	
				ICLK = 4 MHz		1.7	—		
				ICLK = 2 MHz		1.5	—		
			All peripheral operation: Normal*8	ICLK = 8 MHz		7.3	—		
				ICLK = 4 MHz		4.5	—		
				ICLK = 2 MHz		3.1	—		
			All peripheral operation: Max.*7	ICLK = 8 MHz		—	12		
				ICLK = 4 MHz		—	—		
				ICLK = 2 MHz		—	—		
		Sleep mode	No peripheral operation	ICLK = 8 MHz		1.5	—		
				ICLK = 4 MHz		1.4	—		
				ICLK = 2 MHz		1.3	—		
			All peripheral operation: Normal	ICLK = 8 MHz		4.1	—		
				ICLK = 4 MHz		3.0	—		
				ICLK = 2 MHz		2.3	—		
		All-module clock stop mode		ICLK = 8 MHz		1.4	—		
				ICLK = 4 MHz		1.3	—		
				ICLK = 2 MHz		1.2	—		
	Low-speed operating mode 2	Normal operating mode	No peripheral operation*9	ICLK = 32 kHz		0.022	—		
			All peripheral operation: Normal*10	ICLK = 32 kHz		0.06	—		
			All peripheral operation: Max.*10	ICLK = 32 kHz		—	3*11		
		Sleep mode	No peripheral operation	ICLK = 32 kHz		0.017	—		
			All peripheral operation: Normal	ICLK = 32 kHz		0.036	—		
		All-module clock stop mode				0.017	—		

Note 1. Supply current values do not include output charge/discharge current from all pins. The values apply when internal pull-up MOSs are in the off state.
Note 2. Clock supply to the peripheral functions is stopped. This does not include BGO operation. The clock source is PLL and the VCO oscillation frequency is 64 MHz. BCLK, FCLK, and PCLK are set to divided by 64.
Note 3. Clock supply to the peripheral functions is stopped. This does not include BGO operation. The clock source is HOCO and the oscillation frequency is 40 MHz. BCLK, FCLK, and PCLK are set to divided by 64.
Note 4. Clocks are supplied to the peripheral functions. This does not include BGO operation. The clock source is PLL and the VCO oscillation frequency is 64 MHz. BCLK, FCLK, and PCLK are ICLK divided by 1.
Note 5. Clocks are supplied to the peripheral functions. This does not include BGO operation. The clock source is HOCO and the oscillation frequency is 40 MHz. BCLK, FCLK, and PCLK are ICLK divided by 1.
Note 6. This is the increase if data is programmed to or erasing from the ROM or E2 DataFlash during program execution.
Note 7. Clock supply to the peripheral functions is stopped. This does not include BGO operation. The clock source is HOCO and the oscillation frequency is 32 MHz. BCLK, FCLK, and PCLK are set to divided by 64.
Note 8. Clocks are supplied to the peripheral functions. This does not include BGO operation. The clock source is HOCO and the oscillation frequency is 32 MHz. BCLK, FCLK, and PCLK are ICLK divided by 1.
Note 9. Clock supply to the peripheral functions is stopped. This does not include BGO operation. The clock source is the sub oscillation circuit. BCLK, FCLK, and PCLK are set to divided by 64.
Note 10. Clocks are supplied to the peripheral functions. This does not include BGO operation. The clock source is the sub oscillation circuit. BCLK, FCLK, and PCLK are ICLK divided by 1.
Note 11. Value when the main clock continues oscillating at 12.5 MHz.



Note 1. All peripheral operation is normal. This does not include BGO operation.
Average value of the tested middle samples during product evaluation
Note 2. All peripheral operation is maximum. This does not include BGO operation.
Average value of the tested upper-limit samples during product evaluation.

Figure 5.28 Voltage Dependency in Middle-Speed Operating Modes 2A and 2B (Reference Data) for Chip Version B with 768 Kbytes/1 Mbyte of Flash Memory and 100 to 145 Pins



Note 1. All peripheral operation is normal.
Average value of the tested middle samples during product evaluation.
Note 2. All peripheral operation is maximum.
Average value of the tested upper-limit samples during product evaluation.

Figure 5.29 Voltage Dependency in Low-Speed Operating Mode 1 (Reference Data) for Chip Version B with 768 Kbytes/1 Mbyte of Flash Memory and 100 to 145 Pins

[Chip version B with 768 Kbytes/1 Mbyte of flash memory and 100 to 145 pins]

Table 5.17 DC Characteristics (16)

Conditions: VCC = AVCC0 = 1.62 to 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item				Symbol	Typ.*3	Max.	Unit	Test Conditions
Supply current*1	Software standby mode*2	Flash memory power supplied, HOCO power supplied, POR low power consumption function disabled (SOFTCUT[2:0] bits = 000b)	T_a = 25°C	I_{CC}	10	34	µA	
			T_a = 55°C		13	87		
			T_a = 85°C		21	201		
			T_a = 105°C		40	352		
		Flash memory power supplied, HOCO power not supplied, POR low power consumption function enabled (SOFTCUT[2:0] bits = 110b)	T_a = 25°C		1.8	24		
			T_a = 55°C		3.3	70		
			T_a = 85°C		10	168		
			T_a = 105°C		25	302		
	Deep software standby mode*2	Flash memory power not supplied, HOCO power not supplied, POR low power consumption function enabled (DEEPCUT1 bit = 1)	T_a = 25°C		0.4	0.8		
			T_a = 55°C		0.5	1.0		
			T_a = 85°C		0.7	2.5		
			T_a = 105°C		1.4	6.3		
	Increments produced by running voltage detection circuits and disabling the POR low power consumption function				1.4	—		
	Increment for RTC operation (low CL)				0.8	—		
	Increment for RTC operation (standard CL)				2.0	—		

Note 1. Supply current values are with all output pins unloaded and all input pull-up MOSs in the off state.
Note 2. The IWDT and LVD are stopped.
Note 3. VCC = 3.3 V.

[Chip versions B and C]

Table 5.31 Output Values of Voltage (4)

Conditions: VCC = AVCC0 = 2.7 to 4.0 V, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +105°C

Item			Symbol	Min.	Max.	Unit	Test Conditions
Output low	All output pins (other than RIIC)	Normal output mode	V_{OL}	—	0.5	V	I_{OL} = 1.0 mA
		High-drive output mode		—	0.5		I_{OL} = 2.0 mA
	RIIC pins			—	0.4		I_{OL} = 3.0 mA
				—	0.6		I_{OL} = 6.0 mA
Output high	All output pins	Normal output mode	V_{OH}	VCC – 0.5	—	V	I_{OH} = –1.0 mA
		High-drive output mode		VCC – 0.5	—		I_{OH} = –2.0 mA

[Chip versions B and C]

Table 5.32 Output Values of Voltage (5)

Conditions: VCC = AVCC0 = 4.0 to 5.5 V, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +105°C

Item			Symbol	Min.	Max.	Unit	Test Conditions
Output low	All output pins (other than RIIC)	Normal output mode	V_{OL}	—	0.8	V	I_{OL} = 2.0 mA
		High-drive output mode		—	0.8		I_{OL} = 4.0 mA
	RIIC pins			—	0.4		I_{OL} = 3.0 mA
				—	0.6		I_{OL} = 6.0 mA
Output high	All output pins	Normal output mode	V_{OH}	VCC – 0.8	—	V	I_{OH} = –2.0 mA
		High-drive output mode		VCC – 0.8	—		I_{OH} = –4.0 mA

5.2.1 Standard I/O Pin Output Characteristics (1)

Figure 5.45 to Figure 5.49 show the characteristics when normal output is selected by the drive capacity control register.

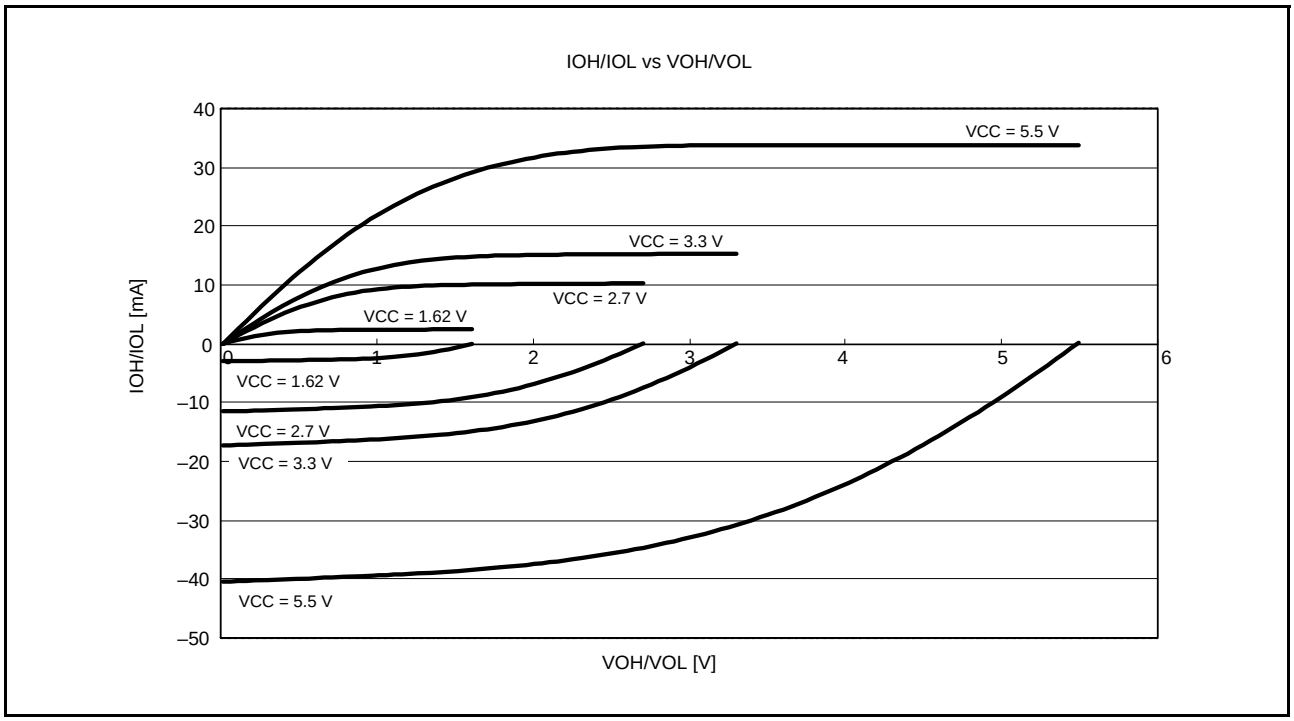


Figure 5.45 VOH/VOL and IOH/IOL Voltage Characteristics at Ta = 25°C when Normal Output is Selected (Reference Data)

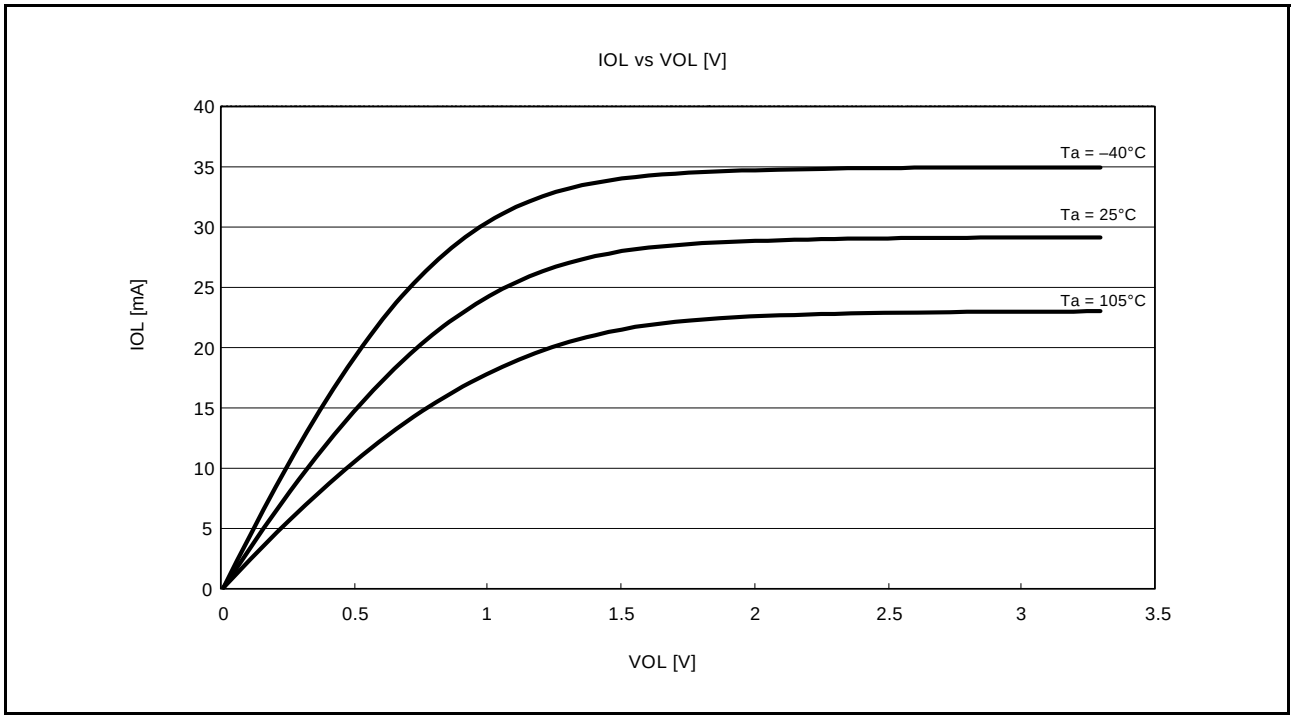


Figure 5.57 VOL and IOL Temperature Characteristics of RIIC Output Pin at VCC = 3.3 V (Reference Data)

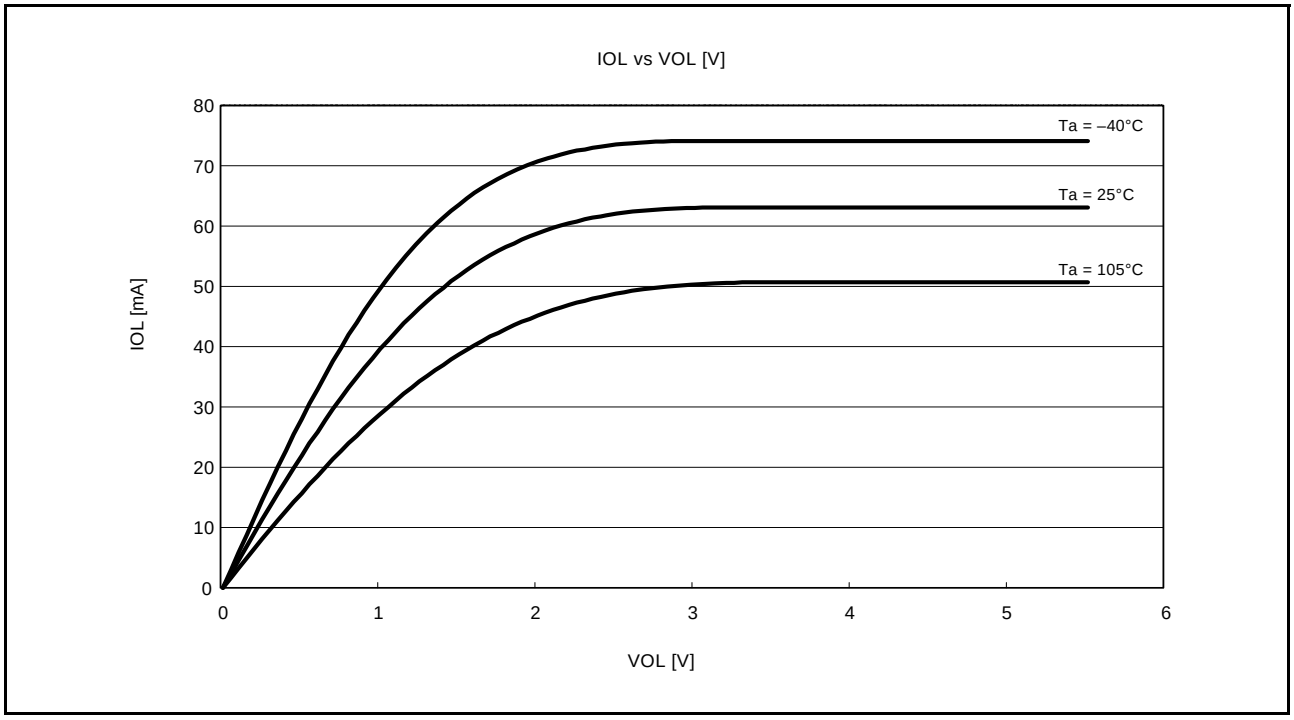


Figure 5.58 VOL and IOL Temperature Characteristics of RIIC Output Pin at VCC = 5.5 V (Reference Data)

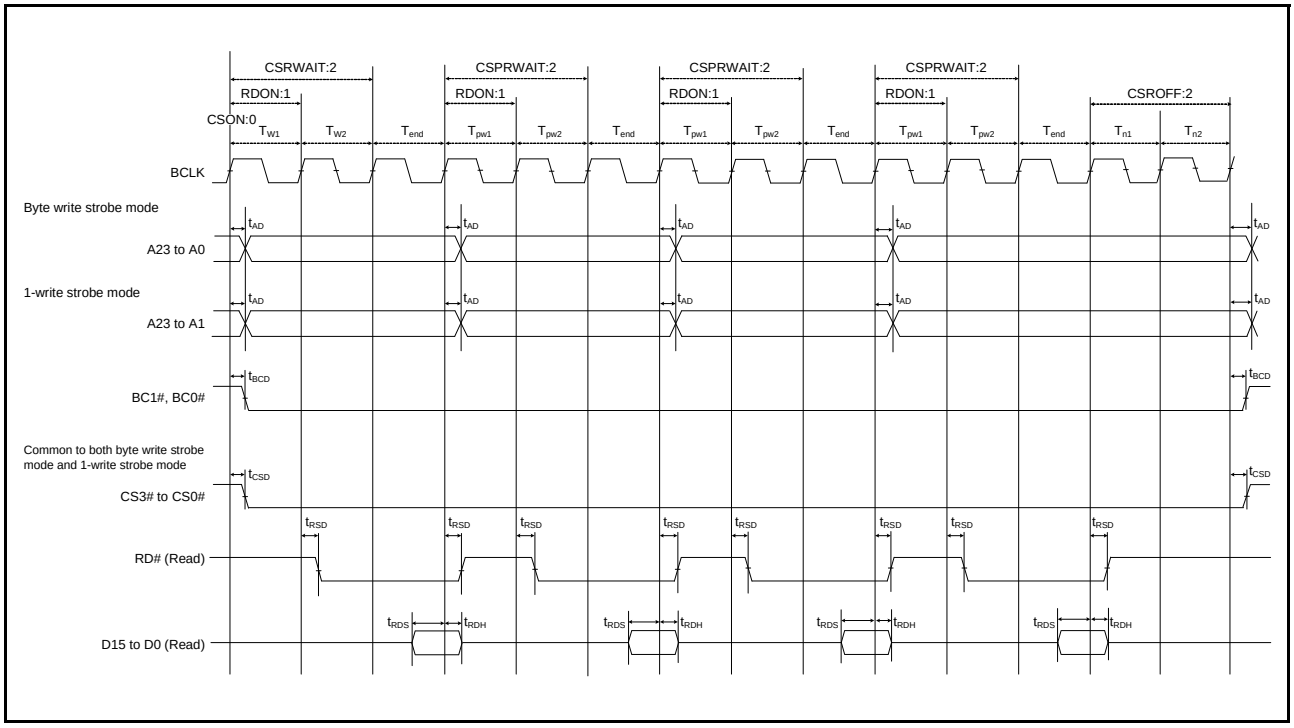
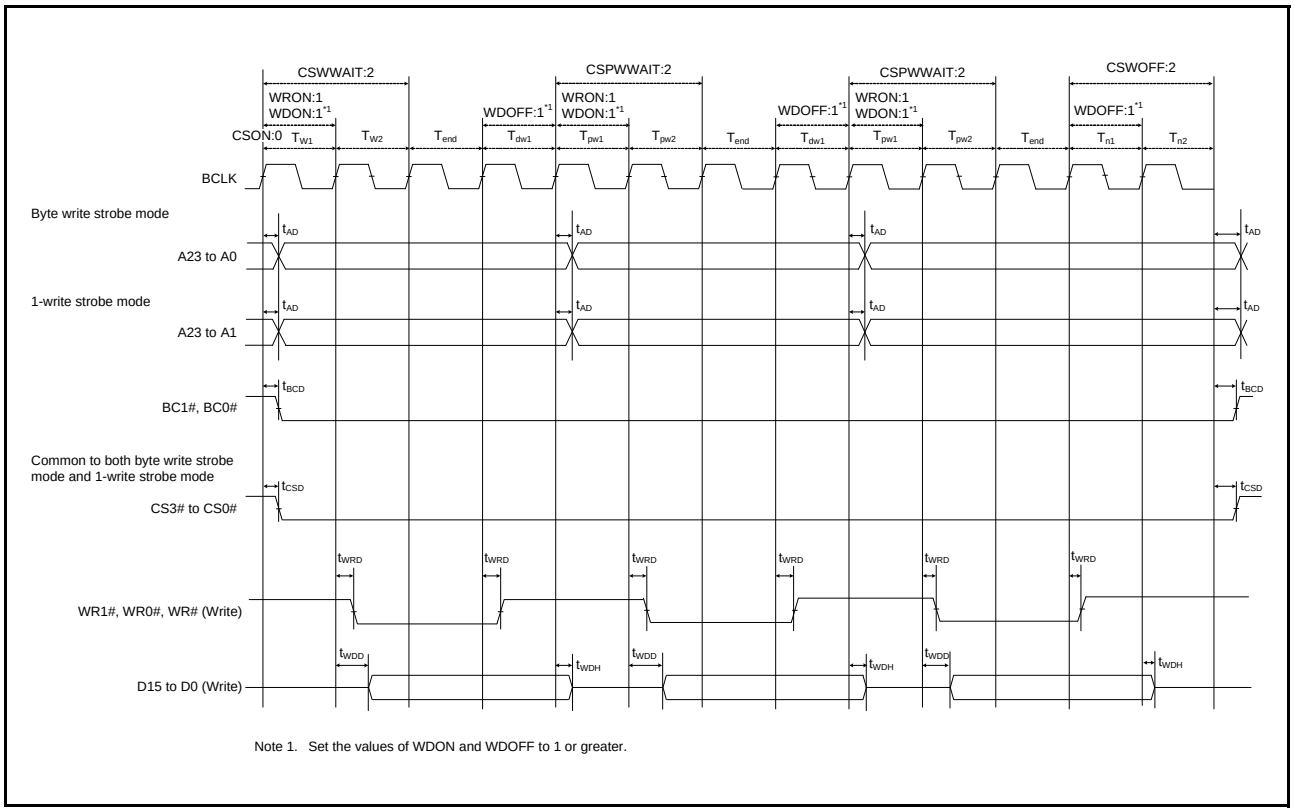


Figure 5.78 External Bus Timing/Page Read Cycle (Bus Clock Synchronized)



Note 1. Set the values of WDON and WDOFF to 1 or greater.

Figure 5.79 External Bus Timing/Page Write Cycle (Bus Clock Synchronized)

Table 5.62 Channel Classification for A/D Converter

Classification	Channel	Channel-Dedicated Sample-and-Hold Circuit	Conditions	
High-precision channel	AN000 to AN002	Used	AVCC0 = 2.7 to 5.5 V AVCC0 - 0.9 V ≤ VREFH0 ≤ AVCC0 VREFH0 ≥ 2.7 V AVSS0 = VREFL0 = 0 V 0.25 V ≤ V_{AN} ≤ AVCC0 - 0.25 V V_{AN} ≤ VREFH0	It is disallowed to use pins AN000 to AN007 as digital outputs when the A/D converter is used.
		Not used	AVCC0 = 1.62 to 5.5 V When AVCC0 ≥ 1.8 V, AVCC0 - 0.9 V ≤ VREFH0 ≤ AVCC0 VREFH0 ≥ 1.8 V When AVCC0 < 1.8 V, VREFH0 = AVCC0 AVSS0 = VREFL0 = 0 V 0 V ≤ V_{AN} ≤ VREFH0	
	AN003 to AN007	—		
Normal-precision channel	AN008 to AN015	—		

Table 5.63 A/D Internal Reference Voltage Characteristics

Conditions: VCC = AVCC0 = 1.62 to 5.5 V, VSS = AVSS0 = VREFL = VREFL0 = 0 V, Ta = −40 to +105°C

Item	Min.	Typ.	Max.	Unit	Test Conditions
A/D internal reference voltage	1.35	1.50	1.65	V	

5.5 D/A Conversion Characteristics

Table 5.67 D/A Conversion Characteristics (1)

Conditions: VCC = AVCC0 = 2.7 to 5.5 V, VREFH = 2.7 V to AVCC0,
VSS = AVSS0 = VREFL = VREFL0 = 0 V, fPCLKB = up to 32 MHz, T_a = –40 to +105°C

Item	Min.	Typ.	Max.	Unit	Test Conditions
Resolution	—	—	10	Bit	
Conversion time	—	—	3.0	µs	20-pF capacitive load
Absolute accuracy	—	±3.0	±5.0	LSB	4-MΩ resistive load
	—	—	±4.0	LSB	8-MΩ resistive load
RO output resistance	—	4.1	—	kΩ	

Table 5.68 D/A Conversion Characteristics (2)

Conditions: VCC = AVCC0 = 2.7 to 5.5 V, VREFH =1.8 V to AVCC0,
VSS = AVSS0 = VREFL = VREFL0 = 0 V, fPCLKB = up to 32 MHz, T_a = –40 to +105°C

Item	Min.	Typ.	Max.	Unit	Test Conditions
Resolution	—	—	10	Bit	
Conversion time	—	—	10.0	µs	20-pF capacitive load
Absolute accuracy	—	±5.0	±6.0	LSB	4-MΩ resistive load
	—	—	±5.0	LSB	8-MΩ resistive load
RO output resistance	—	4.1	—	kΩ	

5.6 Temperature Sensor Characteristics

Table 5.69 Temperature Sensor Characteristics

Conditions: VCC = AVCC0 = VREFH0 = 1.8 to 5.5 V, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Relative accuracy		—	—	±1.0	—	°C	
Temperature slope	1.8 ≤ AVCC0 < 2.7	—	—	7.27	—	mV/°C	PGAGAIN = 00b
	2.7 ≤ AVCC0 < 3.6		—	10.46	—		PGAGAIN = 01b
	3.6 ≤ AVCC0 < 4.5		—	13.98	—		PGAGAIN = 10b
	4.5 ≤ AVCC0 ≤ 5.5		—	21.65	—		PGAGAIN = 11b
Output voltage (@ 25°C)		—	—	1.375	—	V	VCC = 3.6 V
Temperature sensor start time		t_{START}	—	—	80	µs	Figure 5.102
Sampling time		—	30	72	300	µs	
PGA restart time		t_{RST_PGA}	—	—	40	µs	

[Chip versions A and C]

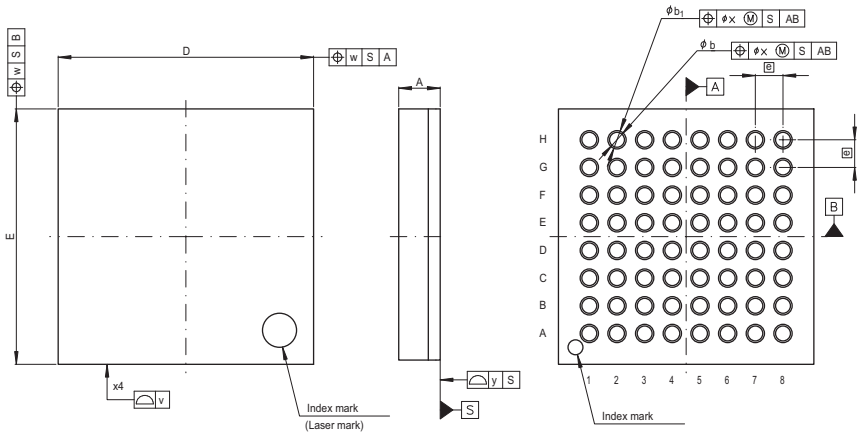
**Table 5.83 E2 DataFlash Characteristics (4)
: middle-speed operating mode 1B**

Conditions: VCC = AVCC0 = 1.62 to 3.6 V, VREFH = VREFH0 = AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V
Temperature range for the programming/erasure operation: T_a = –40 to +105°C

Item		Symbol	FCLK = 4 MHz			FCLK = 32 MHz*1			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Programming time when N_{DPEC} ≤ 100 times	2 bytes	t_{DP2}	—	0.52	5.1	—	0.24	2.8	ms
	8 bytes	t_{DP8}	—	0.57	6.0	—	0.26	3.2	
Programming time when N_{DPEC} > 100 times	2 bytes	t_{DP2}	—	0.77	7.6	—	0.36	4.2	ms
	8 bytes	t_{DP8}	—	0.84	8.8	—	0.38	4.5	
Erasure time when N_{DPEC} ≤ 100 times	128 bytes	t_{DE128}	—	6.8	32.5	—	4.4	12	ms
Erasure time when N_{DPEC} > 100 times	128 bytes	t_{DE128}	—	8.2	51.4	—	5.3	17	ms
Blank check time	2 bytes	t_{DBC2}	—	—	110	—	—	40	µs
	2 Kbytes	t_{DBC2K}	—	—	16.3	—	—	2.6	ms
Suspend delay time during programming (in programming/erasure priority mode)		t_{DSPD}	—	—	1.7	—	—	1.6	ms
First suspend delay time during programming (in suspend priority mode)		t_{DSPSD1}	—	—	220	—	—	120	µs
Second suspend delay time during programming (in suspend priority mode)		t_{DSPSD2}	—	—	1.7	—	—	1.6	ms
Suspend delay time during erasing (in programming/erasure priority mode)		t_{DSED}	—	—	1.7	—	—	1.6	ms
First suspend delay time during erasing (in suspend priority mode)		t_{DSESD1}	—	—	220	—	—	120	µs
Second suspend delay time during erasing (in suspend priority mode)		t_{DSESD2}	—	—	1.7	—	—	1.6	ms

Note 1. The operating frequency is 20 MHz (max.) when the voltage is in the range from 1.62 V to less than 1.8 V.

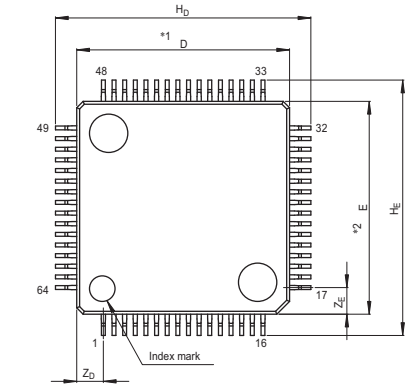
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-TFLGA64-6x6-0.65	PTLG0064JA-A	64F0G	0.07g

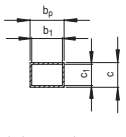


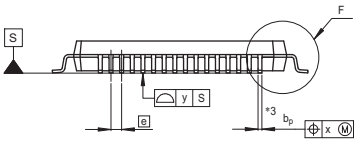
Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	6.0	—
E	—	6.0	—
v	—	—	0.15
w	—	—	0.20
A	—	—	1.05
e	—	0.65	—
b	0.31	0.35	0.39
b_1	0.39	0.43	0.47
x	—	—	0.08
y	—	—	0.10

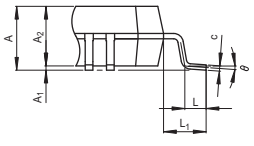
Figure F 64-Pin TFLGA (PTLG0064JA-A)

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LFQFP64-10x10-0.50	PLQP0064KB-A	64P6Q-A / FP-64K / FP-64KV	0.3g









NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	9.9	10.0	10.1
E	9.9	10.0	10.1
A_2	—	1.4	—
H_D	11.8	12.0	12.2
H_E	11.8	12.0	12.2
A	—	—	1.7
A_1	0.05	0.1	0.15
b_p	0.15	0.20	0.25
b_1	—	0.18	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
Z_D	—	1.25	—
Z_E	—	1.25	—
L	0.35	0.5	0.65
L_1	—	1.0	—

Figure J 64-Pin LQFP (PLQP0064KB-A)