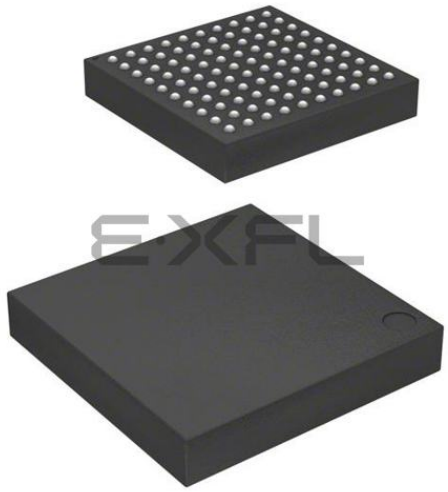

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Not For New Designs |
| Core Processor | RX |
| Core Size | 32-Bit Single-Core |
| Speed | 50MHz |
| Connectivity | EBI/EMI, I²C, SCI, SPI |
| Peripherals | DMA, LVD, POR, PWM, WDT |
| Number of I/O | 84 |
| Program Memory Size | 128KB (128K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | 8K x 8 |
| RAM Size | 20K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.62V ~ 5.5V |
| Data Converters | A/D 16x12b; D/A 2x10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 100-TFLGA |
| Supplier Device Package | 100-TFLGA (5.5x5.5) |
| Purchase URL | https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f52105bdla-u0 |

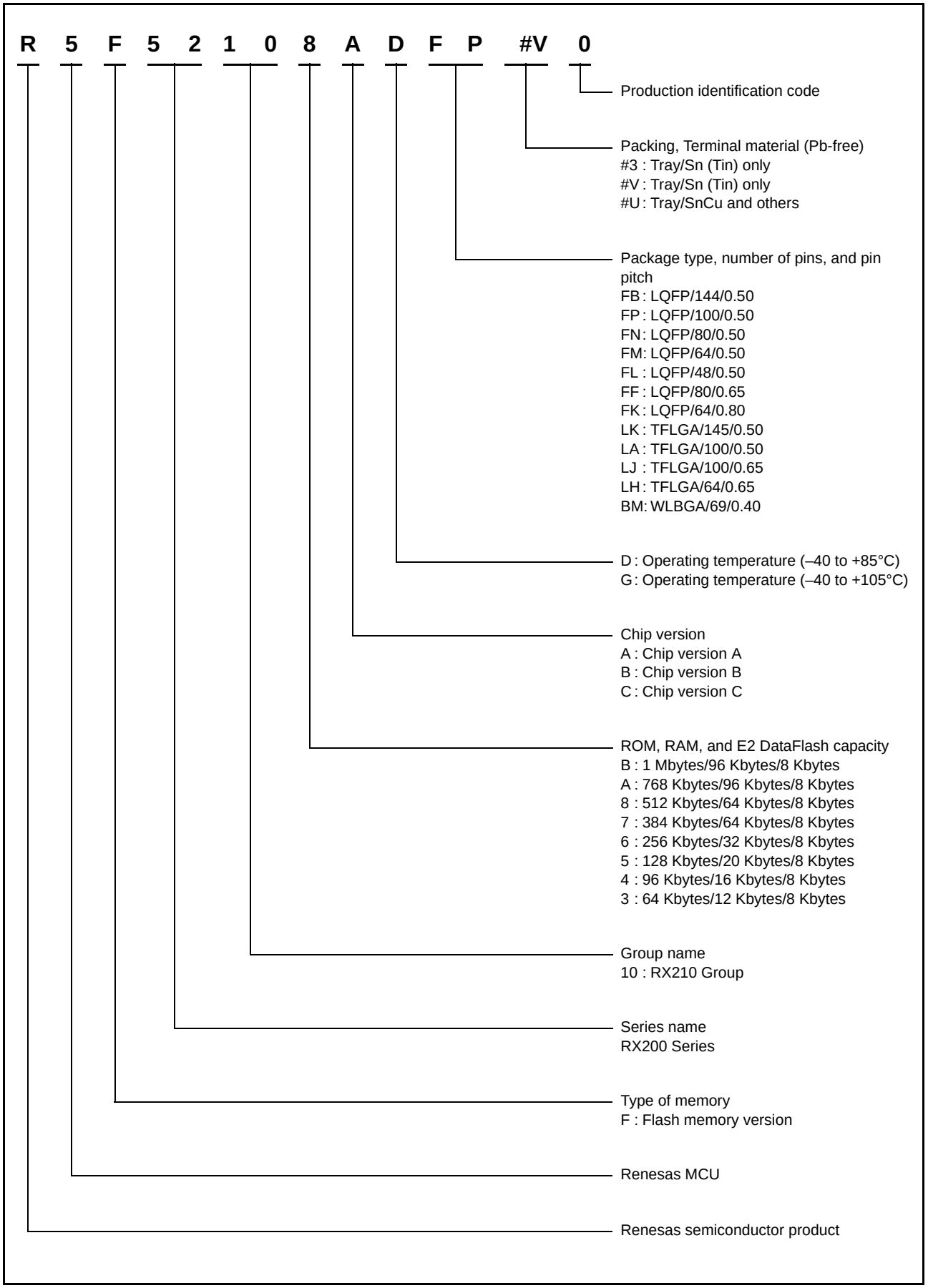



**Figure 1.1 How to Read the Product Part No., Memory Capacity, and Package Type**

**Table 4.1 List of I/O Registers (Address Order) (2 / 29)**

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles ICLK ≥ PCLK | Number of Access Cycles ICLK < PCLK |
|---|---|---|---|---|---|---|---|
| 0008 201Dh | DMAC0 | DMA software start register | DMREQ | 8 | 8 | 2 ICLK | |
| 0008 201Eh | DMAC0 | DMA status register | DMSTS | 8 | 8 | 2 ICLK | |
| 0008 201Fh | DMAC0 | DMA activation source flag control register | DMCSL | 8 | 8 | 2 ICLK | |
| 0008 2040h | DMAC1 | DMA source address register | DMSAR | 32 | 32 | 2 ICLK | |
| 0008 2044h | DMAC1 | DMA destination address register | DMDAR | 32 | 32 | 2 ICLK | |
| 0008 2048h | DMAC1 | DMA transfer count register | DMCRA | 32 | 32 | 2 ICLK | |
| 0008 204Ch | DMAC1 | DMA block transfer count register | DMCRB | 16 | 16 | 2 ICLK | |
| 0008 2050h | DMAC1 | DMA transfer mode register | DMTMD | 16 | 16 | 2 ICLK | |
| 0008 2053h | DMAC1 | DMA interrupt setting register | DMINT | 8 | 8 | 2 ICLK | |
| 0008 2054h | DMAC1 | DMA address mode register | DMAMD | 16 | 16 | 2 ICLK | |
| 0008 205Ch | DMAC1 | DMA transfer enable register | DMCNT | 8 | 8 | 2 ICLK | |
| 0008 205Dh | DMAC1 | DMA software start register | DMREQ | 8 | 8 | 2 ICLK | |
| 0008 205Eh | DMAC1 | DMA status register | DMSTS | 8 | 8 | 2 ICLK | |
| 0008 205Fh | DMAC1 | DMA activation source flag control register | DMCSL | 8 | 8 | 2 ICLK | |
| 0008 2080h | DMAC2 | DMA source address register | DMSAR | 32 | 32 | 2 ICLK | |
| 0008 2084h | DMAC2 | DMA destination address register | DMDAR | 32 | 32 | 2 ICLK | |
| 0008 2088h | DMAC2 | DMA transfer count register | DMCRA | 32 | 32 | 2 ICLK | |
| 0008 208Ch | DMAC2 | DMA block transfer count register | DMCRB | 16 | 16 | 2 ICLK | |
| 0008 2090h | DMAC2 | DMA transfer mode register | DMTMD | 16 | 16 | 2 ICLK | |
| 0008 2093h | DMAC2 | DMA interrupt setting register | DMINT | 8 | 8 | 2 ICLK | |
| 0008 2094h | DMAC2 | DMA address mode register | DMAMD | 16 | 16 | 2 ICLK | |
| 0008 209Ch | DMAC2 | DMA transfer enable register | DMCNT | 8 | 8 | 2 ICLK | |
| 0008 209Dh | DMAC2 | DMA software start register | DMREQ | 8 | 8 | 2 ICLK | |
| 0008 209Eh | DMAC2 | DMA status register | DMSTS | 8 | 8 | 2 ICLK | |
| 0008 209Fh | DMAC2 | DMA activation source flag control register | DMCSL | 8 | 8 | 2 ICLK | |
| 0008 20C0h | DMAC3 | DMA source address register | DMSAR | 32 | 32 | 2 ICLK | |
| 0008 20C4h | DMAC3 | DMA destination address register | DMDAR | 32 | 32 | 2 ICLK | |
| 0008 20C8h | DMAC3 | DMA transfer count register | DMCRA | 32 | 32 | 2 ICLK | |
| 0008 20CCh | DMAC3 | DMA block transfer count register | DMCRB | 16 | 16 | 2 ICLK | |
| 0008 20D0h | DMAC3 | DMA transfer mode register | DMTMD | 16 | 16 | 2 ICLK | |
| 0008 20D3h | DMAC3 | DMA interrupt setting register | DMINT | 8 | 8 | 2 ICLK | |
| 0008 20D4h | DMAC3 | DMA address mode register | DMAMD | 16 | 16 | 2 ICLK | |
| 0008 20DCh | DMAC3 | DMA transfer enable register | DMCNT | 8 | 8 | 2 ICLK | |
| 0008 20DDh | DMAC3 | DMA software start register | DMREQ | 8 | 8 | 2 ICLK | |
| 0008 20DEh | DMAC3 | DMA status register | DMSTS | 8 | 8 | 2 ICLK | |
| 0008 20DFh | DMAC3 | DMA activation source flag control register | DMCSL | 8 | 8 | 2 ICLK | |
| 0008 2200h | DMAC | DMA module activation register | DMAST | 8 | 8 | 2 ICLK | |
| 0008 2400h | DTC | DTC control register | DTCCR | 8 | 8 | 2 ICLK | |
| 0008 2404h | DTC | DTC vector base register | DTCVBR | 32 | 32 | 2 ICLK | |
| 0008 2408h | DTC | DTC address mode register | DTCADMOD | 8 | 8 | 2 ICLK | |
| 0008 240Ch | DTC | DTC module start register | DTCST | 8 | 8 | 2 ICLK | |
| 0008 240Eh | DTC | DTC status register | DTCSTS | 16 | 16 | 2 ICLK | |
| 0008 3002h | BSC | CS0 mode register | CS0MOD | 16 | 16 | 1, 2 BCLK | |
| 0008 3004h | BSC | CS0 wait control register 1 | CS0WCR1 | 32 | 32 | 1, 2 BCLK | |
| 0008 3008h | BSC | CS0 wait control register 2 | CS0WCR2 | 32 | 32 | 1, 2 BCLK | |
| 0008 3012h | BSC | CS1 mode register | CS1MOD | 16 | 16 | 1, 2 BCLK | |
| 0008 3014h | BSC | CS1 wait control register 1 | CS1WCR1 | 32 | 32 | 1, 2 BCLK | |
| 0008 3018h | BSC | CS1 wait control register 2 | CS1WCR2 | 32 | 32 | 1, 2 BCLK | |
| 0008 3022h | BSC | CS2 mode register | CS2MOD | 16 | 16 | 1, 2 BCLK | |
| 0008 3024h | BSC | CS2 wait control register 1 | CS2WCR1 | 32 | 32 | 1, 2 BCLK | |
| 0008 3028h | BSC | CS2 wait control register 2 | CS2WCR2 | 32 | 32 | 1, 2 BCLK | |

**Table 4.1 List of I/O Registers (Address Order) (13 / 29)**

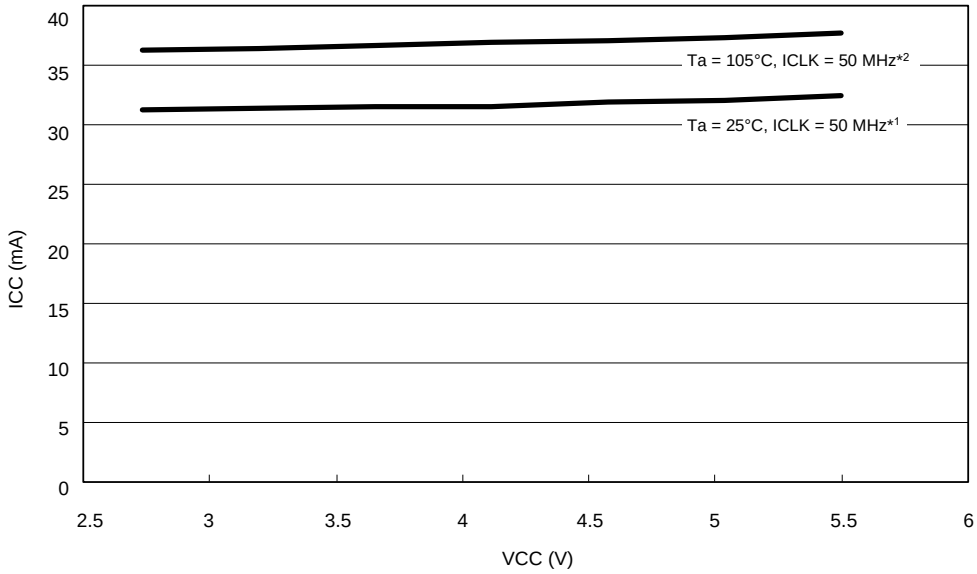
| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles: ICLK ≥ PCLK | Number of Access Cycles: ICLK < PCLK |
|---|---|---|---|---|---|---|---|
| 0008 820Ah | TMR0 | Timer counter control register | TCCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 820Bh | TMR1 | Timer counter control register | TCCR | 8 | 8*1 | 2, 3 PCLKB | 2 ICLK |
| 0008 820Ch | TMR0 | Time count start register | TCSTR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 8210h | TMR2 | Timer control register | TCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 8211h | TMR3 | Timer control register | TCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 8212h | TMR2 | Timer control/status register | TCSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 8213h | TMR3 | Timer control/status register | TCSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 8214h | TMR2 | Time constant register A | TCORA | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 8215h | TMR3 | Time constant register A | TCORA | 8 | 8*1 | 2, 3 PCLKB | 2 ICLK |
| 0008 8216h | TMR2 | Time constant register B | TCORB | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 8217h | TMR3 | Time constant register B | TCORB | 8 | 8*1 | 2, 3 PCLKB | 2 ICLK |
| 0008 8218h | TMR2 | Timer counter | TCNT | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 8219h | TMR3 | Timer counter | TCNT | 8 | 8*1 | 2, 3 PCLKB | 2 ICLK |
| 0008 821Ah | TMR2 | Timer counter control register | TCCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 821Bh | TMR3 | Timer counter control register | TCCR | 8 | 8*1 | 2, 3 PCLKB | 2 ICLK |
| 0008 821Ch | TMR2 | Time count start register | TCSTR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 8280h | CRC | CRC control register | CRCCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 8281h | CRC | CRC data input register | CRCDIR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 8282h | CRC | CRC data output register | CRCDOR | 16 | 16 | 2, 3 PCLKB | 2 ICLK |
| 0008 8300h | RIIC0 | $I^2C$ bus control register 1 | ICCR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 8301h | RIIC0 | $I^2C$ bus control register 2 | ICCR2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 8302h | RIIC0 | $I^2C$ bus mode register 1 | ICMR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 8303h | RIIC0 | $I^2C$ bus mode register 2 | ICMR2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 8304h | RIIC0 | $I^2C$ bus mode register 3 | ICMR3 | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 8305h | RIIC0 | $I^2C$ bus function enable register | ICFER | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 8306h | RIIC0 | $I^2C$ bus status enable register | ICSER | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 8307h | RIIC0 | $I^2C$ bus interrupt enable register | ICIER | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 8308h | RIIC0 | $I^2C$ bus status register 1 | ICSR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 8309h | RIIC0 | $I^2C$ bus status register 2 | ICSR2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 830Ah | RIIC0 | Slave address register L0 | SARL0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 830Ah | RIIC0 | Timeout internal counter L | TMOCNTL | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 830Bh | RIIC0 | Slave address register U0 | SARU0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 830Bh | RIIC0 | Timeout internal counter U | TMOCNTU | 8 | 8*2 | 2, 3 PCLKB | 2 ICLK |
| 0008 830Ch | RIIC0 | Slave address register L1 | SARL1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 830Dh | RIIC0 | Slave address register U1 | SARU1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 830Eh | RIIC0 | Slave address register L2 | SARL2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 830Fh | RIIC0 | Slave address register U2 | SARU2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 8310h | RIIC0 | $I^2C$ bus bit rate low-level register | ICBRL | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 8311h | RIIC0 | $I^2C$ bus bit rate high-level register | ICBRH | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 8312h | RIIC0 | $I^2C$ bus transmit data register | ICDRT | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 8313h | RIIC0 | $I^2C$ bus receive data register | ICDRR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 8380h | RSPI0 | RSPI control register | SPCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 8381h | RSPI0 | RSPI slave select polarity register | SSLP | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 8382h | RSPI0 | RSPI pin control register | SPPCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 8383h | RSPI0 | RSPI status register | SPSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 8384h | RSPI0 | RSPI data register | SPDR | 32 | 16, 32 | 2, 3 PCLKB | 2 ICLK |
| 0008 8388h | RSPI0 | RSPI sequence control register | SPSCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 8389h | RSPI0 | RSPI sequence status register | SPSSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 838Ah | RSPI0 | RSPI bit rate register | SPBR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 838Bh | RSPI0 | RSPI data control register | SPDCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 838Ch | RSPI0 | RSPI clock delay register | SPCKD | 8 | 8 | 2, 3 PCLKB | 2 ICLK |

**Table 4.1 List of I/O Registers (Address Order) (14 / 29)**

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles: ICLK ≥ PCLK | Number of Access Cycles: ICLK < PCLK |
|---|---|---|---|---|---|---|---|
| 0008 838Dh | RSPI0 | RSPI slave select negation delay register | SSLND | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 838Eh | RSPI0 | RSPI next-access delay register | SPND | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 838Fh | RSPI0 | RSPI control register 2 | SPCR2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 8390h | RSPI0 | RSPI command register 0 | SPCMD0 | 16 | 16 | 2, 3 PCLKB | 2 ICLK |
| 0008 8392h | RSPI0 | RSPI command register 1 | SPCMD1 | 16 | 16 | 2, 3 PCLKB | 2 ICLK |
| 0008 8394h | RSPI0 | RSPI command register 2 | SPCMD2 | 16 | 16 | 2, 3 PCLKB | 2 ICLK |
| 0008 8396h | RSPI0 | RSPI command register 3 | SPCMD3 | 16 | 16 | 2, 3 PCLKB | 2 ICLK |
| 0008 8398h | RSPI0 | RSPI command register 4 | SPCMD4 | 16 | 16 | 2, 3 PCLKB | 2 ICLK |
| 0008 839Ah | RSPI0 | RSPI command register 5 | SPCMD5 | 16 | 16 | 2, 3 PCLKB | 2 ICLK |
| 0008 839Ch | RSPI0 | RSPI command register 6 | SPCMD6 | 16 | 16 | 2, 3 PCLKB | 2 ICLK |
| 0008 839Eh | RSPI0 | RSPI command register 7 | SPCMD7 | 16 | 16 | 2, 3 PCLKB | 2 ICLK |
| 0008 8600h | MTU3 | Timer control register | TCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 8601h | MTU4 | Timer control register | TCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 8602h | MTU3 | Timer mode register | TMDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 8603h | MTU4 | Timer mode register | TMDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 8604h | MTU3 | Timer I/O control register H | TIORH | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 8605h | MTU3 | Timer I/O control register L | TIORL | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 8606h | MTU4 | Timer I/O control register H | TIORH | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 8607h | MTU4 | Timer I/O control register L | TIORL | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 8608h | MTU3 | Timer interrupt enable register | TIER | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 8609h | MTU4 | Timer interrupt enable register | TIER | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 860Ah | MTU | Timer output master enable register | TOER | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 860Dh | MTU | Timer gate control register | TGCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 860Eh | MTU | Timer output control register 1 | TOCR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 860Fh | MTU | Timer output control register 2 | TOCR2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 8610h | MTU3 | Timer counter | TCNT | 16 | 16 | 2, 3 PCLKB | 2 ICLK |
| 0008 8612h | MTU4 | Timer counter | TCNT | 16 | 16 | 2, 3 PCLKB | 2 ICLK |
| 0008 8614h | MTU | Timer cycle data register | TCDR | 16 | 16 | 2, 3 PCLKB | 2 ICLK |
| 0008 8616h | MTU | Timer dead time data register | TDDR | 16 | 16 | 2, 3 PCLKB | 2 ICLK |
| 0008 8618h | MTU3 | Timer general register A | TGRA | 16 | 16 | 2, 3 PCLKB | 2 ICLK |
| 0008 861Ah | MTU3 | Timer general register B | TGRB | 16 | 16 | 2, 3 PCLKB | 2 ICLK |
| 0008 861Ch | MTU4 | Timer general register A | TGRA | 16 | 16 | 2, 3 PCLKB | 2 ICLK |
| 0008 861Eh | MTU4 | Timer general register B | TGRB | 16 | 16 | 2, 3 PCLKB | 2 ICLK |
| 0008 8620h | MTU | Timer subcounter | TCNTS | 16 | 16 | 2, 3 PCLKB | 2 ICLK |
| 0008 8622h | MTU | Timer cycle buffer register | TCBR | 16 | 16 | 2, 3 PCLKB | 2 ICLK |
| 0008 8624h | MTU3 | Timer general register C | TGRC | 16 | 16 | 2, 3 PCLKB | 2 ICLK |
| 0008 8626h | MTU3 | Timer general register D | TGRD | 16 | 16 | 2, 3 PCLKB | 2 ICLK |
| 0008 8628h | MTU4 | Timer general register C | TGRC | 16 | 16 | 2, 3 PCLKB | 2 ICLK |
| 0008 862Ah | MTU4 | Timer general register D | TGRD | 16 | 16 | 2, 3 PCLKB | 2 ICLK |
| 0008 862Ch | MTU3 | Timer status register | TSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 862Dh | MTU4 | Timer status register | TSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 8630h | MTU | Timer interrupt skipping set register | TITCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 8631h | MTU | Timer interrupt skipping counter | TITCNT | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 8632h | MTU | Timer buffer transfer set register | TBTER | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 8634h | MTU | Timer dead time enable register | TDER | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 8636h | MTU | Timer output level buffer register | TOLBR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 8638h | MTU3 | Timer buffer operation transfer mode register | TBTM | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 8639h | MTU4 | Timer buffer operation transfer mode register | TBTM | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 8640h | MTU4 | Timer A/D converter start request control register | TADCR | 16 | 16 | 2, 3 PCLKB | 2 ICLK |
| 0008 8644h | MTU4 | Timer A/D converter start request cycle set register A | TADCORA | 16 | 16 | 2, 3 PCLKB | 2 ICLK |
| 0008 8646h | MTU4 | Timer A/D converter start request cycle set register B | TADCORB | 16 | 16 | 2, 3 PCLKB | 2 ICLK |

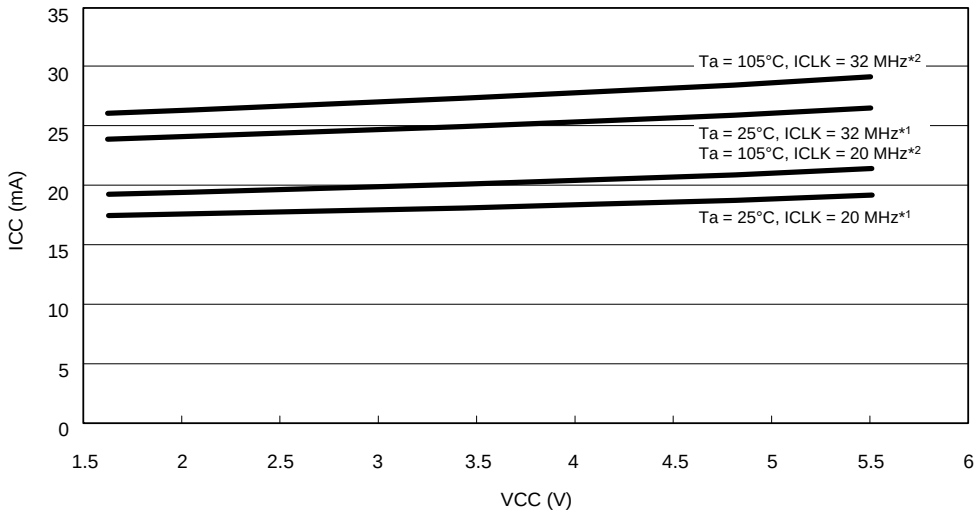
**Table 4.1 List of I/O Registers (Address Order) (24 / 29)**

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles: ICLK ≥ PCLK | Number of Access Cycles: ICLK < PCLK |
|---|---|---|---|---|---|---|---|
| 0008 C04Ch | PORTC | Port input data register | PIDR | 8 | 8 | 3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing | 3 ICLK cycles when reading, 2 ICLK cycles when writing |
| 0008 C04Dh | PORTD | Port input data register | PIDR | 8 | 8 | 3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing | 3 ICLK cycles when reading, 2 ICLK cycles when writing |
| 0008 C04Eh | PORTE | Port input data register | PIDR | 8 | 8 | 3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing | 3 ICLK cycles when reading, 2 ICLK cycles when writing |
| 0008 C04Fh | PORTF | Port input data register | PIDR | 8 | 8 | 3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing | 3 ICLK cycles when reading, 2 ICLK cycles when writing |
| 0008 C051h | PORTH | Port input data register | PIDR | 8 | 8 | 3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing | 3 ICLK cycles when reading, 2 ICLK cycles when writing |
| 0008 C052h | PORTJ | Port input data register | PIDR | 8 | 8 | 3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing | 3 ICLK cycles when reading, 2 ICLK cycles when writing |
| 0008 C053h | PORTK | Port input data register | PIDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 C054h | PORTL | Port input data register | PIDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 C060h | PORT0 | Port mode register | PMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 C061h | PORT1 | Port mode register | PMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 C062h | PORT2 | Port mode register | PMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 C063h | PORT3 | Port mode register | PMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 C064h | PORT4 | Port mode register | PMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 C065h | PORT5 | Port mode register | PMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 C066h | PORT6 | Port mode register | PMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 C067h | PORT7 | Port mode register | PMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 C068h | PORT8 | Port mode register | PMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 C069h | PORT9 | Port mode register | PMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 C06Ah | PORTA | Port mode register | PMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 C06Bh | PORTB | Port mode register | PMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 C06Ch | PORTC | Port mode register | PMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 C06Dh | PORTD | Port mode register | PMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 C06Eh | PORTE | Port mode register | PMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 C06Fh | PORTF | Port mode register | PMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 C071h | PORTH | Port mode register | PMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 C072h | PORTJ | Port mode register | PMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 C073h | PORTK | Port mode register | PMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 C074h | PORTL | Port mode register | PMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |




Note 1. All peripheral operation is normal. This does not include BGO operation.
Average value of the tested middle samples during product evaluation.
Note 2. All peripheral operation is maximum. This does not include BGO operation.
Average value of the tested upper-limit samples during product evaluation.

**Figure 5.1 Voltage Dependency in High-Speed Operating Mode (Reference Data) for Chip Version A**




Note 1. All peripheral operation is normal. This does not include BGO operation.
Average value of the tested middle samples during product evaluation.
Note 2. All peripheral operation is maximum. This does not include BGO operation.
Average value of the tested upper-limit samples during product evaluation.

**Figure 5.2 Voltage Dependency in Middle-Speed Operating Modes 1A and 1B (Reference Data) for Chip Version A**

[Chip version C]

**Table 5.9 DC Characteristics (8)**

Conditions: VCC = AVCC0 = 2.7 to 5.5 V, VSS = AVSS0 = VREFL = VREFL0 = 0 V, $T_a$ = –40 to +105°C

| Item | | | | | Symbol | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|---|---|
| Supply current*1 | High-speed operating mode | Normal operating mode | No peripheral operation*2 | ICLK = 50 MHz | $I_{CC}$ | 10 | — | mA | |
| | | | All peripheral operation: Normal*3 | ICLK = 50 MHz | | 31.5 | — | | |
| | | | All peripheral operation: Max.*3 | ICLK = 50 MHz | | — | 55 | | |
| | | Sleep mode | No peripheral operation | ICLK = 50 MHz | | 7.5 | — | | |
| | | | All peripheral operation: Normal | ICLK = 50 MHz | | 17.5 | — | | |
| | | All-module clock stop mode | | ICLK = 50 MHz | | 6.7 | — | | |
| | | Increase during BGO operation*4 | | | | 25 | — | | |

Note 1. Supply current values do not include output charge/discharge current from all pins. The values apply when internal pull-up MOSs are in the off state.

Note 2. Clock supply to the peripheral functions is stopped. This does not include BGO operation. The clock source is PLL and the VCO oscillation frequency is 100 MHz. BCLK, FCLK, and PCLK are set to divided by 64.

Note 3. Clocks are supplied to the peripheral functions. This does not include BGO operation. The clock source is PLL and the VCO oscillation frequency is 100 MHz. BCLK, FCLK, and PCLK are ICLK divided by 2.

Note 4. This is the increase if data is programmed to or erasing from the ROM or E2 DataFlash during program execution.

| Item | | | | | Symbol | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|---|---|
| Supply current*1 | Low-speed operating mode 1 | Normal operating mode | No peripheral operation*7 | ICLK = 8 MHz | $I_{CC}$ | 2.1 | — | mA | |
| | | | | ICLK = 4 MHz | | 1.7 | — | | |
| | | | | ICLK = 2 MHz | | 1.5 | — | | |
| | | | All peripheral operation: Normal*8 | ICLK = 8 MHz | | 7.3 | — | | |
| | | | | ICLK = 4 MHz | | 4.5 | — | | |
| | | | | ICLK = 2 MHz | | 3.1 | — | | |
| | | | All peripheral operation: Max.*7 | ICLK = 8 MHz | | — | 12 | | |
| | | | | ICLK = 4 MHz | | — | — | | |
| | | | | ICLK = 2 MHz | | — | — | | |
| | | Sleep mode | No peripheral operation | ICLK = 8 MHz | | 1.5 | — | | |
| | | | | ICLK = 4 MHz | | 1.4 | — | | |
| | | | | ICLK = 2 MHz | | 1.3 | — | | |
| | | | All peripheral operation: Normal | ICLK = 8 MHz | | 4.1 | — | | |
| | | | | ICLK = 4 MHz | | 3.0 | — | | |
| | | | | ICLK = 2 MHz | | 2.3 | — | | |
| | | All-module clock stop mode | | ICLK = 8 MHz | | 1.4 | — | | |
| | | | | ICLK = 4 MHz | | 1.3 | — | | |
| | | | | ICLK = 2 MHz | | 1.2 | — | | |
| | Low-speed operating mode 2 | Normal operating mode | No peripheral operation*9 | ICLK = 32 kHz | | 0.022 | — | | |
| | | | All peripheral operation: Normal*10 | ICLK = 32 kHz | | 0.06 | — | | |
| | | | All peripheral operation: Max.*10 | ICLK = 32 kHz | | — | 3*11 | | |
| | | Sleep mode | No peripheral operation | ICLK = 32 kHz | | 0.017 | — | | |
| | | | All peripheral operation: Normal | ICLK = 32 kHz | | 0.036 | — | | |
| | | All-module clock stop mode | | | | 0.017 | — | | |

Note 1. Supply current values do not include output charge/discharge current from all pins. The values apply when internal pull-up MOSs are in the off state.
Note 2. Clock supply to the peripheral functions is stopped. This does not include BGO operation. The clock source is PLL and the VCO oscillation frequency is 64 MHz. BCLK, FCLK, and PCLK are set to divided by 64.
Note 3. Clock supply to the peripheral functions is stopped. This does not include BGO operation. The clock source is HOCO and the oscillation frequency is 40 MHz. BCLK, FCLK, and PCLK are set to divided by 64.
Note 4. Clocks are supplied to the peripheral functions. This does not include BGO operation. The clock source is PLL and the VCO oscillation frequency is 64 MHz. BCLK, FCLK, and PCLK are ICLK divided by 1.
Note 5. Clocks are supplied to the peripheral functions. This does not include BGO operation. The clock source is HOCO and the oscillation frequency is 40 MHz. BCLK, FCLK, and PCLK are ICLK divided by 1.
Note 6. This is the increase if data is programmed to or erasing from the ROM or E2 DataFlash during program execution.
Note 7. Clock supply to the peripheral functions is stopped. This does not include BGO operation. The clock source is HOCO and the oscillation frequency is 32 MHz. BCLK, FCLK, and PCLK are set to divided by 64.
Note 8. Clocks are supplied to the peripheral functions. This does not include BGO operation. The clock source is HOCO and the oscillation frequency is 32 MHz. BCLK, FCLK, and PCLK are ICLK divided by 1.
Note 9. Clock supply to the peripheral functions is stopped. This does not include BGO operation. The clock source is the sub oscillation circuit. BCLK, FCLK, and PCLK are set to divided by 64.
Note 10. Clocks are supplied to the peripheral functions. This does not include BGO operation. The clock source is the sub oscillation circuit. BCLK, FCLK, and PCLK are ICLK divided by 1.
Note 11. Value when the main clock continues oscillating at 12.5 MHz.

[Chip version B with 512 Kbytes or less of flash memory and 144 and 145 pins]

**Table 5.18 DC Characteristics (17)**

Conditions: VCC = AVCC0 = 2.7 to 5.5 V, VSS = AVSS0 = VREFL = VREFL0 = 0 V, $T_a$ = –40 to +105°C

| Item | | | | | Symbol | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|---|---|
| Supply current*1 | High-speed operating mode | Normal operating mode | No peripheral operation*2 | ICLK = 50 MHz | $I_{CC}$ | 7.2 | — | mA | |
| | | | All peripheral operation: Normal*3 | ICLK = 50 MHz | | 25.9 | — | | |
| | | | All peripheral operation: Max.*3 | ICLK = 50 MHz | | — | 45 | | |
| | | Sleep mode | No peripheral operation | ICLK = 50 MHz | | 4.3 | — | | |
| | | | All peripheral operation: Normal | ICLK = 50 MHz | | 13 | — | | |
| | | All-module clock stop mode | | | | 3.7 | — | | |
| | | Increase during BGO operation*4 | | | | 21 | — | | |

Note 1. Supply current values do not include output charge/discharge current from all pins. The values apply when internal pull-up MOSs are in the off state.

Note 2. Clock supply to the peripheral functions is stopped. This does not include BGO operation. The clock source is PLL and the VCO oscillation frequency is 100 MHz. BCLK, FCLK, and PCLK are set to divided by 64.

Note 3. Clocks are supplied to the peripheral functions. This does not include BGO operation. The clock source is PLL and the VCO oscillation frequency is 100 MHz. BCLK, FCLK, and PCLK are ICLK divided by 2.

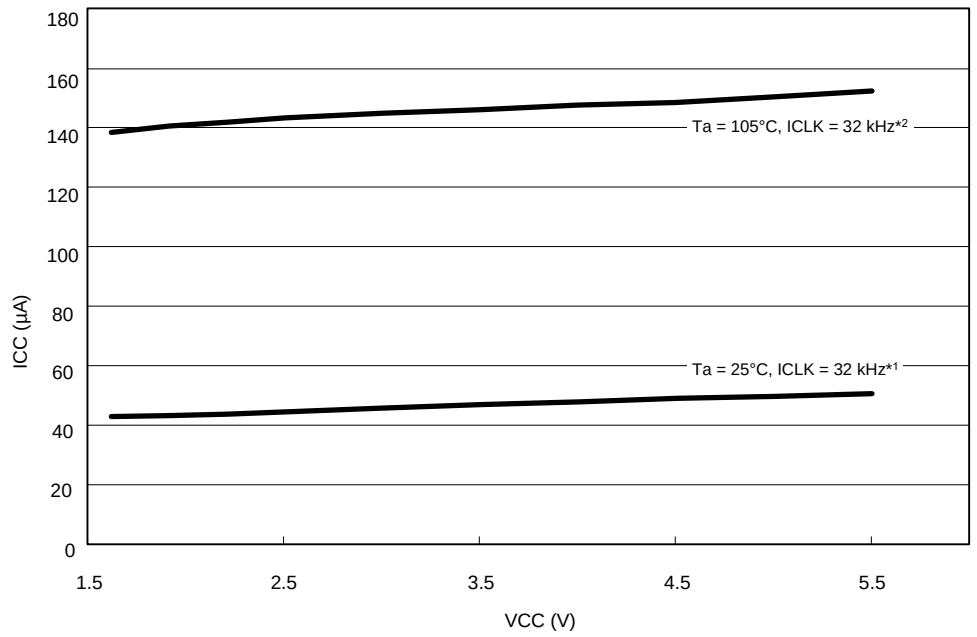
Note 4. This is the increase if data is programmed to or erasing from the ROM or E2 DataFlash during program execution.

[Chip version B with 512 Kbytes or less of flash memory and 144 and 145 pins]

**Table 5.19 DC Characteristics (18)**

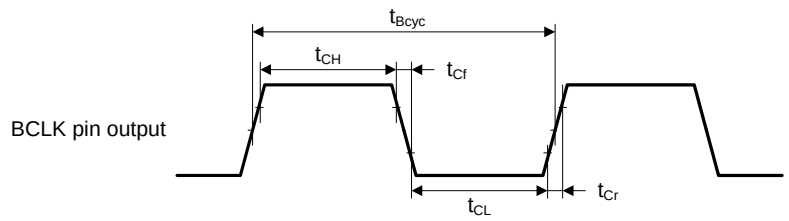
Conditions: VCC = AVCC0 = 1.62 to 5.5 V, VSS = AVSS0 = VREFL = VREFL0 = 0 V, $T_a$ = –40 to +105°C

| Item | | | | | Symbol | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|---|---|
| Supply current*1 | Middle-speed operating modes 1A and 1B | Normal operating mode | No peripheral operation | ICLK = 32 MHz*2 | $I_{CC}$ | 5.3 | — | mA | |
| | | | | ICLK = 20 MHz*3 | | 4.6 | — | | |
| | | | All peripheral operation: Normal | ICLK = 32 MHz*4 | | 22.3 | — | | |
| | | | | ICLK = 20 MHz*5 | | 15.6 | — | | |
| | | | All peripheral operation: Max. | ICLK = 32 MHz*4 | | — | 35 | | |
| | | | | ICLK = 20 MHz*5 | | — | — | | |
| | | Sleep mode | No peripheral operation | ICLK = 32 MHz | | 3.4 | — | | |
| | | | | ICLK = 20 MHz | | 3.3 | — | | |
| | | | All peripheral operation: Normal | ICLK = 32 MHz | | 12.8 | — | | |
| | | | | ICLK = 20 MHz | | 9.8 | — | | |
| | | All-module clock stop mode | | ICLK = 32 MHz | | 3 | — | | |
| | | | | ICLK = 20 MHz | | 3 | — | | |
| | | Increase during BGO operation*6 | Middle-speed operating mode 1A | | | 21 | — | | |
| | | | Middle-speed operating mode 1B | | | 19 | — | | |
| | Middle-speed operating modes 2A and 2B | Normal operating mode | No peripheral operation*2 | ICLK = 32 MHz | | 4.7 | — | | |
| | | | | ICLK = 16 MHz | | 3.4 | — | | |
| | | | | ICLK = 8 MHz | | 2.7 | — | | |
| | | | All peripheral operation: Normal*4 | ICLK = 32 MHz*3 | | 21.7 | — | | |
| | | | | ICLK = 16 MHz*3 | | 12.3 | — | | |
| | | | | ICLK = 8 MHz | | 7.6 | — | | |
| | | | All peripheral operation: Max.*4 | ICLK = 32 MHz*3 | | — | 34 | | |
| | | | | ICLK = 16 MHz*3 | | — | — | | |
| | | | | ICLK = 8 MHz | | — | — | | |
| | | Sleep mode | No peripheral operation | ICLK = 32 MHz | | 2.9 | — | | |
| | | | | ICLK = 16 MHz | | 2.5 | — | | |
| | | | | ICLK = 8 MHz | | 2.2 | — | | |
| | | | All peripheral operation: Normal | ICLK = 32 MHz | | 12.3 | — | | |
| | | | | ICLK = 16 MHz | | 7.8 | — | | |
| | | | | ICLK = 8 MHz | | 5.6 | — | | |
| | | All-module clock stop mode | | ICLK = 32 MHz | | 2.5 | — | | |
| | | | | ICLK = 16 MHz | | 2.2 | — | | |
| | | | | ICLK = 8 MHz | | 2.1 | — | | |
| | | Increase during BGO operation*6 | Middle-speed operating mode 1A | | | 21 | — | | |
| | | | Middle-speed operating mode 1B | | | 19 | — | | |




Note 1. All peripheral operation is normal.
Average value of the tested middle samples during product evaluation.
Note 2. All peripheral operation is maximum.
Average value of the tested upper-limit samples during product evaluation.

**Figure 5.39 Voltage Dependency in Low-Speed Operating Mode 2 (Reference Data) for Chip Version B with 512 Kbytes or Less of Flash Memory and 144 and 145 Pins**




Test conditions: VOH = VCC × 0.7, VOL = VCC × 0.3, IOH = –1.0 mA, IOL = 1.0 mA, C = 30 pF

**Figure 5.59 BCLK Pin Output Timing**

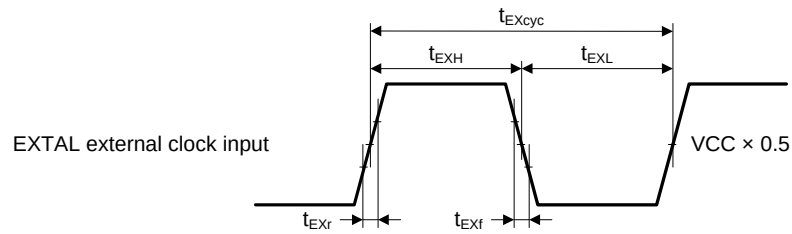



**Figure 5.60 EXTAL External Clock Input Timing**

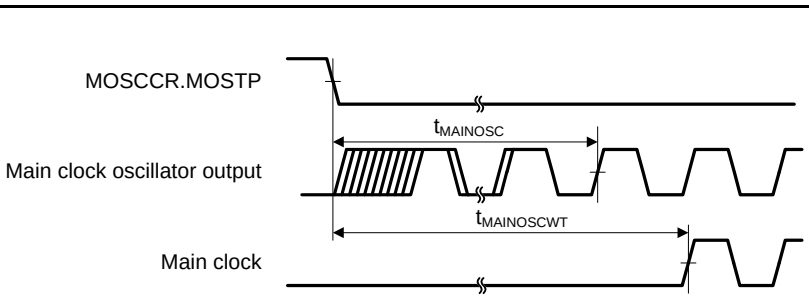



**Figure 5.61 Main Clock Oscillation Start Timing**

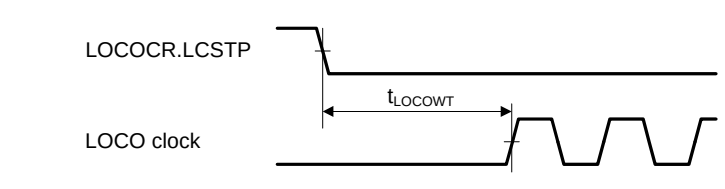



**Figure 5.62 LOCO Clock Oscillation Start Timing**

**Table 5.51 Bus Timing (3)**

Conditions: VCC = AVCC0 = 1.62 to 1.8 V, VSS = AVSS0 = VREFL = VREFL0 = 0 V,
fBCLK ≤ 12 MHz (BCLK pin output frequency ≤ 6 MHz), $T_a$ = –40 to +105°C, $V_{OH}$ = VCC × 0.5,
$V_{OL}$ = VCC × 0.5, $I_{OH}$ = –0.5 mA, $I_{OL}$ = 0.5 mA, $C_L$ = 30 pF
When normal output is selected by the drive capacity register

| Item | Symbol | Min. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|
| Address delay time | $t_{AD}$ | — | 125 | ns | Figure 5.76 to Figure 5.79 |
| Byte control delay time | $t_{BCD}$ | — | 125 | ns | |
| CS# delay time | $t_{CSD}$ | — | 125 | ns | |
| RD# delay time | $t_{RSD}$ | — | 125 | ns | |
| Read data setup time | $t_{RDS}$ | 85 | — | ns | |
| Read data hold time | $t_{RDH}$ | 0 | — | ns | |
| WR# delay time | $t_{WRD}$ | — | 125 | ns | |
| Write data delay time | $t_{WDD}$ | — | 125 | ns | |
| Write data hold time | $t_{WDH}$ | 0 | — | ns | |
| WAIT# setup time | $t_{WTS}$ | 85 | — | ns | Figure 5.80 |
| WAIT# hold time | $t_{WTH}$ | 0 | — | ns | |

**Table 5.54 Bus Timing (Multiplexed Bus) (3)**

Conditions: VCC = AVCC0 = 1.62 to 1.8 V, VSS = AVSS0 = VREFL = VREFL0 = 0 V,
fBCLK ≤ 12 MHz (BCLK pin output frequency ≤ 6 MHz), $T_a$ = –40 to +105°C, $V_{OH}$ = VCC × 0.5,
$V_{OL}$ = VCC × 0.5, $I_{OH}$ = –0.5 mA, $I_{OL}$ = 0.5 mA, $C_L$ = 30 pF
When normal output is selected by the drive capacity register

| Item | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| Address delay time | $t_{AD}$ | — | 125 | ns | Figure 5.81 and Figure 5.82 |
| Byte control delay time | $t_{BCD}$ | — | 125 | ns | |
| CS# delay time | $t_{CSD}$ | — | 125 | ns | |
| RD# delay time | $t_{RSD}$ | — | 125 | ns | |
| ALE delay time | $t_{ALED}$ | — | 125 | ns | |
| Read data setup time | $t_{RDS}$ | 85 | — | ns | |
| Read data hold time | $t_{RDH}$ | 0 | — | ns | |
| WR# delay time | $t_{WRD}$ | — | 125 | ns | |
| Write data delay time | $t_{WDD}$ | — | 125 | ns | |
| Write data hold time | $t_{WDH}$ | 0 | — | ns | |
| WAIT# setup time | $t_{WTS}$ | 85 | — | ns | Figure 5.80 |
| WAIT# hold time | $t_{WTH}$ | 0 | — | ns | |

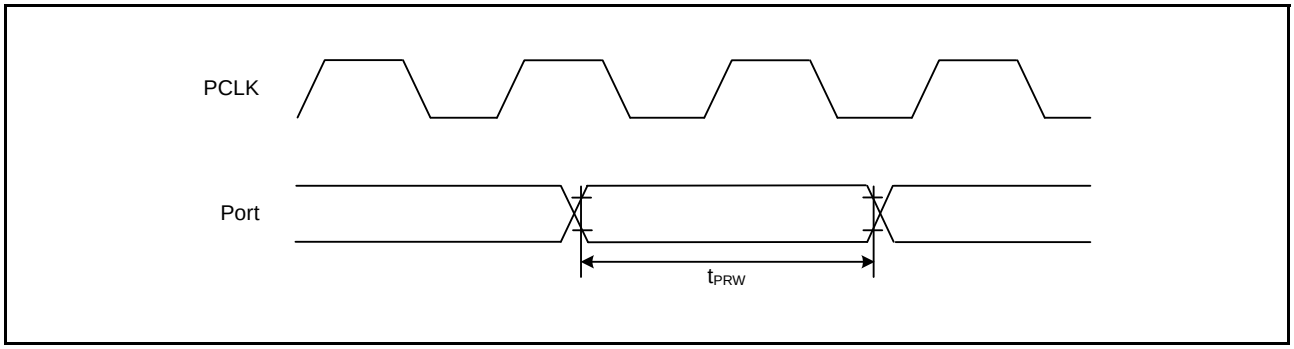



**Figure 5.83 I/O Port Input Timing**

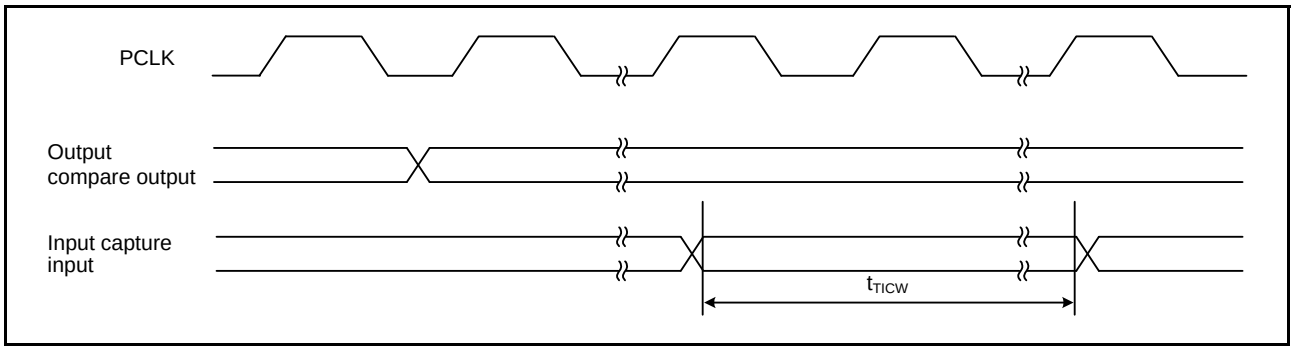



**Figure 5.84 MTU/TPU Input/Output Timing**

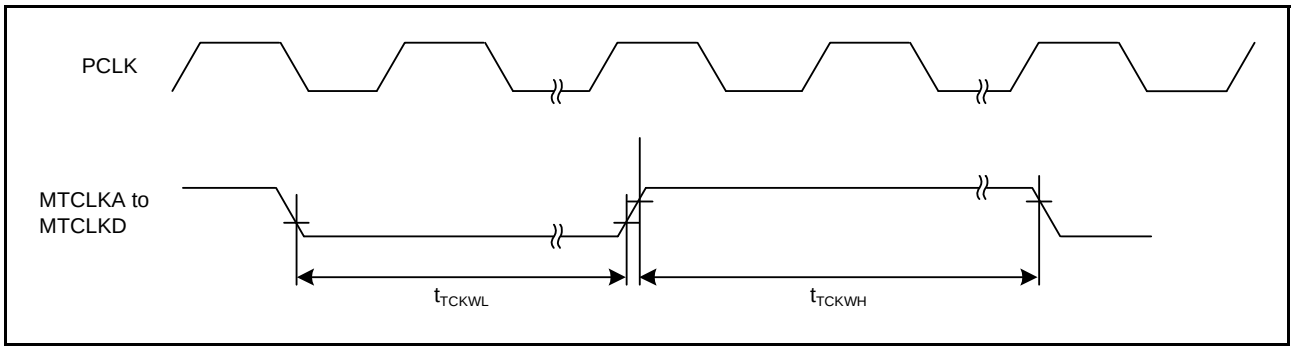



**Figure 5.85 MTU/TPU Clock Input Timing**

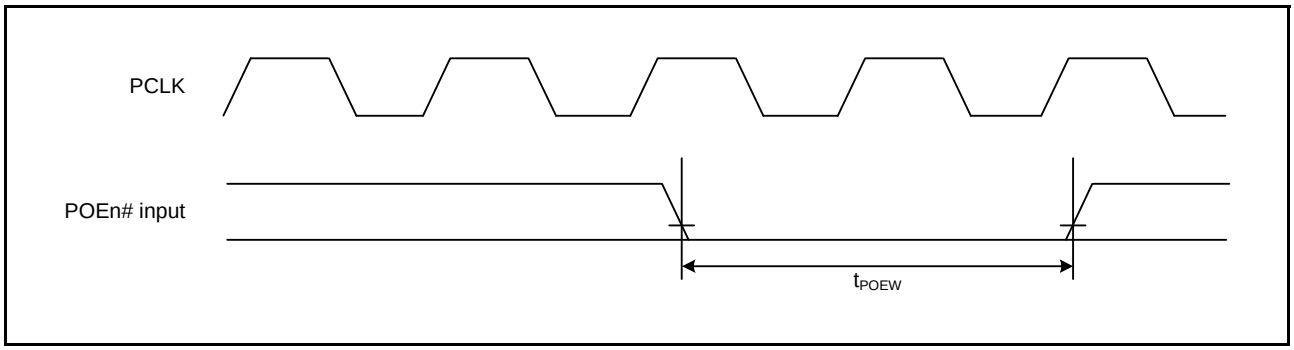



**Figure 5.86 POE# Input Timing**

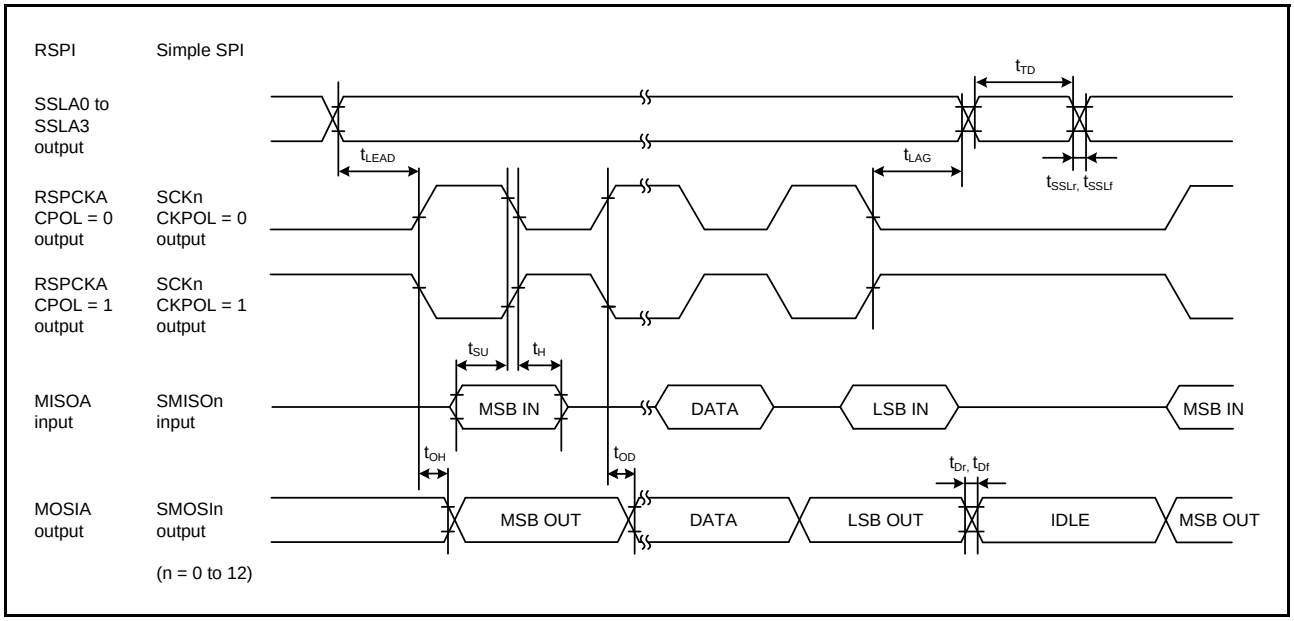



**Figure 5.94 RSPI Timing (Master, CPHA = 1) (Bit Rate: PCLKB Set to Division Ratio Other Than Divided by 2) and Simple SPI Timing (Master, CKPH = 0)**

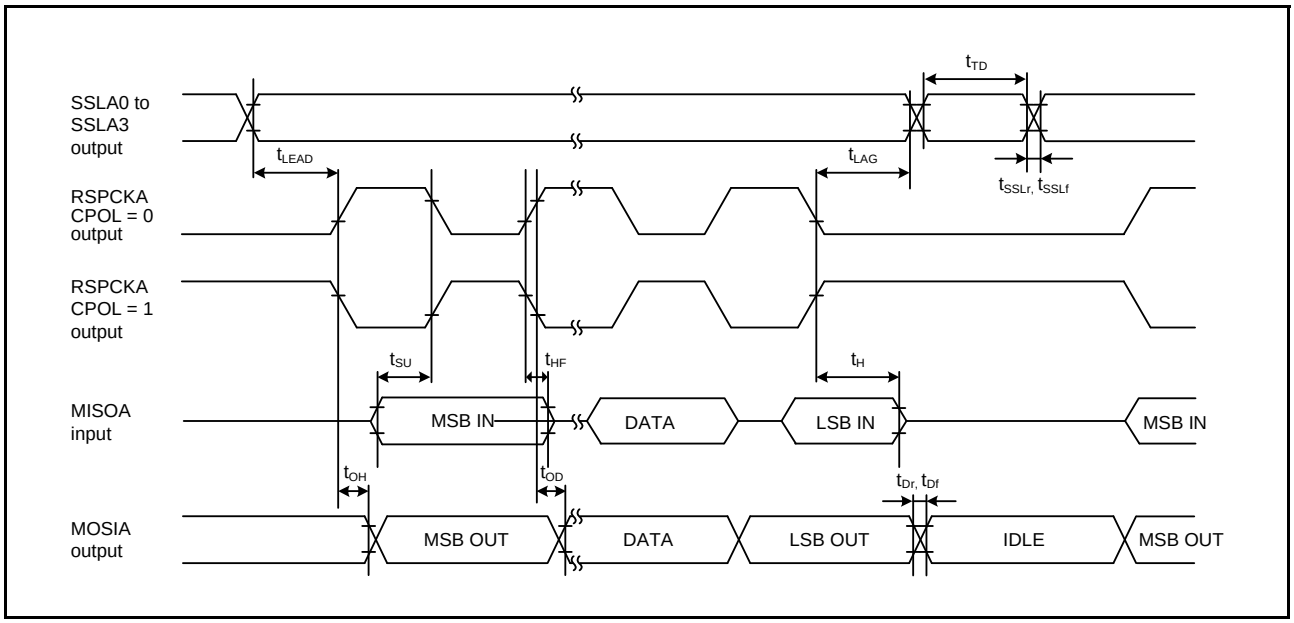



**Figure 5.95 RSPI Timing (Master, CPHA = 1) (Bit Rate: PCLKB Set to Divided by 2)**

**Table 5.66 Sampling Time**

Conditions: VCC = AVCC0 = 1.62 to 5.5 V, VSS = AVSS0 = VREFL = VREFL0 = 0 V, $T_a$ = –40 to +105°C

| Item | | Symbol | Typ. | Unit | Test Conditions |
|---|---|---|---|---|---|
| Sampling time | High-precision channel | Ts | 0.2 + 0.14 × R0 (KΩ) | µs | Figure 5.100 |
| | Normal-precision channel | | 0.35 + 0.14 × R0 (KΩ) | | |

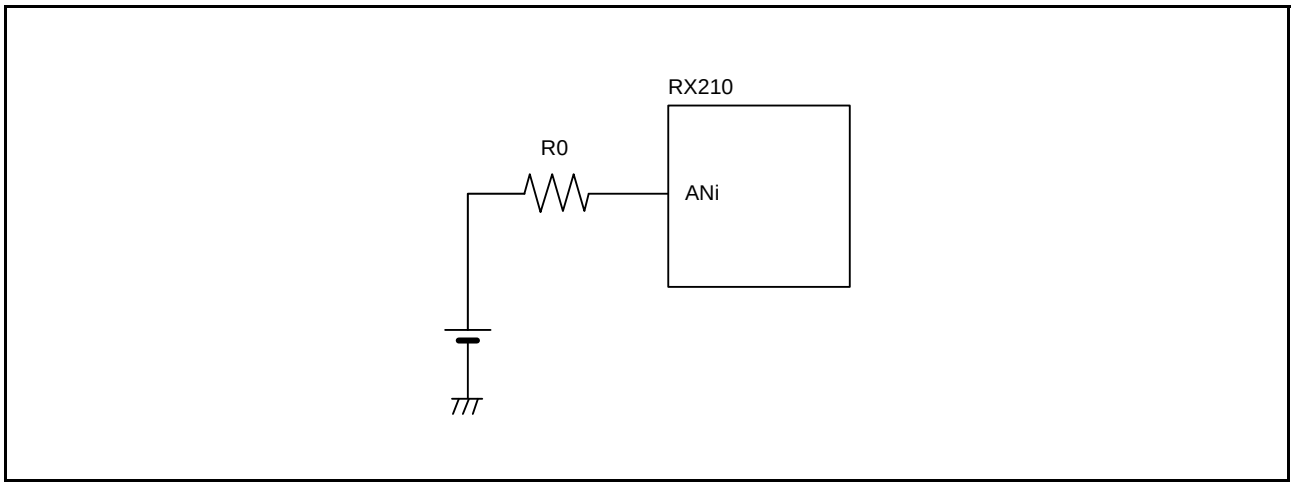



**Figure 5.100 Internal Equivalent Circuit of Analog Input Pin**

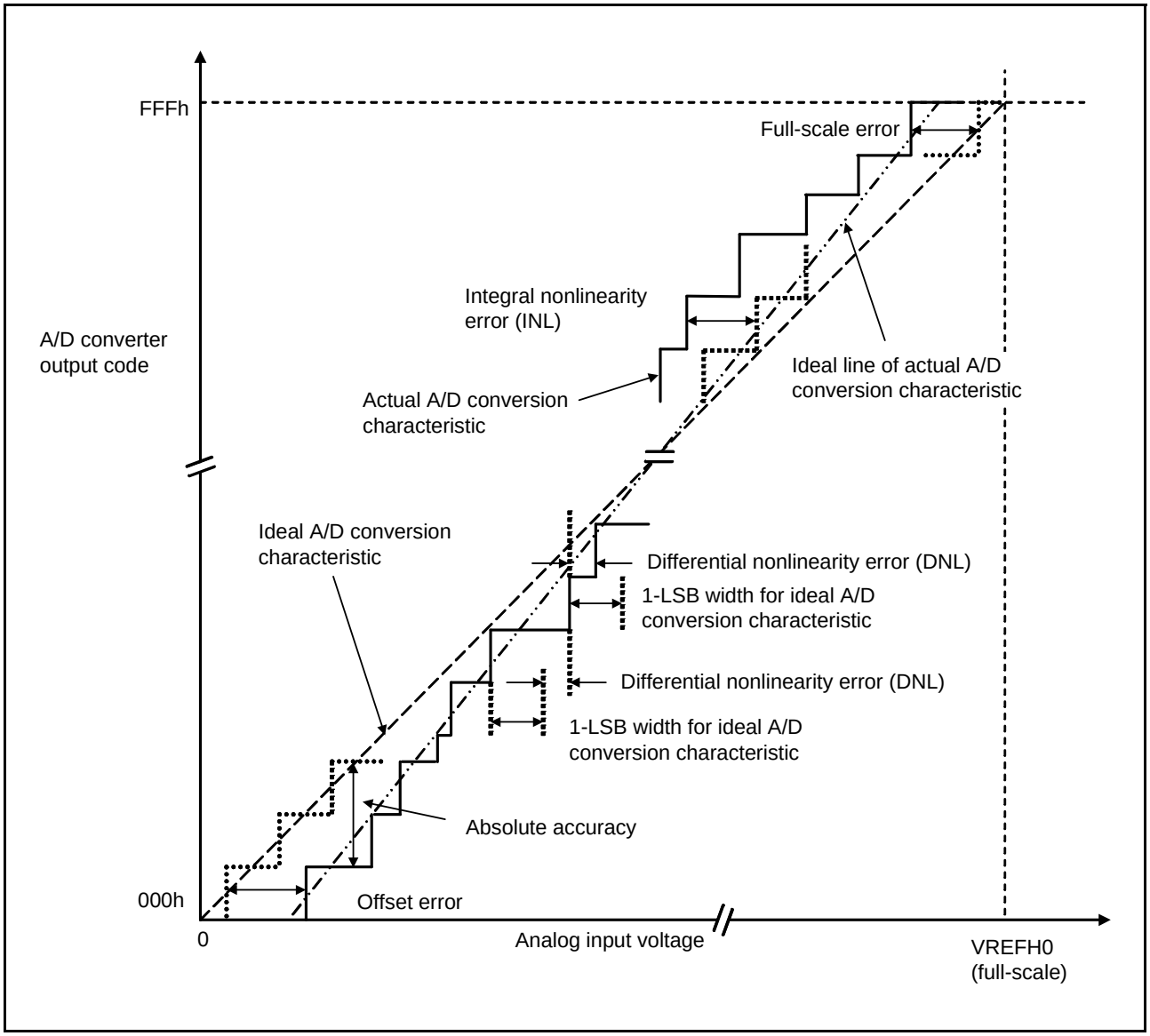



**Figure 5.101 Illustration of A/D Converter Characteristic Terms**

### Absolute accuracy

Absolute accuracy is the difference between output code based on the theoretical A/D conversion characteristics, and the actual A/D conversion result. When measuring absolute accuracy, the voltage at the midpoint of the width of analog input voltage (1-LSB width), that can meet the expectation of outputting an equal code based on the theoretical A/D conversion characteristics, is used as an analog input voltage. For example, if 12-bit resolution is used and if reference voltage (VREFH0 = 5.12 V), then 1-LSB width becomes 1.25 mV, and 0 mV, 1.25 mV, 2.5 mV, ... are used as analog input voltages.

If analog input voltage is 10 mV, absolute accuracy = ±5 LSB means that the actual A/D conversion result is in the range of 003h to 00Dh though an output code, 008h, can be expected from the theoretical A/D conversion characteristics.

### Integral nonlinearity error (INL)

Integral nonlinearity error is the maximum deviation between the ideal line when the measured offset and full-scale errors are zeroed, and the actual output code.

| Rev. | Date | Description | |
|---|---|---|---|
| | | Page | Summary |
| 1.30 | Jan 22, 2013 | 11 | Table 1.6 List of Products Chip Version C: D Version (Ta = -40 to +85°C),<br>Table 1.7 List of Products Chip Version C: G Version (Ta = -40 to +105°C), changed |
| | | 12 | Figure 1.1 How to Read the Product Part No., Memory Capacity, and Package Type, changed |
| | | 13 | Figure 1.2 Block Diagram, changed |
| | | 14 to 17 | Table 1.8 Pin Functions, changed |
| | | 18 | Figure 1.3 Pin Assignments of the 145-Pin TFLGA (Upper Perspective View), added |
| | | 19 | Figure 1.4 Pin Assignments of the 144-Pin LQFP, added |
| | | 25 to 28 | Table 1.9 List of Pins and Pin Functions (145-Pin TFLGA), changed |
| | | 29 to 32 | Table 1.10 List of Pins and Pin Functions (144-Pin LQFP), changed |
| | | 3. Address Space | |
| | | 48 | Figure 3.1 Memory Map in Each Operating Mode, changed |
| | | 4. I/O Registers | |
| | | 52 to 81 | Table 4.1 List of I/O Registers (Address Order, changed |
| | | 5. Electrical Characteristics | |
| | | 83 | Table 5.2 DC Characteristics (1),<br>Table 5.3 DC Characteristics (2), changed |
| | | 84 to 122 | Table 5.6 DC Characteristics (5) to Table 5.20 DC Characteristics (19), changed<br>Figure 5.1 Voltage Dependency in High-Speed .... for Chip Version A to<br>Figure 5.34 Temperature Dependency in .... and 100 to 145 pins, changed |
| | | 158 | Table 5.55 Timing of On-Chip Peripheral Modules (1), changed |
| | | 159 | [512 Kbytes or less of flash memory and 48 to 100 pins]<br>Table 5.56 Timing of On-Chip Peripheral Modules (2), added |
| | | 160, 161 | [768 Kbytes/1 Mbyte of flash memory or 145/145 pins]<br>Table 5.57 Timing of On-Chip Peripheral Modules (3), added |
| | | 162 | Table 5.58 Timing of On-Chip Peripheral Modules (4), changed |
| | | 165 | Figure 5.75 MTU/TPU Input/Output Timing,<br>Figure 5.76 MTU/TPU Clock Input Timing, changed |
| | | 166 | Figure 5.79 SCK Clock Input Timing,<br>Figure 5.80 SCI Input/Output Timing: Clock Synchronous Mode, changed |
| | | 167 | Figure 5.82 RSPI Clock Timing and Simple SPI Clock Timing, changed |
| | | 168 | Figure 5.83 RSPI Timing (Master, CPHA = 0) .... and Simple SPI Timing (Master, CKPH = 1),<br>Figure 5.84 RSPI Timing (Master, CPHA = 0) (Bit Rate: PCLKB Set to Divided by 2), changed |
| | | 169 | Figure 5.85 RSPI Timing (Master, CPHA = 1) .... and Simple SPI Timing (Master, CKPH = 0),<br>Figure 5.86 RSPI Timing (Master, CPHA = 1) (Bit Rate: PCLKB Set to Divided by 2), changed |
| | | 170 | Figure 5.87 RSPI Timing (Slave, CPHA = 0) and Simple SPI Timing (Slave, CKPH = 1),<br>Figure 5.88 RSPI Timing (Slave, CPHA = 1) and Simple SPI Timing (Slave, CKPH = 0), changed |
| | | 173 | Table 5.64 A/D Conversion Characteristics (2), changed |
| | | 175 | Figure 5.91 Illustration of A/D Converter Characteristic Terms,<br>Absolute accuracy, changed |
| | | 184 | Table 5.74 ROM (Flash Memory for Code Storage) Characteristics (1), changed |
| | | 189 | Table 5.80 E2 DataFlash Characteristics (1),<br>Table 5.81 E2 DataFlash Characteristics (2), changed |
| | | Appendix 1. Package Dimensions | |
| | | 195 | Figure A 145-Pin TFLGA (PTLG0145KA-A), added |
| | | 196 | Figure B 144-Pin LQFP (PLQP0144KA-A), added |
| 1.40 | Feb 19, 2013 | 1. Overview | |
| | | 2 to 6 | Table 1.1 Outline of Specifications, changed<br>Note 2, added |
| | | 9 | Table 1.4 List of Products Chip Version B: D Version (Ta = -40 to +85°C), changed |
| | | 10 | Table 1.5 List of Products Chip Version B: G Version (Ta = -40 to +105°C), changed<br>Note, added |
| | | 11 | Table 1.6 List of Products Chip Version C: D Version (Ta = -40 to +85°C): Note 1,<br>Table 1.7 List of Products Chip Version C: G Version (Ta = -40 to +105°C): Note 1 deleted,<br>Note added |
| | | 12 | Figure 1.1 How to Read the Product Part No., Memory Capacity, and Package Type, changed |
| | | 4. I/O Registers | |
| | | 58 | Table 5.1 List of I/O Registers (Address Order), changed |
| | | 5. Electrical Characteristics | |
| | | 83 | Table 5.4 DC Characteristics (3), changed |
| | | 88 | Table 5.8 DC Characteristics (7), changed |

# Notice

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