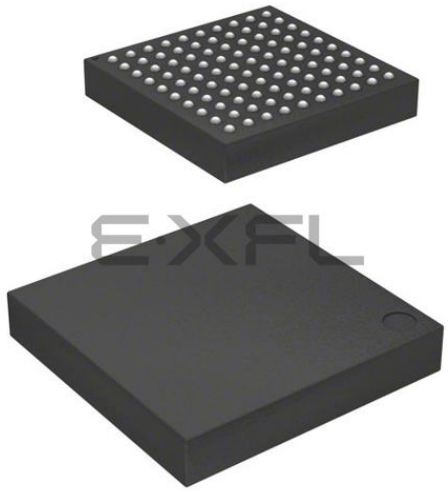
Renesas Electronics America Inc - R5F52105BDLJ#U0 Datasheet



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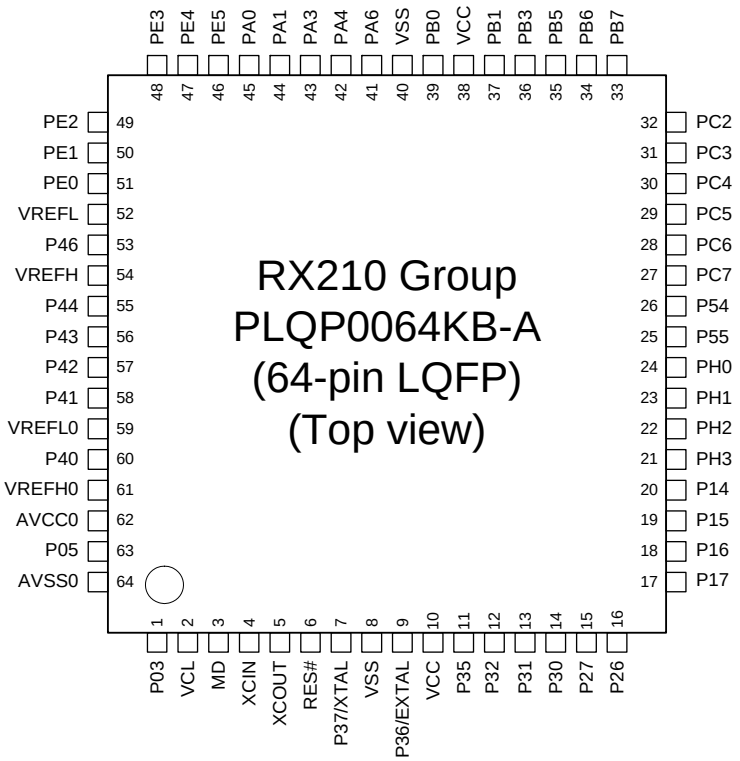
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	EBI/EMI, I²C, SCI, SPI
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	84
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	20K x 8
Voltage - Supply (Vcc/Vdd)	1.62V ~ 5.5V
Data Converters	A/D 16x12b; D/A 2x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TFLGA
Supplier Device Package	100-TFLGA (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f52105bdlj-u0

Table 1.8 Pin Functions (4 / 4)

Classifications	Pin Name	I/O	Description
Analog power supply	AVCC0	Input	Analog voltage supply pin for the 12-bit A/D converter. Connect this pin to VCC if the 12-bit A/D converter is not to be used.
	AVSS0	Input	Analog ground pin for the 12-bit A/D converter. Connect this pin to VSS if the 12-bit A/D converter is not to be used.
	VREFH0	Input	Analog reference voltage supply pin for the 12-bit A/D converter. Connect this pin to VCC if the 12-bit A/D converter is not to be used.
	VREFL0	Input	Analog reference ground pin for the 12-bit A/D converter. Connect this pin to VSS if the 12-bit A/D converter is not to be used.
	VREFH	Input	Analog voltage supply pin for the D/A converter. Connect this pin to VCC if the D/A converter is not to be used.
	VREFL	Input	Analog ground pin for the D/A converter. Connect this pin to VSS if the D/A converter is not to be used.
I/O ports	P00 to P03, P05, P07	I/O	6-bit input/output pins.
	P12 to P17	I/O	6-bit input/output pins.
	P20 to P27	I/O	8-bit input/output pins.
	P30 to P37	I/O	8-bit input/output pins. (P35 input pin)
	P40 to P47	I/O	8-bit input/output pins.
	P50 to P56	I/O	7-bit input/output pins.
	P60 to P67	I/O	8-bit input/output pins.
	P70 to P77	I/O	8-bit input/output pins.
	P80 to P83, P86, P87	I/O	6-bit input/output pins.
	P90 to P93	I/O	4-bit input/output pins.
	PA0 to PA7	I/O	8-bit input/output pins.
	PB0 to PB7	I/O	8-bit input/output pins.
	PC0 to PC7	I/O	8-bit input/output pins.
	PD0 to PD7	I/O	8-bit input/output pins.
	PE0 to PE7	I/O	8-bit input/output pins.
	PF5	I/O	1-bit input/output pin.
	PH0 to PH3	I/O	4-bit input/output pins.
	PJ1, PJ3, PJ5	I/O	3-bit input/output pins.
	PK2 to PK5	I/O	4-bit input/output pins.
	PL0, PL1	I/O	2-bit input/output pins.



Note: • This figure indicates the power supply pins and I/O port pins. For the pin configuration, see the table “List of Pins and Pin Functions (64-Pin LQFP)”.

Figure 1.10 Pin Assignments of the 64-Pin LQFP

Table 1.10 List of Pins and Pin Functions (144-Pin LQFP) (2 / 4)

Pin No.	Power Supply, Clock, System Control	I/O Port	External Bus	Timers (MTU, TMR, POE)	Communications (SCIc, SCId, RSPI, RIIC)	Others
40		P16		MTIOC3C/MTIOC3D/ TMO2/TIOCB1/TCLKC	TXD1/SMOSI1/SSDA1/ MOSIA/SCL-DS/RXD3/ SMISO3/SSCL3	IRQ6/RTCOUT/ ADTRG0#
41		P86		TIOCA0		
42		P15		MTIOC0B/MTCLKB/ TMCI2/TIOCB2/TCLKB	RXD1/SMISO1/SSCL1/ SCK3	IRQ5
43		P14		MTIOC3A/MTCLKA/ TMRI2/TIOCB5/TCLKA	CTS1#/RTS1#/SS1#	IRQ4
44		P13		MTIOC0B/TMO3/ TIOCA5	SDA/TXD2/SMOSI2/ SSDA2	IRQ3
45		P12		TMCI1	SCL/RXD2/SMISO2/ SSCL2	IRQ2
46		PH3		TMCI0		
47		PH2		TMRI0		IRQ1
48		PH1		TMO0		IRQ0
49		PH0				CACREF
50		P56		MTIOC3C/TIOCA1		
51		P55	WAIT#	MTIOC4D/TMO3		
52		P54	ALE	MTIOC4B/TMCI1	CTS2#/RTS2#/SS2#	
53	BCLK	P53				
54		P52	RD#		RXD2/SMISO2/SSCL2	
55		P51	WR1#/BC1#/WAIT#		SCK2	
56		P50	WR0#/WR#		TXD2/SMOSI2/SSDA2	
57	VSS					
58		P83		MTIOC4C	CTS10#/RTS10#	
59	VCC					
60		PC7	A23/CS0#	MTIOC3A/TMO2/ MTCLKB	TXD8/SMOSI8/SSDA8/ MISOA	CACREF
61		PC6	A22/CS1#	MTIOC3C/MTCLKA/ TMCI2	RXD8/SMISO8/SSCL8/ MOSIA	
62		PC5	A21/CS2#/WAIT#	MTIOC3B/MTCLKD/ TMRI2	SCK8/RSPCKA	
63		P82		MTIOC4A	TXD10/SMOSI10/SSDA10	
64		P81		MTIOC3D	RXD10/SMISO10/SSCL10	
65		P80		MTIOC3B	SCK10	
66		PC4	A20/CS3#	MTIOC3D/MTCLKC/ TMCI1/POE0#	SCK5/CTS8#/RTS8#/ SS8#/SSLA0	
67		PC3	A19	MTIOC4D/TCLKB	TXD5/SMOSI5/SSDA5	
68		P77			TXD11/SMOSI11/SSDA11	
69		P76			RXD11/SMISO11/SSCL11	
70		PC2	A18	MTIOC4B/TCLKA	RXD5/SMISO5/SSCL5/ ISSLA3	
71		P75			SCK11	
72		P74			CTS11#/RTS11#/SS11#	
73		PC1	A17	MTIOC3A/TCLKD	SCK5/SSLA2	
74		PL1				
75		PC0	A16	MTIOC3C/TCLKC	CTS5#/RTS5#/SS5#/ SSLA1	
76		PL0				
77		P73				
78		PB7	A15	MTIOC3B/TIOCB5	TXD9/SMOSI9/SSDA9	
79		PB6	A14	MTIOC3D/TIOCA5	RXD9/SMISO9/SSCL9	
80		PB5	A13	MTIOC2A/MTIOC1B/ TMRI1/POE1#/TIOCB4	SCK9	

Table 1.16 List of Pins and Pin Functions (64-Pin LQFP) (1 / 2)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (MTU, TMR, POE)	Communication (SCIc, SCId, RSPI, RIIC)	Others
1		P03			DA0
2	VCL				
3	MD				FINED
4	XCIN				
5	XCOUT				
6	RES#				
7	XTAL	P37			
8	VSS				
9	EXTAL	P36			
10	VCC				
11		P35			NMI
12		P32	MTIOC0C/TMO3	TXD6/SMOSI6/SSDA6	IRQ2-DS/RTCOUT/ RTCIC2
13		P31	MTIOC4D/TMCI2	CTS1#/RTS1#/SS1#	IRQ1-DS/RTCIC1
14		P30	MTIOC4B/TMRI3/POE8#	RXD1/SMISO1/SSCL1	IRQ0-DS/RTCIC0
15		P27	MTIOC2B/TMCI3	SCK1	
16		P26	MTIOC2A/TMO1	TXD1/SMOSI1/SSDA1	
17		P17	MTIOC3A/MTIOC3B/TMO1/ POE8#	SCK1/MISOA/SDA-DS	IRQ7
18		P16	MTIOC3C/MTIOC3D/TMO2	TXD1/SMOSI1/SSDA1/MOSIA/ SCL-DS	IRQ6/RTCOUT/ ADTRG0#
19		P15	MTIOC0B/MTCLKB/TMCI2	RXD1/SMISO1/SSCL1	IRQ5
20		P14	MTIOC3A/MTCLKA/TMRI2	CTS1#/RTS1#/SS1#	IRQ4
21		PH3	TMCI0		
22		PH2	TMRI0		IRQ1
23		PH1	TMO0		IRQ0
24		PH0			CACREF
25		P55	MTIOC4D/TMO3		
26		P54	MTIOC4B/TMCI1		
27		PC7	MTIOC3A/TMO2/MTCLKB	TXD8/SMOSI8/SSDA8/MISOA	CACREF
28		PC6	MTIOC3C/MTCLKA/TMCI2	RXD8/SMISO8/SSCL8/MOSIA	
29		PC5	MTIOC3B/MTCLKD/TMRI2	SCK8/RSPCKA	
30		PC4	MTIOC3D/MTCLKC/TMCI1/ POE0#	SCK5/CTS8#/RTS8#/SS8#/ SSLA0	
31		PC3	MTIOC4D	TXD5/SMOSI5/SSDA5	
32		PC2	MTIOC4B	RXD5/SMISO5/SSCL5/SSLA3	
33		PB7	MTIOC3B	TXD9/SMOSI9/SSDA9	
34		PB6	MTIOC3D	RXD9/SMISO9/SSCL9	
35		PB5	MTIOC2A/MTIOC1B/TMRI1/ POE1#	SCK9	
36		PB3	MTIOC0A/MTIOC4A/TMO0/ POE3#	SCK6	
37		PB1	MTIOC0C/MTIOC4C/TMCI0	TXD6/SMOSI6/SSDA6	IRQ4-DS
38	VCC				
39		PB0	MTIC5W	RXD6/SMISO6/SSCL6/RSPCKA	
40	VSS				
41		PA6	MTIC5V/MTCLKB/TMCI3/ POE2#	CTS5#/RTS5#/SS5#/MOSIA	
42		PA4	MTIC5U/MTCLKA/TMRI0	TXD5/SMOSI5/SSDA5/SSLA0	IRQ5-DS/CVREFB1
43		PA3	MTIOC0D/MTCLKD	RXD5/SMISO5/SSCL5	IRQ6-DS/CMPB1

Table 4.1 List of I/O Registers (Address Order) (2 / 29)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles ICLK ≥ PCLK	Number of Access Cycles ICLK < PCLK
0008 201Dh	DMAC0	DMA software start register	DMREQ	8	8	2 ICLK	
0008 201Eh	DMAC0	DMA status register	DMSTS	8	8	2 ICLK	
0008 201Fh	DMAC0	DMA activation source flag control register	DMCSL	8	8	2 ICLK	
0008 2040h	DMAC1	DMA source address register	DMSAR	32	32	2 ICLK	
0008 2044h	DMAC1	DMA destination address register	DMDAR	32	32	2 ICLK	
0008 2048h	DMAC1	DMA transfer count register	DMCRA	32	32	2 ICLK	
0008 204Ch	DMAC1	DMA block transfer count register	DMCRB	16	16	2 ICLK	
0008 2050h	DMAC1	DMA transfer mode register	DMTMD	16	16	2 ICLK	
0008 2053h	DMAC1	DMA interrupt setting register	DMINT	8	8	2 ICLK	
0008 2054h	DMAC1	DMA address mode register	DMAMD	16	16	2 ICLK	
0008 205Ch	DMAC1	DMA transfer enable register	DMCNT	8	8	2 ICLK	
0008 205Dh	DMAC1	DMA software start register	DMREQ	8	8	2 ICLK	
0008 205Eh	DMAC1	DMA status register	DMSTS	8	8	2 ICLK	
0008 205Fh	DMAC1	DMA activation source flag control register	DMCSL	8	8	2 ICLK	
0008 2080h	DMAC2	DMA source address register	DMSAR	32	32	2 ICLK	
0008 2084h	DMAC2	DMA destination address register	DMDAR	32	32	2 ICLK	
0008 2088h	DMAC2	DMA transfer count register	DMCRA	32	32	2 ICLK	
0008 208Ch	DMAC2	DMA block transfer count register	DMCRB	16	16	2 ICLK	
0008 2090h	DMAC2	DMA transfer mode register	DMTMD	16	16	2 ICLK	
0008 2093h	DMAC2	DMA interrupt setting register	DMINT	8	8	2 ICLK	
0008 2094h	DMAC2	DMA address mode register	DMAMD	16	16	2 ICLK	
0008 209Ch	DMAC2	DMA transfer enable register	DMCNT	8	8	2 ICLK	
0008 209Dh	DMAC2	DMA software start register	DMREQ	8	8	2 ICLK	
0008 209Eh	DMAC2	DMA status register	DMSTS	8	8	2 ICLK	
0008 209Fh	DMAC2	DMA activation source flag control register	DMCSL	8	8	2 ICLK	
0008 20C0h	DMAC3	DMA source address register	DMSAR	32	32	2 ICLK	
0008 20C4h	DMAC3	DMA destination address register	DMDAR	32	32	2 ICLK	
0008 20C8h	DMAC3	DMA transfer count register	DMCRA	32	32	2 ICLK	
0008 20CCh	DMAC3	DMA block transfer count register	DMCRB	16	16	2 ICLK	
0008 20D0h	DMAC3	DMA transfer mode register	DMTMD	16	16	2 ICLK	
0008 20D3h	DMAC3	DMA interrupt setting register	DMINT	8	8	2 ICLK	
0008 20D4h	DMAC3	DMA address mode register	DMAMD	16	16	2 ICLK	
0008 20DCh	DMAC3	DMA transfer enable register	DMCNT	8	8	2 ICLK	
0008 20DDh	DMAC3	DMA software start register	DMREQ	8	8	2 ICLK	
0008 20DEh	DMAC3	DMA status register	DMSTS	8	8	2 ICLK	
0008 20DFh	DMAC3	DMA activation source flag control register	DMCSL	8	8	2 ICLK	
0008 2200h	DMAC	DMA module activation register	DMAST	8	8	2 ICLK	
0008 2400h	DTC	DTC control register	DTCCR	8	8	2 ICLK	
0008 2404h	DTC	DTC vector base register	DTCVBR	32	32	2 ICLK	
0008 2408h	DTC	DTC address mode register	DTCADMOD	8	8	2 ICLK	
0008 240Ch	DTC	DTC module start register	DTCST	8	8	2 ICLK	
0008 240Eh	DTC	DTC status register	DTCSTS	16	16	2 ICLK	
0008 3002h	BSC	CS0 mode register	CS0MOD	16	16	1, 2 BCLK	
0008 3004h	BSC	CS0 wait control register 1	CS0WCR1	32	32	1, 2 BCLK	
0008 3008h	BSC	CS0 wait control register 2	CS0WCR2	32	32	1, 2 BCLK	
0008 3012h	BSC	CS1 mode register	CS1MOD	16	16	1, 2 BCLK	
0008 3014h	BSC	CS1 wait control register 1	CS1WCR1	32	32	1, 2 BCLK	
0008 3018h	BSC	CS1 wait control register 2	CS1WCR2	32	32	1, 2 BCLK	
0008 3022h	BSC	CS2 mode register	CS2MOD	16	16	1, 2 BCLK	
0008 3024h	BSC	CS2 wait control register 1	CS2WCR1	32	32	1, 2 BCLK	
0008 3028h	BSC	CS2 wait control register 2	CS2WCR2	32	32	1, 2 BCLK	

Table 4.1 List of I/O Registers (Address Order) (9 / 29)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles ICLK ≥ PCLK	Number of Access Cycles ICLK < PCLK
0008 7301h	ICU	Interrupt source priority register 001	IPR001	8	8	2 ICLK	
0008 7302h	ICU	Interrupt source priority register 002	IPR002	8	8	2 ICLK	
0008 7303h	ICU	Interrupt source priority register 003	IPR003	8	8	2 ICLK	
0008 7304h	ICU	Interrupt source priority register 004	IPR004	8	8	2 ICLK	
0008 7305h	ICU	Interrupt source priority register 005	IPR005	8	8	2 ICLK	
0008 7306h	ICU	Interrupt source priority register 006	IPR006	8	8	2 ICLK	
0008 7307h	ICU	Interrupt source priority register 007	IPR007	8	8	2 ICLK	
0008 7320h	ICU	Interrupt source priority register 032	IPR032	8	8	2 ICLK	
0008 7321h	ICU	Interrupt source priority register 033	IPR033	8	8	2 ICLK	
0008 7322h	ICU	Interrupt source priority register 034	IPR034	8	8	2 ICLK	
0008 732Ch	ICU	Interrupt source priority register 044	IPR044	8	8	2 ICLK	
0008 7339h	ICU	Interrupt source priority register 057	IPR057	8	8	2 ICLK	
0008 733Ah	ICU	Interrupt source priority register 058	IPR058	8	8	2 ICLK	
0008 733Bh	ICU	Interrupt source priority register 059	IPR059	8	8	2 ICLK	
0008 733Fh	ICU	Interrupt source priority register 063	IPR063	8	8	2 ICLK	
0008 7340h	ICU	Interrupt source priority register 064	IPR064	8	8	2 ICLK	
0008 7341h	ICU	Interrupt source priority register 065	IPR065	8	8	2 ICLK	
0008 7342h	ICU	Interrupt source priority register 066	IPR066	8	8	2 ICLK	
0008 7343h	ICU	Interrupt source priority register 067	IPR067	8	8	2 ICLK	
0008 7344h	ICU	Interrupt source priority register 068	IPR068	8	8	2 ICLK	
0008 7345h	ICU	Interrupt source priority register 069	IPR069	8	8	2 ICLK	
0008 7346h	ICU	Interrupt source priority register 070	IPR070	8	8	2 ICLK	
0008 7347h	ICU	Interrupt source priority register 071	IPR071	8	8	2 ICLK	
0008 7358h	ICU	Interrupt source priority register 088	IPR088	8	8	2 ICLK	
0008 7359h	ICU	Interrupt source priority register 089	IPR089	8	8	2 ICLK	
0008 735Ch	ICU	Interrupt source priority register 092	IPR092	8	8	2 ICLK	
0008 735Dh	ICU	Interrupt source priority register 093	IPR093	8	8	2 ICLK	
0008 7366h	ICU	Interrupt source priority register 102	IPR102	8	8	2 ICLK	
0008 7367h	ICU	Interrupt source priority register 103	IPR103	8	8	2 ICLK	
0008 736Ah	ICU	Interrupt source priority register 106	IPR106	8	8	2 ICLK	
0008 736Bh	ICU	Interrupt source priority register 107	IPR107	8	8	2 ICLK	
0008 7372h	ICU	Interrupt source priority register 114	IPR114	8	8	2 ICLK	
0008 7376h	ICU	Interrupt source priority register 118	IPR118	8	8	2 ICLK	
0008 7379h	ICU	Interrupt source priority register 121	IPR121	8	8	2 ICLK	
0008 737Bh	ICU	Interrupt source priority register 123	IPR123	8	8	2 ICLK	
0008 737Dh	ICU	Interrupt source priority register 125	IPR125	8	8	2 ICLK	
0008 737Fh	ICU	Interrupt source priority register 127	IPR127	8	8	2 ICLK	
0008 7381h	ICU	Interrupt source priority register 129	IPR129	8	8	2 ICLK	
0008 7385h	ICU	Interrupt source priority register 133	IPR133	8	8	2 ICLK	
0008 7386h	ICU	Interrupt source priority register 134	IPR134	8	8	2 ICLK	
0008 738Ah	ICU	Interrupt source priority register 138	IPR138	8	8	2 ICLK	
0008 738Bh	ICU	Interrupt source priority register 139	IPR139	8	8	2 ICLK	
0008 738Eh	ICU	Interrupt source priority register 142	IPR142	8	8	2 ICLK	
0008 7392h	ICU	Interrupt source priority register 146	IPR146	8	8	2 ICLK	
0008 7393h	ICU	Interrupt source priority register 147	IPR147	8	8	2 ICLK	
0008 7395h	ICU	Interrupt source priority register 149	IPR149	8	8	2 ICLK	
0008 7397h	ICU	Interrupt source priority register 151	IPR151	8	8	2 ICLK	
0008 7399h	ICU	Interrupt source priority register 153	IPR153	8	8	2 ICLK	
0008 739Bh	ICU	Interrupt source priority register 155	IPR155	8	8	2 ICLK	
0008 739Fh	ICU	Interrupt source priority register 159	IPR159	8	8	2 ICLK	
0008 73A0h	ICU	Interrupt source priority register 160	IPR160	8	8	2 ICLK	

Table 4.1 List of I/O Registers (Address Order) (17 / 29)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles: ICLK ≥ PCLK	Number of Access Cycles: ICLK < PCLK
0008 9076h	S12AD	A/D sampling state register 4	ADSSTR4	8	8	2, 3 PCLKB	2 ICLK
0008 9077h	S12AD	A/D sampling state register 5	ADSSTR5	8	8	2, 3 PCLKB	2 ICLK
0008 9078h	S12AD	A/D sampling state register 6	ADSSTR6	8	8	2, 3 PCLKB	2 ICLK
0008 9079h	S12AD	A/D sampling state register 7	ADSSTR7	8	8	2, 3 PCLKB	2 ICLK
0008 907Ah	S12AD	A/D disconnecting detection control register	ADDISCR	8	8	2, 3 PCLKB	2 ICLK
0008 A000h	SCI0	Serial mode register	SMR	8	8	2, 3 PCLKB	2 ICLK
0008 A001h	SCI0	Bit rate register	BRR	8	8	2, 3 PCLKB	2 ICLK
0008 A002h	SCI0	Serial control register	SCR	8	8	2, 3 PCLKB	2 ICLK
0008 A003h	SCI0	Transmit data register	TDR	8	8	2, 3 PCLKB	2 ICLK
0008 A004h	SCI0	Serial status register	SSR	8	8	2, 3 PCLKB	2 ICLK
0008 A005h	SCI0	Receive data register	RDR	8	8	2, 3 PCLKB	2 ICLK
0008 A006h	SCI0	Smart card mode register	SCMR	8	8	2, 3 PCLKB	2 ICLK
0008 A007h	SCI0	Serial extended mode register	SEMR	8	8	2, 3 PCLKB	2 ICLK
0008 A008h	SCI0	Noise filter setting register	SNFR	8	8	2, 3 PCLKB	2 ICLK
0008 A009h	SCI0	I^2C mode register 1	SIMR1	8	8	2, 3 PCLKB	2 ICLK
0008 A00Ah	SCI0	I^2C mode register 2	SIMR2	8	8	2, 3 PCLKB	2 ICLK
0008 A00Bh	SCI0	I^2C mode register 3	SIMR3	8	8	2, 3 PCLKB	2 ICLK
0008 A00Ch	SCI0	I^2C status register	SISR	8	8	2, 3 PCLKB	2 ICLK
0008 A00Dh	SCI0	SPI mode register	SPMR	8	8	2, 3 PCLKB	2 ICLK
0008 A020h	SCI1	Serial mode register	SMR	8	8	2, 3 PCLKB	2 ICLK
0008 A021h	SCI1	Bit rate register	BRR	8	8	2, 3 PCLKB	2 ICLK
0008 A022h	SCI1	Serial control register	SCR	8	8	2, 3 PCLKB	2 ICLK
0008 A023h	SCI1	Transmit data register	TDR	8	8	2, 3 PCLKB	2 ICLK
0008 A024h	SCI1	Serial status register	SSR	8	8	2, 3 PCLKB	2 ICLK
0008 A025h	SCI1	Receive data register	RDR	8	8	2, 3 PCLKB	2 ICLK
0008 A026h	SCI1	Smart card mode register	SCMR	8	8	2, 3 PCLKB	2 ICLK
0008 A027h	SCI1	Serial extended mode register	SEMR	8	8	2, 3 PCLKB	2 ICLK
0008 A028h	SCI1	Noise filter setting register	SNFR	8	8	2, 3 PCLKB	2 ICLK
0008 A029h	SCI1	I^2C mode register 1	SIMR1	8	8	2, 3 PCLKB	2 ICLK
0008 A02Ah	SCI1	I^2C mode register 2	SIMR2	8	8	2, 3 PCLKB	2 ICLK
0008 A02Bh	SCI1	I^2C mode register 3	SIMR3	8	8	2, 3 PCLKB	2 ICLK
0008 A02Ch	SCI1	I^2C status register	SISR	8	8	2, 3 PCLKB	2 ICLK
0008 A02Dh	SCI1	SPI mode register	SPMR	8	8	2, 3 PCLKB	2 ICLK
0008 A040h	SCI2	Serial mode register	SMR	8	8	2, 3 PCLKB	2 ICLK
0008 A041h	SCI2	Bit rate register	BRR	8	8	2, 3 PCLKB	2 ICLK
0008 A042h	SCI2	Serial control register	SCR	8	8	2, 3 PCLKB	2 ICLK
0008 A043h	SCI2	Transmit data register	TDR	8	8	2, 3 PCLKB	2 ICLK
0008 A044h	SCI2	Serial status register	SSR	8	8	2, 3 PCLKB	2 ICLK
0008 A045h	SCI2	Receive data register	RDR	8	8	2, 3 PCLKB	2 ICLK
0008 A046h	SCI2	Smart card mode register	SCMR	8	8	2, 3 PCLKB	2 ICLK
0008 A047h	SCI2	Serial extended mode register	SEMR	8	8	2, 3 PCLKB	2 ICLK
0008 A048h	SCI2	Noise filter setting register	SNFR	8	8	2, 3 PCLKB	2 ICLK
0008 A049h	SCI2	I^2C mode register 1	SIMR1	8	8	2, 3 PCLKB	2 ICLK
0008 A04Ah	SCI2	I^2C mode register 2	SIMR2	8	8	2, 3 PCLKB	2 ICLK
0008 A04Bh	SCI2	I^2C mode register 3	SIMR3	8	8	2, 3 PCLKB	2 ICLK
0008 A04Ch	SCI2	I^2C status register	SISR	8	8	2, 3 PCLKB	2 ICLK
0008 A04Dh	SCI2	SPI mode register	SPMR	8	8	2, 3 PCLKB	2 ICLK
0008 A060h	SCI3	Serial mode register	SMR	8	8	2, 3 PCLKB	2 ICLK
0008 A061h	SCI3	Bit rate register	BRR	8	8	2, 3 PCLKB	2 ICLK
0008 A062h	SCI3	Serial control register	SCR	8	8	2, 3 PCLKB	2 ICLK
0008 A063h	SCI3	Transmit data register	TDR	8	8	2, 3 PCLKB	2 ICLK

[Chip version C]

Table 5.10 DC Characteristics (9)

Conditions: VCC = AVCC0 = 1.62 to 5.5 V, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +105°C

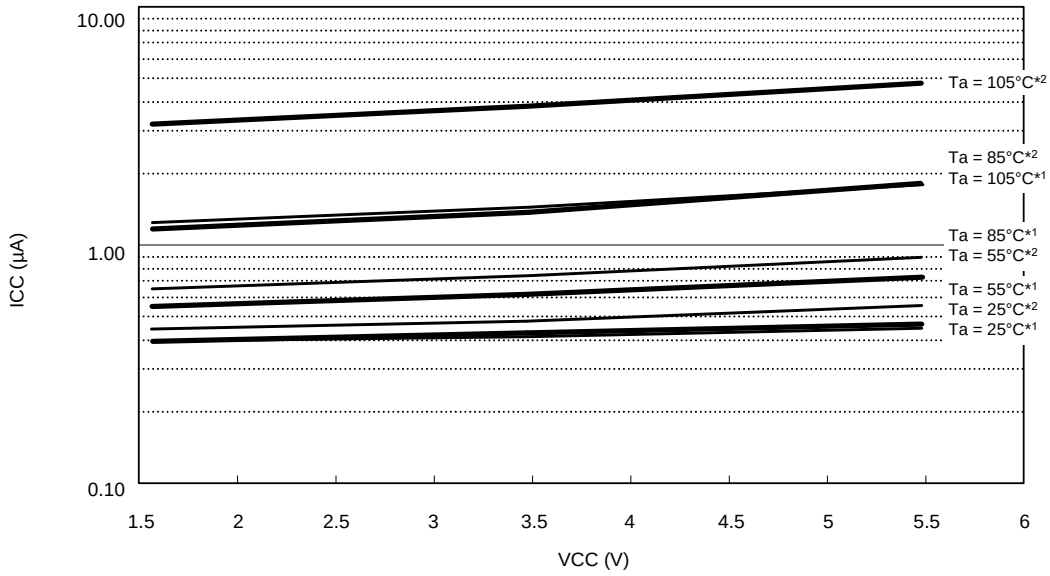
Item					Symbol	Typ.	Max.	Unit	Test Conditions
Supply current*1	Middle-speed operating modes 1A and 1B	Normal operating mode	No peripheral operation	ICLK = 32 MHz*2	I_{CC}	7.0	—	mA	
				ICLK = 20 MHz*3		6.0	—		
			All peripheral operation: Normal	ICLK = 32 MHz*4		26	—		
				ICLK = 20 MHz*5		18.5	—		
			All peripheral operation: Max.	ICLK = 32 MHz*4		—	40		
				ICLK = 20 MHz*5		—	30		
		Sleep mode	No peripheral operation	ICLK = 32 MHz		5.0	—		
				ICLK = 20 MHz		4.6	—		
			All peripheral operation: Normal	ICLK = 32 MHz		15.5	—		
				ICLK = 20 MHz		12	—		
		All-module clock stop mode		ICLK = 32 MHz		4.5	—		
				ICLK = 20 MHz		4.5	—		
		Increase during BGO operation*6	Middle-speed operating mode 1A			25	—		
			Middle-speed operating mode 1B			20	—		
	Low-speed operating mode 1	Normal operating mode	No peripheral operation*7	ICLK = 1 MHz		0.68	—		
			All peripheral operation: Normal*8	ICLK = 1 MHz		2.4	—		
			All peripheral operation: Max. *8	ICLK = 1 MHz		—	7		
		Sleep mode	No peripheral operation	ICLK = 1 MHz		0.6	—		
			All peripheral operation: Normal	ICLK = 1 MHz		2	—		
		All-module clock stop mode				0.58	—		
	Low-speed operating mode 2	Normal operating mode	No peripheral operation*9	ICLK = 32 kHz		0.024	—		
			All peripheral operation: Normal*10	ICLK = 32 kHz		0.05	—		
			All peripheral operation: Max. *10	ICLK = 32 kHz		—	3*11		
		Sleep mode	No peripheral operation	ICLK = 32 kHz		0.02	—		
			All peripheral operation: Normal	ICLK = 32 kHz		0.04	—		
		All-module clock stop mode				0.018	—		

Note 1. Supply current values do not include output charge/discharge current from all pins. The values apply when internal pull-up MOSs are in the off state.

Note 2. Clock supply to the peripheral functions is stopped. This does not include BGO operation. The clock source is PLL and the VCO oscillation frequency is 64 MHz. BCLK, FCLK, and PCLK are set to divided by 64.

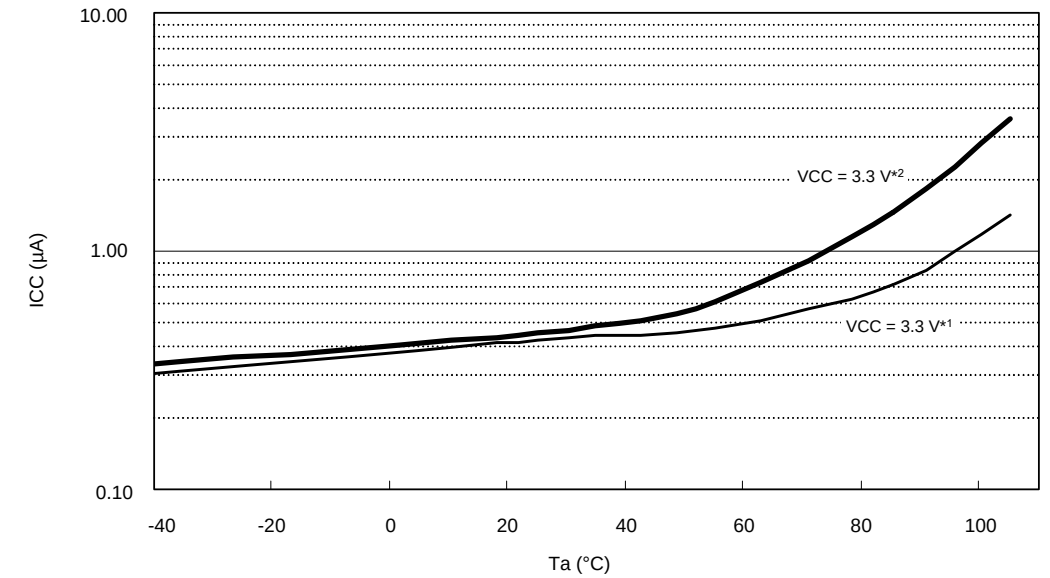
Note 3. Clock supply to the peripheral functions is stopped. This does not include BGO operation. The clock source is HOCO and the oscillation frequency is 40 MHz. BCLK, FCLK, and PCLK are set to divided by 64.

Note 4. Clocks are supplied to the peripheral functions. This does not include BGO operation. The clock source is PLL and the VCO oscillation frequency is 64 MHz. BCLK, FCLK, and PCLK are ICLK divided by 1.



Note 1. Average value of the tested middle samples during product evaluation.
Note 2. Average value of the tested upper-limit samples during product evaluation.

Figure 5.24 Voltage Dependency in Deep Software Standby Mode (DEEPCUT1 Bit = 1) (Reference Data) for Chip Version B with 256 Kbytes or Less of Flash Memory and 48 to 100 Pins

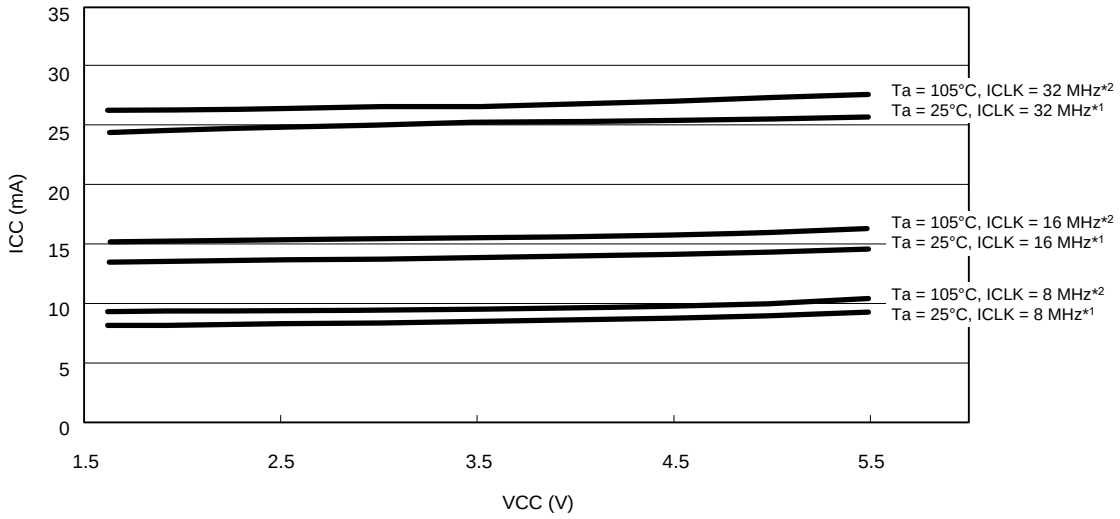


Note 1. Average value of the tested middle samples during product evaluation.
Note 2. Average value of the tested upper-limit samples during product evaluation.

Figure 5.25 Temperature Dependency in Deep Software Standby Mode (DEEPCUT1 Bit = 1) (Reference Data) for Chip Version B with 256 Kbytes or Less of Flash Memory and 48 to 100 Pins

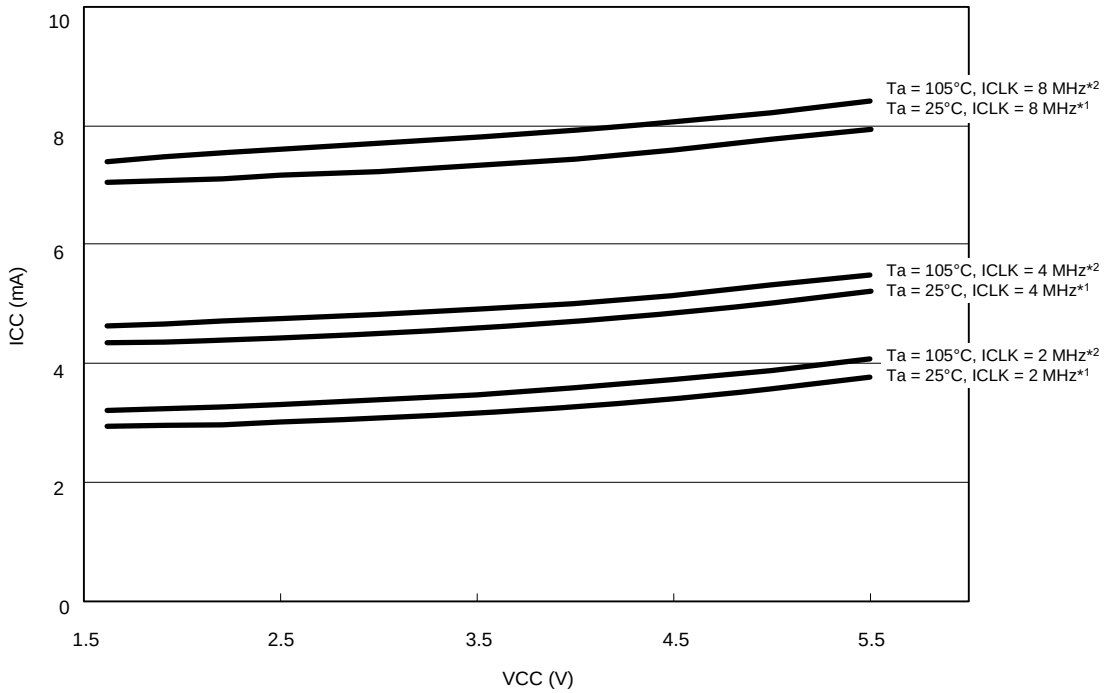
Item					Symbol	Typ.	Max.	Unit	Test Conditions
Supply current*1	Low-speed operating mode 1	Normal operating mode	No peripheral operation*7	ICLK = 8 MHz	I_{CC}	2.1	—	mA	
				ICLK = 4 MHz		1.7	—		
				ICLK = 2 MHz		1.5	—		
			All peripheral operation: Normal*8	ICLK = 8 MHz		7.3	—		
				ICLK = 4 MHz		4.5	—		
				ICLK = 2 MHz		3.1	—		
			All peripheral operation: Max.*7	ICLK = 8 MHz		—	12		
				ICLK = 4 MHz		—	—		
				ICLK = 2 MHz		—	—		
		Sleep mode	No peripheral operation	ICLK = 8 MHz		1.5	—		
				ICLK = 4 MHz		1.4	—		
				ICLK = 2 MHz		1.3	—		
			All peripheral operation: Normal	ICLK = 8 MHz		4.1	—		
				ICLK = 4 MHz		3.0	—		
				ICLK = 2 MHz		2.3	—		
		All-module clock stop mode		ICLK = 8 MHz		1.4	—		
				ICLK = 4 MHz		1.3	—		
				ICLK = 2 MHz		1.2	—		
	Low-speed operating mode 2	Normal operating mode	No peripheral operation*9	ICLK = 32 kHz		0.022	—		
			All peripheral operation: Normal*10	ICLK = 32 kHz		0.06	—		
			All peripheral operation: Max.*10	ICLK = 32 kHz		—	3*11		
		Sleep mode	No peripheral operation	ICLK = 32 kHz		0.017	—		
			All peripheral operation: Normal	ICLK = 32 kHz		0.036	—		
		All-module clock stop mode				0.017	—		

Note 1. Supply current values do not include output charge/discharge current from all pins. The values apply when internal pull-up MOSs are in the off state.
Note 2. Clock supply to the peripheral functions is stopped. This does not include BGO operation. The clock source is PLL and the VCO oscillation frequency is 64 MHz. BCLK, FCLK, and PCLK are set to divided by 64.
Note 3. Clock supply to the peripheral functions is stopped. This does not include BGO operation. The clock source is HOCO and the oscillation frequency is 40 MHz. BCLK, FCLK, and PCLK are set to divided by 64.
Note 4. Clocks are supplied to the peripheral functions. This does not include BGO operation. The clock source is PLL and the VCO oscillation frequency is 64 MHz. BCLK, FCLK, and PCLK are ICLK divided by 1.
Note 5. Clocks are supplied to the peripheral functions. This does not include BGO operation. The clock source is HOCO and the oscillation frequency is 40 MHz. BCLK, FCLK, and PCLK are ICLK divided by 1.
Note 6. This is the increase if data is programmed to or erasing from the ROM or E2 DataFlash during program execution.
Note 7. Clock supply to the peripheral functions is stopped. This does not include BGO operation. The clock source is HOCO and the oscillation frequency is 32 MHz. BCLK, FCLK, and PCLK are set to divided by 64.
Note 8. Clocks are supplied to the peripheral functions. This does not include BGO operation. The clock source is HOCO and the oscillation frequency is 32 MHz. BCLK, FCLK, and PCLK are ICLK divided by 1.
Note 9. Clock supply to the peripheral functions is stopped. This does not include BGO operation. The clock source is the sub oscillation circuit. BCLK, FCLK, and PCLK are set to divided by 64.
Note 10. Clocks are supplied to the peripheral functions. This does not include BGO operation. The clock source is the sub oscillation circuit. BCLK, FCLK, and PCLK are ICLK divided by 1.
Note 11. Value when the main clock continues oscillating at 12.5 MHz.



Note 1. All peripheral operation is normal. This does not include BGO operation.
Average value of the tested middle samples during product evaluation
Note 2. All peripheral operation is maximum. This does not include BGO operation.
Average value of the tested upper-limit samples during product evaluation.

Figure 5.28 Voltage Dependency in Middle-Speed Operating Modes 2A and 2B (Reference Data) for Chip Version B with 768 Kbytes/1 Mbyte of Flash Memory and 100 to 145 Pins



Note 1. All peripheral operation is normal.
Average value of the tested middle samples during product evaluation.
Note 2. All peripheral operation is maximum.
Average value of the tested upper-limit samples during product evaluation.

Figure 5.29 Voltage Dependency in Low-Speed Operating Mode 1 (Reference Data) for Chip Version B with 768 Kbytes/1 Mbyte of Flash Memory and 100 to 145 Pins

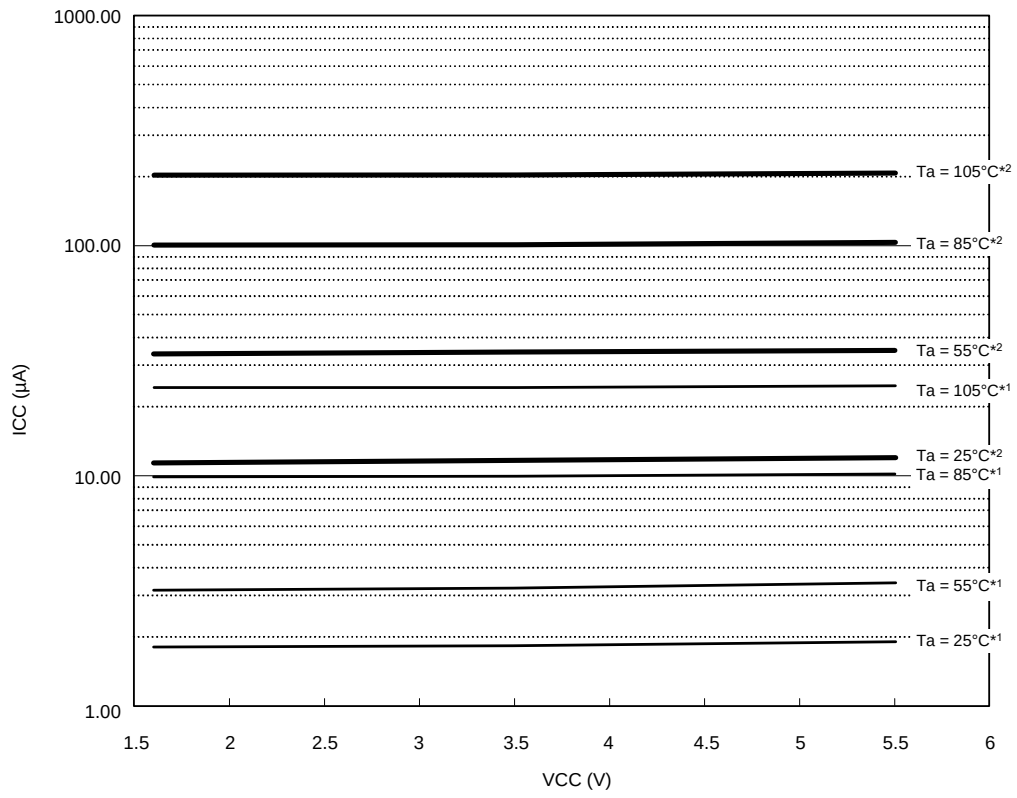
[Chip version B with 768 Kbytes/1 Mbyte of flash memory and 100 to 145 pins]

Table 5.17 DC Characteristics (16)

Conditions: VCC = AVCC0 = 1.62 to 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

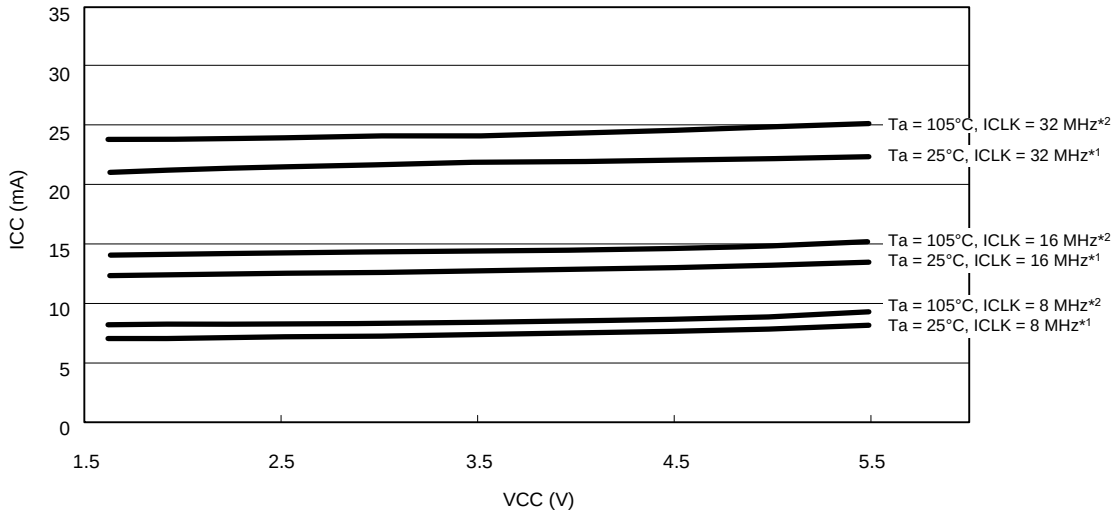
Item				Symbol	Typ.*3	Max.	Unit	Test Conditions
Supply current*1	Software standby mode*2	Flash memory power supplied, HOCO power supplied, POR low power consumption function disabled (SOFTCUT[2:0] bits = 000b)	T_a = 25°C	I_{CC}	10	34	µA	
			T_a = 55°C		13	87		
			T_a = 85°C		21	201		
			T_a = 105°C		40	352		
		Flash memory power supplied, HOCO power not supplied, POR low power consumption function enabled (SOFTCUT[2:0] bits = 110b)	T_a = 25°C		1.8	24		
			T_a = 55°C		3.3	70		
			T_a = 85°C		10	168		
			T_a = 105°C		25	302		
	Deep software standby mode*2	Flash memory power not supplied, HOCO power not supplied, POR low power consumption function enabled (DEEPCUT1 bit = 1)	T_a = 25°C		0.4	0.8		
			T_a = 55°C		0.5	1.0		
			T_a = 85°C		0.7	2.5		
			T_a = 105°C		1.4	6.3		
	Increments produced by running voltage detection circuits and disabling the POR low power consumption function				1.4	—		
	Increment for RTC operation (low CL)				0.8	—		
	Increment for RTC operation (standard CL)				2.0	—		

Note 1. Supply current values are with all output pins unloaded and all input pull-up MOSs in the off state.
Note 2. The IWDT and LVD are stopped.
Note 3. VCC = 3.3 V.



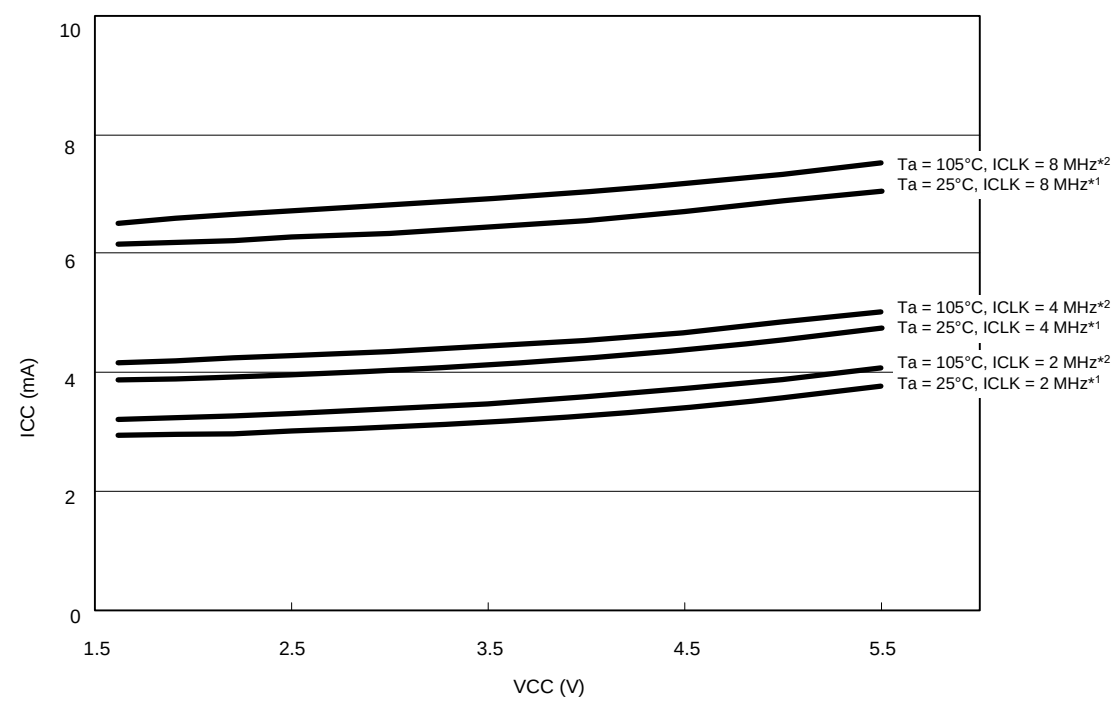
Note 1. Average value of the tested middle samples during product evaluation.
Note 2. Average value of the tested upper-limit samples during product evaluation.

Figure 5.31 Voltage Dependency in Software Standby Mode (SOFTCUT[2:0] Bits = 110b) (Reference Data) for Chip Version B with 768 Kbytes/1 Mbyte of Flash Memory and 100 to 145 Pins



Note 1. All peripheral operation is normal. This does not include BGO operation.
Average value of the tested middle samples during product evaluation
Note 2. All peripheral operation is maximum. This does not include BGO operation.
Average value of the tested upper-limit samples during product evaluation.

Figure 5.37 Voltage Dependency in Middle-Speed Operating Modes 2A and 2B (Reference Data) for Chip Version B with 512 Kbytes or Less of Flash Memory and 144 and 145 Pins



Note 1. All peripheral operation is normal.
Average value of the tested middle samples during product evaluation.
Note 2. All peripheral operation is maximum.
Average value of the tested upper-limit samples during product evaluation.

Figure 5.38 Voltage Dependency in Low-Speed Operating Mode 1 (Reference Data) for Chip Version B with 512 Kbytes or Less of Flash Memory and 144 and 145 Pins

5.3.2 Reset Timing

Table 5.45 Reset Timing

Conditions: VCC = AVCC0 = 1.62 to 5.5 V, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
RES# pulse width	Power-on	t_{RESWP}	8	—	—	ms	Figure 5.70
	Deep software standby mode	t_{RESWD}	8	—	—	ms	Figure 5.71
	Software standby mode, low-speed operating modes 1 and 2	t_{RESWS}	1	—	—	ms	
	Programming or erasure of the ROM or E2 DataFlash memory or blank checking of the E2 DataFlash memory	t_{RESWF}	200	—	—	µs	
	Other than above	t_{RESW}	200	—	—	µs	
Wait time after RES# cancellation		t_{RESWT}	—	—	912	µs	Figure 5.70
Internal reset time (independent watchdog timer reset, watchdog timer reset, software reset)		t_{RESW2}	—	—	1.4	ms	

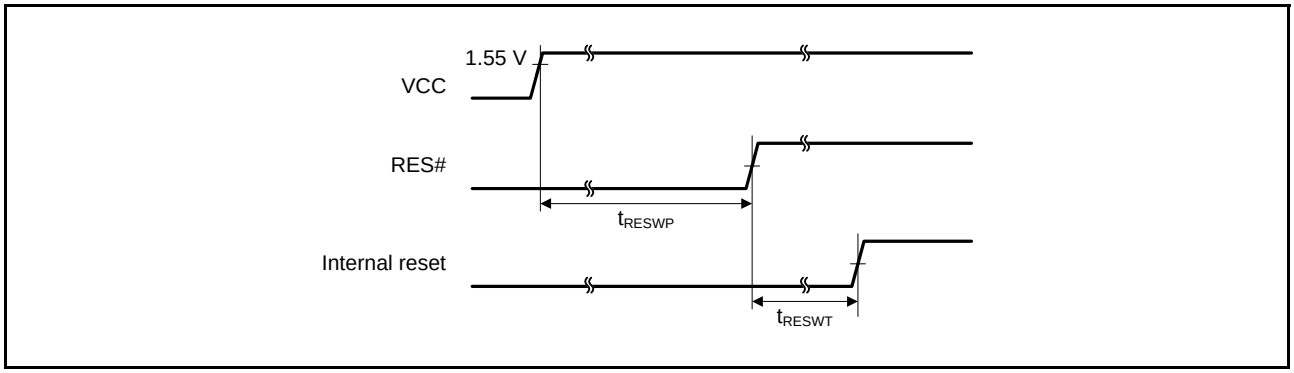


Figure 5.70 Reset Input Timing at Power-On

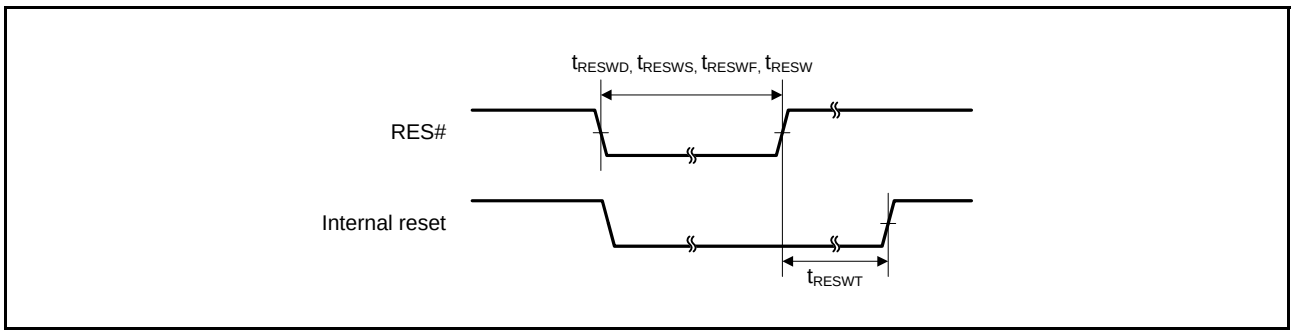


Figure 5.71 Reset Input Timing

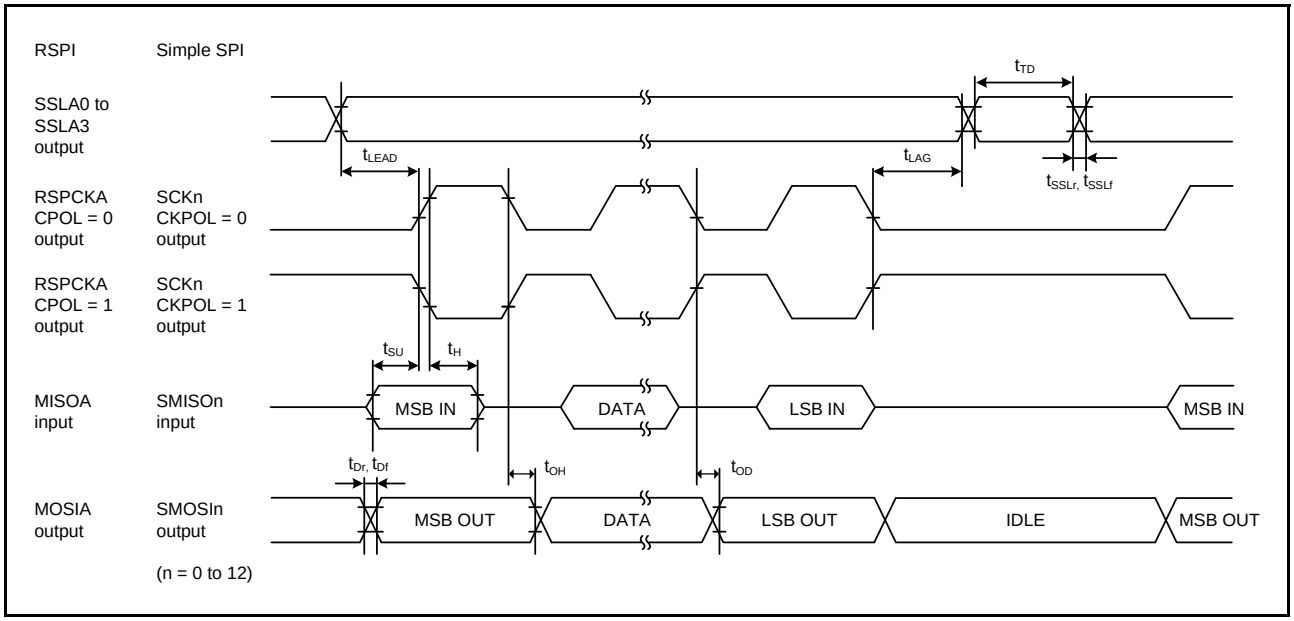


Figure 5.92 RSPI Timing (Master, CPHA = 0) (Bit Rate: PCLKB Set to Division Ratio Other Than Divided by 2) and Simple SPI Timing (Master, CKPH = 1)

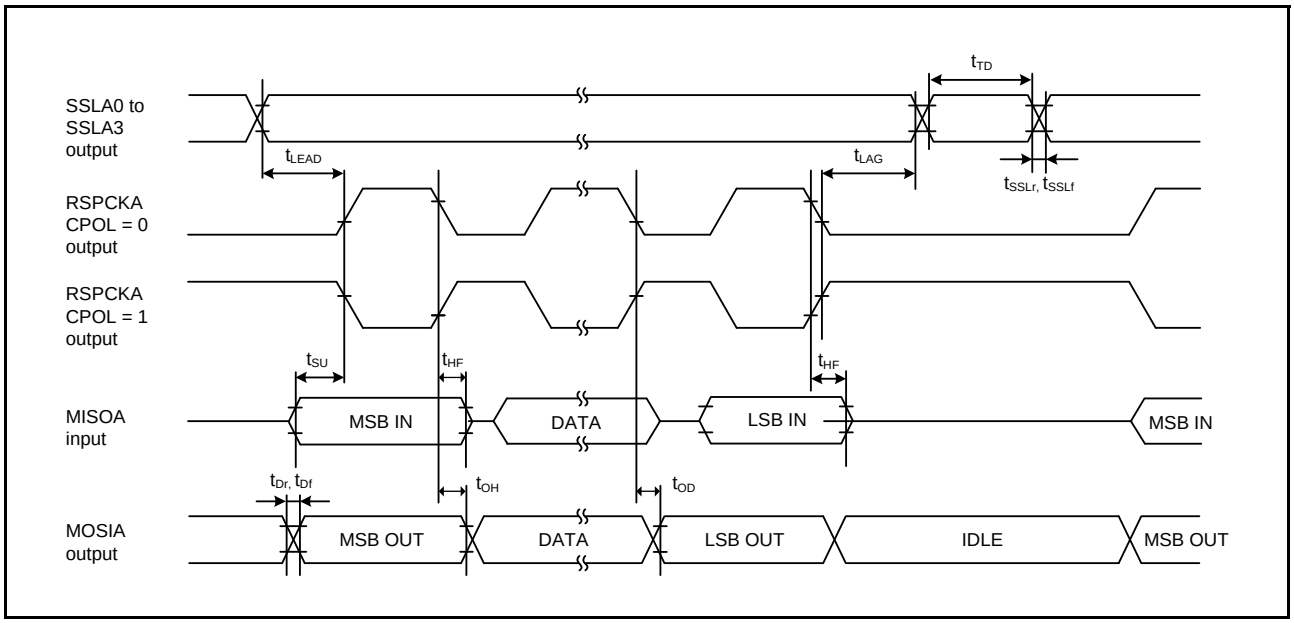


Figure 5.93 RSPI Timing (Master, CPHA = 0) (Bit Rate: PCLKB Set to Divided by 2)

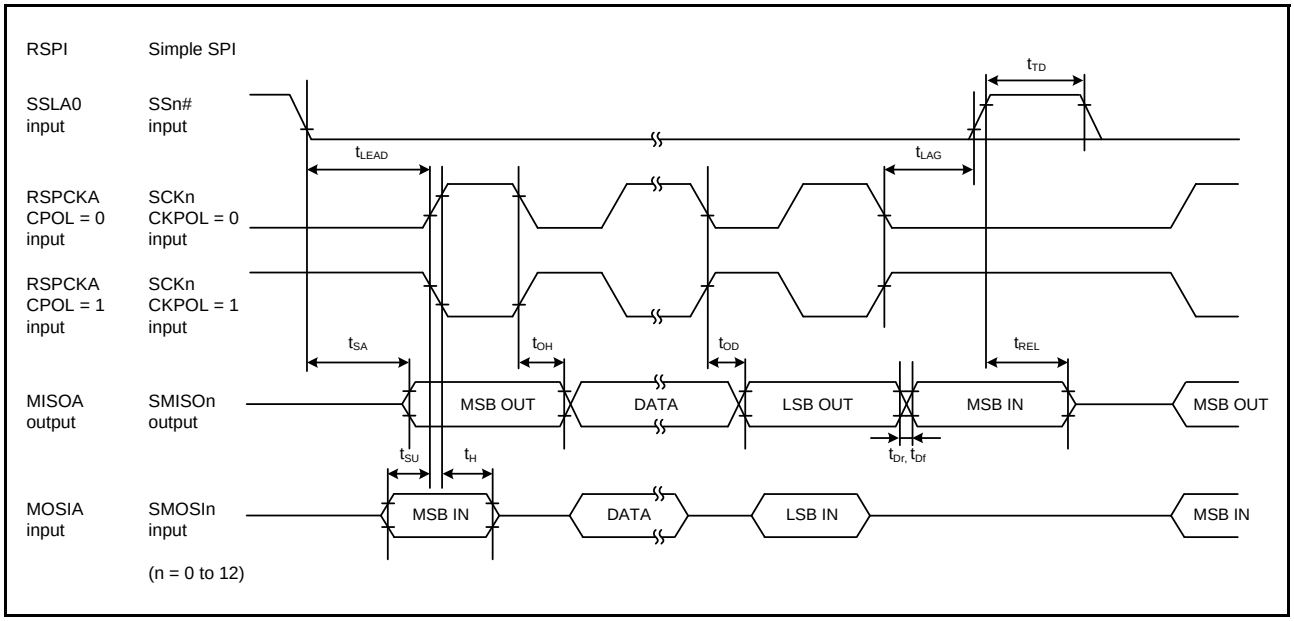


Figure 5.96 RSPI Timing (Slave, CPHA = 0) and Simple SPI Timing (Slave, CKPH = 1)

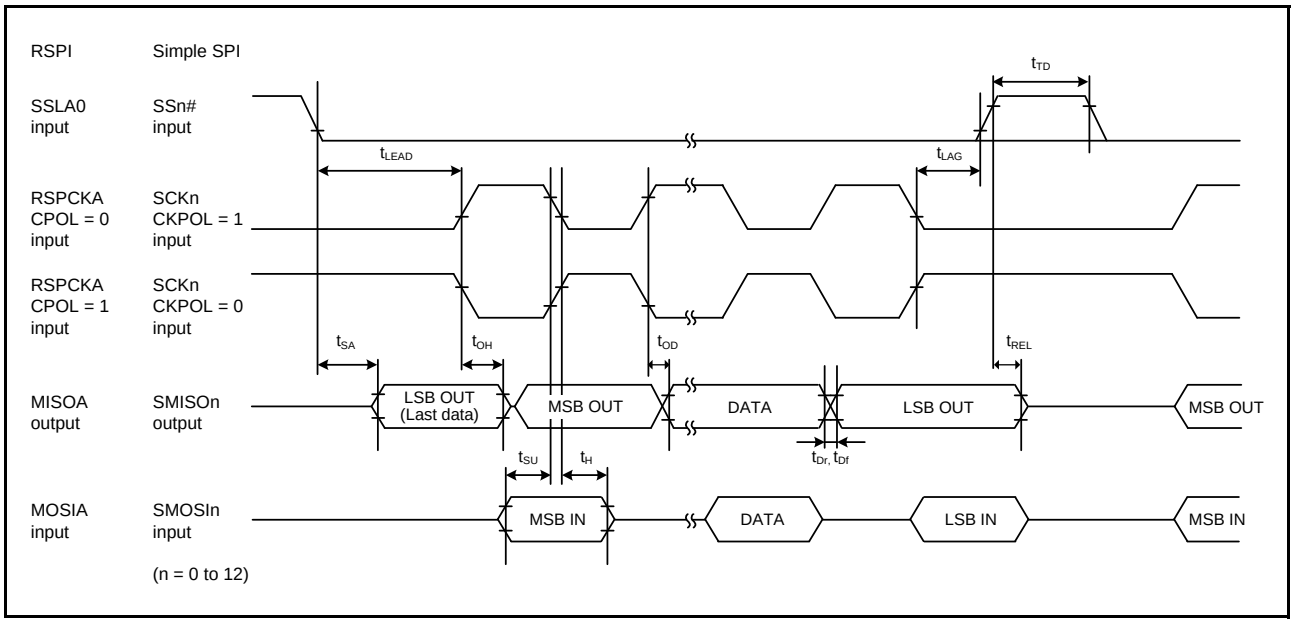


Figure 5.97 RSPI Timing (Slave, CPHA = 1) and Simple SPI Timing (Slave, CKPH = 0)

[Chip versions A and C]

Table 5.76 ROM (Flash Memory for Code Storage) Characteristics (3) : high-speed operating mode, middle-speed operating mode 1A

Conditions: VCC = AVCC0 = 2.7 to 5.5 V, VREFH = VREFH0 = AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V
Temperature range for the programming/erasure operation: T_a = –40 to +105°C

Item		Symbol	FCLK = 4 MHz			FCLK = 32 MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Programming time when N_{PEC} ≤ 100 times	2 bytes	t_{P2}	—	0.52	4.8	—	0.19	2.5	ms
	8 bytes	t_{P8}	—	0.52	4.9	—	0.19	2.5	
	128 bytes	t_{P128}	—	1.50	10.7	—	0.57	4.8	
Programming time when N_{PEC} > 100 times	2 bytes	t_{P2}	—	0.61	5.7	—	0.23	3.0	ms
	8 bytes	t_{P8}	—	0.61	6.2	—	0.23	3.2	
	128 bytes	t_{P128}	—	1.71	13.2	—	0.65	6.0	
Erasure time when N_{PEC} ≤ 100 times	2 Kbytes	t_{E2K}	—	17.0	92.9	—	11.0	29	ms
Erasure time when N_{PEC} > 100 times	2 Kbytes	t_{E2K}	—	20.8	195.8	—	13.5	60	ms
Suspend delay time during programming (in programming/erasure priority mode)		t_{SPD}	—	—	0.9	—	—	0.8	ms
First suspend delay time during programming (in suspend priority mode)		t_{SPSD1}	—	—	220	—	—	120	µs
Second suspend delay time during programming (in suspend priority mode)		t_{SPSD2}	—	—	0.9	—	—	0.8	ms
Suspend delay time during erasing (in programming/erasure priority mode)		t_{SED}	—	—	0.9	—	—	0.8	ms
First suspend delay time during erasing (in suspend priority mode)		t_{SESD1}	—	—	220	—	—	120	µs
Second suspend delay time during erasing (in suspend priority mode)		t_{SESD2}	—	—	0.9	—	—	0.8	ms
FCU reset time		t_{FCUR}	20 µs or longer and FCLK × 6 or greater	—	—	20 µs or longer and FCLK × 6 or greater	—	—	µs

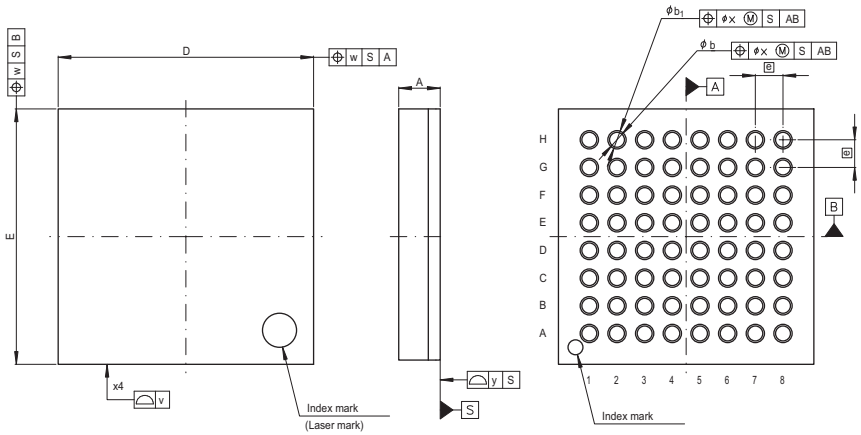
[Chip version B]

Table 5.84 E2 DataFlash Characteristics (5)
: high-speed operating mode, middle-speed operating modes 1A and 2A

Conditions: VCC = AVCC0 = 2.7 to 5.5 V, VREFH = VREFH0 = AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V
Temperature range for the programming/erasure operation: T_a = –40 to +105°C

Item		Symbol	FCLK = 4 MHz			FCLK = 32 MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Programming time when N_{DPEC} ≤ 100 times	2 bytes	t_{DP2}	—	0.19	4.4	—	0.13	2.0	ms
	8 bytes	t_{DP8}	—	0.24	5.1	—	0.13	2.2	
Programming time when N_{DPEC} > 100 times	2 bytes	t_{DP2}	—	0.25	6.4	—	0.17	3.0	ms
	8 bytes	t_{DP8}	—	0.32	7.5	—	0.18	3.2	
Erasure time when N_{DPEC} ≤ 100 times	128 bytes	t_{DE128}	—	3.3	27.1	—	2.5	8	ms
Erasure time when N_{DPEC} > 100 times	128 bytes	t_{DE128}	—	4.0	45.1	—	3.0	12	ms
Blank check time	2 bytes	t_{DBC2}	—	—	98	—	—	35	µs
	2 Kbytes	t_{DBC2K}	—	—	16	—	—	2.5	ms
Suspend delay time during programming (in programming/erasure priority mode)		t_{DSPD}	—	—	0.9	—	—	0.8	ms
First suspend delay time during programming (in suspend priority mode)		t_{DSPSD1}	—	—	220	—	—	120	µs
Second suspend delay time during programming (in suspend priority mode)		t_{DSPSD2}	—	—	0.9	—	—	0.8	ms
Suspend delay time during erasing (in programming/erasure priority mode)		t_{DSED}	—	—	0.9	—	—	0.8	ms
First suspend delay time during erasing (in suspend priority mode)		t_{DSESD1}	—	—	220	—	—	120	µs
Second suspend delay time during erasing (in suspend priority mode)		t_{DSESD2}	—	—	0.9	—	—	0.8	ms

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-TFLGA64-6x6-0.65	PTLG0064JA-A	64F0G	0.07g



Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	6.0	—
E	—	6.0	—
v	—	—	0.15
w	—	—	0.20
A	—	—	1.05
e	—	0.65	—
b	0.31	0.35	0.39
b_1	0.39	0.43	0.47
x	—	—	0.08
y	—	—	0.10

Figure F 64-Pin TFLGA (PTLG0064JA-A)