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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I²C, SCI, SPI
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	48
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.62V ~ 5.5V
Data Converters	A/D 12x12b; D/A 2x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	69-WFBGA
Supplier Device Package	69-WFBGA (3.91x4.26)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f52106bdbm-u0

1.4 Pin Functions

Table 1.8 lists the pin functions.

Table 1.8 Pin Functions (1 / 4)

Classifications	Pin Name	I/O	Description
Power supply	VCC	Input	Power supply pin. Connect it to the system power supply.
	VCL	—	Connect this pin to the VSS pin via the 0.1 µF smoothing capacitor used to stabilize the internal power supply. Place the capacitor close to the pin.
	VSS	Input	Ground pin. Connect it to the system power supply (0 V).
Clock	XTAL	Output	Pins for connecting a crystal resonator. An external clock signal can be input through the EXTAL pin.
	EXTAL	Input	
	BCLK	Output	Outputs the external bus clock for external devices.
	XCIN	Input	Input/output pins for the sub-clock oscillator. Connect a crystal resonator between XCIN and XCOUT.
	XCOUT	Output	
Operating mode control	MD	Input	Pin for setting the operating mode. The signal levels on this pin must not be changed during operation.
System control	RES#	Input	Reset pin. This LSI enters the reset state when this signal goes low.
CAC	CACREF	Input	Input pin for the clock frequency accuracy measurement circuit.
On-chip emulator	FINED	I/O	FINE interface pin.
Address bus	A0 to A23	Output	Output pins for the address.
Data bus	D0 to D15	I/O	Input and output pins for the bidirectional data bus.
Multiplexed bus	A0/D0 to A15/D15	I/O	Address/data multiplexed bus
Bus control	RD#	Output	Strobe signal which indicates that reading from the external bus interface space is in progress.
	WR#	Output	Strobe signal which indicates that writing to the external bus interface space is in progress, in single-write strobe mode.
	WR0#, WR1#	Output	Strobe signals which indicate that either group of data bus pins (D7 to D0, and D15 to D8) is valid in writing to the external bus interface space, in byte strobe mode.
	BC0#, BC1#	Output	Strobe signals which indicate that either group of data bus pins (D7 to D0 and D15 to D8) is valid in access to the external bus interface space, in single-write strobe mode.
	CS0# to CS3#	Output	Select signals for areas 0 to 3.
	WAIT#	Input	Input pin for wait request signals in access to the external space.
	ALE	Output	Address latch signal when address/data multiplexed bus is selected.
Interrupt	NMI	Input	Non-maskable interrupt request pin.
	IRQ0 to IRQ7	Input	Interrupt request pins.

Table 1.11 List of Pins and Pin Functions (100-Pin TFLGA) (2 / 3)

Pin No.	Power Supply, Clock, System Control	I/O Port	External Bus	Timers (MTU, TMR, POE)	Communications (SCIc, SCId, RSPI, RIIC)	Others
E6		PA2	A2		RXD5/SMISO5/SSCL5/ SSLA3	
E7		PA6	A6	MTIC5V/MTCLKB/ TMCI3/POE2#	CTS5#/RTS5#/SS5#/ MOSIA	
E8		PA4	A4	MTIC5U/MTCLKA/ TMRI0	TXD5/SMOSI5/SSDA5/ SSLA0	IRQ5-DS/CVREFB1
E9		PA5	A5		RSPCKA	
E10		PA3	A3	MTIOC0D/MTCLKD	RXD5/SMISO5/SSCL5	IRQ6-DS/CMPB1
F1	EXTAL	P36				
F2	VCC					
F3		P35				NMI
F4		P32		MTIOC0C/TMO3	TXD6/SMOSI6/SSDA6	IRQ2-DS/RTCOUT/ RTCIC2
F5		P12		TMCI1	SCL	IRQ2
F6		PB3	A11	MTIOC0A/MTIOC4A/ TMO0/POE3#	SCK6	
F7		PB2	A10		CTS6#/RTS6#/SS6#	
F8		PB0	A8	MTIC5W	RXD6/SMISO6/SSCL6/ RSPCKA	
F9		PA7	A7		MISOA	
F10	VSS					
G1		P33		MTIOC0D/TMRI3/ POE3#	RXD6/SMISO6/SSCL6	IRQ3-DS
G2		P31		MTIOC4D/TMCI2	CTS1#/RTS1#/SS1#	IRQ1-DS/RTCIC1
G3		P30		MTIOC4B/TMRI3/ POE8#	RXD1/SMISO1/SSCL1	IRQ0-DS/RTCIC0
G4		P27	CS3#	MTIOC2B/TMCI3	SCK1	
G5	BCLK	P53				
G6		P52	RD#			
G7		PB5	A13	MTIOC2A/MTIOC1B/ TMRI1/POE1#	SCK9	
G8		PB4	A12		CTS9#/RTS9#/SS9#	
G9		PB1	A9	MTIOC0C/MTIOC4C/ TMCI0	TXD6/SMOSI6/SSDA6	IRQ4-DS
G10	VCC					
H1		P26	CS2#	MTIOC2A/TMO1	TXD1/SMOSI1/SSDA1	
H2		P25	CS1#	MTIOC4C/MTCLKB		ADTRG0#
H3		P16		MTIOC3C/MTIOC3D/ TMO2	TXD1/SMOSI1/SSDA1/ MOSIA/SCL-DS	IRQ6/RTCOUT/ ADTRG0#
H4		P15		MTIOC0B/MTCLKB/ TMCI2	RXD1/SMISO1/SSCL1	IRQ5
H5		P55	WAIT#	MTIOC4D/TMO3		
H6		P54	ALE	MTIOC4B/TMCI1		
H7		PC7	A23/CS0#	MTIOC3A/TMO2/ MTCLKB	TXD8/SMOSI8/SSDA8/ MISOA	CACREF
H8		PC6	A22/CS1#	MTIOC3C/MTCLKA/ TMCI2	RXD8/SMISO8/SSCL8/ MOSIA	
H9		PB6	A14	MTIOC3D	RXD9/SMISO9/SSCL9	
H10		PB7	A15	MTIOC3B	TXD9/SMOSI9/SSDA9	
J1		P24	CS0#	MTIOC4A/MTCLKA/ TMRI1		
J2		P21		MTIOC1B/TMCI0	RXD0/SMISO0/SSCL0	
J3		P17		MTIOC3A/MTIOC3B/ TMO1/POE8#	SCK1/MISOA/ SDA-DS	IRQ7

Table 1.12 List of Pins and Pin Functions (100-Pin LQFP) (2 / 3)

Pin No.	Power Supply, Clock, System Control	I/O Port	External Bus	Timers (MTU, TMR, POE)	Communications (SCIc, SCId, RSPI, RIIC)	Others
42		P52	RD#			
43		P51	WR1#/BC1#/WAIT#			
44		P50	WR0#/WR#			
45		PC7	A23/CS0#	MTIOC3A/TMO2/ MTCLKB	TXD8/SMOSI8/SSDA8/ MISOA	CACREF
46		PC6	A22/CS1#	MTIOC3C/MTCLKA/ TMCI2	RXD8/SMISO8/SSCL8/ MOSIA	
47		PC5	A21/CS2#/WAIT#	MTIOC3B/MTCLKD/ TMRI2	SCK8/RSPCKA	
48		PC4	A20/CS3#	MTIOC3D/MTCLKC/ TMCI1/POE0#	SCK5/CTS8#/RTS8#/ SS8#/SSLA0	
49		PC3	A19	MTIOC4D	TXD5/SMOSI5/SSDA5	
50		PC2	A18	MTIOC4B	RXD5/SMISO5/SSCL5/ SSLA3	
51		PC1	A17	MTIOC3A	SCK5/SSLA2	
52		PC0	A16	MTIOC3C	CTS5#/RTS5#/SS5#/ SSLA1	
53		PB7	A15	MTIOC3B	TXD9/SMOSI9/SSDA9	
54		PB6	A14	MTIOC3D	RXD9/SMISO9/SSCL9	
55		PB5	A13	MTIOC2A/MTIOC1B/ TMRI1/POE1#	SCK9	
56		PB4	A12		CTS9#/RTS9#/SS9#	
57		PB3	A11	MTIOC0A/MTIOC4A/ TMO0/POE3#	SCK6	
58		PB2	A10		CTS6#/RTS6#/SS6#	
59		PB1	A9	MTIOC0C/MTIOC4C/ TMCI0	TXD6/SMOSI6/SSDA6	IRQ4-DS
60	VCC					
61		PB0	A8	MTIC5W	RXD6/SMISO6/SSCL6/ RSPCKA	
62	VSS					
63		PA7	A7		MISOA	
64		PA6	A6	MTIC5V/MTCLKB/ TMCI3/POE2#	CTS5#/RTS5#/SS5#/ MOSIA	
65		PA5	A5		RSPCKA	
66		PA4	A4	MTIC5U/MTCLKA/ TMRI0	TXD5/SMOSI5/SSDA5/ SSLA0	IRQ5-DS/CVREFB1
67		PA3	A3	MTIOC0D/MTCLKD	RXD5/SMISO5/SSCL5	IRQ6-DS/CMPB1
68		PA2	A2		RXD5/SMISO5/SSCL5/ SSLA3	
69		PA1	A1	MTIOC0B/MTCLKC	SCK5/SSLA2	CVREFA
70		PA0	A0/BC0#	MTIOC4A	SSLA1	CACREF
71		PE7	D15[A15/D15]			IRQ7/AN015
72		PE6	D14[A14/D14]			IRQ6/AN014
73		PE5	D13[A13/D13]	MTIOC4C/MTIOC2B		IRQ5/AN013
74		PE4	D12[A12/D12]	MTIOC4D/MTIOC1A		AN012/CMPA2
75		PE3	D11[A11/D11]	MTIOC4B/POE8#	CTS12#/RTS12#/SS12#	AN011/CMPA1
76		PE2	D10[A10/D10]	MTIOC4A	RXD12/RXDX12/ SMISO12/SSCL12	IRQ7-DS/AN010/ CVREFB0
77		PE1	D9[A9/D9]	MTIOC4C	TXD12/TXDX12/SIOX12/ SMOSI12/SSDA12	AN009/CMPB0
78		PE0	D8[A8/D8]		SCK12	AN008
79		PD7	D7[A7/D7]	MTIC5U/POE0#		IRQ7

Table 1.13 List of Pins and Pin Functions (80-Pin LQFP) (2 / 2)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (MTU, TMR, POE)	Communications (SCIc, SCId, RSPI, RIIC)	Others
45		PB3	MTIOC0A/MTIOC4A/TMO0/ POE3#	SCK6	
46		PB2		CTS6#/RTS6#/SS6#	
47		PB1	MTIOC0C/MTIOC4C/TMCI0	TXD6/SMOSI6/SSDA6	IRQ4-DS
48	VCC				
49		PB0	MTIC5W	RXD6/SMISO6/SSCL6/RSPCKA	
50	VSS				
51		PA6	MTIC5V/MTCLKB/TMCI3/ POE2#	CTS5#/RTS5#/SS5#/MOSIA	
52		PA5		RSPCKA	
53		PA4	MTIC5U/MTCLKA/TMRI0	TXD5/SMOSI5/SSDA5/SSLA0	IRQ5-DS/CVREFB1
54		PA3	MTIOC0D/MTCLKD	RXD5/SMISO5/SSCL5	IRQ6-DS/CMPB1
55		PA2		RXD5/SMISO5/SSCL5/SSLA3	
56		PA1	MTIOC0B/MTCLKC	SCK5/SSLA2	CVREFA
57		PA0	MTIOC4A	SSLA1	CACREF
58		PE5	MTIOC4C/MTIOC2B		IRQ5/AN013
59		PE4	MTIOC4D/MTIOC1A		AN012/CMPA2
60		PE3	MTIOC4B/POE8#	CTS12#/RTS12#/SS12#	AN011/CMPA1
61		PE2	MTIOC4A	RXD12/RXDX12/SMISO12/ SSCL12	IRQ7-DS/AN010/ CVREFB0
62		PE1	MTIOC4C	TXD12/TXDX12/SIOX12/ SMOSI12/SSDA12	AN009/CMPB0
63		PE0		SCK12	AN008
64		PD2	MTIOC4D		IRQ2
65		PD1	MTIOC4B		IRQ1
66		PD0			IRQ0
67		P47			AN007
68		P46			AN006
69		P45			AN005
70		P44			AN004
71		P43			AN003
72		P42			AN002
73		P41			AN001
74	VREFL0				
75		P40			AN000
76	VREFH0				
77	AVCC0				
78		P07			ADTRG0#
79	AVSS0				
80		P05			DA1

Note: • Pin names to which –DS is appended are for pins that can be used to trigger release from deep software standby mode.

4.1 I/O Register Addresses (Address Order)

Table 4.1 List of I/O Registers (Address Order) (1 / 29)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles: ICLK ≥ PCLK	Number of Access Cycles: ICLK < PCLK
0008 0000h	SYSTEM	Mode monitor register	MDMONR	16	16		3 ICLK
0008 0002h	SYSTEM	Mode status register	MDSR	16	16		3 ICLK
0008 0006h	SYSTEM	System control register 0	SYSCR0	16	16		3 ICLK
0008 0008h	SYSTEM	System control register 1	SYSCR1	16	16		3 ICLK
0008 000Ch	SYSTEM	Standby control register	SBYCR	16	16		3 ICLK
0008 0010h	SYSTEM	Module stop control register A	MSTPCRA	32	32		3 ICLK
0008 0014h	SYSTEM	Module stop control register B	MSTPCRB	32	32		3 ICLK
0008 0018h	SYSTEM	Module stop control register C	MSTPCRC	32	32		3 ICLK
0008 0020h	SYSTEM	System clock control register	SCKCR	32	32		3 ICLK
0008 0026h	SYSTEM	System clock control register 3	SCKCR3	16	16		3 ICLK
0008 0028h	SYSTEM	PLL control register	PLLCR	16	16		3 ICLK
0008 002Ah	SYSTEM	PLL control register 2	PLLCR2	8	8		3 ICLK
0008 0030h	SYSTEM	External bus clock control register	BCKCR	8	8		3 ICLK
0008 0032h	SYSTEM	Main clock oscillator control register	MOSCCR	8	8		3 ICLK
0008 0033h	SYSTEM	Sub-clock oscillator control register	SOSCCR	8	8		3 ICLK
0008 0034h	SYSTEM	Low-speed on-chip oscillator control register	LOCOCR	8	8		3 ICLK
0008 0035h	SYSTEM	IWDT-dedicated on-chip oscillator control register	ILOCOCR	8	8		3 ICLK
0008 0036h	SYSTEM	High-speed on-chip oscillator control register	HOCOCR	8	8		3 ICLK
0008 0037h	SYSTEM	High-speed on-chip oscillator control register 2	HOCOCR2	8	8		3 ICLK
0008 0040h	SYSTEM	Oscillation stop detection control register	OSTDCR	8	8		3 ICLK
0008 0041h	SYSTEM	Oscillation stop detection status register	OSTDSR	8	8		3 ICLK
0008 00A0h	SYSTEM	Operating power control register	OPCCR	8	8		3 ICLK
0008 00A1h	SYSTEM	Sleep mode return clock source switching register	RSTCKCR	8	8		3 ICLK
0008 00A2h	SYSTEM	Main clock oscillator wait control register	MOSCWTCR	8	8		3 ICLK
0008 00A3h	SYSTEM	Sub-clock oscillator wait control register	SOSCWTCR	8	8		3 ICLK
0008 00A6h	SYSTEM	PLL wait control register	PLLWTCR	8	8		3 ICLK
0008 00A9h	SYSTEM	HOCO wait control register 2	HOCOWTCR2	8	8		3 ICLK
0008 00C0h	SYSTEM	Reset status register 2	RSTSR2	8	8		3 ICLK
0008 00C2h	SYSTEM	Software reset register	SWRR	16	16		3 ICLK
0008 00E0h	SYSTEM	Voltage monitoring 1 circuit/comparator A1 control register 1	LVD1CR1	8	8		3 ICLK
0008 00E1h	SYSTEM	Voltage monitoring 1 circuit/comparator A1 status register	LVD1SR	8	8		3 ICLK
0008 00E2h	SYSTEM	Voltage monitoring 2 circuit/comparator A2 control register 1	LVD2CR1	8	8		3 ICLK
0008 00E3h	SYSTEM	Voltage monitoring 2 circuit/comparator A2 status register	LVD2SR	8	8		3 ICLK
0008 0200h	SYSTEM	Voltage regulator control register	VRCR	8	8		3 ICLK
0008 03FEh	SYSTEM	Protect register	PRCR	16	16		3 ICLK
0008 1300h	BSC	Bus error status clear register	BERCLR	8	8		2 ICLK
0008 1304h	BSC	Bus error monitoring enable register	BEREN	8	8		2 ICLK
0008 1308h	BSC	Bus error status register 1	BERSR1	8	8		2 ICLK
0008 130Ah	BSC	Bus error status register 2	BERSR2	16	16		2 ICLK
0008 1310h	BSC	Bus priority control register	BUSPRI	16	16		2 ICLK
0008 2000h	DMAC0	DMA source address register	DMSAR	32	32		2 ICLK
0008 2004h	DMAC0	DMA destination address register	DMDAR	32	32		2 ICLK
0008 2008h	DMAC0	DMA transfer count register	DMCRA	32	32		2 ICLK
0008 200Ch	DMAC0	DMA block transfer count register	DMCRB	16	16		2 ICLK
0008 2010h	DMAC0	DMA transfer mode register	DMTMD	16	16		2 ICLK
0008 2013h	DMAC0	DMA interrupt setting register	DMINT	8	8		2 ICLK
0008 2014h	DMAC0	DMA address mode register	DMAMD	16	16		2 ICLK
0008 2018h	DMAC0	DMA offset register	DMOFR	32	32		2 ICLK
0008 201Ch	DMAC0	DMA transfer enable register	DMCNT	8	8		2 ICLK

Table 4.1 List of I/O Registers (Address Order) (3 / 29)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles ICLK ≥ PCLK	Number of Access Cycles ICLK < PCLK
0008 3032h	BSC	CS3 mode register	CS3MOD	16	16	1, 2 BCLK	
0008 3034h	BSC	CS3 wait control register 1	CS3WCR1	32	32	1, 2 BCLK	
0008 3038h	BSC	CS3 wait control register 2	CS3WCR2	32	32	1, 2 BCLK	
0008 3802h	BSC	CS0 control register	CS0CR	16	16	1, 2 BCLK	
0008 380Ah	BSC	CS0 recovery cycle register	CS0REC	16	16	1, 2 BCLK	
0008 3812h	BSC	CS1 control register	CS1CR	16	16	1, 2 BCLK	
0008 381Ah	BSC	CS1 recovery cycle register	CS1REC	16	16	1, 2 BCLK	
0008 3822h	BSC	CS2 control register	CS2CR	16	16	1, 2 BCLK	
0008 382Ah	BSC	CS2 recovery cycle register	CS2REC	16	16	1, 2 BCLK	
0008 3832h	BSC	CS3 control register	CS3CR	16	16	1, 2 BCLK	
0008 383Ah	BSC	CS3 recovery cycle register	CS3REC	16	16	1, 2 BCLK	
0008 3880h	BSC	CS recovery cycle insertion enable register	CSRECEN	16	16	1, 2 BCLK	
0008 7010h	ICU	Interrupt request register 016	IR016	8	8	2 ICLK	
0008 7015h	ICU	Interrupt request register 021	IR021	8	8	2 ICLK	
0008 7017h	ICU	Interrupt request register 023	IR023	8	8	2 ICLK	
0008 701Bh	ICU	Interrupt request register 027	IR027	8	8	2 ICLK	
0008 701Ch	ICU	Interrupt request register 028	IR028	8	8	2 ICLK	
0008 701Dh	ICU	Interrupt request register 029	IR029	8	8	2 ICLK	
0008 701Eh	ICU	Interrupt request register 030	IR030	8	8	2 ICLK	
0008 701Fh	ICU	Interrupt request register 031	IR031	8	8	2 ICLK	
0008 7020h	ICU	Interrupt request register 032	IR032	8	8	2 ICLK	
0008 7021h	ICU	Interrupt request register 033	IR033	8	8	2 ICLK	
0008 7022h	ICU	Interrupt request register 034	IR034	8	8	2 ICLK	
0008 702Ch	ICU	Interrupt request register 044	IR044	8	8	2 ICLK	
0008 702Dh	ICU	Interrupt request register 045	IR045	8	8	2 ICLK	
0008 702Eh	ICU	Interrupt request register 046	IR046	8	8	2 ICLK	
0008 702Fh	ICU	Interrupt request register 047	IR047	8	8	2 ICLK	
0008 7039h	ICU	Interrupt request register 057	IR057	8	8	2 ICLK	
0008 703Ah	ICU	Interrupt request register 058	IR058	8	8	2 ICLK	
0008 703Bh	ICU	Interrupt request register 059	IR059	8	8	2 ICLK	
0008 703Fh	ICU	Interrupt request register 063	IR063	8	8	2 ICLK	
0008 7040h	ICU	Interrupt request register 064	IR064	8	8	2 ICLK	
0008 7041h	ICU	Interrupt request register 065	IR065	8	8	2 ICLK	
0008 7042h	ICU	Interrupt request register 066	IR066	8	8	2 ICLK	
0008 7043h	ICU	Interrupt request register 067	IR067	8	8	2 ICLK	
0008 7044h	ICU	Interrupt request register 068	IR068	8	8	2 ICLK	
0008 7045h	ICU	Interrupt request register 069	IR069	8	8	2 ICLK	
0008 7046h	ICU	Interrupt request register 070	IR070	8	8	2 ICLK	
0008 7047h	ICU	Interrupt request register 071	IR071	8	8	2 ICLK	
0008 7058h	ICU	Interrupt request register 088	IR088	8	8	2 ICLK	
0008 7059h	ICU	Interrupt request register 089	IR089	8	8	2 ICLK	
0008 705Ch	ICU	Interrupt request register 092	IR092	8	8	2 ICLK	
0008 705Dh	ICU	Interrupt request register 093	IR093	8	8	2 ICLK	
0008 7066h	ICU	Interrupt request register 102	IR102	8	8	2 ICLK	
0008 7067h	ICU	Interrupt request register 103	IR103	8	8	2 ICLK	
0008 706Ah	ICU	Interrupt request register 106	IR106	8	8	2 ICLK	
0008 706Bh	ICU	Interrupt request register 107	IR107	8	8	2 ICLK	
0008 7072h	ICU	Interrupt request register 114	IR114	8	8	2 ICLK	
0008 7073h	ICU	Interrupt request register 115	IR115	8	8	2 ICLK	
0008 7074h	ICU	Interrupt request register 116	IR116	8	8	2 ICLK	
0008 7075h	ICU	Interrupt request register 117	IR117	8	8	2 ICLK	

Table 4.1 List of I/O Registers (Address Order) (19 / 29)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles: ICLK ≥ PCLK	Number of Access Cycles: ICLK < PCLK
0008 A0CDh	SCI6	SPI mode register	SPMR	8	8	2, 3 PCLKB	2 ICLK
0008 A0E0h	SCI7	Serial mode register	SMR	8	8	2, 3 PCLKB	2 ICLK
0008 A0E1h	SCI7	Bit rate register	BRR	8	8	2, 3 PCLKB	2 ICLK
0008 A0E2h	SCI7	Serial control register	SCR	8	8	2, 3 PCLKB	2 ICLK
0008 A0E3h	SCI7	Transmit data register	TDR	8	8	2, 3 PCLKB	2 ICLK
0008 A0E4h	SCI7	Serial status register	SSR	8	8	2, 3 PCLKB	2 ICLK
0008 A0E5h	SCI7	Receive data register	RDR	8	8	2, 3 PCLKB	2 ICLK
0008 A0E6h	SCI7	Smart card mode register	SCMR	8	8	2, 3 PCLKB	2 ICLK
0008 A0E7h	SCI7	Serial extended mode register	SEMR	8	8	2, 3 PCLKB	2 ICLK
0008 A0E8h	SCI7	Noise filter setting register	SNFR	8	8	2, 3 PCLKB	2 ICLK
0008 A0E9h	SCI7	I^2C mode register 1	SIMR1	8	8	2, 3 PCLKB	2 ICLK
0008 A0EAh	SCI7	I^2C mode register 2	SIMR2	8	8	2, 3 PCLKB	2 ICLK
0008 A0EBh	SCI7	I^2C mode register 3	SIMR3	8	8	2, 3 PCLKB	2 ICLK
0008 A0ECh	SCI7	I^2C status register	SISR	8	8	2, 3 PCLKB	2 ICLK
0008 A0EDh	SCI7	SPI mode register	SPMR	8	8	2, 3 PCLKB	2 ICLK
0008 A100h	SCI8	Serial mode register	SMR	8	8	2, 3 PCLKB	2 ICLK
0008 A101h	SCI8	Bit rate register	BRR	8	8	2, 3 PCLKB	2 ICLK
0008 A102h	SCI8	Serial control register	SCR	8	8	2, 3 PCLKB	2 ICLK
0008 A103h	SCI8	Transmit data register	TDR	8	8	2, 3 PCLKB	2 ICLK
0008 A104h	SCI8	Serial status register	SSR	8	8	2, 3 PCLKB	2 ICLK
0008 A105h	SCI8	Receive data register	RDR	8	8	2, 3 PCLKB	2 ICLK
0008 A106h	SCI8	Smart card mode register	SCMR	8	8	2, 3 PCLKB	2 ICLK
0008 A107h	SCI8	Serial extended mode register	SEMR	8	8	2, 3 PCLKB	2 ICLK
0008 A108h	SCI8	Noise filter setting register	SNFR	8	8	2, 3 PCLKB	2 ICLK
0008 A109h	SCI8	I^2C mode register 1	SIMR1	8	8	2, 3 PCLKB	2 ICLK
0008 A10Ah	SCI8	I^2C mode register 2	SIMR2	8	8	2, 3 PCLKB	2 ICLK
0008 A10Bh	SCI8	I^2C mode register 3	SIMR3	8	8	2, 3 PCLKB	2 ICLK
0008 A10Ch	SCI8	I^2C status register	SISR	8	8	2, 3 PCLKB	2 ICLK
0008 A10Dh	SCI8	SPI mode register	SPMR	8	8	2, 3 PCLKB	2 ICLK
0008 A120h	SCI9	Serial mode register	SMR	8	8	2, 3 PCLKB	2 ICLK
0008 A121h	SCI9	Bit rate register	BRR	8	8	2, 3 PCLKB	2 ICLK
0008 A122h	SCI9	Serial control register	SCR	8	8	2, 3 PCLKB	2 ICLK
0008 A123h	SCI9	Transmit data register	TDR	8	8	2, 3 PCLKB	2 ICLK
0008 A124h	SCI9	Serial status register	SSR	8	8	2, 3 PCLKB	2 ICLK
0008 A125h	SCI9	Receive data register	RDR	8	8	2, 3 PCLKB	2 ICLK
0008 A126h	SCI9	Smart card mode register	SCMR	8	8	2, 3 PCLKB	2 ICLK
0008 A127h	SCI9	Serial extended mode register	SEMR	8	8	2, 3 PCLKB	2 ICLK
0008 A128h	SCI9	Noise filter setting register	SNFR	8	8	2, 3 PCLKB	2 ICLK
0008 A129h	SCI9	I^2C mode register 1	SIMR1	8	8	2, 3 PCLKB	2 ICLK
0008 A12Ah	SCI9	I^2C mode register 2	SIMR2	8	8	2, 3 PCLKB	2 ICLK
0008 A12Bh	SCI9	I^2C mode register 3	SIMR3	8	8	2, 3 PCLKB	2 ICLK
0008 A12Ch	SCI9	I^2C status register	SISR	8	8	2, 3 PCLKB	2 ICLK
0008 A12Dh	SCI9	SPI mode register	SPMR	8	8	2, 3 PCLKB	2 ICLK
0008 A140h	SCI10	Serial mode register	SMR	8	8	2, 3 PCLKB	2 ICLK
0008 A141h	SCI10	Bit rate register	BRR	8	8	2, 3 PCLKB	2 ICLK
0008 A142h	SCI10	Serial control register	SCR	8	8	2, 3 PCLKB	2 ICLK
0008 A143h	SCI10	Transmit data register	TDR	8	8	2, 3 PCLKB	2 ICLK
0008 A144h	SCI10	Serial status register	SSR	8	8	2, 3 PCLKB	2 ICLK
0008 A145h	SCI10	Receive data register	RDR	8	8	2, 3 PCLKB	2 ICLK
0008 A146h	SCI10	Smart card mode register	SCMR	8	8	2, 3 PCLKB	2 ICLK
0008 A147h	SCI10	Serial extended mode register	SEMR	8	8	2, 3 PCLKB	2 ICLK

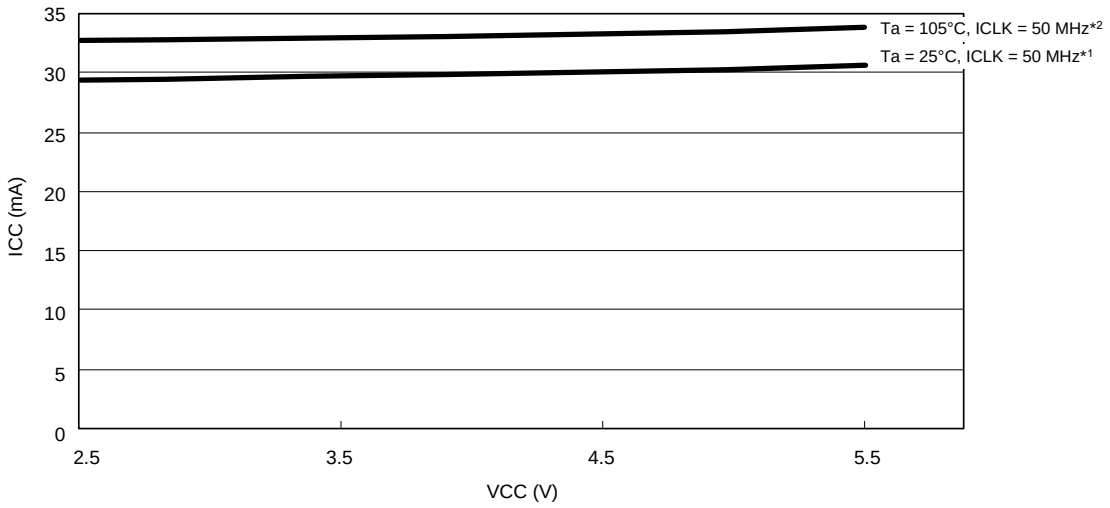
Table 4.1 List of I/O Registers (Address Order) (26 / 29)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles: ICLK ≥ PCLK	Number of Access Cycles: ICLK < PCLK
0008 C0EAh	PORTA	Drive capacity control register	DSCR	8	8	2, 3 PCLKB	2 ICLK
0008 C0EBh	PORTB	Drive capacity control register	DSCR	8	8	2, 3 PCLKB	2 ICLK
0008 C0ECh	PORTC	Drive capacity control register	DSCR	8	8	2, 3 PCLKB	2 ICLK
0008 C0EDh	PORTD	Drive capacity control register	DSCR	8	8	2, 3 PCLKB	2 ICLK
0008 C0EEh	PORTE	Drive capacity control register	DSCR	8	8	2, 3 PCLKB	2 ICLK
0008 C0F1h	PORTH	Drive capacity control register	DSCR	8	8	2, 3 PCLKB	2 ICLK
0008 C0F2h	PORTJ	Drive capacity control register	DSCR	8	8	2, 3 PCLKB	2 ICLK
0008 C0F3h	PORTK	Drive capacity control register	DSCR	8	8	2, 3 PCLKB	2 ICLK
0008 C100h	MPC	CS output enable register	PFCSE	8	8	2, 3 PCLKB	2 ICLK
0008 C104h	MPC	Address output enable register 0	PFAOE0	8	8, 16	2, 3 PCLKB	2 ICLK
0008 C105h	MPC	Address output enable register 1	PFAOE1	8	8, 16	2, 3 PCLKB	2 ICLK
0008 C106h	MPC	External bus control register 0	PFBCR0	8	8, 16	2, 3 PCLKB	2 ICLK
0008 C107h	MPC	External bus control register 1	PFBCR1	8	8, 16	2, 3 PCLKB	2 ICLK
0008 C11Fh	MPC	Write-protect register	PWPR	8	8	2, 3 PCLKB	2 ICLK
0008 C140h	MPC	P00 pin function control register	P00PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C141h	MPC	P01 pin function control register	P01PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C142h	MPC	P02 pin function control register	P02PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C143h	MPC	P03 pin function control register	P03PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C145h	MPC	P05 pin function control register	P05PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C147h	MPC	P07 pin function control register	P07PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C14Ah	MPC	P12 pin function control register	P12PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C14Bh	MPC	P13 pin function control register	P13PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C14Ch	MPC	P14 pin function control register	P14PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C14Dh	MPC	P15 pin function control register	P15PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C14Eh	MPC	P16 pin function control register	P16PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C14Fh	MPC	P17 pin function control register	P17PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C150h	MPC	P20 pin function control register	P20PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C151h	MPC	P21 pin function control register	P21PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C152h	MPC	P22 pin function control register	P22PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C153h	MPC	P23 pin function control register	P23PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C154h	MPC	P24 pin function control register	P24PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C155h	MPC	P25 pin function control register	P25PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C156h	MPC	P26 pin function control register	P26PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C157h	MPC	P27 pin function control register	P27PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C158h	MPC	P30 pin function control register	P30PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C159h	MPC	P31 pin function control register	P31PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C15Ah	MPC	P32 pin function control register	P32PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C15Bh	MPC	P33 pin function control register	P33PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C15Ch	MPC	P34 pin function control register	P34PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C160h	MPC	P40 pin function control register	P40PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C161h	MPC	P41 pin function control register	P41PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C162h	MPC	P42 pin function control register	P42PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C163h	MPC	P43 pin function control register	P43PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C164h	MPC	P44 pin function control register	P44PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C165h	MPC	P45 pin function control register	P45PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C166h	MPC	P46 pin function control register	P46PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C167h	MPC	P47 pin function control register	P47PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C168h	MPC	P50 pin function control register	P50PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C169h	MPC	P51 pin function control register	P51PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C16Ah	MPC	P52 pin function control register	P52PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C16Ch	MPC	P54 pin function control register	P54PFS	8	8	2, 3 PCLKB	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (28 / 29)

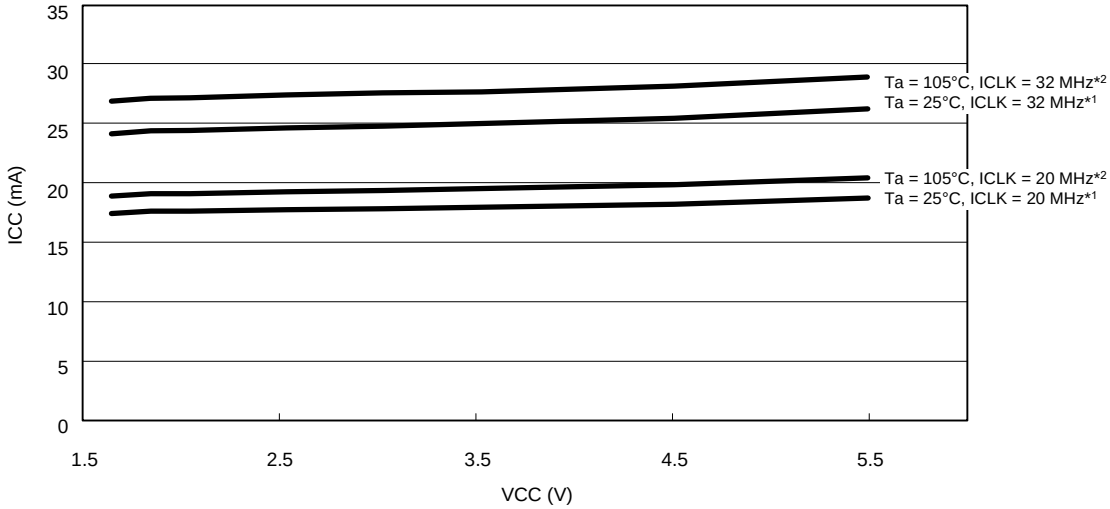
Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles: ICLK ≥ PCLK	Number of Access Cycles: ICLK < PCLK
0008 C1B0h	MPC	PE0 pin function control register	PE0PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C1B1h	MPC	PE1 pin function control register	PE1PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C1B2h	MPC	PE2 pin function control register	PE2PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C1B3h	MPC	PE3 pin function control register	PE3PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C1B4h	MPC	PE4 pin function control register	PE4PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C1B5h	MPC	PE5 pin function control register	PE5PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C1B6h	MPC	PE6 pin function control register	PE6PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C1B7h	MPC	PE7 pin function control register	PE7PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C1BDh	MPC	PF5 pin function control register	PF5PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C1C8h	MPC	PH0 pin function control register	PH0PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C1C9h	MPC	PH1 pin function control register	PH1PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C1CAh	MPC	PH2 pin function control register	PH2PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C1CBh	MPC	PH3 pin function control register	PH3PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C1D1h	MPC	PJ1 pin function control register	PJ1PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C1D3h	MPC	PJ3 pin function control register	PJ3PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C1DAh	MPC	PK2 pin function control register	PK2PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C1DBh	MPC	PK3 pin function control register	PK3PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C1DCh	MPC	PK4 pin function control register	PK4PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C1DDh	MPC	PK5 pin function control register	PK5PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C280h	SYSTEM	Deep standby control register	DPSBYCR	8	8	4, 5 PCLKB	2, 3 ICLK
0008 C282h	SYSTEM	Deep standby interrupt enable register 0	DPSIER0	8	8	4, 5 PCLKB	2, 3 ICLK
0008 C284h	SYSTEM	Deep standby interrupt enable register 2	DPSIER2	8	8	4, 5 PCLKB	2, 3 ICLK
0008 C286h	SYSTEM	Deep standby interrupt flag register 0	DPSIFR0	8	8	4, 5 PCLKB	2, 3 ICLK
0008 C288h	SYSTEM	Deep standby interrupt flag register 2	DPSIFR2	8	8	4, 5 PCLKB	2, 3 ICLK
0008 C28Ah	SYSTEM	Deep standby interrupt edge register 0	DPSIEGR0	8	8	4, 5 PCLKB	2, 3 ICLK
0008 C28Ch	SYSTEM	Deep standby interrupt edge register 2	DPSIEGR2	8	8	4, 5 PCLKB	2, 3 ICLK
0008 C28Fh	SYSTEM	Flash HOCO software standby control register	FHSSBYCR	8	8	4, 5 PCLKB	2, 3 ICLK
0008 C290h	SYSTEM	Reset status register 0	RSTSR0	8	8	4, 5 PCLKB	2, 3 ICLK
0008 C291h	SYSTEM	Reset status register 1	RSTSR1	8	8	4, 5 PCLKB	2, 3 ICLK
0008 C293h	SYSTEM	Main clock oscillator forced oscillation control register	MOFCR	8	8	4, 5 PCLKB	2, 3 ICLK
0008 C294h	SYSTEM	High-speed clock oscillator power supply control register	HOCOPCR	8	8	4, 5 PCLKB	2, 3 ICLK
0008 C295h	SYSTEM	PLL power control register	PLLPCR	8	8	4, 5 PCLKB	2, 3 ICLK
0008 C296h	FLASH	Flash write erase protection register	FWEPROR	8	8	4, 5 PCLKB	2, 3 ICLK
0008 C297h	SYSTEM	Voltage monitoring circuit/comparator A control register	LVCMPCR	8	8	4, 5 PCLKB	2, 3 ICLK
0008 C298h	SYSTEM	Voltage detection level select register	LVDLVLR	8	8	4, 5 PCLKB	2, 3 ICLK
0008 C29Ah	SYSTEM	Voltage monitoring 1 circuit/comparator A1 control register 0	LVD1CR0	8	8	4, 5 PCLKB	2, 3 ICLK
0008 C29Bh	SYSTEM	Voltage monitoring 2 circuit/comparator A2 control register 0	LVD2CR0	8	8	4, 5 PCLKB	2, 3 ICLK
0008 C2A0h to 0008 C2BFh	SYSTEM	Deep standby backup register 0 to 31	DPSBKR0 to DPSBKR31	8	8	4, 5 PCLKB	2, 3 ICLK
0008 C400h	RTC	64-Hz counter	R64CNT	8	8	2, 3 PCLKB	2 ICLK
0008 C402h	RTC	Second counter	RSECCNT	8	8	2, 3 PCLKB	2 ICLK
0008 C404h	RTC	Minute counter	RMINCNT	8	8	2, 3 PCLKB	2 ICLK
0008 C406h	RTC	Hour counter	RHRCNT	8	8	2, 3 PCLKB	2 ICLK
0008 C408h	RTC	Day-of-week counter	RWKCNT	8	8	2, 3 PCLKB	2 ICLK
0008 C40Ah	RTC	Date counter	RDAYCNT	8	8	2, 3 PCLKB	2 ICLK
0008 C40Ch	RTC	Month counter	RMONCNT	8	8	2, 3 PCLKB	2 ICLK
0008 C40Eh	RTC	Year counter	RYRCNT	16	16	2, 3 PCLKB	2 ICLK
0008 C410h	RTC	Second alarm register	RSECAR	8	8	2, 3 PCLKB	2 ICLK
0008 C412h	RTC	Minute alarm register	RMINAR	8	8	2, 3 PCLKB	2 ICLK
0008 C414h	RTC	Hour alarm register	RHRAR	8	8	2, 3 PCLKB	2 ICLK
0008 C416h	RTC	Day-of-week alarm register	RWKAR	8	8	2, 3 PCLKB	2 ICLK
0008 C418h	RTC	Date alarm register	RDAYAR	8	8	2, 3 PCLKB	2 ICLK

Note 5. Clocks are supplied to the peripheral functions. This does not include BGO operation. The clock source is HOCO and the oscillation frequency is 40 MHz. BCLK, FCLK, and PCLK are ICLK divided by 1.
Note 6. This is the increase if data is programmed to or erasing from the ROM or E2 DataFlash during program execution.
Note 7. Clock supply to the peripheral functions is stopped. This does not include BGO operation. The clock source is HOCO and the oscillation frequency is 32 MHz. BCLK, FCLK, and PCLK are set to divided by 64.
Note 8. Clocks are supplied to the peripheral functions. This does not include BGO operation. The clock source is HOCO and the oscillation frequency is 32 MHz. BCLK, FCLK, and PCLK are ICLK divided by 1.
Note 9. Clock supply to the peripheral functions is stopped. This does not include BGO operation. The clock source is the sub oscillation circuit. BCLK, FCLK, and PCLK are set to divided by 64.
Note 10. Clocks are supplied to the peripheral functions. This does not include BGO operation. The clock source is the sub oscillation circuit. BCLK, FCLK, and PCLK are ICLK divided by 1.
Note 11. Value when the main clock continues oscillating at 12.5 MHz.



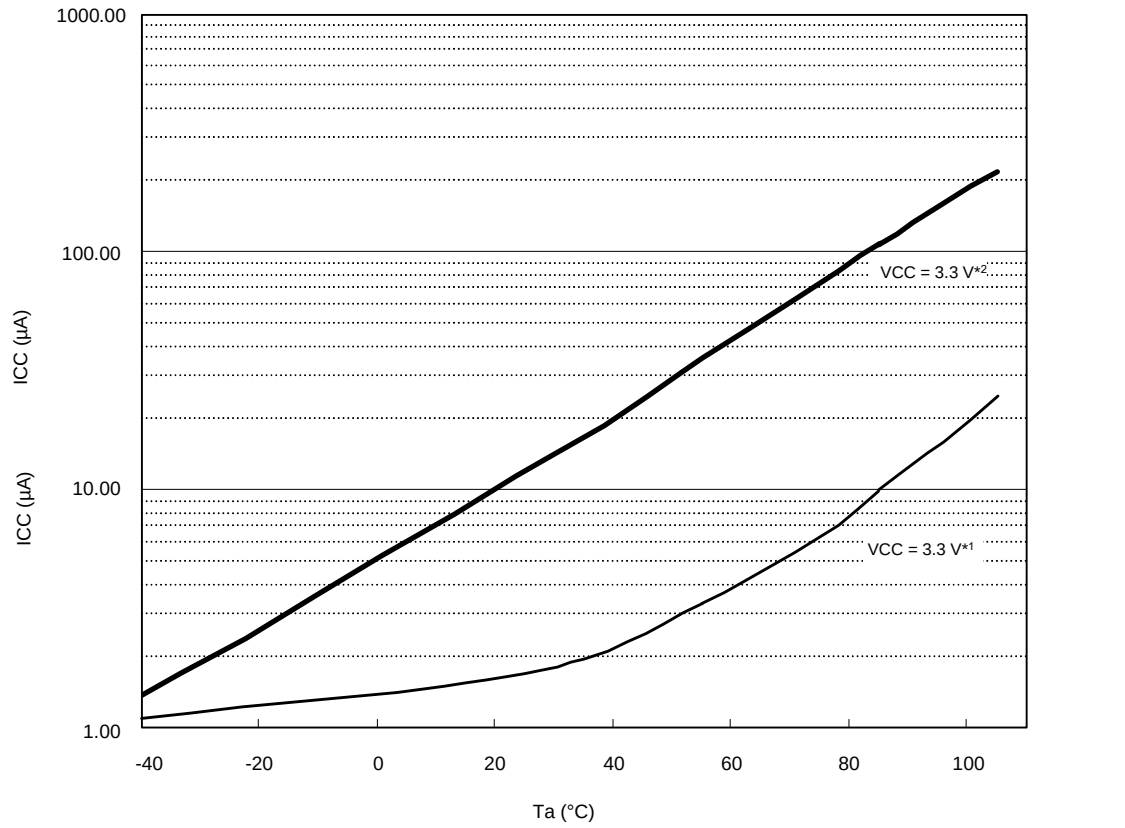
Note 1. All peripheral operation is normal. This does not include BGO operation.
Average value of the tested middle samples during product evaluation.
Note 2. All peripheral operation is maximum. This does not include BGO operation.
Average value of the tested upper-limit samples during product evaluation.

Figure 5.26 Voltage Dependency in High-Speed Operating Mode (Reference Data) for Chip Version B with 768 Kbytes/1 Mbyte of Flash Memory and 100 to 145 Pins



Note 1. All peripheral operation is normal. This does not include BGO operation.
Average value of the tested middle samples during product evaluation.
Note 2. All peripheral operation is maximum. This does not include BGO operation.
Average value of the tested upper-limit samples during product evaluation.

Figure 5.27 Voltage Dependency in Middle-Speed Operating Modes 1A and 1B (Reference Data) for Chip Version B with 768 Kbytes/1 Mbyte of Flash Memory and 100 to 145 Pins



Note 1. Average value of the tested middle samples during product evaluation.
Note 2. Average value of the tested upper-limit samples during product evaluation.

Figure 5.32 Temperature Dependency in Software Standby Mode (SOFTCUT[2:0] Bits = 110b) (Reference Data) for Chip Version B with 768 Kbytes/1 Mbyte of Flash Memory and 100 to 145 Pins

[Chip versions B and C]

Table 5.31 Output Values of Voltage (4)

Conditions: VCC = AVCC0 = 2.7 to 4.0 V, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +105°C

Item			Symbol	Min.	Max.	Unit	Test Conditions
Output low	All output pins (other than RIIC)	Normal output mode	V_{OL}	—	0.5	V	I_{OL} = 1.0 mA
		High-drive output mode		—	0.5		I_{OL} = 2.0 mA
	RIIC pins			—	0.4		I_{OL} = 3.0 mA
				—	0.6		I_{OL} = 6.0 mA
Output high	All output pins	Normal output mode	V_{OH}	VCC – 0.5	—	V	I_{OH} = –1.0 mA
		High-drive output mode		VCC – 0.5	—		I_{OH} = –2.0 mA

[Chip versions B and C]

Table 5.32 Output Values of Voltage (5)

Conditions: VCC = AVCC0 = 4.0 to 5.5 V, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +105°C

Item			Symbol	Min.	Max.	Unit	Test Conditions
Output low	All output pins (other than RIIC)	Normal output mode	V_{OL}	—	0.8	V	I_{OL} = 2.0 mA
		High-drive output mode		—	0.8		I_{OL} = 4.0 mA
	RIIC pins			—	0.4		I_{OL} = 3.0 mA
				—	0.6		I_{OL} = 6.0 mA
Output high	All output pins	Normal output mode	V_{OH}	VCC – 0.8	—	V	I_{OH} = –2.0 mA
		High-drive output mode		VCC – 0.8	—		I_{OH} = –4.0 mA

5.2.1 Standard I/O Pin Output Characteristics (1)

Figure 5.45 to Figure 5.49 show the characteristics when normal output is selected by the drive capacity control register.

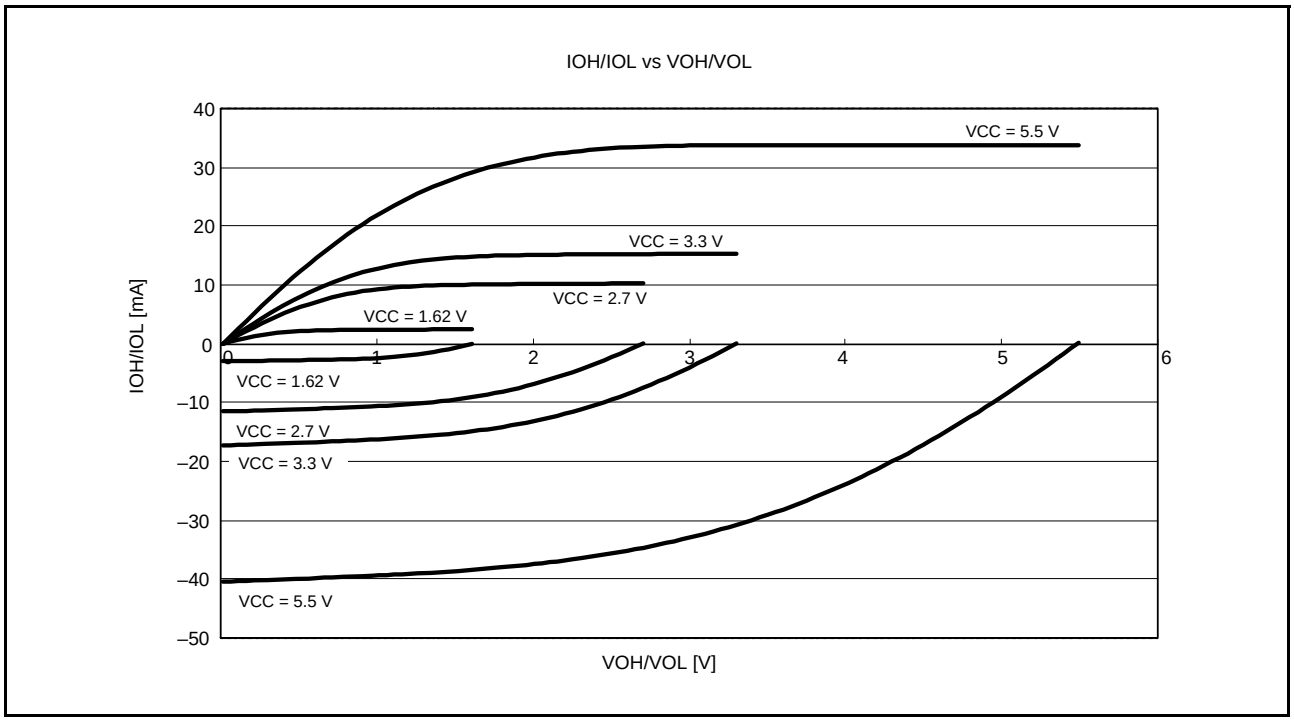


Figure 5.45 VOH/VOL and IOH/IOL Voltage Characteristics at Ta = 25°C when Normal Output is Selected (Reference Data)

5.2.2 Standard I/O Pin Output Characteristics (2)

Figure 5.50 to Figure 5.54 show the characteristics when high-drive output is selected by the drive capacity control register.

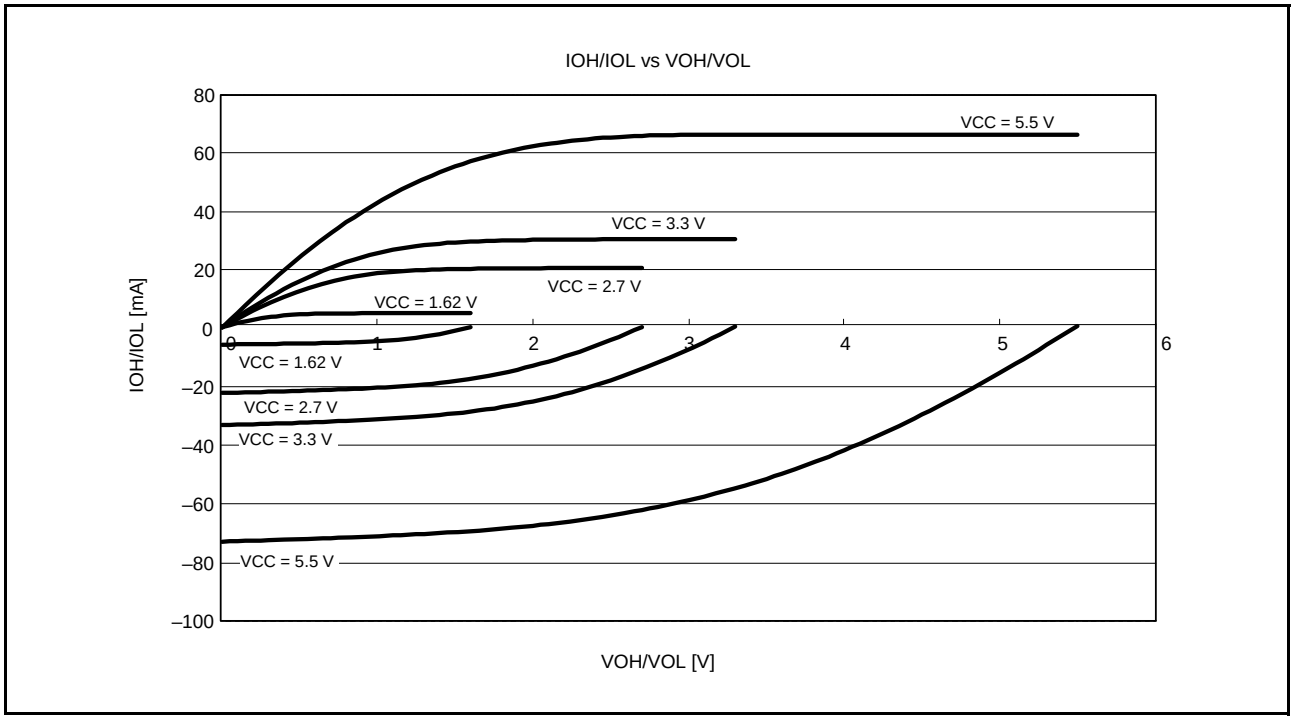


Figure 5.50 VOH/VOL and IOH/IOL Voltage Characteristics at Ta = 25°C when High-Drive Output is Selected (Reference Data)

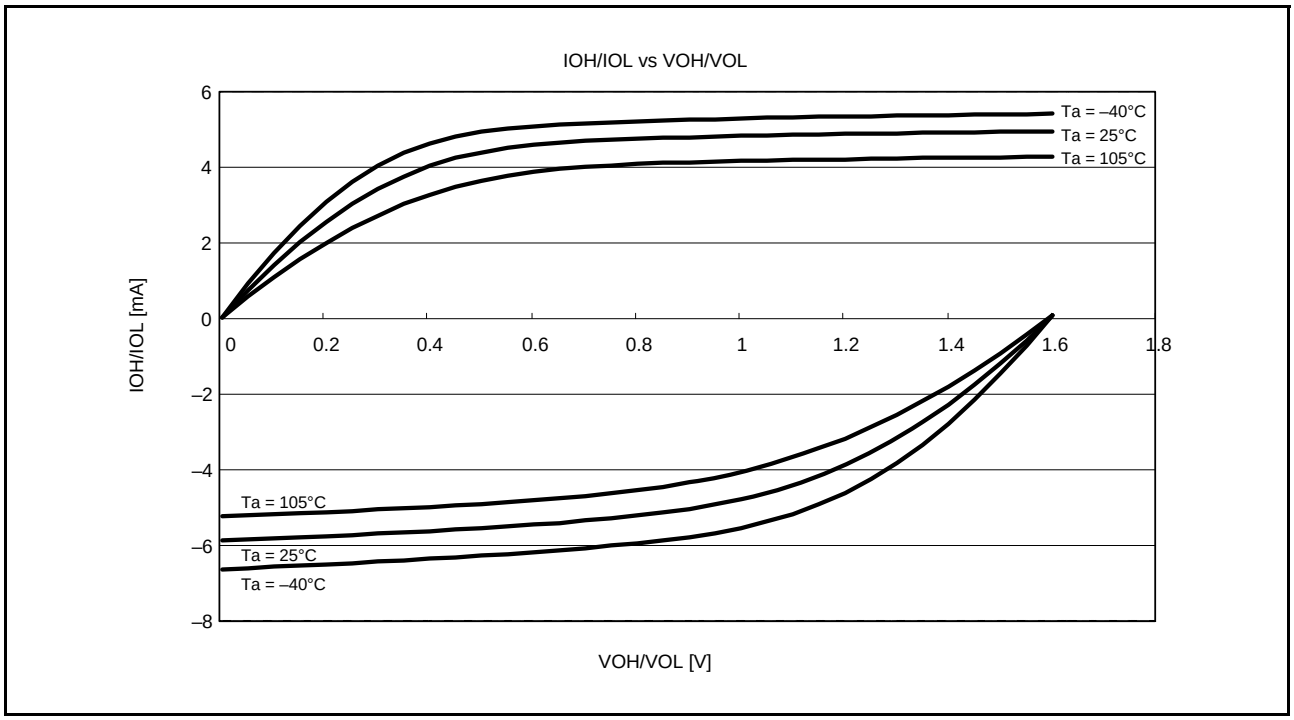


Figure 5.51 VOH/VOL and IOH/IOL Temperature Characteristics at VCC = 1.62 V when High-Drive Output is Selected (Reference Data)

Table 5.44 Clock Timing

Conditions: VCC = AVCC0 = 1.62 to 5.5 V, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
EXTAL external clock input cycle time		t_{EXcyc}	50	—	—	ns	Figure 5.60
EXTAL external clock input high pulse width		t_{EXH}	20	—	—	ns	
EXTAL external clock input low pulse width		t_{EXL}	20	—	—	ns	
EXTAL external clock rising time		t_{EXr}	—	—	5	ns	
EXTAL external clock falling time		t_{EXf}	—	—	5	ns	
EXTAL external clock input wait time*1		t_{EXWT}	1	—	—	ms	
Main clock oscillator oscillation frequency*2		f_{MAIN}	1	—	20	MHz	
Main clock oscillation stabilization time (crystal)*2		$t_{MAINOSC}$	—	3	—	ms	Figure 5.61
Main clock oscillation stabilization time (ceramic resonator)*2		$t_{MAINOSC}$	—	50		µs	
Main clock oscillation stabilization wait time (crystal)*2		$t_{MAINOSCWT}$	—	6	—	ms	
Main clock oscillation stabilization wait time (ceramic resonator)*2		$t_{MAINOSCWT}$	—	100		µs	
LOCO clock cycle time		t_{cyc}	7.27	8	8.89	µs	
LOCO clock oscillation frequency*6		f_{LOCO}	112.5	125	137.5	kHz	
LOCO clock oscillation stabilization wait time		t_{LOCOWT}	—	—	20	µs	Figure 5.62
HOCO clock oscillation frequency*7		f_{HOCO}	31.680	32	32.320	MHz	Ta = 0 to 50°C
			36.495	36.864	37.233		
			39.600	40	40.400		
			49.500	50	50.500		
			31.520	32	32.480		Ta = -40 to 105°C
			36.311	36.864	37.417		
			39.400	40	40.600		
			49.250	50	50.750		
HOCO clock oscillation stabilization time 1		t_{HOCO1}	—	—	300	µs	Figure 5.63
HOCO clock oscillation stabilization time 2		t_{HOCO2}	—	—	175	µs	Figure 5.64
HOCO clock oscillation stabilization wait time		t_{HOCOWT}	—	—	350	µs	Figure 5.64
HOCO clock power supply stabilization time		t_{HOCOP}	—	—	350	µs	Figure 5.65
PLL input frequency		f_{PLLIN}	4	—	12.5	MHz	
PLL circuit oscillation frequency		f_{PLL}	50	—	100	MHz	
PLL clock oscillation stabilization time	PLL operation started after main clock oscillation has settled	t_{PLL1}	—	—	500	µs	Figure 5.66
PLL clock oscillation stabilization wait time		t_{PLLWT1}	1.5	—	—	ms	
PLL clock oscillation stabilization time*4	PLL operation started before main clock oscillation has settled	t_{PLL2}	—	3.5*3	—	ms	Figure 5.67
PLL clock oscillation stabilization wait time*4		t_{PLLWT2}	—	7	—	ms	
PLL clock power supply stabilization time (for chip version B only)		t_{PLLPW}	—	—	30	µs	Figure 5.68
Sub-clock oscillator oscillation frequency		f_{SUB}	—	32.768	—	kHz	
Sub-clock oscillation stabilization time*5		t_{SUBOSC}	2	—	—	s	Figure 5.69
Sub-clock oscillation stabilization wait time*5		$t_{SUBOSCWT}$	4	—	—	s	

Note 1. The time interval from the time P36 and P37 are configured for input and the main clock oscillator stopping bit (MOSCCR.MOSTP) is set to 0 (operating) until the clock becomes available.

5.3.4 Control Signal Timing

Table 5.48 Control Signal Timing

Conditions: VCC = AVCC0 = 1.62 to 5.5 V, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +105°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
NMI pulse width	t_{NMIW}	200	—	—	ns	$t_{c(PCLKB)}$ × 2 ≤ 200 ns, Figure 5.74
		$t_{c(PCLKB)}$ × 2	—	—	ns	$t_{c(PCLKB)}$ × 2 > 200 ns, Figure 5.74
IRQ pulse width	t_{IRQW}	200	—	—	ns	$t_{c(PCLKB)}$ × 2 ≤ 200 ns, Figure 5.75
		$t_{c(PCLKB)}$ × 2	—	—	ns	$t_{c(PCLKB)}$ × 2 > 200 ns, Figure 5.75

Note: • 200 ns minimum in deep software standby and software standby modes.

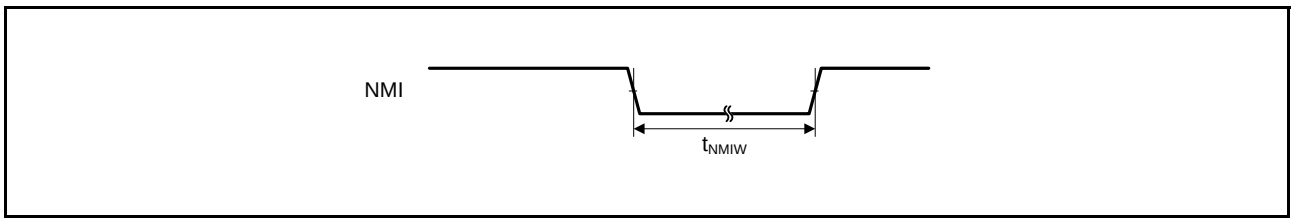


Figure 5.74 NMI Interrupt Input Timing

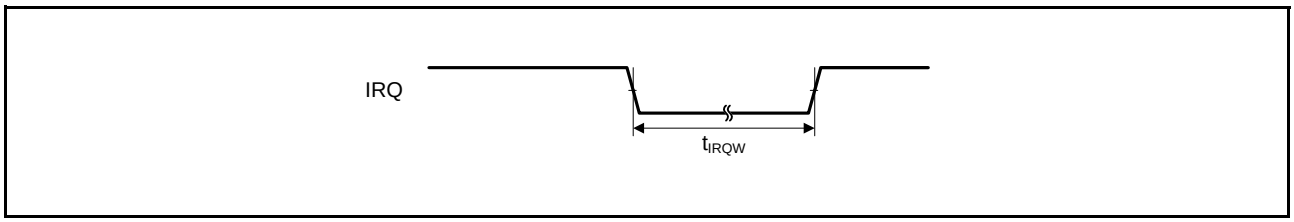


Figure 5.75 IRQ Interrupt Input Timing

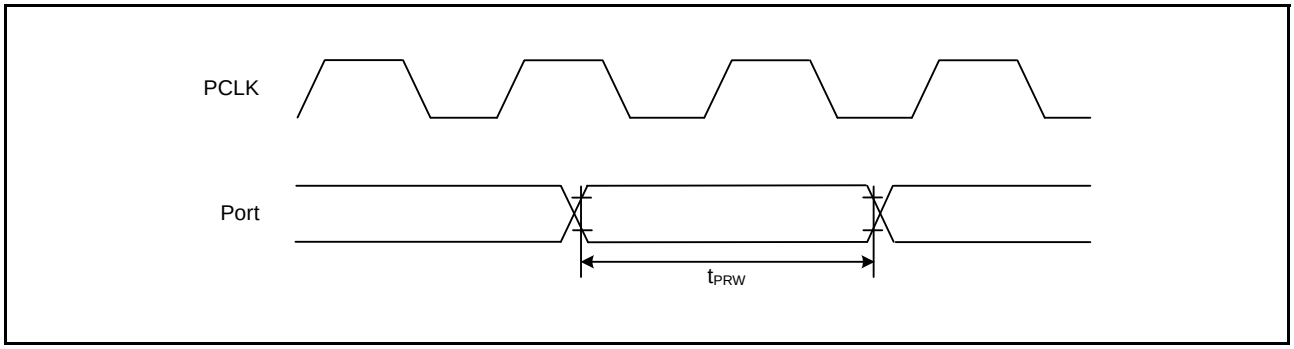


Figure 5.83 I/O Port Input Timing

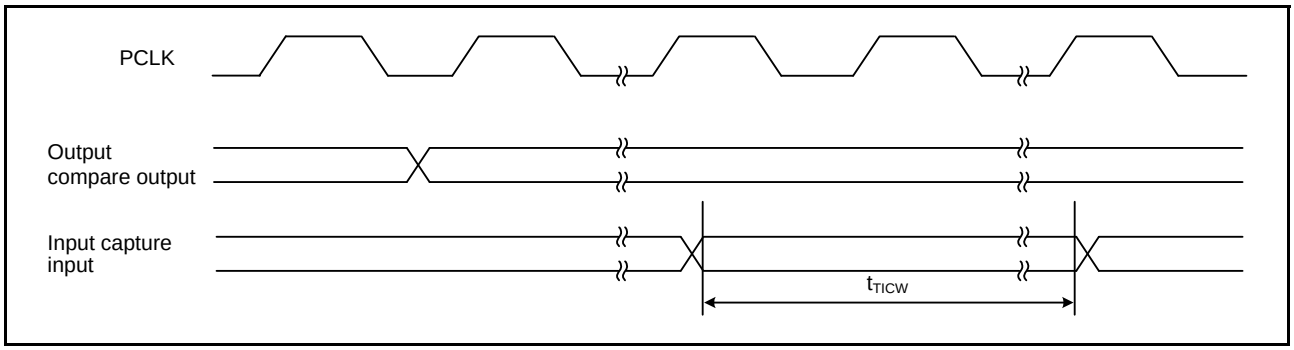


Figure 5.84 MTU/TPU Input/Output Timing

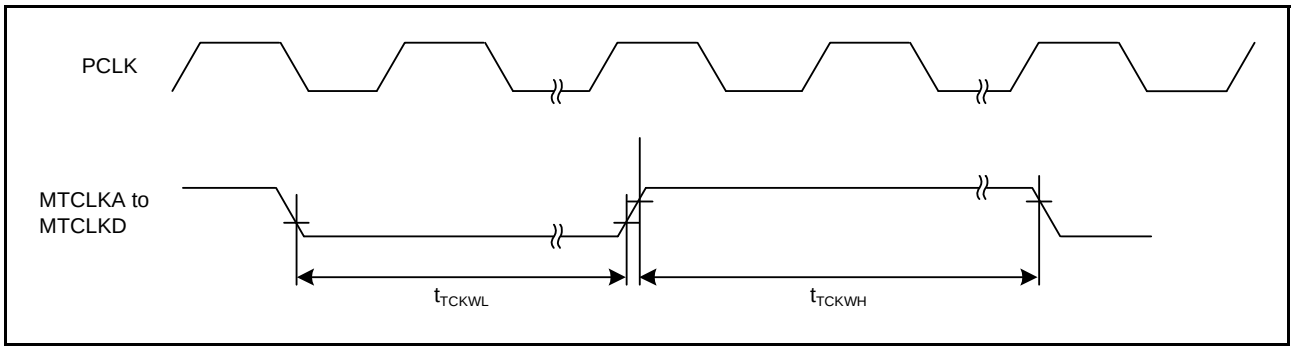


Figure 5.85 MTU/TPU Clock Input Timing

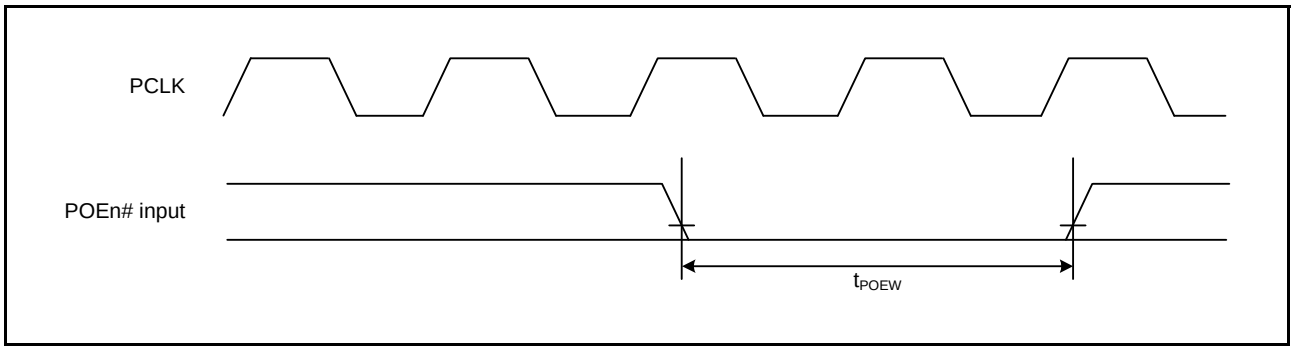


Figure 5.86 POE# Input Timing

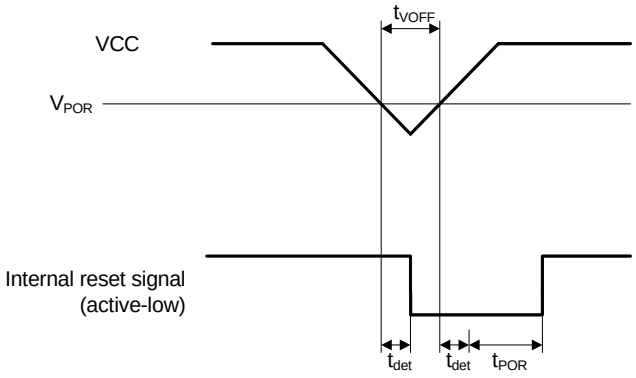
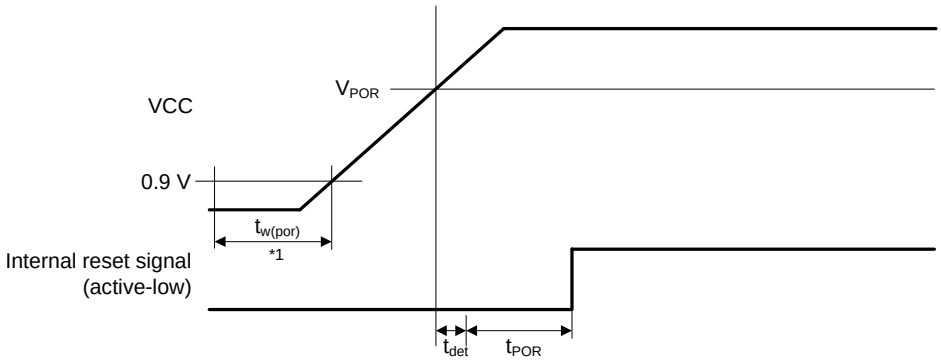


Figure 5.103 Voltage Detection Reset Timing



Note 1. $t_{w(por)}$ is the time required for a power-on reset to be enabled while the external power VCC is being held below the valid voltage (0.9 V).
When VCC turns on, maintain $t_{w(por)}$ for 1 ms or more.

Figure 5.104 Power-on Reset Timing

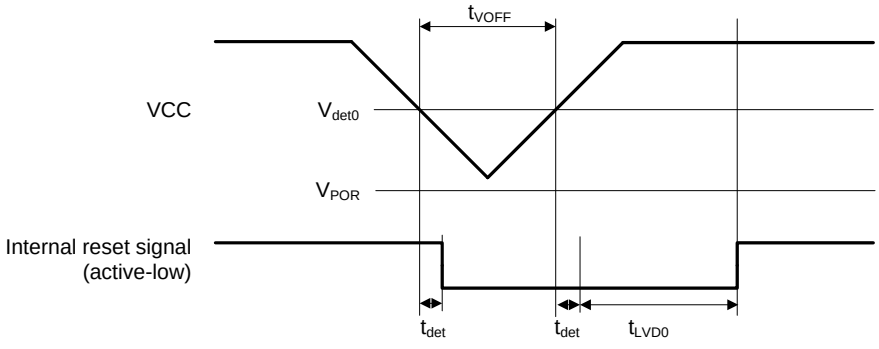
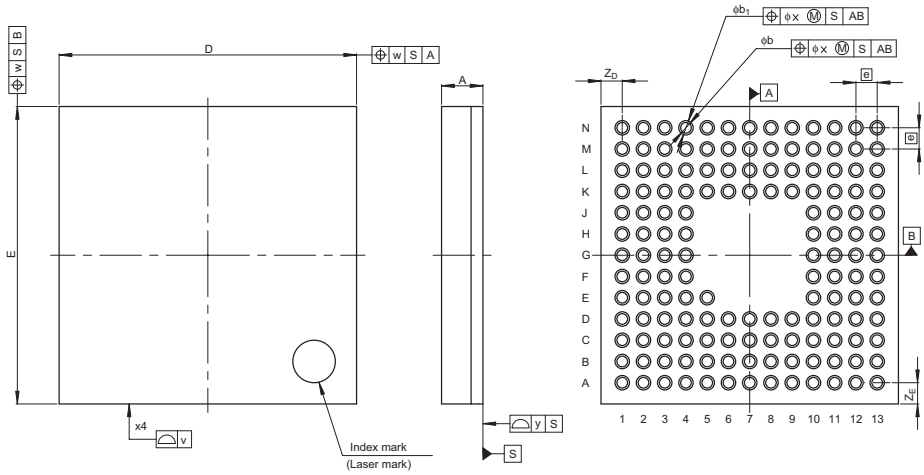


Figure 5.105 Voltage Detection Circuit Timing (V_{det0})

Appendix 1. Package Dimensions

Information on the latest version of the package dimensions or mountings has been displayed in “Packages” on Renesas Electronics Corporation website.

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-TFLGA145-7x7-0.50	PTLG0145KA-A	145F0G	0.1g



Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	7.0	—
E	—	7.0	—
v	—	—	0.15
w	—	—	0.20
A	—	—	1.05
e	—	0.5	—
b	0.21	0.25	0.29
b_1	0.29	0.34	0.39
x	—	—	0.08
y	—	—	0.08
Z_D	—	0.5	—
Z_E	—	0.5	—

Figure A 145-Pin TFLGA (PTLG0145KA-A)

Rev.	Date	Description	
		Page	Summary
1.30	Jan 22, 2013	11	Table 1.6 List of Products Chip Version C: D Version (Ta = -40 to +85°C), Table 1.7 List of Products Chip Version C: G Version (Ta = -40 to +105°C), changed
		12	Figure 1.1 How to Read the Product Part No., Memory Capacity, and Package Type, changed
		13	Figure 1.2 Block Diagram, changed
		14 to 17	Table 1.8 Pin Functions, changed
		18	Figure 1.3 Pin Assignments of the 145-Pin TFLGA (Upper Perspective View), added
		19	Figure 1.4 Pin Assignments of the 144-Pin LQFP, added
		25 to 28	Table 1.9 List of Pins and Pin Functions (145-Pin TFLGA), changed
		29 to 32	Table 1.10 List of Pins and Pin Functions (144-Pin LQFP), changed
		3. Address Space	
		48	Figure 3.1 Memory Map in Each Operating Mode, changed
		4. I/O Registers	
		52 to 81	Table 4.1 List of I/O Registers (Address Order, changed
		5. Electrical Characteristics	
		83	Table 5.2 DC Characteristics (1), Table 5.3 DC Characteristics (2), changed
		84 to 122	Table 5.6 DC Characteristics (5) to Table 5.20 DC Characteristics (19), changed Figure 5.1 Voltage Dependency in High-Speed .... for Chip Version A to Figure 5.34 Temperature Dependency in .... and 100 to 145 pins, changed
		158	Table 5.55 Timing of On-Chip Peripheral Modules (1), changed
		159	[512 Kbytes or less of flash memory and 48 to 100 pins] Table 5.56 Timing of On-Chip Peripheral Modules (2), added
		160, 161	[768 Kbytes/1 Mbyte of flash memory or 145/145 pins] Table 5.57 Timing of On-Chip Peripheral Modules (3), added
		162	Table 5.58 Timing of On-Chip Peripheral Modules (4), changed
		165	Figure 5.75 MTU/TPU Input/Output Timing, Figure 5.76 MTU/TPU Clock Input Timing, changed
		166	Figure 5.79 SCK Clock Input Timing, Figure 5.80 SCI Input/Output Timing: Clock Synchronous Mode, changed
		167	Figure 5.82 RSPI Clock Timing and Simple SPI Clock Timing, changed
		168	Figure 5.83 RSPI Timing (Master, CPHA = 0) .... and Simple SPI Timing (Master, CKPH = 1), Figure 5.84 RSPI Timing (Master, CPHA = 0) (Bit Rate: PCLKB Set to Divided by 2), changed
		169	Figure 5.85 RSPI Timing (Master, CPHA = 1) .... and Simple SPI Timing (Master, CKPH = 0), Figure 5.86 RSPI Timing (Master, CPHA = 1) (Bit Rate: PCLKB Set to Divided by 2), changed
		170	Figure 5.87 RSPI Timing (Slave, CPHA = 0) and Simple SPI Timing (Slave, CKPH = 1), Figure 5.88 RSPI Timing (Slave, CPHA = 1) and Simple SPI Timing (Slave, CKPH = 0), changed
		173	Table 5.64 A/D Conversion Characteristics (2), changed
		175	Figure 5.91 Illustration of A/D Converter Characteristic Terms, Absolute accuracy, changed
		184	Table 5.74 ROM (Flash Memory for Code Storage) Characteristics (1), changed
		189	Table 5.80 E2 DataFlash Characteristics (1), Table 5.81 E2 DataFlash Characteristics (2), changed
		Appendix 1. Package Dimensions	
		195	Figure A 145-Pin TFLGA (PTLG0145KA-A), added
		196	Figure B 144-Pin LQFP (PLQP0144KA-A), added
1.40	Feb 19, 2013	1. Overview	
		2 to 6	Table 1.1 Outline of Specifications, changed Note 2, added
		9	Table 1.4 List of Products Chip Version B: D Version (Ta = -40 to +85°C), changed
		10	Table 1.5 List of Products Chip Version B: G Version (Ta = -40 to +105°C), changed Note, added
		11	Table 1.6 List of Products Chip Version C: D Version (Ta = -40 to +85°C): Note 1, Table 1.7 List of Products Chip Version C: G Version (Ta = -40 to +105°C): Note 1 deleted, Note added
		12	Figure 1.1 How to Read the Product Part No., Memory Capacity, and Package Type, changed
		4. I/O Registers	
		58	Table 5.1 List of I/O Registers (Address Order), changed
		5. Electrical Characteristics	
		83	Table 5.4 DC Characteristics (3), changed
		88	Table 5.8 DC Characteristics (7), changed