Renesas Electronics America Inc - R5F52106BDFB#30 Datasheet

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

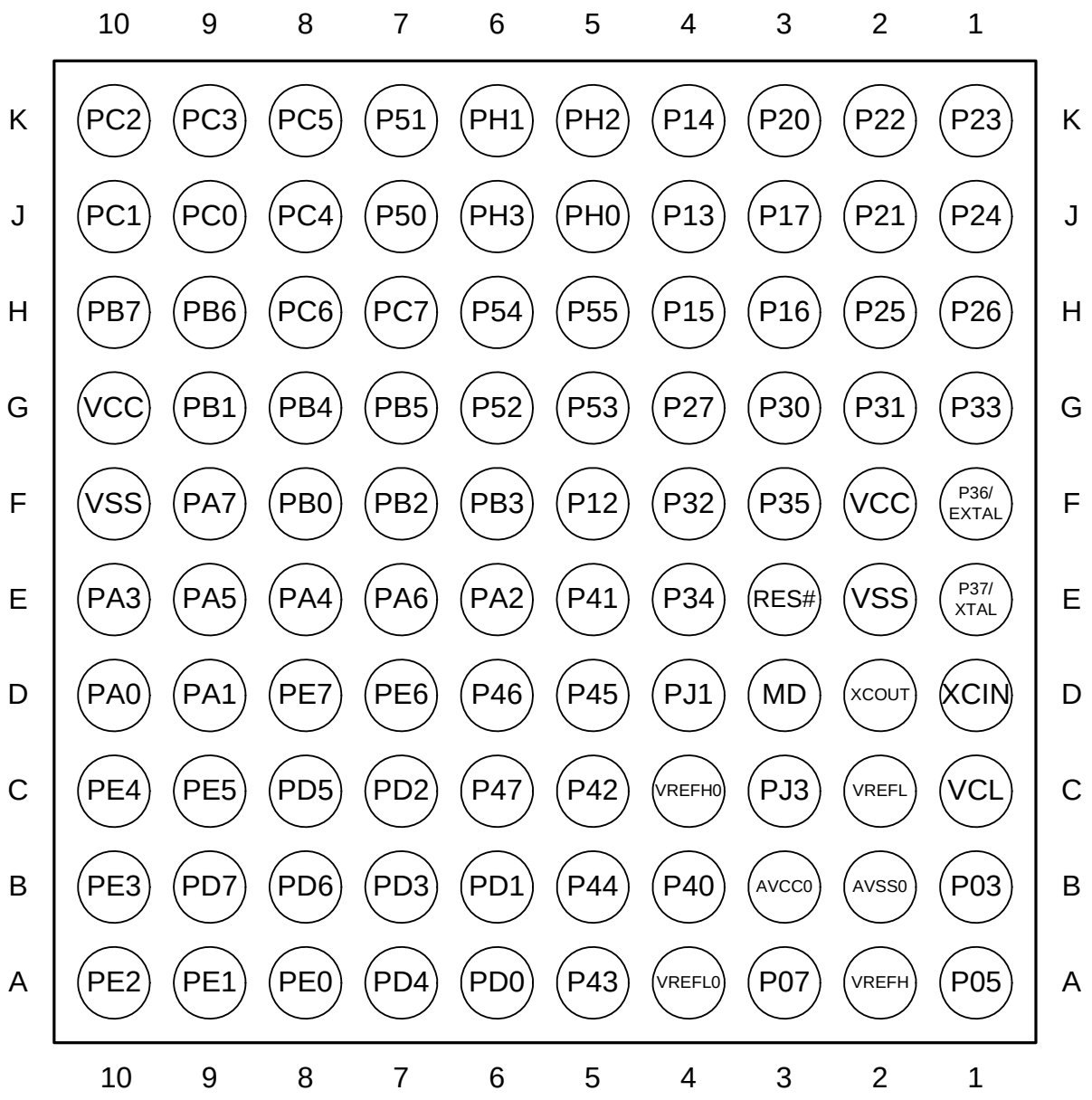
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	EBI/EMI, I²C, SCI, SPI
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	122
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.62V ~ 5.5V
Data Converters	A/D 16x12b; D/A 2x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LFQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f52106bdfb-30

Table 1.8 Pin Functions (4 / 4)

Classifications	Pin Name	I/O	Description
Analog power supply	AVCC0	Input	Analog voltage supply pin for the 12-bit A/D converter. Connect this pin to VCC if the 12-bit A/D converter is not to be used.
	AVSS0	Input	Analog ground pin for the 12-bit A/D converter. Connect this pin to VSS if the 12-bit A/D converter is not to be used.
	VREFH0	Input	Analog reference voltage supply pin for the 12-bit A/D converter. Connect this pin to VCC if the 12-bit A/D converter is not to be used.
	VREFL0	Input	Analog reference ground pin for the 12-bit A/D converter. Connect this pin to VSS if the 12-bit A/D converter is not to be used.
	VREFH	Input	Analog voltage supply pin for the D/A converter. Connect this pin to VCC if the D/A converter is not to be used.
	VREFL	Input	Analog ground pin for the D/A converter. Connect this pin to VSS if the D/A converter is not to be used.
I/O ports	P00 to P03, P05, P07	I/O	6-bit input/output pins.
	P12 to P17	I/O	6-bit input/output pins.
	P20 to P27	I/O	8-bit input/output pins.
	P30 to P37	I/O	8-bit input/output pins. (P35 input pin)
	P40 to P47	I/O	8-bit input/output pins.
	P50 to P56	I/O	7-bit input/output pins.
	P60 to P67	I/O	8-bit input/output pins.
	P70 to P77	I/O	8-bit input/output pins.
	P80 to P83, P86, P87	I/O	6-bit input/output pins.
	P90 to P93	I/O	4-bit input/output pins.
	PA0 to PA7	I/O	8-bit input/output pins.
	PB0 to PB7	I/O	8-bit input/output pins.
	PC0 to PC7	I/O	8-bit input/output pins.
	PD0 to PD7	I/O	8-bit input/output pins.
	PE0 to PE7	I/O	8-bit input/output pins.
	PF5	I/O	1-bit input/output pin.
	PH0 to PH3	I/O	4-bit input/output pins.
	PJ1, PJ3, PJ5	I/O	3-bit input/output pins.
	PK2 to PK5	I/O	4-bit input/output pins.
	PL0, PL1	I/O	2-bit input/output pins.

RX210 Group
PTLG0100JA-A
(100-pin TFLGA)
(Upper perspective view)



Note: • This figure indicates the power supply pins and I/O port pins. For the pin configuration, see the table “List of Pins and Pin Functions (100-Pin TFLGA)”.
Note: • For the position of A1 pin in the package, see “Package Dimensions”.

Figure 1.5 Pin Assignments of the 100-Pin TFLGA (Upper Perspective View)

Table 1.10 List of Pins and Pin Functions (144-Pin LQFP) (2 / 4)

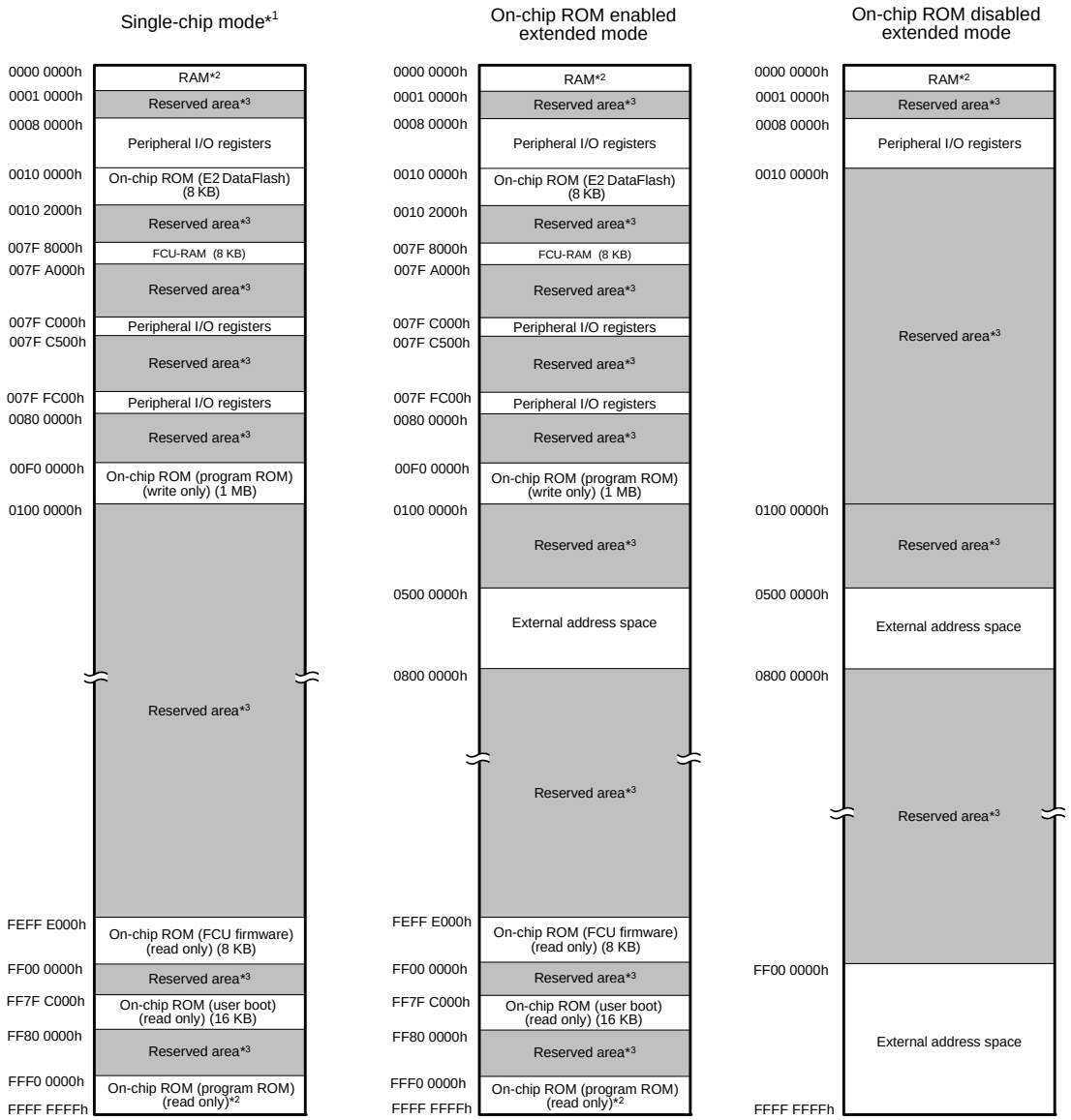
Pin No.	Power Supply, Clock, System Control	I/O Port	External Bus	Timers (MTU, TMR, POE)	Communications (SCIc, SCId, RSPI, RIIC)	Others
40		P16		MTIOC3C/MTIOC3D/ TMO2/TIOCB1/TCLKC	TXD1/SMOSI1/SSDA1/ MOSIA/SCL-DS/RXD3/ SMISO3/SSCL3	IRQ6/RTCOUT/ ADTRG0#
41		P86		TIOCA0		
42		P15		MTIOC0B/MTCLKB/ TMCI2/TIOCB2/TCLKB	RXD1/SMISO1/SSCL1/ SCK3	IRQ5
43		P14		MTIOC3A/MTCLKA/ TMRI2/TIOCB5/TCLKA	CTS1#/RTS1#/SS1#	IRQ4
44		P13		MTIOC0B/TMO3/ TIOCA5	SDA/TXD2/SMOSI2/ SSDA2	IRQ3
45		P12		TMCI1	SCL/RXD2/SMISO2/ SSCL2	IRQ2
46		PH3		TMCI0		
47		PH2		TMRI0		IRQ1
48		PH1		TMO0		IRQ0
49		PH0				CACREF
50		P56		MTIOC3C/TIOCA1		
51		P55	WAIT#	MTIOC4D/TMO3		
52		P54	ALE	MTIOC4B/TMCI1	CTS2#/RTS2#/SS2#	
53	BCLK	P53				
54		P52	RD#		RXD2/SMISO2/SSCL2	
55		P51	WR1#/BC1#/WAIT#		SCK2	
56		P50	WR0#/WR#		TXD2/SMOSI2/SSDA2	
57	VSS					
58		P83		MTIOC4C	CTS10#/RTS10#	
59	VCC					
60		PC7	A23/CS0#	MTIOC3A/TMO2/ MTCLKB	TXD8/SMOSI8/SSDA8/ MISOA	CACREF
61		PC6	A22/CS1#	MTIOC3C/MTCLKA/ TMCI2	RXD8/SMISO8/SSCL8/ MOSIA	
62		PC5	A21/CS2#/WAIT#	MTIOC3B/MTCLKD/ TMRI2	SCK8/RSPCKA	
63		P82		MTIOC4A	TXD10/SMOSI10/SSDA10	
64		P81		MTIOC3D	RXD10/SMISO10/SSCL10	
65		P80		MTIOC3B	SCK10	
66		PC4	A20/CS3#	MTIOC3D/MTCLKC/ TMCI1/POE0#	SCK5/CTS8#/RTS8#/ SS8#/SSLA0	
67		PC3	A19	MTIOC4D/TCLKB	TXD5/SMOSI5/SSDA5	
68		P77			TXD11/SMOSI11/SSDA11	
69		P76			RXD11/SMISO11/SSCL11	
70		PC2	A18	MTIOC4B/TCLKA	RXD5/SMISO5/SSCL5/ ISSLA3	
71		P75			SCK11	
72		P74			CTS11#/RTS11#/SS11#	
73		PC1	A17	MTIOC3A/TCLKD	SCK5/SSLA2	
74		PL1				
75		PC0	A16	MTIOC3C/TCLKC	CTS5#/RTS5#/SS5#/ SSLA1	
76		PL0				
77		P73				
78		PB7	A15	MTIOC3B/TIOCB5	TXD9/SMOSI9/SSDA9	
79		PB6	A14	MTIOC3D/TIOCA5	RXD9/SMISO9/SSCL9	
80		PB5	A13	MTIOC2A/MTIOC1B/ TMRI1/POE1#/TIOCB4	SCK9	

Table 1.10 List of Pins and Pin Functions (144-Pin LQFP) (3 / 4)

Pin No.	Power Supply, Clock, System Control	I/O Port	External Bus	Timers (MTU, TMR, POE)	Communications (SCIc, SCId, RSPI, RIIC)	Others
81		PB4	A12	TIOCA4	CTS9#/RTS9#/SS9#	
82		PB3	A11	MTIOC0A/MTIOC4A/ TMO0/POE3#/ TIOCD3/TCLKD	SCK4/SCK6	
83		PB2	A10	TIOCC3/TCLKC	CTS4#/RTS4#/SS4#/ CTS6#/RTS6#/SS6#	
84		PB1	A9	MTIOC0C/MTIOC4C/ TMCI0/TIOCB3	TXD4/SMOSI4/SSDA4/ TXD6/SMOSI6/SSDA6	IRQ4-DS
85		P72				
86		P71				
87		PB0	A8	MTIC5W/TIOCA3	RXD4/SMISO4/SSCL4/ RXD6/SMISO6/SSCL6/ RSPCKA	
88		PA7	A7	TIOCB2	MISOA	
89		PA6	A6	MTIC5V/MTCLKB/ TMCI3/POE2#/TIOCA2	CTS5#/RTS5#/SS5#/ MOSIA/	
90		PA5	A5	TIOCB1	RSPCKA	
91	VCC					
92		PA4	A4	MTIC5U/MTCLKA/ TMRI0/TIOCA1	TXD5/SMOSI5/SSDA5/ SSLA0	IRQ5-DS/CVREFB1
93	VSS					
94		PA3	A3	MTIOC0D/MTCLKD/ TIOCD0/TCLKB	RXD5/SMISO5/SSCL5	IRQ6-DS/CMPB1
95		PA2	A2		RXD5/SMISO5/SSCL5/ SSLA3	
96		PA1	A1	MTIOC0B/MTCLKC/ TIOCB0	SCK5/SSLA2	CVREFA
97		PA0	A0/BC0#	MTIOC4A/TIOCA0	SSLA1	CACREF
98		P67				
99		P66				
100		P65				
101		PE7	D15[A15/D15]			IRQ7/AN015
102		PE6	D14[A14/D14]		CTS4#/RTS4#/SS4#	IRQ6/AN014
103		PK5			TXD4/SMOSI4/SSDA4	
104		P70			SCK4	
105		PK4			RXD4/SMISO4/SSCL4	
106		PE5	D13[A13/D13]	MTIOC4C/MTIOC2B		IRQ5/AN013
107		PE4	D12[A12/D12]	MTIOC4D/MTIOC1A		AN012/CMPA2
108		PE3	D11[A11/D11]	MTIOC4B/POE8#	CTS12#/RTS12#/SS12#	AN011/CMPA1
109		PE2	D10[A10/D10]	MTIOC4A	RXD12/RXDX12/ SMISO12/SSCL12	IRQ7-DS/AN010/ CVREFB0
110		PE1	D9[A9/D9]	MTIOC4C	TXD12/TXDX12/SIOX12/ SMOSI12/SSDA12	AN009/CMPB0
111		PE0	D8[A8/D8]		SCK12	AN008
112		P64				
113		P63				
114		P62				
115		P61			CTS9#/RTS9#/SS9#	
116		PK3			RXD9/SMISO9/SSCL9	
117		P60			SCK9	
118		PK2			TXD9/SMOSI9/SSDA9	
119		PD7	D7[A7/D7]	MTIC5U/POE0#		IRQ7
120		PD6	D6[A6/D6]	MTIC5V/POE1#		IRQ6
121		PD5	D5[A5/D5]	MTIC5W/POE2#		IRQ5

Table 1.16 List of Pins and Pin Functions (64-Pin LQFP) (1 / 2)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (MTU, TMR, POE)	Communication (SCIc, SCId, RSPI, RIIC)	Others
1		P03			DA0
2	VCL				
3	MD				FINED
4	XCIN				
5	XCOUT				
6	RES#				
7	XTAL	P37			
8	VSS				
9	EXTAL	P36			
10	VCC				
11		P35			NMI
12		P32	MTIOC0C/TMO3	TXD6/SMOSI6/SSDA6	IRQ2-DS/RTCOUT/ RTCIC2
13		P31	MTIOC4D/TMCI2	CTS1#/RTS1#/SS1#	IRQ1-DS/RTCIC1
14		P30	MTIOC4B/TMRI3/POE8#	RXD1/SMISO1/SSCL1	IRQ0-DS/RTCIC0
15		P27	MTIOC2B/TMCI3	SCK1	
16		P26	MTIOC2A/TMO1	TXD1/SMOSI1/SSDA1	
17		P17	MTIOC3A/MTIOC3B/TMO1/ POE8#	SCK1/MISOA/SDA-DS	IRQ7
18		P16	MTIOC3C/MTIOC3D/TMO2	TXD1/SMOSI1/SSDA1/MOSIA/ SCL-DS	IRQ6/RTCOUT/ ADTRG0#
19		P15	MTIOC0B/MTCLKB/TMCI2	RXD1/SMISO1/SSCL1	IRQ5
20		P14	MTIOC3A/MTCLKA/TMRI2	CTS1#/RTS1#/SS1#	IRQ4
21		PH3	TMCI0		
22		PH2	TMRI0		IRQ1
23		PH1	TMO0		IRQ0
24		PH0			CACREF
25		P55	MTIOC4D/TMO3		
26		P54	MTIOC4B/TMCI1		
27		PC7	MTIOC3A/TMO2/MTCLKB	TXD8/SMOSI8/SSDA8/MISOA	CACREF
28		PC6	MTIOC3C/MTCLKA/TMCI2	RXD8/SMISO8/SSCL8/MOSIA	
29		PC5	MTIOC3B/MTCLKD/TMRI2	SCK8/RSPCKA	
30		PC4	MTIOC3D/MTCLKC/TMCI1/ POE0#	SCK5/CTS8#/RTS8#/SS8#/ SSLA0	
31		PC3	MTIOC4D	TXD5/SMOSI5/SSDA5	
32		PC2	MTIOC4B	RXD5/SMISO5/SSCL5/SSLA3	
33		PB7	MTIOC3B	TXD9/SMOSI9/SSDA9	
34		PB6	MTIOC3D	RXD9/SMISO9/SSCL9	
35		PB5	MTIOC2A/MTIOC1B/TMRI1/ POE1#	SCK9	
36		PB3	MTIOC0A/MTIOC4A/TMO0/ POE3#	SCK6	
37		PB1	MTIOC0C/MTIOC4C/TMCI0	TXD6/SMOSI6/SSDA6	IRQ4-DS
38	VCC				
39		PB0	MTIC5W	RXD6/SMISO6/SSCL6/RSPCKA	
40	VSS				
41		PA6	MTIC5V/MTCLKB/TMCI3/ POE2#	CTS5#/RTS5#/SS5#/MOSIA	
42		PA4	MTIC5U/MTCLKA/TMRI0	TXD5/SMOSI5/SSDA5/SSLA0	IRQ5-DS/CVREFB1
43		PA3	MTIOC0D/MTCLKD	RXD5/SMISO5/SSCL5	IRQ6-DS/CMPB1



Note 1. The address space in boot mode and user boot mode is the same as the address space in single-chip mode.
Note 2. The capacity of ROM/RAM differs depending on the products.

ROM (bytes)		RAM (bytes)	
Capacity	**Address**	**Capacity**	**Address**
1 M	FFF0 0000h to FFFF FFFFh	96 K	0000 0000h to 0001 7FFFh
768 K	FFF4 0000h to FFFF FFFFh		
512 K	FFF8 0000h to FFFF FFFFh	64 K	0000 0000h to 0000 FFFFh
384 K	FFFA 0000h to FFFF FFFFh		
256 K	FFFC 0000h to FFFF FFFFh	32 K	0000 0000h to 0000 7FFFh
128 K	FFFE 0000h to FFFF FFFFh	20 K	0000 0000h to 0000 4FFFh
96 K	FFFE 8000h to FFFF FFFFh	16 K	0000 0000h to 0000 3FFFh
64 K	FFFF 0000h to FFFF FFFFh	12 K	0000 0000h to 0000 2FFFh

Note:•See Table 1.3 to Table 1.7 List of Products, for the product type name.

Note 3. Reserved areas should not be accessed.

Figure 3.1 Memory Map in Each Operating Mode

Table 4.1 List of I/O Registers (Address Order) (23 / 29)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles: ICLK ≥ PCLK	Number of Access Cycles: ICLK < PCLK
0008 C042h	PORT2	Port input data register	PIDR	8	8	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing	3 ICLK cycles when reading, 2 ICLK cycles when writing
0008 C043h	PORT3	Port input data register	PIDR	8	8	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing	3 ICLK cycles when reading, 2 ICLK cycles when writing
0008 C044h	PORT4	Port input data register	PIDR	8	8	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing	3 ICLK cycles when reading, 2 ICLK cycles when writing
0008 C045h	PORT5	Port input data register	PIDR	8	8	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing	3 ICLK cycles when reading, 2 ICLK cycles when writing
0008 C046h	PORT6	Port input data register	PIDR	8	8	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing	3 ICLK cycles when reading, 2 ICLK cycles when writing
0008 C047h	PORT7	Port input data register	PIDR	8	8	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing	3 ICLK cycles when reading, 2 ICLK cycles when writing
0008 C048h	PORT8	Port input data register	PIDR	8	8	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing	3 ICLK cycles when reading, 2 ICLK cycles when writing
0008 C049h	PORT9	Port input data register	PIDR	8	8	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing	3 ICLK cycles when reading, 2 ICLK cycles when writing
0008 C04Ah	PORTA	Port input data register	PIDR	8	8	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing	3 ICLK cycles when reading, 2 ICLK cycles when writing
0008 C04Bh	PORTB	Port input data register	PIDR	8	8	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing	3 ICLK cycles when reading, 2 ICLK cycles when writing

Table 4.1 List of I/O Registers (Address Order) (29 / 29)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles: ICLK ≥ PCLK	Number of Access Cycles: ICLK < PCLK
0008 C41Ah	RTC	Month alarm register	RMONAR	8	8	2, 3 PCLKB	2 ICLK
0008 C41Ch	RTC	Year alarm register	RYRAR	16	16	2, 3 PCLKB	2 ICLK
0008 C41Eh	RTC	Year alarm enable register	RYRAREN	8	8	2, 3 PCLKB	2 ICLK
0008 C422h	RTC	RTC control register 1	RCR1	8	8	2, 3 PCLKB	2 ICLK
0008 C424h	RTC	RTC control register 2	RCR2	8	8	2, 3 PCLKB	2 ICLK
0008 C426h	RTC	RTC control register 3	RCR3	8	8	2, 3 PCLKB	2 ICLK
0008 C42Eh	RTC	Time error adjustment register	RADJ	8	8	2, 3 PCLKB	2 ICLK
0008 C440h	RTC	Time capture control register 0	RTCCR0	8	8	2, 3 PCLKB	2 ICLK
0008 C442h	RTC	Time capture control register 1	RTCCR1	8	8	2, 3 PCLKB	2 ICLK
0008 C444h	RTC	Time capture control register 2	RTCCR2	8	8	2, 3 PCLKB	2 ICLK
0008 C452h	RTC	Second capture register 0	RSECCP0	8	8	2, 3 PCLKB	2 ICLK
0008 C454h	RTC	Minute capture register 0	RMINCP0	8	8	2, 3 PCLKB	2 ICLK
0008 C456h	RTC	Hour capture register 0	RHRCP0	8	8	2, 3 PCLKB	2 ICLK
0008 C45Ah	RTC	Date capture register 0/	RDAYCP0	8	8	2, 3 PCLKB	2 ICLK
0008 C45Ch	RTC	Month capture register 0	RMONCP0	8	8	2, 3 PCLKB	2 ICLK
0008 C462h	RTC	Second capture register 1	RSECCP1	8	8	2, 3 PCLKB	2 ICLK
0008 C464h	RTC	Minute capture register 1	RMINCP1	8	8	2, 3 PCLKB	2 ICLK
0008 C466h	RTC	Hour capture register 1	RHRCP1	8	8	2, 3 PCLKB	2 ICLK
0008 C46Ah	RTC	Date capture register 1	RDAYCP1	8	8	2, 3 PCLKB	2 ICLK
0008 C46Ch	RTC	Month capture register 1	RMONCP1	8	8	2, 3 PCLKB	2 ICLK
0008 C472h	RTC	Second capture register 2	RSECCP2	8	8	2, 3 PCLKB	2 ICLK
0008 C474h	RTC	Minute capture register 2	RMINCP2	8	8	2, 3 PCLKB	2 ICLK
0008 C476h	RTC	Hour capture register 2	RHRCP2	8	8	2, 3 PCLKB	2 ICLK
0008 C47Ah	RTC	Date capture register 2	RDAYCP2	8	8	2, 3 PCLKB	2 ICLK
0008 C47Ch	RTC	Month capture register 2	RMONCP2	8	8	2, 3 PCLKB	2 ICLK
0008 C500h	TEMPS	Temperature sensor control register	TSCR	8	8	2, 3 PCLKB	2 ICLK
0008 C580h	CMPB	Comparator B control register 1	CPBCNT1	8	8	2, 3 PCLKB	2 ICLK
0008 C582h	CMPB	Comparator B flag register	CPBFLG	8	8	2, 3 PCLKB	2 ICLK
0008 C583h	CMPB	Comparator B interrupt control register	CPBINT	8	8	2, 3 PCLKB	2 ICLK
0008 C584h	CMPB	Comparator B filter select register	CPBF	8	8	2, 3 PCLKB	2 ICLK
007F C402h	FLASH	Flash mode register	FMODR	8	8	2, 3 FCLK	2 ICLK
007F C410h	FLASH	Flash access status register	FASTAT	8	8	2, 3 FCLK	2 ICLK
007F C411h	FLASH	Flash access error interrupt enable register	FAEINT	8	8	2, 3 FCLK	2 ICLK
007F C412h	FLASH	Flash ready interrupt enable register	FRDYIE	8	8	2, 3 FCLK	2 ICLK
007F C440h	FLASH	E2 DataFlash read enable register 0	DFLRE0	16	16	2, 3 FCLK	2 ICLK
007F C450h	FLASH	E2 DataFlash programming/erasure enable register 0	DFLWE0	16	16	2, 3 FCLK	2 ICLK
007F C454h	FLASH	FCU RAM enable register	FCURAME	16	16	2, 3 FCLK	2 ICLK
007F FFB0h	FLASH	Flash status register 0	FSTATR0	8	8	2, 3 FCLK	2 ICLK
007F FFB1h	FLASH	Flash status register 1	FSTATR1	8	8	2, 3 FCLK	2 ICLK
007F FFB2h	FLASH	Flash P/E mode entry register	FENTRYR	16	16	2, 3 FCLK	2 ICLK
007F FFB4h	FLASH	Flash protection register	FPROTR	16	16	2, 3 FCLK	2 ICLK
007F FFB6h	FLASH	Flash reset register	FRESETR	16	16	2, 3 FCLK	2 ICLK
007F FFBAh	FLASH	FCU command register	FCMDR	16	16	2, 3 FCLK	2 ICLK
007F FFC8h	FLASH	FCU processing switching register	FCPSR	16	16	2, 3 FCLK	2 ICLK
007F FFCAh	FLASH	E2 DataFlash blank check control register	DFLBCCNT	16	16	2, 3 FCLK	2 ICLK
007F FFCCh	FLASH	Flash P/E status register	FPESTAT	16	16	2, 3 FCLK	2 ICLK
007F FFCEh	FLASH	E2 DataFlash blank check status register	DFLBCSTAT	16	16	2, 3 FCLK	2 ICLK
007F FFE8h	FLASH	Peripheral clock notification register	PCKAR	16	16	2, 3 FCLK	2 ICLK

Note 1. Odd addresses cannot be accessed in 16-bit units. When accessing a register in 16-bit units, access the address of the TMR0 or TMR2 register.
Note 2. Odd addresses cannot be accessed in 16-bit units. When accessing a register in 16-bit units, access the address of the TMOCNTL register.

5.2 DC Characteristics

Table 5.2 DC Characteristics (1)

Conditions: VCC = AVCC0 = 2.7 to 5.5 V, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Schmitt trigger input voltage	RIIC input pin (except for SMBus, 5 V tolerant)	V_{IH}	VCC × 0.7	—	5.8	V	
	Ports 12, 13, 16, and 17 (5 V tolerant)		VCC × 0.8	—	5.8		
	Ports 0, 14, 15, 2 to 9, A to L, and RES#		VCC × 0.8	—	VCC + 0.3		
	RIIC input pin (except for SMBus)	V_{IL}	–0.3	—	VCC × 0.3		
	Other than RIIC input pin		–0.3	—	VCC × 0.2		
	RIIC input pin (except for SMBus)	ΔV_T	VCC × 0.05	—	—		
	Other than RIIC input pin		VCC × 0.1	—	—		
Input level voltage (except for Schmitt trigger input pins)	MD pin	V_{IH}	VCC × 0.9	—	VCC + 0.3	V	
	EXTAL, WAIT#		VCC × 0.8	—	VCC + 0.3		
	D0 to D15		VCC × 0.7	—	VCC + 0.3		
	RIIC input pin (SMBus)		2.1	—	VCC + 0.3		
	MD pin	V_{IL}	–0.3	—	VCC × 0.1		
	EXTAL, WAIT#		–0.3	—	VCC × 0.2		
	D0 to D15		–0.3	—	VCC × 0.3		
	RIIC input pin (SMBus)		–0.3	—	0.8		

Table 5.3 DC Characteristics (2)

Conditions: VCC = AVCC0 = 1.62 to 2.7 V, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +105°C

Item			Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Schmitt trigger input voltage	Ports 12, 13, 16, and 17 (5 V tolerant)		V_{IH}	VCC × 0.8	—	5.8	V	
	Ports 0, 14, 15, 2 to 9, A to L, and RES#			VCC × 0.8	—	VCC + 0.3		
	All input pins		V_{IL}	–0.3	—	VCC × 0.2		
	Ports 0 to 9, A to L	VCC ≥ 2.2V	ΔV_T	VCC × 0.05	—	—		
		VCC < 2.2V		VCC × 0.01				
	RES#			VCC × 0.1				
Input level voltage (except for Schmitt trigger input pins)	MD pin		V_{IH}	VCC × 0.9	—	VCC + 0.3	V	
	EXTAL, WAIT#			VCC × 0.8	—	VCC + 0.3		
	D0 to D15			VCC × 0.7	—	VCC + 0.3		
	MD pin		V_{IL}	–0.3	—	VCC × 0.1		
	EXTAL, WAIT#			–0.3	—	VCC × 0.2		
	D0 to D15			–0.3	—	VCC × 0.3		

Table 5.4 DC Characteristics (3)

Conditions: VCC = AVCC0 = 1.62 to 5.5 V, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Input leakage current	RES#, MD pin, P35/NMI	$\lvert I_{in} \rvert$	—	—	1.0	µA	V_{in} = 0 V, VCC
Three-state leakage current (off-state)	Port 4	$\lvert I_{TSI} \rvert$	—	—	1.0	µA	V_{in} = 0 V, VCC
	Other pins except for ports for 5 V tolerant and port 4		—	—	0.2		
	Ports for 5 V tolerant		—	—	1.0		V_{in} = 0 V, 5.8 V
Input capacitance	All input pins (except for ports 12, 13, 16, 17, 4, A1, A3, A4, and E)	C_{in}	—	—	15	pF	V_{in} = 0 V, f = 1 MHz, T_a = 25°C
	Ports 12, 13, 16, 17, 4, A1, A3, A4, and E		—	—	30		

Table 5.5 DC Characteristics (4)

Conditions: VCC = AVCC0 = 1.62 to 5.5 V, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +105°C

Item		Symbol	VCC						Unit	Test Conditions
			1.62 to 2.7 V		2.7 to 4.0 V		4.0 to 5.5 V			
			Min.	Max.	Min.	Max.	Min.	Max.		
Input pull-up MOS current	All ports (except for port 35)	I_p	–150	–5	–200	–10	–400	–50	µA	V_{in} = 0 V

[Chip version A]

Table 5.6 DC Characteristics (5)

Conditions: VCC = AVCC0 = 2.7 to 5.5 V, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +105°C

Item					Symbol	Typ.	Max.	Unit	Test Conditions
Supply current*1	High-speed operating mode	Normal operating mode	No peripheral operation*2	ICLK = 50 MHz	I_{CC}	10	—	mA	
			All peripheral operation: Normal*3	ICLK = 50 MHz		31.5	—		
			All peripheral operation: Max.*3	ICLK = 50 MHz		—	55		
		Sleep mode	No peripheral operation	ICLK = 50 MHz		7.5	—		
			All peripheral operation: Normal	ICLK = 50 MHz		17.5	—		
		All-module clock stop mode		ICLK = 50 MHz		6.7	—		
		Increase during BGO operation*4				25	—		

Note 1. Supply current values do not include output charge/discharge current from all pins. The values apply when internal pull-up MOSs are in the off state.

Note 2. Clock supply to the peripheral functions is stopped. This does not include BGO operation. The clock source is PLL and the VCO oscillation frequency is 100 MHz. BCLK, FCLK, and PCLK are set to divided by 64.

Note 3. Clocks are supplied to the peripheral functions. This does not include BGO operation. The clock source is PLL and the VCO oscillation frequency is 100 MHz. BCLK, FCLK, and PCLK are ICLK divided by 2.

Note 4. This is the increase if data is programmed to or erasing from the ROM or E2 DataFlash during program execution.

[Chip version A]

Table 5.7 DC Characteristics (6)

Conditions: VCC = AVCC0 = 1.62 to 5.5 V, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +105°C

Item					Symbol	Typ.	Max.	Unit	Test Conditions
Supply current*1	Middle-speed operating modes 1A and 1B	Normal operating mode	No peripheral operation	ICLK = 32 MHz*2	I_{CC}	7.0	—	mA	
				ICLK = 20 MHz*3		6.0	—		
			All peripheral operation: Normal	ICLK = 32 MHz*4		26	—		
				ICLK = 20 MHz*5		18.5	—		
			All peripheral operation: Max.	ICLK = 32 MHz*4		—	40		
				ICLK = 20 MHz*5		—	30		
		Sleep mode	No peripheral operation	ICLK = 32 MHz		5.0	—		
				ICLK = 20 MHz		4.6	—		
			All peripheral operation: Normal	ICLK = 32 MHz		15.5	—		
				ICLK = 20 MHz		12	—		
		All-module clock stop mode		ICLK = 32 MHz		4.5	—		
				ICLK = 20 MHz		4.3	—		
		Increase during BGO operation*6	Middle-speed operating mode 1A			25	—		
			Middle-speed operating mode 1B			20	—		
	Low-speed operating mode 1	Normal operating mode	No peripheral operation*7	ICLK = 1 MHz		0.68	—		
			All peripheral operation: Normal*8	ICLK = 1 MHz		2.4	—		
			All peripheral operation: Max.*8	ICLK = 1 MHz		—	7		
		Sleep mode	No peripheral operation	ICLK = 1 MHz		0.6	—		
			All peripheral operation: Normal	ICLK = 1 MHz		2	—		
		All-module clock stop mode				0.58	—		
	Low-speed operating mode 2	Normal operating mode	No peripheral operation*9	ICLK = 32 kHz		0.024	—		
			All peripheral operation: Normal*10	ICLK = 32 kHz		0.05	—		
			All peripheral operation: Max.*10	ICLK = 32 kHz		—	3*11		
		Sleep mode	No peripheral operation	ICLK = 32 kHz		0.02	—		
			All peripheral operation: Normal	ICLK = 32 kHz		0.04	—		
		All-module clock stop mode				0.018	—		

Note 1. Supply current values do not include output charge/discharge current from all pins. The values apply when internal pull-up MOSs are in the off state.

Note 2. Clock supply to the peripheral functions is stopped. This does not include BGO operation. The clock source is PLL and the VCO oscillation frequency is 64 MHz. BCLK, FCLK, and PCLK are set to divided by 64.

Note 3. Clock supply to the peripheral functions is stopped. This does not include BGO operation. The clock source is HOCO and the oscillation frequency is 40 MHz. BCLK, FCLK, and PCLK are set to divided by 64.

Note 4. Clocks are supplied to the peripheral functions. This does not include BGO operation. The clock source is PLL and the VCO oscillation frequency is 64 MHz. BCLK, FCLK, and PCLK are ICLK divided by 1.

[Chip version C]

Table 5.10 DC Characteristics (9)

Conditions: VCC = AVCC0 = 1.62 to 5.5 V, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +105°C

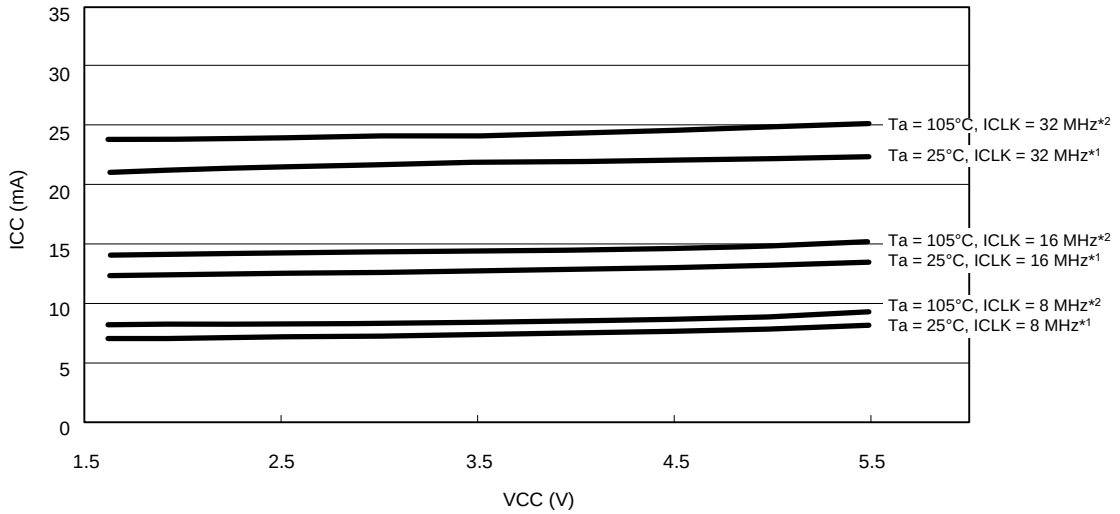
Item					Symbol	Typ.	Max.	Unit	Test Conditions
Supply current*1	Middle-speed operating modes 1A and 1B	Normal operating mode	No peripheral operation	ICLK = 32 MHz*2	I_{CC}	7.0	—	mA	
				ICLK = 20 MHz*3		6.0	—		
			All peripheral operation: Normal	ICLK = 32 MHz*4		26	—		
				ICLK = 20 MHz*5		18.5	—		
			All peripheral operation: Max.	ICLK = 32 MHz*4		—	40		
				ICLK = 20 MHz*5		—	30		
		Sleep mode	No peripheral operation	ICLK = 32 MHz		5.0	—		
				ICLK = 20 MHz		4.6	—		
			All peripheral operation: Normal	ICLK = 32 MHz		15.5	—		
				ICLK = 20 MHz		12	—		
		All-module clock stop mode		ICLK = 32 MHz		4.5	—		
				ICLK = 20 MHz		4.5	—		
		Increase during BGO operation*6	Middle-speed operating mode 1A			25	—		
			Middle-speed operating mode 1B			20	—		
	Low-speed operating mode 1	Normal operating mode	No peripheral operation*7	ICLK = 1 MHz		0.68	—		
			All peripheral operation: Normal*8	ICLK = 1 MHz		2.4	—		
			All peripheral operation: Max. *8	ICLK = 1 MHz		—	7		
		Sleep mode	No peripheral operation	ICLK = 1 MHz		0.6	—		
			All peripheral operation: Normal	ICLK = 1 MHz		2	—		
		All-module clock stop mode				0.58	—		
	Low-speed operating mode 2	Normal operating mode	No peripheral operation*9	ICLK = 32 kHz		0.024	—		
			All peripheral operation: Normal*10	ICLK = 32 kHz		0.05	—		
			All peripheral operation: Max. *10	ICLK = 32 kHz		—	3*11		
		Sleep mode	No peripheral operation	ICLK = 32 kHz		0.02	—		
			All peripheral operation: Normal	ICLK = 32 kHz		0.04	—		
		All-module clock stop mode				0.018	—		

Note 1. Supply current values do not include output charge/discharge current from all pins. The values apply when internal pull-up MOSs are in the off state.

Note 2. Clock supply to the peripheral functions is stopped. This does not include BGO operation. The clock source is PLL and the VCO oscillation frequency is 64 MHz. BCLK, FCLK, and PCLK are set to divided by 64.

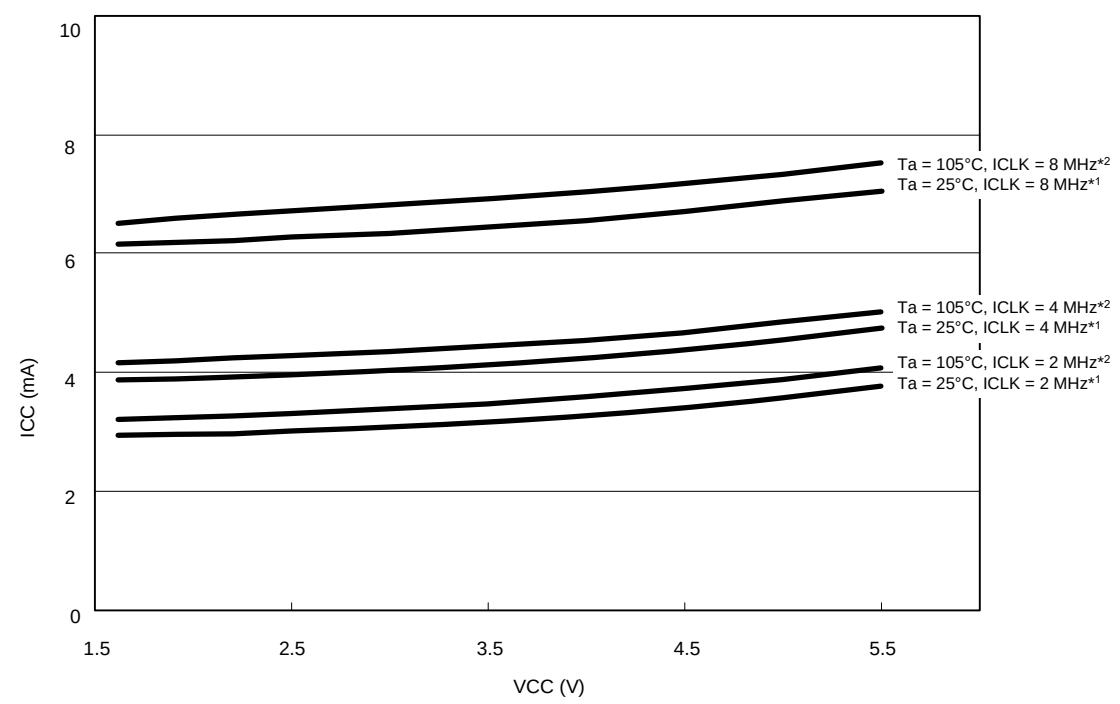
Note 3. Clock supply to the peripheral functions is stopped. This does not include BGO operation. The clock source is HOCO and the oscillation frequency is 40 MHz. BCLK, FCLK, and PCLK are set to divided by 64.

Note 4. Clocks are supplied to the peripheral functions. This does not include BGO operation. The clock source is PLL and the VCO oscillation frequency is 64 MHz. BCLK, FCLK, and PCLK are ICLK divided by 1.



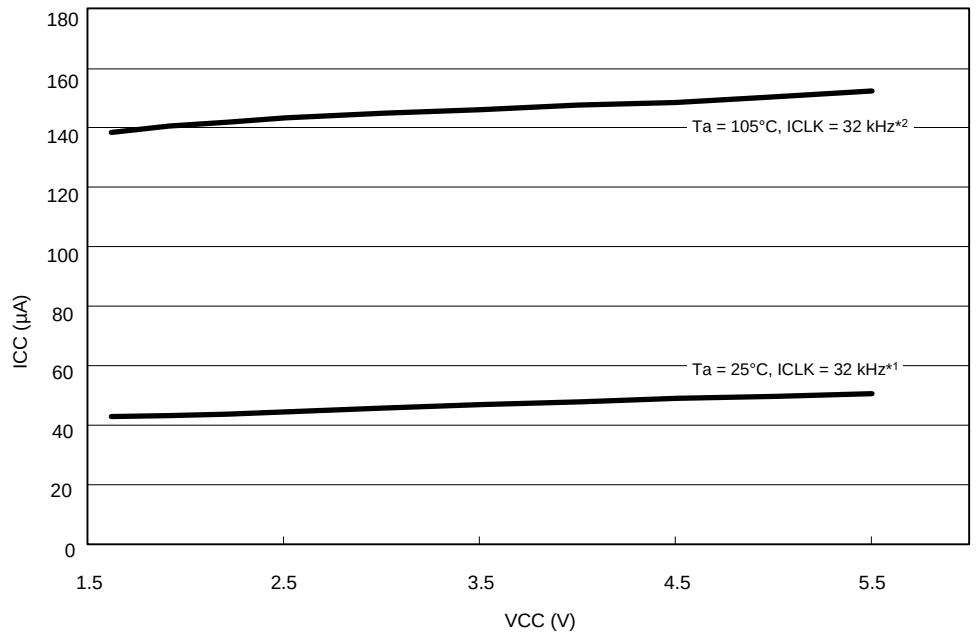
Note 1. All peripheral operation is normal. This does not include BGO operation.
Average value of the tested middle samples during product evaluation
Note 2. All peripheral operation is maximum. This does not include BGO operation.
Average value of the tested upper-limit samples during product evaluation.

Figure 5.37 Voltage Dependency in Middle-Speed Operating Modes 2A and 2B (Reference Data) for Chip Version B with 512 Kbytes or Less of Flash Memory and 144 and 145 Pins



Note 1. All peripheral operation is normal.
Average value of the tested middle samples during product evaluation.
Note 2. All peripheral operation is maximum.
Average value of the tested upper-limit samples during product evaluation.

Figure 5.38 Voltage Dependency in Low-Speed Operating Mode 1 (Reference Data) for Chip Version B with 512 Kbytes or Less of Flash Memory and 144 and 145 Pins



Note 1. All peripheral operation is normal.
Average value of the tested middle samples during product evaluation.
Note 2. All peripheral operation is maximum.
Average value of the tested upper-limit samples during product evaluation.

Figure 5.39 Voltage Dependency in Low-Speed Operating Mode 2 (Reference Data) for Chip Version B with 512 Kbytes or Less of Flash Memory and 144 and 145 Pins

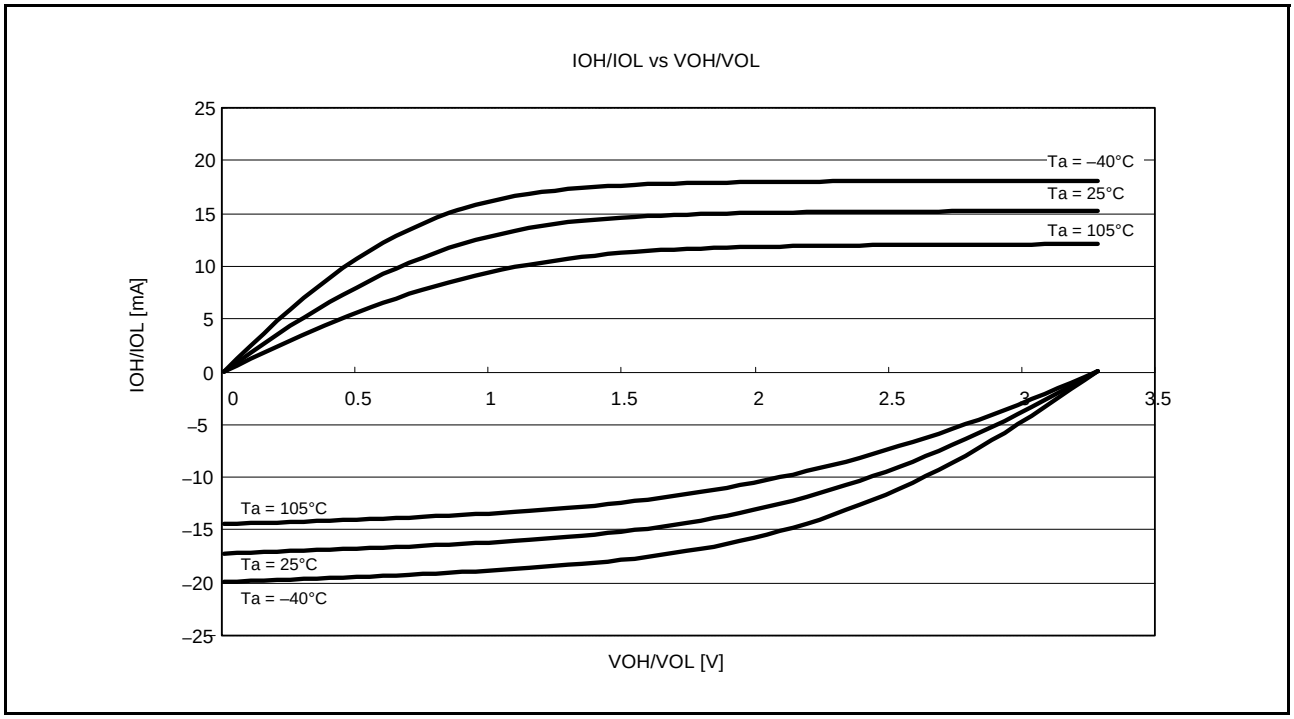


Figure 5.48 VOH/VOL and IOH/IOL Temperature Characteristics at VCC = 3.3 V when Normal Output is Selected (Reference Data)

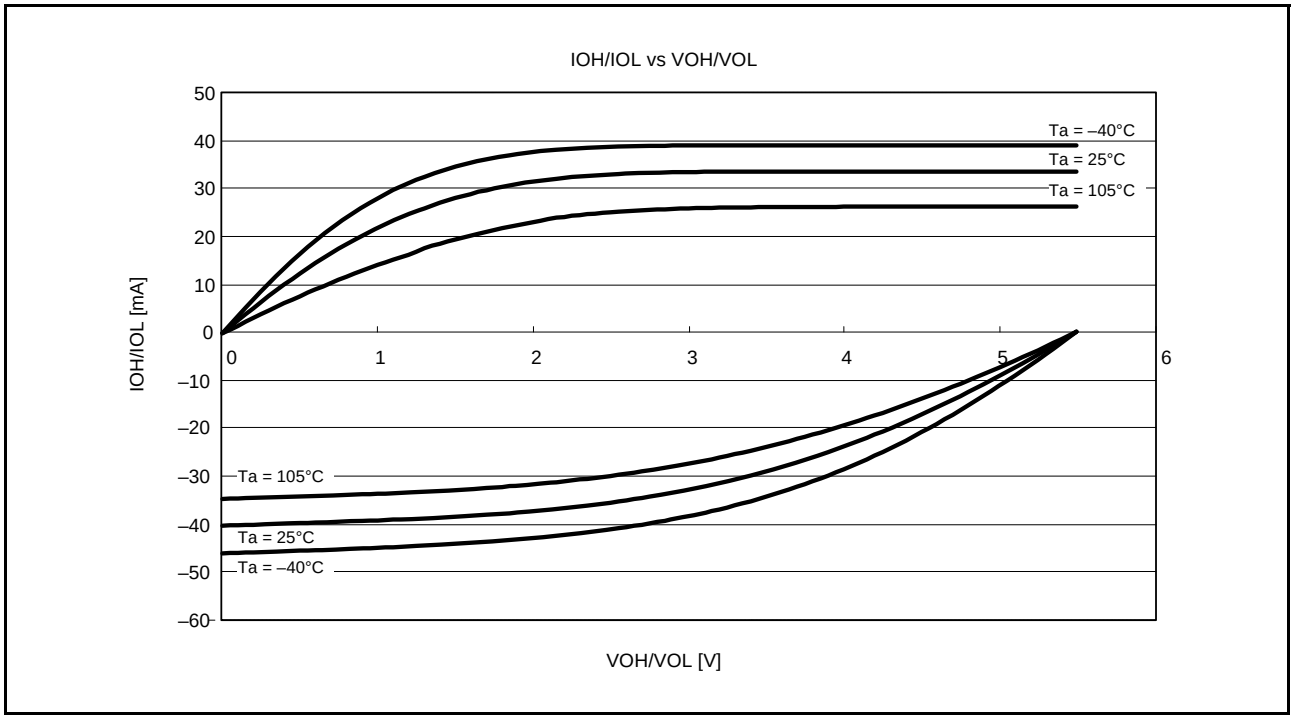


Figure 5.49 VOH/VOL and IOH/IOL Temperature Characteristics at VCC = 5.5 V when Normal Output is Selected (Reference Data)

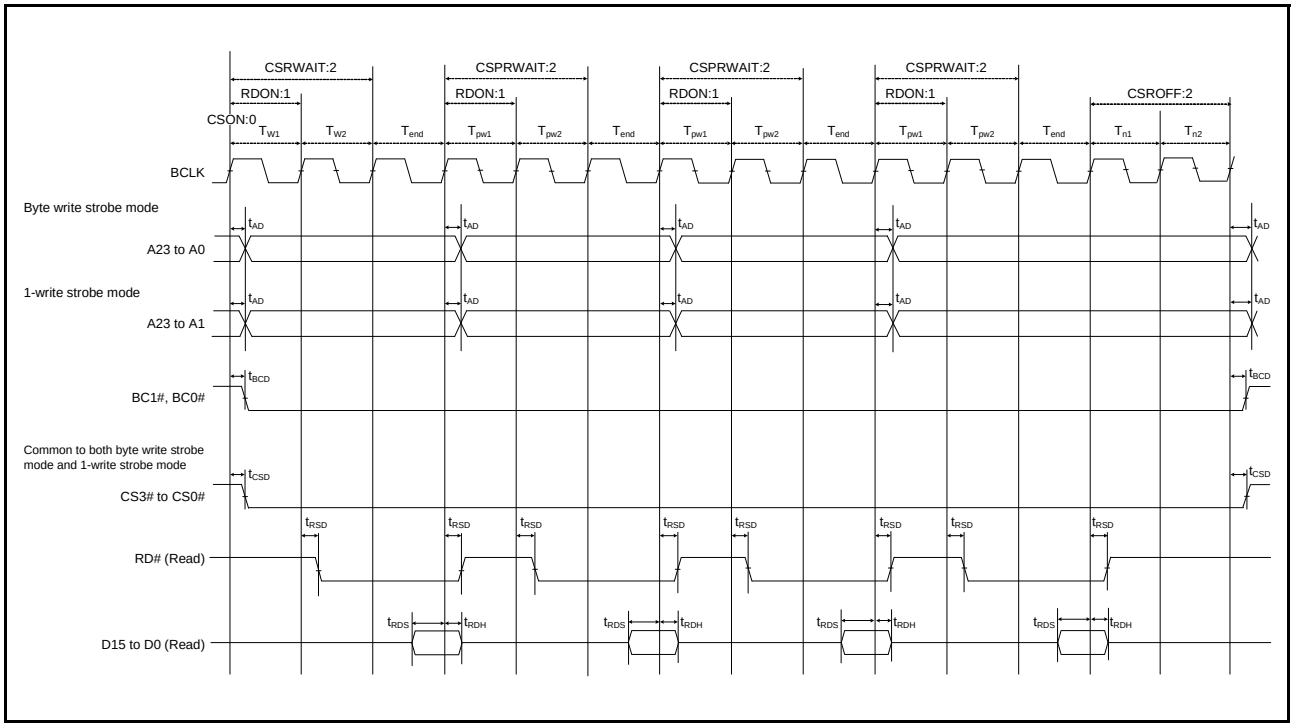
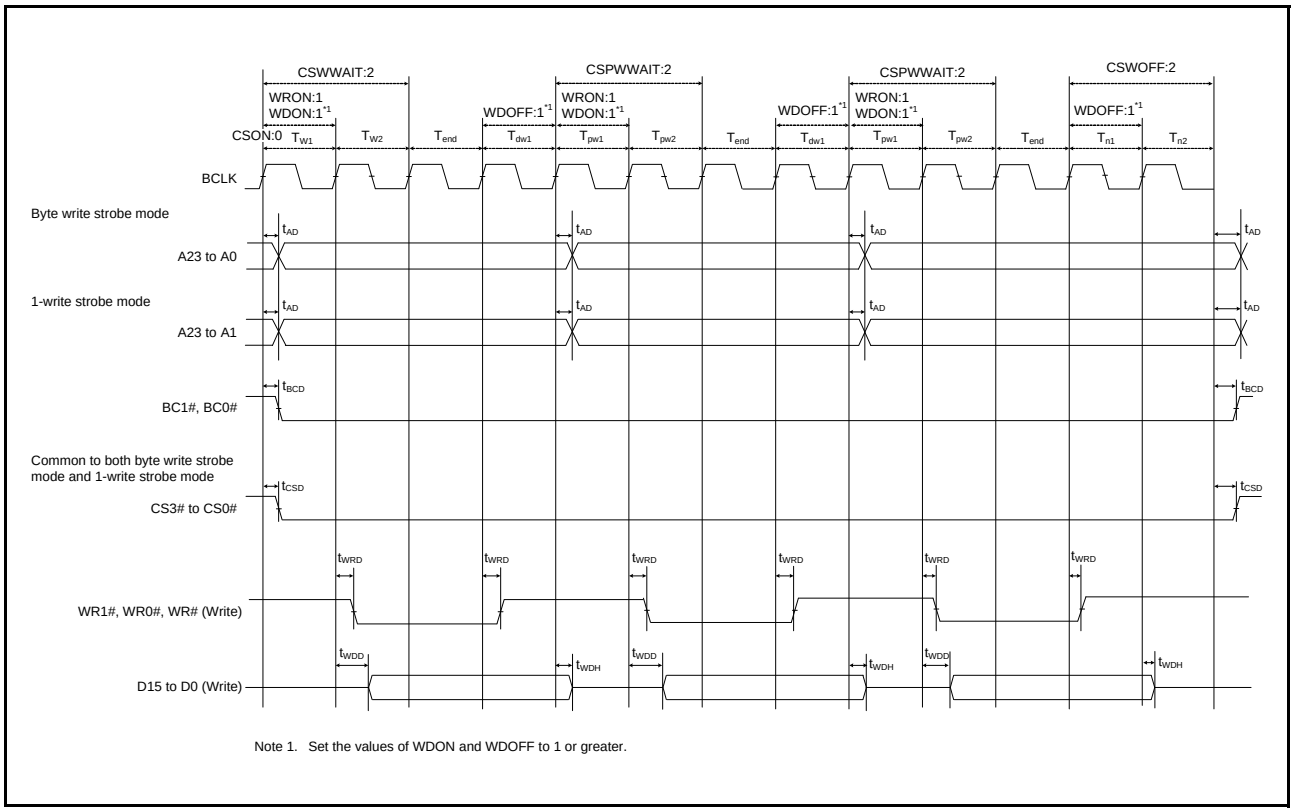


Figure 5.78 External Bus Timing/Page Read Cycle (Bus Clock Synchronized)



Note 1. Set the values of WDON and WDOFF to 1 or greater.

Figure 5.79 External Bus Timing/Page Write Cycle (Bus Clock Synchronized)

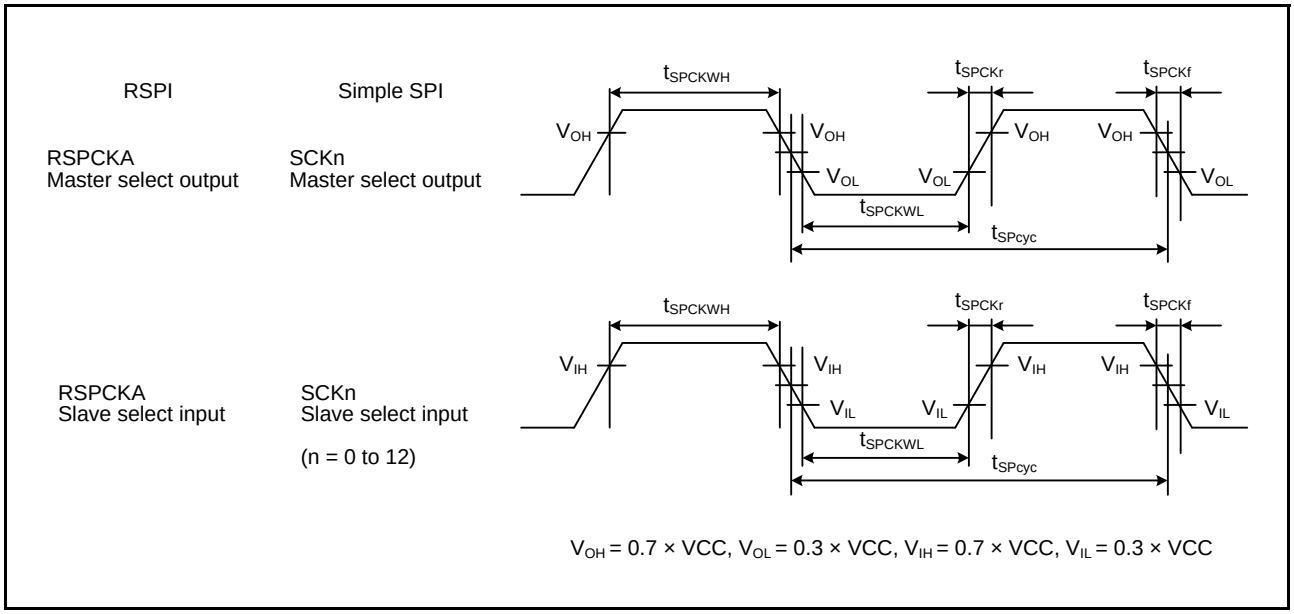


Figure 5.91 RSPI Clock Timing and Simple SPI Clock Timing

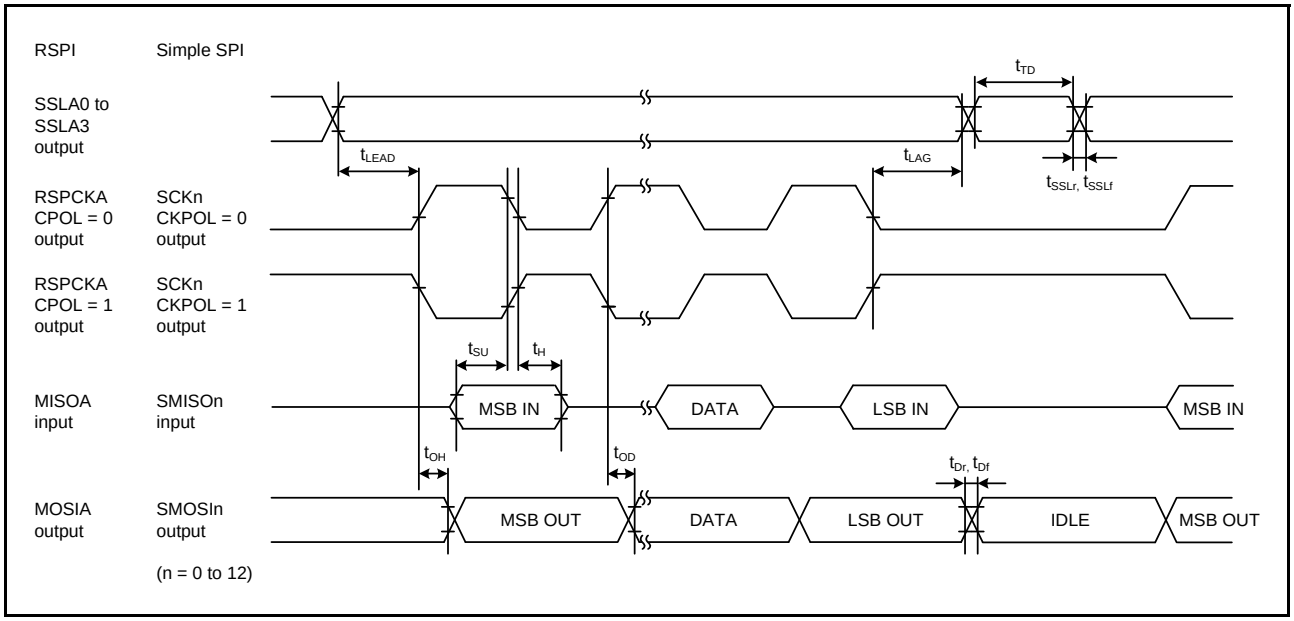


Figure 5.94 RSPI Timing (Master, CPHA = 1) (Bit Rate: PCLKB Set to Division Ratio Other Than Divided by 2) and Simple SPI Timing (Master, CKPH = 0)

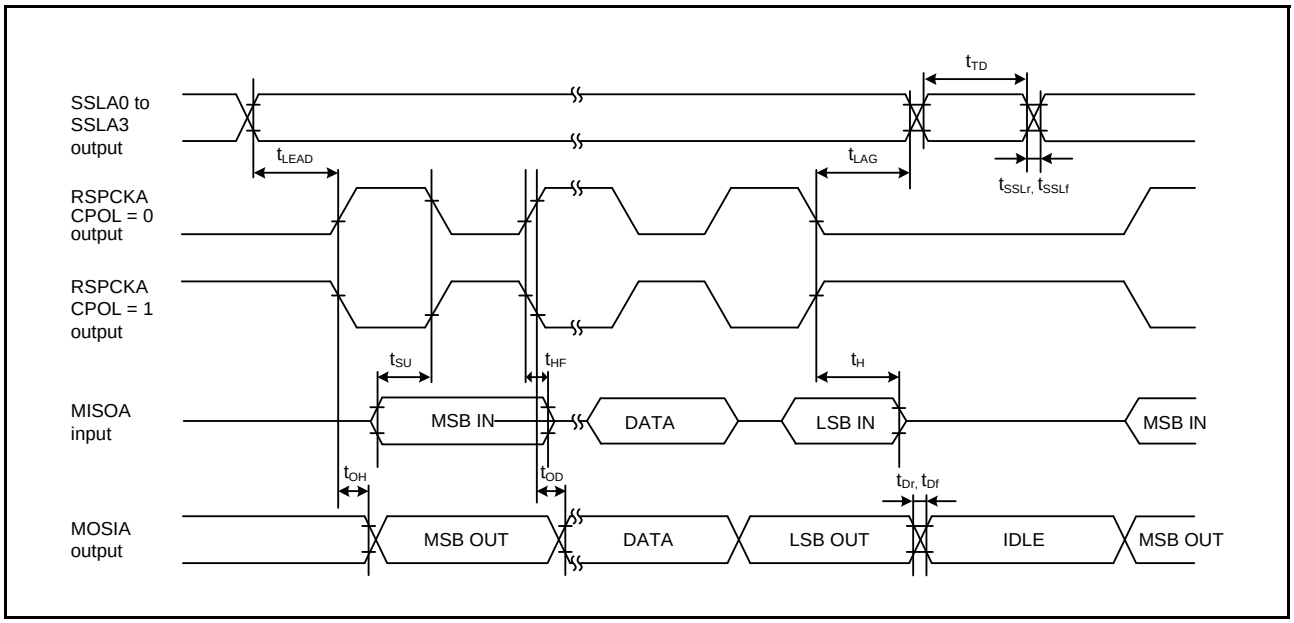


Figure 5.95 RSPI Timing (Master, CPHA = 1) (Bit Rate: PCLKB Set to Divided by 2)

5.9 Oscillation Stop Detection Timing

Table 5.73 Oscillation Stop Detection Circuit Characteristics

Conditions: VCC = AVCC0 = 1.62 to 5.5 V, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +105°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Detection time	t_{dr}	—	—	1	ms	Figure 5.108

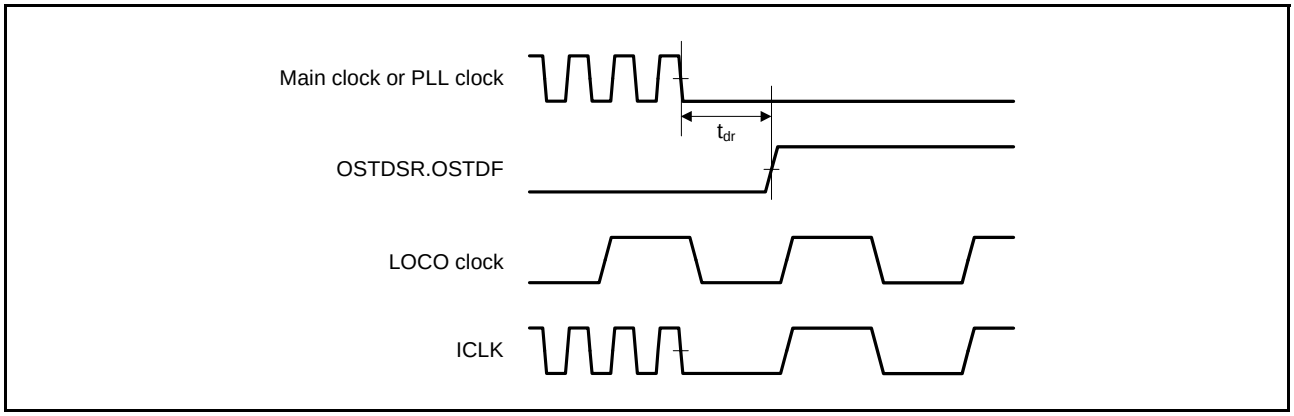


Figure 5.108 Oscillation Stop Detection Timing

[Chip version B]

Table 5.85 E2 DataFlash Characteristics (6)
: middle-speed operating modes 1B and 2B

Conditions: VCC = AVCC0 = 1.62 to 3.6 V, VREFH = VREFH0 = AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V
Temperature range for the programming/erasure operation: T_a = –40 to +105°C

Item		Symbol	FCLK = 4 MHz			FCLK = 32 MHz*1			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Programming time when N_{DPEC} ≤ 100 times	2 bytes	t_{DP2}	—	0.28	5.1	—	0.20	2.8	ms
	8 bytes	t_{DP8}	—	0.32	6.0	—	0.22	3.2	
Programming time when N_{DPEC} > 100 times	2 bytes	t_{DP2}	—	0.36	7.6	—	0.25	4.2	ms
	8 bytes	t_{DP8}	—	0.40	8.8	—	0.28	4.5	
Erasure time when N_{DPEC} ≤ 100 times	128 bytes	t_{DE128}	—	4.8	32.4	—	4.1	12	ms
Erasure time when N_{DPEC} > 100 times	128 bytes	t_{DE128}	—	5.8	51.4	—	4.9	17	ms
Blank check time	2 bytes	t_{DBC2}	—	—	110	—	—	40	µs
	2 Kbytes	t_{DBC2K}	—	—	16.3	—	—	2.6	ms
Suspend delay time during programming (in programming/erasure priority mode)		t_{DSPD}	—	—	1.7	—	—	1.6	ms
First suspend delay time during programming (in suspend priority mode)		t_{DSPSD1}	—	—	220	—	—	120	µs
Second suspend delay time during programming (in suspend priority mode)		t_{DSPSD2}	—	—	1.7	—	—	1.6	ms
Suspend delay time during erasing (in programming/erasure priority mode)		t_{DSED}	—	—	1.7	—	—	1.6	ms
First suspend delay time during erasing (in suspend priority mode)		t_{DSESD1}	—	—	220	—	—	120	µs
Second suspend delay time during erasing (in suspend priority mode)		t_{DSESD2}	—	—	1.7	—	—	1.6	ms

Note 1. The operating frequency is 20 MHz (max.) when the voltage is in the range from 1.62 V to less than 1.8 V.