# Renesas Electronics America Inc - R5F52106BDFF#V0 Datasheet

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Not For New Designs |
| Core Processor | RX |
| Core Size | 32-Bit Single-Core |
| Speed | 50MHz |
| Connectivity | I²C, SCI, SPI |
| Peripherals | DMA, LVD, POR, PWM, WDT |
| Number of I/O | 64 |
| Program Memory Size | 256KB (256K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | 8K x 8 |
| RAM Size | 32K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.62V ~ 5.5V |
| Data Converters | A/D 14x12b; D/A 2x10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 80-LQFP |
| Supplier Device Package | 80-LQFP (14x14) |
| Purchase URL | https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f52106bdff-v0 |

**Table 1.6 List of Products Chip Version C: D Version (Ta = –40 to +85°C)**

| Group | Part No. | Orderable Part No. | Package | ROM Capacity | RAM Capacity | E2 DataFlash | Operating Frequency (Max.) | Operating Temperature |
|---|---|---|---|---|---|---|---|---|
| RX210 | R5F52108CDFP | R5F52108CDFP#30 | PLQP0100KB-A | 512 Kbytes | 64 Kbytes | 8 Kbytes | 50 MHz | –40 to +85°C |
| | R5F52108CDFN | R5F52108CDFN#30 | PLQP0080KB-A | | | | | |
| | R5F52108CDFM | R5F52108CDFM#30 | PLQP0064KB-A | | | | | |
| | R5F52108CDLJ | R5F52108CDLJ#U0 | PTLG0100JA-A | | | | | |
| | R5F52108CDFF | R5F52108CDFF#V0 | PLQP0080JA-A | | | | | |
| | R5F52108CDFK | R5F52108CDFK#30 | PLQP0064GA-A | | | | | |
| | R5F52107CDFP | R5F52107CDFP#30 | PLQP0100KB-A | 384 Kbytes | | | | |
| | R5F52107CDFN | R5F52107CDFN#30 | PLQP0080KB-A | | | | | |
| | R5F52107CDFM | R5F52107CDFM#30 | PLQP0064KB-A | | | | | |
| | R5F52107CDLJ | R5F52107CDLJ#U0 | PTLG0100JA-A | | | | | |
| | R5F52107CDFF | R5F52107CDFF#V0 | PLQP0080JA-A | | | | | |
| | R5F52107CDFK | R5F52107CDFK#30 | PLQP0064GA-A | | | | | |

Note: • Orderable part numbers are current as of when this manual was published. Please make sure to refer to the relevant product page on the Renesas website for the latest part numbers.

**Table 1.7 List of Products Chip Version C: G Version (Ta = –40 to +105°C)**

| Group | Part No. | Orderable Part No. | Package | ROM Capacity | RAM Capacity | E2 DataFlash | Operating Frequency (Max.) | Operating Temperature |
|---|---|---|---|---|---|---|---|---|
| RX210 | R5F52108CGFP | R5F52108CGFP#30 | PLQP0100KB-A | 512 Kbytes | 64 Kbytes | 8 Kbytes | 50 MHz | –40 to +105°C |
| | R5F52108CGFN | R5F52108CGFN#30 | PLQP0080KB-A | | | | | |
| | R5F52108CGFM | R5F52108CGFM#30 | PLQP0064KB-A | | | | | |
| | R5F52108CGFF | R5F52108CGFF#V0 | PLQP0080JA-A | | | | | |
| | R5F52108CGFK | R5F52108CGFK#30 | PLQP0064GA-A | | | | | |
| | R5F52107CGFP | R5F52107CGFP#30 | PLQP0100KB-A | 384 Kbytes | | | | |
| | R5F52107CGFN | R5F52107CGFN#30 | PLQP0080KB-A | | | | | |
| | R5F52107CGFM | R5F52107CGFM#30 | PLQP0064KB-A | | | | | |
| | R5F52107CGFF | R5F52107CGFF#V0 | PLQP0080JA-A | | | | | |
| | R5F52107CGFK | R5F52107CGFK#30 | PLQP0064GA-A | | | | | |

Note: • Please contact Renesas Electronics sales office for derating of operation under Ta = +85°C to +105°C. Derating is the systematic reduction of load for the sake of improved reliability.

Note: • Orderable part numbers are current as of when this manual was published. Please make sure to refer to the relevant product page on the Renesas website for the latest part numbers.

## 1.4 Pin Functions

Table 1.8 lists the pin functions.

**Table 1.8 Pin Functions (1 / 4)**

| Classifications | Pin Name | I/O | Description |
|---|---|---|---|
| Power supply | VCC | Input | Power supply pin. Connect it to the system power supply. |
| | VCL | — | Connect this pin to the VSS pin via the 0.1 µF smoothing capacitor used to stabilize the internal power supply. Place the capacitor close to the pin. |
| | VSS | Input | Ground pin. Connect it to the system power supply (0 V). |
| Clock | XTAL | Output | Pins for connecting a crystal resonator. An external clock signal can be input through the EXTAL pin. |
| | EXTAL | Input | |
| | BCLK | Output | Outputs the external bus clock for external devices. |
| | XCIN | Input | Input/output pins for the sub-clock oscillator. Connect a crystal resonator between XCIN and XCOUT. |
| | XCOUT | Output | |
| Operating mode control | MD | Input | Pin for setting the operating mode. The signal levels on this pin must not be changed during operation. |
| System control | RES# | Input | Reset pin. This LSI enters the reset state when this signal goes low. |
| CAC | CACREF | Input | Input pin for the clock frequency accuracy measurement circuit. |
| On-chip emulator | FINED | I/O | FINE interface pin. |
| Address bus | A0 to A23 | Output | Output pins for the address. |
| Data bus | D0 to D15 | I/O | Input and output pins for the bidirectional data bus. |
| Multiplexed bus | A0/D0 to A15/D15 | I/O | Address/data multiplexed bus |
| Bus control | RD# | Output | Strobe signal which indicates that reading from the external bus interface space is in progress. |
| | WR# | Output | Strobe signal which indicates that writing to the external bus interface space is in progress, in single-write strobe mode. |
| | WR0#, WR1# | Output | Strobe signals which indicate that either group of data bus pins (D7 to D0, and D15 to D8) is valid in writing to the external bus interface space, in byte strobe mode. |
| | BC0#, BC1# | Output | Strobe signals which indicate that either group of data bus pins (D7 to D0 and D15 to D8) is valid in access to the external bus interface space, in single-write strobe mode. |
| | CS0# to CS3# | Output | Select signals for areas 0 to 3. |
| | WAIT# | Input | Input pin for wait request signals in access to the external space. |
| | ALE | Output | Address latch signal when address/data multiplexed bus is selected. |
| Interrupt | NMI | Input | Non-maskable interrupt request pin. |
| | IRQ0 to IRQ7 | Input | Interrupt request pins. |

**Table 1.8 Pin Functions (2 / 4)**

| Classifications | Pin Name | I/O | Description |
|---|---|---|---|
| 16-bit timer pulse unit | TIOCA0, TIOCB0 TIOCC0, TIOCD0 | I/O | The TGRA0 to TGRD0 input capture input/output compare output/ PWM output pins. |
| | TIOCA1, TIOCB1 | I/O | The TGRA1 and TGRB1 input capture input/output compare output/ PWM output pins. |
| | TIOCA2, TIOCB2 | I/O | The TGRA2 and TGRB2 input capture input/output compare output/ PWM output pins. |
| | TIOCA3, TIOCB3 TIOCC3, TIOCD3 | I/O | The TGRA3 to TGRD3 input capture input/output compare output/ PWM output pins. |
| | TIOCA4, TIOCB4 | I/O | The TGRA4 and TGRB4 input capture input/output compare output/ PWM output pins. |
| | TIOCA5, TIOCB5 | I/O | The TGRA5 and TGRB5 input capture input/output compare output/ PWM output pins. |
| | TCLKA, TCLKB TCLKC, TCLKD | Input | Input pins for external clock signals. |
| Multi-function timer pulse unit 2 | MTIOC0A, MTIOC0B MTIOC0C, MTIOC0D | I/O | The TGRA0 to TGRD0 input capture input/output compare output/ PWM output pins. |
| | MTIOC1A, MTIOC1B | I/O | The TGRA1 and TGRB1 input capture input/output compare output/ PWM output pins. |
| | MTIOC2A, MTIOC2B | I/O | The TGRA2 and TGRB2 input capture input/output compare output/ PWM output pins. |
| | MTIOC3A, MTIOC3B MTIOC3C, MTIOC3D | I/O | The TGRA3 to TGRD3 input capture input/output compare output/ PWM output pins. |
| | MTIOC4A, MTIOC4B MTIOC4C, MTIOC4D | I/O | The TGRA4 to TGRD4 input capture input/output compare output/ PWM output pins. |
| | MTIC5U, MTIC5V, MTIC5W | Input | The TGRU5, TGRV5, and TGRW5 input capture input/external pulse input pins. |
| | MTCLKA, MTCLKB, MTCLKC, MTCLKD | Input | Input pins for the external clock. |
| Port output enable 2 | POE0# to POE3#, POE8# | Input | Input pins for request signals to place the MTU pins in the high impedance state. |
| 8-bit timer | TMO0 to TMO3 | Output | Compare match output pins. |
| | TMCI0 to TMCI3 | Input | Input pins for external clocks to be input to the counter. |
| | TMRI0 to TMRI3 | Input | Input pins for the counter reset. |
| Realtime clock | RTCOUT | Output | Output pin for 1-Hz clock. |
| | RTCIC0 to RTCIC2 | Input | Time capture event input pins. |
| Serial communications interface (SCIc) | • Asynchronous mode/clock synchronous mode | | |
| | SCK0 to SCK11 | I/O | Input/output pins for the clock |
| | RXD0 to RXD11 | Input | Input pins for received data |
| | TXD0 to TXD11 | Output | Output pins for transmitted data |
| | CTS0# to CTS11# | Input | Input pins for controlling the start of transmission and reception |
| | RTS0# to RTS11# | Output | Output pins for controlling the start of transmission and reception |
| | • Simple $I^2C$ mode | | |
| | SSCL0 to SSCL11 | I/O | Input/output pins for the $I^2C$ clock |
| | SSDA0 to SSDA11 | I/O | Input/output pins for the $I^2C$ data |
| | • Simple SPI mode | | |
| | SCK0 to SCK11 | I/O | Input/output pins for the clock |
| | SMISO0 to SMISO11 | I/O | Input/output pins for slave transmission of data |
| | SMOSI0 to SMOSI11 | I/O | Input/output pins for master transmission of data |
| | SS0# to SS11# | Input | Chip-select input pins |

**Table 1.9 List of Pins and Pin Functions (145-Pin TFLGA) (1 / 4)**

| Pin No. | Power Supply, Clock, System Control | I/O Port | External Bus | Timers (MTU, TMR, POE) | Communications (SCIc, SCId, RSPI, RIIC) | Others |
|---|---|---|---|---|---|---|
| A1 | AVSS0 | | | | | |
| A2 | | P07 | | | | ADTRG0# |
| A3 | | P40 | | | | AN000 |
| A4 | | P42 | | | | AN002 |
| A5 | | P45 | | | | AN005 |
| A6 | | P90 | | | TXD7/SMOSI7/SSDA7 | |
| A7 | | P92 | | | RXD7/SMISO7/SSCL7 | |
| A8 | | PD2 | D2[A2/D2] | MTIOC4D | | IRQ2 |
| A9 | | PD6 | D6[A6/D6] | MTIC5V/POE1# | | IRQ6 |
| A10 | | PK3 | | | RXD9/SMISO9/SSCL9 | |
| A11 | | P62 | | | | |
| A12 | | PE1 | D9[A9/D9] | MTIOC4C | TXD12/TXDX12/SIOX12/ SMOSI12/SSDA12 | AN009/CMPB0 |
| A13 | | PE3 | D11[A11/D11] | MTIOC4B/POE8# | CTS12#/RTS12#/SS12# | AN011/CMPA1 |
| B1 | VREFH | | | | | |
| B2 | AVCC0 | | | | | |
| B3 | | P05 | | | | DA1 |
| B4 | VREFL0 | | | | | |
| B5 | | P43 | | | | AN003 |
| B6 | | P47 | | | | AN007 |
| B7 | | P91 | | | SCK7 | |
| B8 | | PD0 | D0[A0/D0] | | | IRQ0 |
| B9 | | PD4 | D4[A4/D4] | POE3# | | IRQ4 |
| B10 | | PK2 | | | TXD9/SMOSI9/SSDA9 | |
| B11 | | P61 | | | CTS9#/RTS9#/SS9# | |
| B12 | | PE2 | D10[A10/D10] | MTIOC4A | RXD12/RXDX12/ SMISO12/SSCL12 | IRQ7-DS/AN010/ CVREFB0 |
| B13 | | PE4 | D12[A12/D12] | MTIOC4D/MTIOC1A | | AN012/CMPA2 |
| C1 | VREFL | | | | | |
| C2 | | P02 | | TMCI1 | SCK6 | |
| C3 | VREFH0 | | | | | |
| C4 | | P41 | | | | AN001 |
| C5 | | P46 | | | | AN006 |
| C6 | VSS | | | | | |
| C7 | | PD1 | D1[A1/D1] | MTIOC4B | | IRQ1 |
| C8 | | PD3 | D3[A3/D3] | POE8# | | IRQ3 |
| C9 | | PD7 | D7[A7/D7] | MTIC5U/POE0# | | IRQ7 |
| C10 | | P63 | | | | |
| C11 | | PE0 | D8[A8/D8] | | SCK12 | AN008 |
| C12 | | P70 | | | SCK4 | |
| C13 | | PK4 | | | RXD4/SMISO4/SSCL4 | |
| D1 | | P00 | | TMRI0 | TXD6/SMOSI6/SSDA6 | |
| D2 | | PF5 | | | | IRQ4 |
| D3 | | P03 | | | | DA0 |
| D4 | | P01 | | TMCI0 | RXD6/SMISO6/SSCL6 | |
| D5 | VCC | | | | | |
| D6 | | P93 | | | CTS7#/RTS7#/SS7# | |
| D7 | | PD5 | D5[A5/D5] | MTIC5W/POE2# | | IRQ5 |
| D8 | | P60 | | | SCK9 | |
| D9 | | P64 | | | | |
| D10 | | PE7 | D15[A15/D15] | | | IRQ7/AN015 |

**Table 1.10 List of Pins and Pin Functions (144-Pin LQFP) (2 / 4)**

| Pin No. | Power Supply, Clock, System Control | I/O Port | External Bus | Timers (MTU, TMR, POE) | Communications (SCIc, SCId, RSPI, RIIC) | Others |
|---|---|---|---|---|---|---|
| 40 | | P16 | | MTIOC3C/MTIOC3D/ TMO2/TIOCB1/TCLKC | TXD1/SMOSI1/SSDA1/ MOSIA/SCL-DS/RXD3/ SMISO3/SSCL3 | IRQ6/RTCOUT/ ADTRG0# |
| 41 | | P86 | | TIOCA0 | | |
| 42 | | P15 | | MTIOC0B/MTCLKB/ TMCI2/TIOCB2/TCLKB | RXD1/SMISO1/SSCL1/ SCK3 | IRQ5 |
| 43 | | P14 | | MTIOC3A/MTCLKA/ TMRI2/TIOCB5/TCLKA | CTS1#/RTS1#/SS1# | IRQ4 |
| 44 | | P13 | | MTIOC0B/TMO3/ TIOCA5 | SDA/TXD2/SMOSI2/ SSDA2 | IRQ3 |
| 45 | | P12 | | TMCI1 | SCL/RXD2/SMISO2/ SSCL2 | IRQ2 |
| 46 | | PH3 | | TMCI0 | | |
| 47 | | PH2 | | TMRI0 | | IRQ1 |
| 48 | | PH1 | | TMO0 | | IRQ0 |
| 49 | | PH0 | | | | CACREF |
| 50 | | P56 | | MTIOC3C/TIOCA1 | | |
| 51 | | P55 | WAIT# | MTIOC4D/TMO3 | | |
| 52 | | P54 | ALE | MTIOC4B/TMCI1 | CTS2#/RTS2#/SS2# | |
| 53 | BCLK | P53 | | | | |
| 54 | | P52 | RD# | | RXD2/SMISO2/SSCL2 | |
| 55 | | P51 | WR1#/BC1#/WAIT# | | SCK2 | |
| 56 | | P50 | WR0#/WR# | | TXD2/SMOSI2/SSDA2 | |
| 57 | VSS | | | | | |
| 58 | | P83 | | MTIOC4C | CTS10#/RTS10# | |
| 59 | VCC | | | | | |
| 60 | | PC7 | A23/CS0# | MTIOC3A/TMO2/ MTCLKB | TXD8/SMOSI8/SSDA8/ MISOA | CACREF |
| 61 | | PC6 | A22/CS1# | MTIOC3C/MTCLKA/ TMCI2 | RXD8/SMISO8/SSCL8/ MOSIA | |
| 62 | | PC5 | A21/CS2#/WAIT# | MTIOC3B/MTCLKD/ TMRI2 | SCK8/RSPCKA | |
| 63 | | P82 | | MTIOC4A | TXD10/SMOSI10/SSDA10 | |
| 64 | | P81 | | MTIOC3D | RXD10/SMISO10/SSCL10 | |
| 65 | | P80 | | MTIOC3B | SCK10 | |
| 66 | | PC4 | A20/CS3# | MTIOC3D/MTCLKC/ TMCI1/POE0# | SCK5/CTS8#/RTS8#/ SS8#/SSLA0 | |
| 67 | | PC3 | A19 | MTIOC4D/TCLKB | TXD5/SMOSI5/SSDA5 | |
| 68 | | P77 | | | TXD11/SMOSI11/SSDA11 | |
| 69 | | P76 | | | RXD11/SMISO11/SSCL11 | |
| 70 | | PC2 | A18 | MTIOC4B/TCLKA | RXD5/SMISO5/SSCL5/ ISSLA3 | |
| 71 | | P75 | | | SCK11 | |
| 72 | | P74 | | | CTS11#/RTS11#/SS11# | |
| 73 | | PC1 | A17 | MTIOC3A/TCLKD | SCK5/SSLA2 | |
| 74 | | PL1 | | | | |
| 75 | | PC0 | A16 | MTIOC3C/TCLKC | CTS5#/RTS5#/SS5#/ SSLA1 | |
| 76 | | PL0 | | | | |
| 77 | | P73 | | | | |
| 78 | | PB7 | A15 | MTIOC3B/TIOCB5 | TXD9/SMOSI9/SSDA9 | |
| 79 | | PB6 | A14 | MTIOC3D/TIOCA5 | RXD9/SMISO9/SSCL9 | |
| 80 | | PB5 | A13 | MTIOC2A/MTIOC1B/ TMRI1/POE1#/TIOCB4 | SCK9 | |

**Table 1.11 List of Pins and Pin Functions (100-Pin TFLGA) (2 / 3)**

| Pin No. | Power Supply, Clock, System Control | I/O Port | External Bus | Timers (MTU, TMR, POE) | Communications (SCIc, SCId, RSPI, RIIC) | Others |
|---|---|---|---|---|---|---|
| E6 | | PA2 | A2 | | RXD5/SMISO5/SSCL5/ SSLA3 | |
| E7 | | PA6 | A6 | MTIC5V/MTCLKB/ TMCI3/POE2# | CTS5#/RTS5#/SS5#/ MOSIA | |
| E8 | | PA4 | A4 | MTIC5U/MTCLKA/ TMRI0 | TXD5/SMOSI5/SSDA5/ SSLA0 | IRQ5-DS/CVREFB1 |
| E9 | | PA5 | A5 | | RSPCKA | |
| E10 | | PA3 | A3 | MTIOC0D/MTCLKD | RXD5/SMISO5/SSCL5 | IRQ6-DS/CMPB1 |
| F1 | EXTAL | P36 | | | | |
| F2 | VCC | | | | | |
| F3 | | P35 | | | | NMI |
| F4 | | P32 | | MTIOC0C/TMO3 | TXD6/SMOSI6/SSDA6 | IRQ2-DS/RTCOUT/ RTCIC2 |
| F5 | | P12 | | TMCI1 | SCL | IRQ2 |
| F6 | | PB3 | A11 | MTIOC0A/MTIOC4A/ TMO0/POE3# | SCK6 | |
| F7 | | PB2 | A10 | | CTS6#/RTS6#/SS6# | |
| F8 | | PB0 | A8 | MTIC5W | RXD6/SMISO6/SSCL6/ RSPCKA | |
| F9 | | PA7 | A7 | | MISOA | |
| F10 | VSS | | | | | |
| G1 | | P33 | | MTIOC0D/TMRI3/ POE3# | RXD6/SMISO6/SSCL6 | IRQ3-DS |
| G2 | | P31 | | MTIOC4D/TMCI2 | CTS1#/RTS1#/SS1# | IRQ1-DS/RTCIC1 |
| G3 | | P30 | | MTIOC4B/TMRI3/ POE8# | RXD1/SMISO1/SSCL1 | IRQ0-DS/RTCIC0 |
| G4 | | P27 | CS3# | MTIOC2B/TMCI3 | SCK1 | |
| G5 | BCLK | P53 | | | | |
| G6 | | P52 | RD# | | | |
| G7 | | PB5 | A13 | MTIOC2A/MTIOC1B/ TMRI1/POE1# | SCK9 | |
| G8 | | PB4 | A12 | | CTS9#/RTS9#/SS9# | |
| G9 | | PB1 | A9 | MTIOC0C/MTIOC4C/ TMCI0 | TXD6/SMOSI6/SSDA6 | IRQ4-DS |
| G10 | VCC | | | | | |
| H1 | | P26 | CS2# | MTIOC2A/TMO1 | TXD1/SMOSI1/SSDA1 | |
| H2 | | P25 | CS1# | MTIOC4C/MTCLKB | | ADTRG0# |
| H3 | | P16 | | MTIOC3C/MTIOC3D/ TMO2 | TXD1/SMOSI1/SSDA1/ MOSIA/SCL-DS | IRQ6/RTCOUT/ ADTRG0# |
| H4 | | P15 | | MTIOC0B/MTCLKB/ TMCI2 | RXD1/SMISO1/SSCL1 | IRQ5 |
| H5 | | P55 | WAIT# | MTIOC4D/TMO3 | | |
| H6 | | P54 | ALE | MTIOC4B/TMCI1 | | |
| H7 | | PC7 | A23/CS0# | MTIOC3A/TMO2/ MTCLKB | TXD8/SMOSI8/SSDA8/ MISOA | CACREF |
| H8 | | PC6 | A22/CS1# | MTIOC3C/MTCLKA/ TMCI2 | RXD8/SMISO8/SSCL8/ MOSIA | |
| H9 | | PB6 | A14 | MTIOC3D | RXD9/SMISO9/SSCL9 | |
| H10 | | PB7 | A15 | MTIOC3B | TXD9/SMOSI9/SSDA9 | |
| J1 | | P24 | CS0# | MTIOC4A/MTCLKA/ TMRI1 | | |
| J2 | | P21 | | MTIOC1B/TMCI0 | RXD0/SMISO0/SSCL0 | |
| J3 | | P17 | | MTIOC3A/MTIOC3B/ TMO1/POE8# | SCK1/MISOA/ SDA-DS | IRQ7 |

**Table 1.14 List of Pins and Pin Functions (69-Pin WLBGA) (2 / 2)**

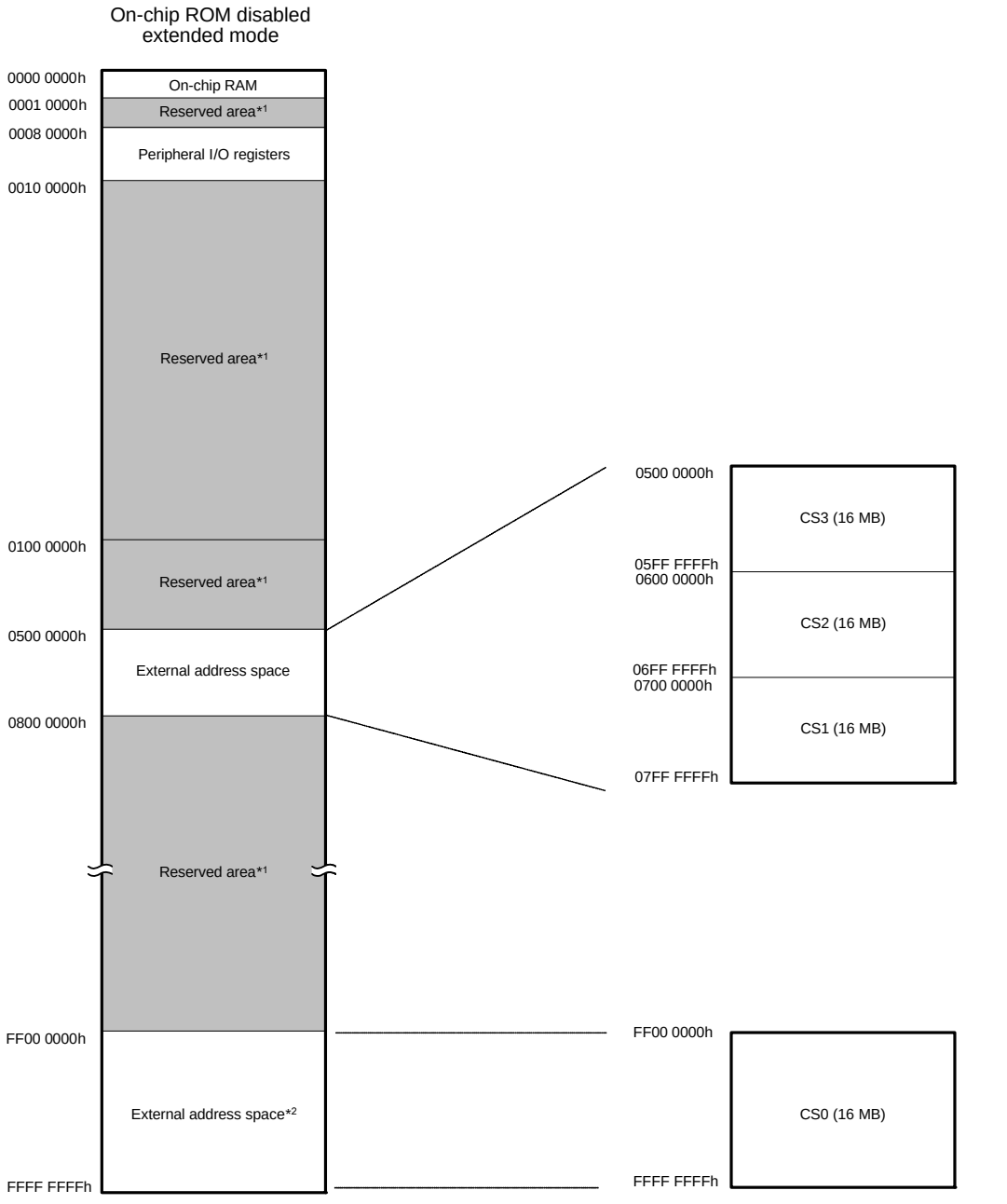
| Pin No. | Power Supply, Clock, System Control | I/O Port | Timers (MTU, TMR, POE) | Communications (SCIc, SCId, RSPI, RIIC) | Others |
|---|---|---|---|---|---|
| G3 | NC | | | | |
| G4 | | P54 | MTIOC4B/TMCI1 | | |
| G5 | | PH1 | TMO0 | | IRQ0 |
| G6 | | P14 | MTIOC3A/MTCLKA/TMRI2 | CTS1#/RTS1#/SS1# | IRQ4 |
| G7 | | P27 | MTIOC2B/TMCI3 | SCK1 | |
| G8 | | P32 | MTIOC0C/TMO3 | TXD6/SMOSI6/SSDA6 | IRQ2-DS/RTCOUT/ RTCIC2 |
| G9 | | P35 | | | NMI |
| H1 | | PB7 | MTIOC3B | TXD9/SMOSI9/SSDA9 | |
| H2 | | PC3 | MTIOC4D | TXD5/SMOSI5/SSDA5 | |
| H3 | | PC5 | MTIOC3B/MTCLKD/TMRI2 | SCK8/RSPCKA | |
| H4 | | PC6 | MTIOC3C/MTCLKA/TMCI2 | RXD8/SMISO8/SSCL8/MOSIA | |
| H5 | | P55 | MTIOC4D/TMO3 | | |
| H6 | | PH3 | TMCI0 | | |
| H7 | | P17 | MTIOC3A/MTIOC3B/TMO1/ POE8# | SCK1/MISOA/SDA-DS | IRQ7 |
| H8 | | P26 | MTIOC2A/TMO1 | TXD1/SMOSI1/SSDA1 | |
| H9 | | P30 | MTIOC4B/TMRI3/POE8# | RXD1/SMISO1/SSCL1 | IRQ0-DS/RTCIC0 |
| J1 | NC | | | | |
| J2 | | PC2 | MTIOC4B | RXD5/SMISO5/SSCL5/SSLA3 | |
| J3 | | PC4 | MTIOC3D/MTCLKC/TMCI1/ POE0# | SCK5/CTS8#/RTS8#/SS8#/ SSLA0 | |
| J4 | | PC7 | MTIOC3A/TMO2/MTCLKB | TXD8/SMOSI8/SSDA8/MISOA | CACREF |
| J5 | | PH0 | | | CACREF |
| J6 | | PH2 | TMRI0 | | IRQ1 |
| J7 | | P15 | MTIOC0B/MTCLKB/TMCI2 | RXD1/SMISO1/SSCL1 | IRQ5 |
| J8 | | P16 | MTIOC3C/MTIOC3D/TMO2 | TXD1/SMOSI1/SSDA1/ MOSIA/SCL-DS | IRQ6/RTCOUT/ ADTRG0# |
| J9 | NC | | | | |

Note: • Pin names to which –DS is appended are for pins that can be used to trigger release from deep software standby mode.
Note: • Leave the NC pin open.

## 3.2 External Address Space

The external address space is divided into up to four CS areas (CS0 to CS3), each corresponding to the CSn# signal output from a CSn# (n = 0 to 3) pin.

Figure 3.2 shows the address ranges corresponding to the individual CS areas (CS0 to CS3) in on-chip ROM disabled extended mode.




Note 1. Reserved areas should not be accessed.

Note 2. The CS0 area is disabled in on-chip ROM enabled extended mode. In this mode, the address space for addresses above 0800 0000h is as shown in figure on this section “Memory Map in Each Operating Mode”.

**Figure 3.2 Correspondence between External Address Spaces and CS Areas (In On-Chip ROM Disabled Extended Mode)**

**Table 4.1 List of I/O Registers (Address Order) (10 / 29)**

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles: ICLK ≥ PCLK | Number of Access Cycles: ICLK < PCLK |
|---|---|---|---|---|---|---|---|
| 0008 738A2 | ICU | Interrupt source priority register 162 | IPR162 | 8 | 8 | | 2 ICLK |
| 0008 73A4h | ICU | Interrupt source priority register 164 | IPR164 | 8 | 8 | | 2 ICLK |
| 0008 73A6h | ICU | Interrupt source priority register 166 | IPR166 | 8 | 8 | | 2 ICLK |
| 0008 73AAh | ICU | Interrupt source priority register 170 | IPR170 | 8 | 8 | | 2 ICLK |
| 0008 73ABh | ICU | Interrupt source priority register 171 | IPR171 | 8 | 8 | | 2 ICLK |
| 0008 73AEh | ICU | Interrupt source priority register 174 | IPR174 | 8 | 8 | | 2 ICLK |
| 0008 73B1h | ICU | Interrupt source priority register 177 | IPR177 | 8 | 8 | | 2 ICLK |
| 0008 73B4h | ICU | Interrupt source priority register 180 | IPR180 | 8 | 8 | | 2 ICLK |
| 0008 73B7h | ICU | Interrupt source priority register 183 | IPR183 | 8 | 8 | | 2 ICLK |
| 0008 73BAh | ICU | Interrupt source priority register 186 | IPR186 | 8 | 8 | | 2 ICLK |
| 0008 73BEh | ICU | Interrupt source priority register 190 | IPR190 | 8 | 8 | | 2 ICLK |
| 0008 73C2h | ICU | Interrupt source priority register 194 | IPR194 | 8 | 8 | | 2 ICLK |
| 0008 73C6h | ICU | Interrupt source priority register 198 | IPR198 | 8 | 8 | | 2 ICLK |
| 0008 73C7h | ICU | Interrupt source priority register 199 | IPR199 | 8 | 8 | | 2 ICLK |
| 0008 73C8h | ICU | Interrupt source priority register 200 | IPR200 | 8 | 8 | | 2 ICLK |
| 0008 73C9h | ICU | Interrupt source priority register 201 | IPR201 | 8 | 8 | | 2 ICLK |
| 0008 73CEh | ICU | Interrupt source priority register 206 | IPR206 | 8 | 8 | | 2 ICLK |
| 0008 73D2h | ICU | Interrupt source priority register 210 | IPR210 | 8 | 8 | | 2 ICLK |
| 0008 73D6h | ICU | Interrupt source priority register 214 | IPR214 | 8 | 8 | | 2 ICLK |
| 0008 73DAh | ICU | Interrupt source priority register 218 | IPR218 | 8 | 8 | | 2 ICLK |
| 0008 73DEh | ICU | Interrupt source priority register 222 | IPR222 | 8 | 8 | | 2 ICLK |
| 0008 73E2h | ICU | Interrupt source priority register 226 | IPR226 | 8 | 8 | | 2 ICLK |
| 0008 73E6h | ICU | Interrupt source priority register 230 | IPR230 | 8 | 8 | | 2 ICLK |
| 0008 73EAh | ICU | Interrupt source priority register 234 | IPR234 | 8 | 8 | | 2 ICLK |
| 0008 73EEh | ICU | Interrupt source priority register 238 | IPR238 | 8 | 8 | | 2 ICLK |
| 0008 73F2h | ICU | Interrupt source priority register 242 | IPR242 | 8 | 8 | | 2 ICLK |
| 0008 73F3h | ICU | Interrupt source priority register 243 | IPR243 | 8 | 8 | | 2 ICLK |
| 0008 73F4h | ICU | Interrupt source priority register 244 | IPR244 | 8 | 8 | | 2 ICLK |
| 0008 73F5h | ICU | Interrupt source priority register 245 | IPR245 | 8 | 8 | | 2 ICLK |
| 0008 73F6h | ICU | Interrupt source priority register 246 | IPR246 | 8 | 8 | | 2 ICLK |
| 0008 73F7h | ICU | Interrupt source priority register 247 | IPR247 | 8 | 8 | | 2 ICLK |
| 0008 73F8h | ICU | Interrupt source priority register 248 | IPR248 | 8 | 8 | | 2 ICLK |
| 0008 73F9h | ICU | Interrupt source priority register 249 | IPR249 | 8 | 8 | | 2 ICLK |
| 0008 73FAh | ICU | Interrupt source priority register 250 | IPR250 | 8 | 8 | | 2 ICLK |
| 0008 7400h | ICU | DMAC activation request select register 0 | DMRSR0 | 8 | 8 | | 2 ICLK |
| 0008 7404h | ICU | DMAC activation request select register 1 | DMRSR1 | 8 | 8 | | 2 ICLK |
| 0008 7408h | ICU | DMAC activation request select register 2 | DMRSR2 | 8 | 8 | | 2 ICLK |
| 0008 740Ch | ICU | DMAC activation request select register 3 | DMRSR3 | 8 | 8 | | 2 ICLK |
| 0008 7500h | ICU | IRQ control register 0 | IRQCR0 | 8 | 8 | | 2 ICLK |
| 0008 7501h | ICU | IRQ control register 1 | IRQCR1 | 8 | 8 | | 2 ICLK |
| 0008 7502h | ICU | IRQ control register 2 | IRQCR2 | 8 | 8 | | 2 ICLK |
| 0008 7503h | ICU | IRQ control register 3 | IRQCR3 | 8 | 8 | | 2 ICLK |
| 0008 7504h | ICU | IRQ control register 4 | IRQCR4 | 8 | 8 | | 2 ICLK |
| 0008 7505h | ICU | IRQ control register 5 | IRQCR5 | 8 | 8 | | 2 ICLK |
| 0008 7506h | ICU | IRQ control register 6 | IRQCR6 | 8 | 8 | | 2 ICLK |
| 0008 7507h | ICU | IRQ control register 7 | IRQCR7 | 8 | 8 | | 2 ICLK |
| 0008 7510h | ICU | IRQ pin digital filter enable register 0 | IRQFLTE0 | 8 | 8 | | 2 ICLK |
| 0008 7514h | ICU | IRQ pin digital filter setting register 0 | IRQFLTC0 | 16 | 16 | | 2 ICLK |
| 0008 7580h | ICU | Non-maskable interrupt status register | NMISR | 8 | 8 | | 2 ICLK |
| 0008 7581h | ICU | Non-maskable interrupt enable register | NMIER | 8 | 8 | | 2 ICLK |
| 0008 7582h | ICU | Non-maskable interrupt clear register | NMICLR | 8 | 8 | | 2 ICLK |

**Table 4.1 List of I/O Registers (Address Order) (18 / 29)**

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles: ICLK ≥ PCLK | Number of Access Cycles: ICLK < PCLK |
|---|---|---|---|---|---|---|---|
| 0008 A064h | SCI3 | Serial status register | SSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 A065h | SCI3 | Receive data register | RDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 A066h | SCI3 | Smart card mode register | SCMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 A067h | SCI3 | Serial extended mode register | SEMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 A068h | SCI3 | Noise filter setting register | SNFR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 A069h | SCI3 | $I^2C$ mode register 1 | SIMR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 A06Ah | SCI3 | $I^2C$ mode register 2 | SIMR2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 A06Bh | SCI3 | $I^2C$ mode register 3 | SIMR3 | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 A06Ch | SCI3 | $I^2C$ status register | SISR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 A06Dh | SCI3 | SPI mode register | SPMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 A080h | SCI4 | Serial mode register | SMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 A081h | SCI4 | Bit rate register | BRR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 A082h | SCI4 | Serial control register | SCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 A083h | SCI4 | Transmit data register | TDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 A084h | SCI4 | Serial status register | SSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 A085h | SCI4 | Receive data register | RDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 A086h | SCI4 | Smart card mode register | SCMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 A087h | SCI4 | Serial extended mode register | SEMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 A088h | SCI4 | Noise filter setting register | SNFR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 A089h | SCI4 | $I^2C$ mode register 1 | SIMR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 A08Ah | SCI4 | $I^2C$ mode register 2 | SIMR2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 A08Bh | SCI4 | $I^2C$ mode register 3 | SIMR3 | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 A08Ch | SCI4 | $I^2C$ status register | SISR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 A08Dh | SCI4 | SPI mode register | SPMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 A0A0h | SCI5 | Serial mode register | SMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 A0A1h | SCI5 | Bit rate register | BRR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 A0A2h | SCI5 | Serial control register | SCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 A0A3h | SCI5 | Transmit data register | TDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 A0A4h | SCI5 | Serial status register | SSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 A0A5h | SCI5 | Receive data register | RDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 A0A6h | SCI5 | Smart card mode register | SCMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 A0A7h | SCI5 | Serial extended mode register | SEMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 A0A8h | SCI5 | Noise filter setting register | SNFR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 A0A9h | SCI5 | $I^2C$ mode register 1 | SIMR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 A0AAh | SCI5 | $I^2C$ mode register 2 | SIMR2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 A0ABh | SCI5 | $I^2C$ mode register 3 | SIMR3 | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 A0ACh | SCI5 | $I^2C$ status register | SISR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 A0ADh | SCI5 | SPI mode register | SPMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 A0C0h | SCI6 | Serial mode register | SMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 A0C1h | SCI6 | Bit rate register | BRR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 A0C2h | SCI6 | Serial control register | SCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 A0C3h | SCI6 | Transmit data register | TDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 A0C4h | SCI6 | Serial status register | SSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 A0C5h | SCI6 | Receive data register | RDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 A0C6h | SCI6 | Smart card mode register | SCMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 A0C7h | SCI6 | Serial extended mode register | SEMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 A0C8h | SCI6 | Noise filter setting register | SNFR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 A0C9h | SCI6 | $I^2C$ mode register 1 | SIMR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 A0CAh | SCI6 | $I^2C$ mode register 2 | SIMR2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 A0CBh | SCI6 | $I^2C$ mode register 3 | SIMR3 | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 A0CCh | SCI6 | $I^2C$ status register | SISR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |

[Chip version C]

**Table 5.9 DC Characteristics (8)**

Conditions: VCC = AVCC0 = 2.7 to 5.5 V, VSS = AVSS0 = VREFL = VREFL0 = 0 V, $T_a$ = –40 to +105°C

| Item | | | | | Symbol | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|---|---|
| Supply current*1 | High-speed operating mode | Normal operating mode | No peripheral operation*2 | ICLK = 50 MHz | $I_{CC}$ | 10 | — | mA | |
| | | | All peripheral operation: Normal*3 | ICLK = 50 MHz | | 31.5 | — | | |
| | | | All peripheral operation: Max.*3 | ICLK = 50 MHz | | — | 55 | | |
| | | Sleep mode | No peripheral operation | ICLK = 50 MHz | | 7.5 | — | | |
| | | | All peripheral operation: Normal | ICLK = 50 MHz | | 17.5 | — | | |
| | | All-module clock stop mode | | ICLK = 50 MHz | | 6.7 | — | | |
| | | Increase during BGO operation*4 | | | | 25 | — | | |

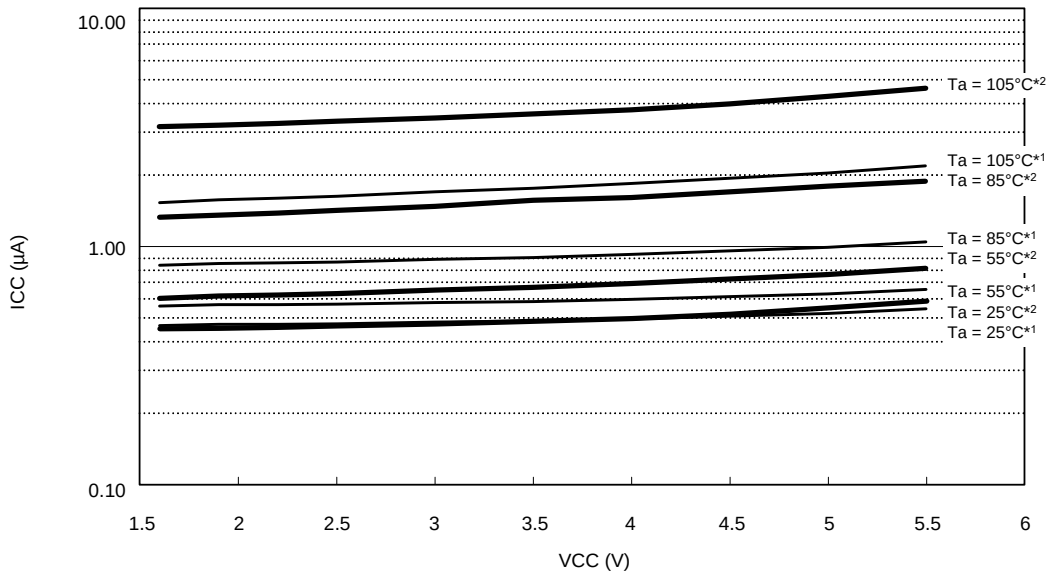
Note 1. Supply current values do not include output charge/discharge current from all pins. The values apply when internal pull-up MOSs are in the off state.

Note 2. Clock supply to the peripheral functions is stopped. This does not include BGO operation. The clock source is PLL and the VCO oscillation frequency is 100 MHz. BCLK, FCLK, and PCLK are set to divided by 64.

Note 3. Clocks are supplied to the peripheral functions. This does not include BGO operation. The clock source is PLL and the VCO oscillation frequency is 100 MHz. BCLK, FCLK, and PCLK are ICLK divided by 2.

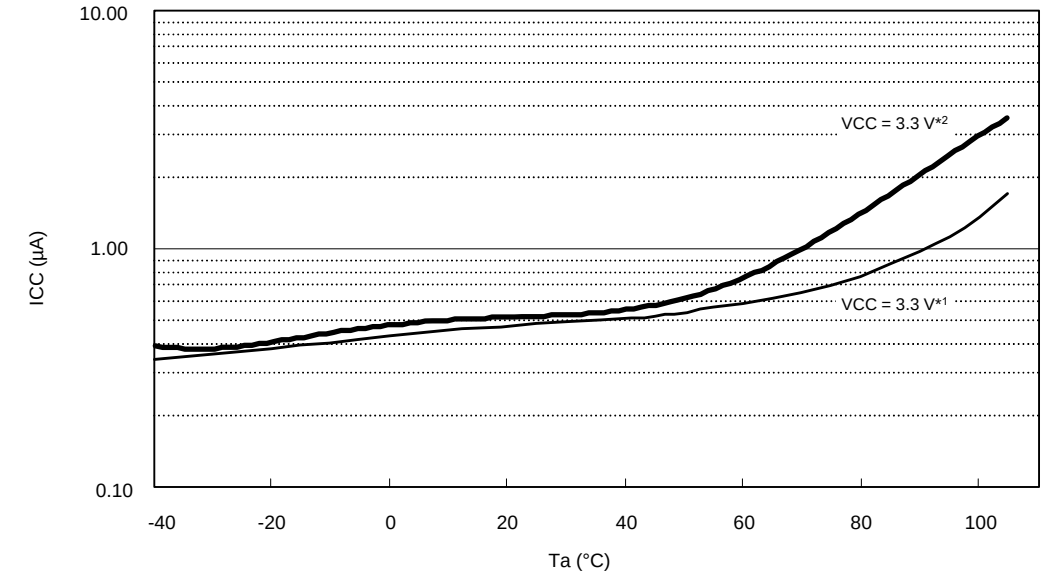
Note 4. This is the increase if data is programmed to or erasing from the ROM or E2 DataFlash during program execution.

Note 5. Clocks are supplied to the peripheral functions. This does not include BGO operation. The clock source is HOCO and the oscillation frequency is 40 MHz. BCLK, FCLK, and PCLK are ICLK divided by 1.
Note 6. This is the increase if data is programmed to or erasing from the ROM or E2 DataFlash during program execution.
Note 7. Clock supply to the peripheral functions is stopped. This does not include BGO operation. The clock source is HOCO and the oscillation frequency is 32 MHz. BCLK, FCLK, and PCLK are set to divided by 64.
Note 8. Clocks are supplied to the peripheral functions. This does not include BGO operation. The clock source is HOCO and the oscillation frequency is 32 MHz. BCLK, FCLK, and PCLK are ICLK divided by 1.
Note 9. Clock supply to the peripheral functions is stopped. This does not include BGO operation. The clock source is the sub oscillation circuit. BCLK, FCLK, and PCLK are set to divided by 64.
Note 10. Clocks are supplied to the peripheral functions. This does not include BGO operation. The clock source is the sub oscillation circuit. BCLK, FCLK, and PCLK are ICLK divided by 1.
Note 11. Value when the main clock continues oscillating at 12.5 MHz.




Note 1. Average value of the tested middle samples during product evaluation.
Note 2. Average value of the tested upper-limit samples during product evaluation.

**Figure 5.15 Voltage Dependency in Deep Software Standby Mode (DEEPCUT1 Bit = 1) (Reference Data) for Chip Version C**




Note 1. Average value of the tested middle samples during product evaluation
Note 2. Average value of the tested upper-limit samples during product evaluation.

**Figure 5.16 Temperature Dependency in Deep Software Standby Mode (DEEPCUT1 Bit = 1) (Reference Data) for Chip Version C**

[Chip version B with 256 Kbytes or less of flash memory and 48 to 100 pins]

**Table 5.14 DC Characteristics (13)**

Conditions: VCC = AVCC0 = 1.62 to 5.5 V, VSS = AVSS0 = 0 V, $T_a$ = –40 to +105°C

| Item | | | | Symbol | Typ.*3 | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|---|
| Supply current*1 | Software standby mode*2 | Flash memory power supplied, HOCO power supplied, POR low power consumption function disabled (SOFTCUT[2:0] bits = 000b) | $T_a$ = 25°C | $I_{CC}$ | 10 | 18 | µA | |
| | | | $T_a$ = 55°C | | 13 | 35 | | |
| | | | $T_a$ = 85°C | | 20 | 81 | | |
| | | | $T_a$ = 105°C | | 34 | 154 | | |
| | | Flash memory power supplied, HOCO power not supplied, POR low power consumption function enabled (SOFTCUT[2:0] bits = 110b) | $T_a$ = 25°C | | 1.8 | 7.7 | | |
| | | | $T_a$ = 55°C | | 3.3 | 20 | | |
| | | | $T_a$ = 85°C | | 9.2 | 60 | | |
| | | | $T_a$ = 105°C | | 20 | 124 | | |
| | Deep software standby mode*2 | Flash memory power not supplied, HOCO power not supplied, POR low power consumption function enabled (DEEPCUT1 bit = 1) | $T_a$ = 25°C | | 0.4 | 0.8 | | |
| | | | $T_a$ = 55°C | | 0.5 | 1.0 | | |
| | | | $T_a$ = 85°C | | 0.7 | 2.5 | | |
| | | | $T_a$ = 105°C | | 1.4 | 6.3 | | |
| | Increments produced by running voltage detection circuits and disabling the POR low power consumption function | | | | 1.4 | — | | |
| | Increment for RTC operation (low CL) | | | | 0.8 | — | | |
| | Increment for RTC operation (standard CL) | | | | 2.0 | — | | |

Note 1. Supply current values are with all output pins unloaded and all input pull-up MOSs in the off state.
Note 2. The IWDT and LVD are stopped.
Note 3. VCC = 3.3 V.

[Chip version B with 768 Kbytes/1 Mbyte of flash memory and 100 to 145 pins]

**Table 5.15 DC Characteristics (14)**

Conditions: VCC = AVCC0 = 2.7 to 5.5 V, VSS = AVSS0 = VREFL = VREFL0 = 0 V, $T_a$ = –40 to +105°C

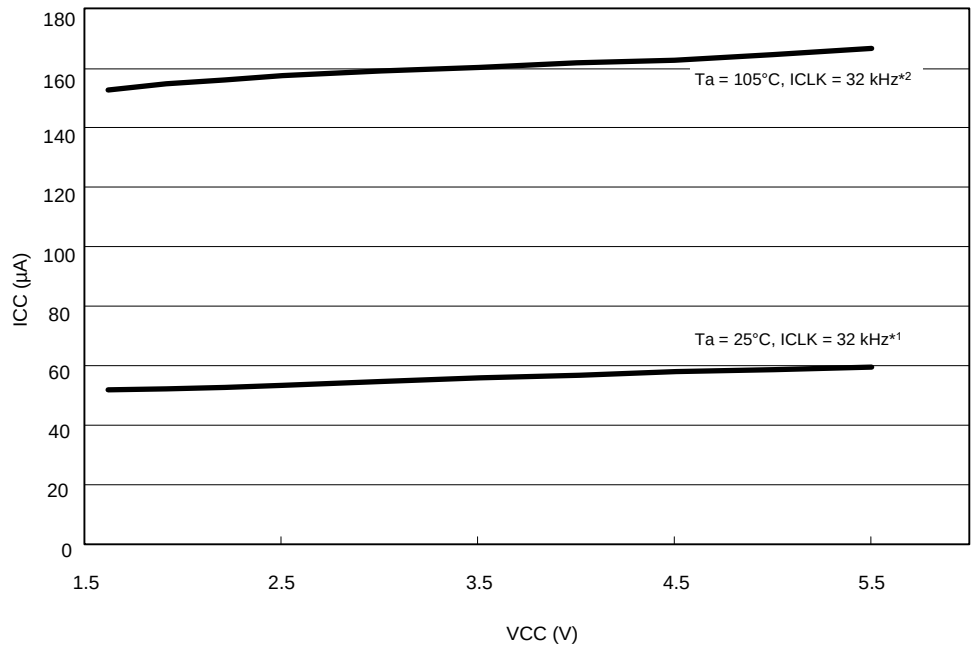
| Item | | | | | Symbol | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|---|---|
| Supply current*1 | High-speed operating mode | Normal operating mode | No peripheral operation*2 | ICLK = 50 MHz | $I_{CC}$ | 7.8 | — | mA | |
| | | | All peripheral operation: Normal*3 | ICLK = 50 MHz | | 29.8 | — | | |
| | | | All peripheral operation: Max.*3 | ICLK = 50 MHz | | — | 45 | | |
| | | Sleep mode | No peripheral operation | ICLK = 50 MHz | | 4.3 | — | | |
| | | | All peripheral operation: Normal | ICLK = 50 MHz | | 13.5 | — | | |
| | | All-module clock stop mode | | | | 3.7 | — | | |
| | | Increase during BGO operation*4 | | | | 23 | — | | |

Note 1. Supply current values do not include output charge/discharge current from all pins. The values apply when internal pull-up MOSs are in the off state.

Note 2. Clock supply to the peripheral functions is stopped. This does not include BGO operation. The clock source is PLL and the VCO oscillation frequency is 100 MHz. BCLK, FCLK, and PCLK are set to divided by 64.

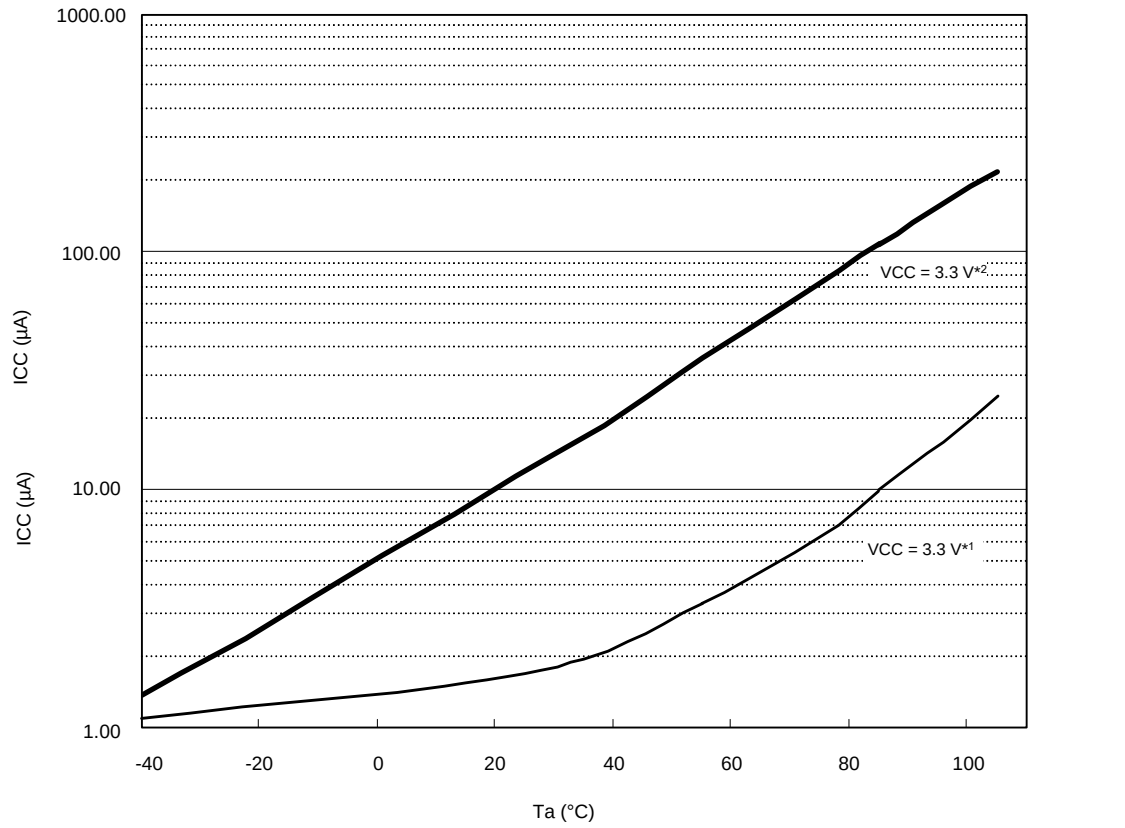
Note 3. Clocks are supplied to the peripheral functions. This does not include BGO operation. The clock source is PLL and the VCO oscillation frequency is 100 MHz. BCLK, FCLK, and PCLK are ICLK divided by 2.

Note 4. This is the increase if data is programmed to or erasing from the ROM or E2 DataFlash during program execution.




Note 1. All peripheral operation is normal.
Average value of the tested middle samples during product evaluation.
Note 2. All peripheral operation is maximum.
Average value of the tested upper-limit samples during product evaluation.

**Figure 5.30 Voltage Dependency in Low-Speed Operating Mode 2 (Reference Data) for Chip Version B with 768 Kbytes/1 Mbyte of Flash Memory and 100 to 145 Pins**




Note 1. Average value of the tested middle samples during product evaluation.
Note 2. Average value of the tested upper-limit samples during product evaluation.

**Figure 5.32 Temperature Dependency in Software Standby Mode (SOFTCUT[2:0] Bits = 110b) (Reference Data) for Chip Version B with 768 Kbytes/1 Mbyte of Flash Memory and 100 to 145 Pins**

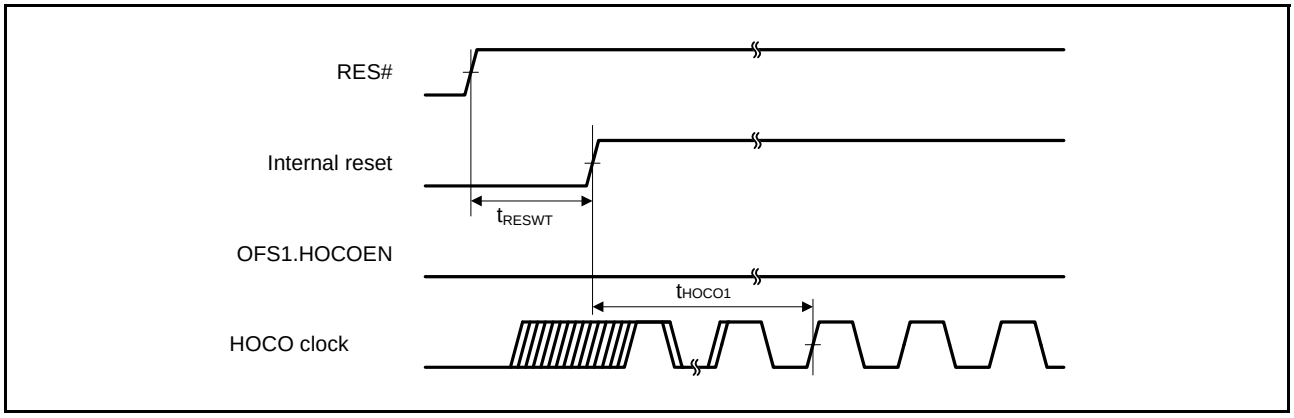



**Figure 5.63 HOCO Clock Oscillation Start Timing (After Reset is Canceled by Setting the OFS1.HOCOEN Bit to 0)**

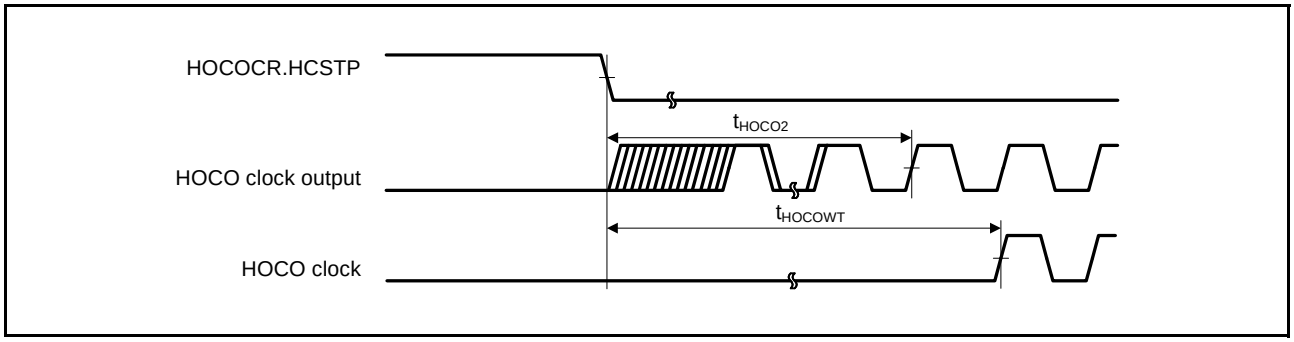



**Figure 5.64 HOCO Clock Oscillation Start Timing (Oscillation is Started by Setting the HOCOCR.HCSTP Bit)**

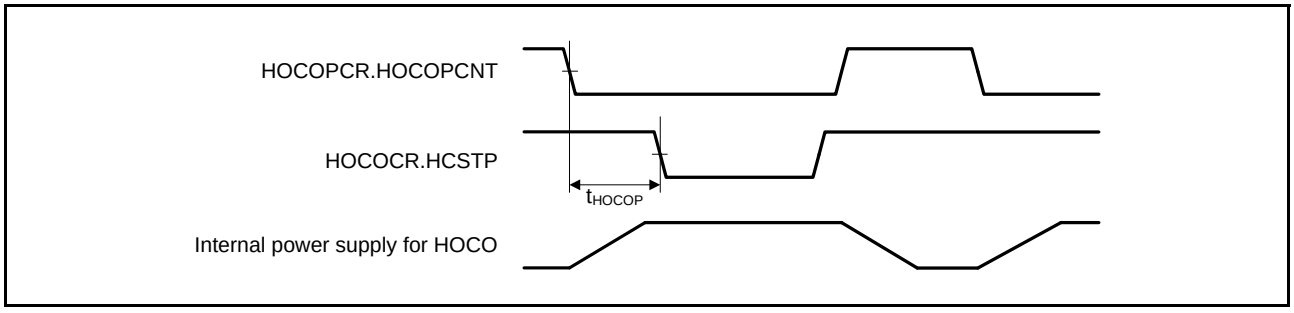



**Figure 5.65 HOCO Power Control Timing**

## 5.3.5 Bus Timing

**Table 5.49 Bus Timing (1)**

Conditions: VCC = AVCC0 = 2.7 to 5.5 V, VSS = AVSS0 = VREFL = VREFL0 = 0 V,
fBCLK ≤ 25 MHz (BCLK pin output frequency ≤ 12.5 MHz), $T_a$ = –40 to +105°C, $V_{OH}$ = VCC × 0.5,
$V_{OL}$ = VCC × 0.5, $I_{OH}$ = –1.0 mA, $I_{OL}$ = 1.0 mA, $C_L$ = 30 pF
When normal output is selected by the drive capacity register

| Item | Symbol | Min. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|
| Address delay time | $t_{AD}$ | — | 60 | ns | Figure 5.76 to Figure 5.79 |
| Byte control delay time | $t_{BCD}$ | — | 60 | ns | |
| CS# delay time | $t_{CSD}$ | — | 60 | ns | |
| RD# delay time | $t_{RSD}$ | — | 60 | ns | |
| Read data setup time | $t_{RDS}$ | 40 | — | ns | |
| Read data hold time | $t_{RDH}$ | 0 | — | ns | |
| WR# delay time | $t_{WRD}$ | — | 60 | ns | |
| Write data delay time | $t_{WDD}$ | — | 60 | ns | |
| Write data hold time | $t_{WDH}$ | 0 | — | ns | |
| WAIT# setup time | $t_{WTS}$ | 40 | — | ns | Figure 5.80 |
| WAIT# hold time | $t_{WTH}$ | 0 | — | ns | |

**Table 5.50 Bus Timing (2)**

Conditions: VCC = AVCC0 = 1.8 to 2.7 V, VSS = AVSS0 = VREFL = VREFL0 = 0 V,
fBCLK ≤ 16 MHz (BCLK pin output frequency ≤ 8 MHz), $T_a$ = –40 to +105°C, $V_{OH}$ = VCC × 0.5,
$V_{OL}$ = VCC × 0.5, $I_{OH}$ = –1.0 mA, $I_{OL}$ = 1.0 mA, $C_L$ = 30 pF
When normal output is selected by the drive capacity register

| Item | Symbol | Min. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|
| Address delay time | $t_{AD}$ | — | 90 | ns | Figure 5.76 to Figure 5.79 |
| Byte control delay time | $t_{BCD}$ | — | 90 | ns | |
| CS# delay time | $t_{CSD}$ | — | 90 | ns | |
| RD# delay time | $t_{RSD}$ | — | 90 | ns | |
| Read data setup time | $t_{RDS}$ | 60 | — | ns | |
| Read data hold time | $t_{RDH}$ | 0 | — | ns | |
| WR# delay time | $t_{WRD}$ | — | 90 | ns | |
| Write data delay time | $t_{WDD}$ | — | 90 | ns | |
| Write data hold time | $t_{WDH}$ | 0 | — | ns | |
| WAIT# setup time | $t_{WTS}$ | 60 | — | ns | Figure 5.80 |
| WAIT# hold time | $t_{WTH}$ | 0 | — | ns | |

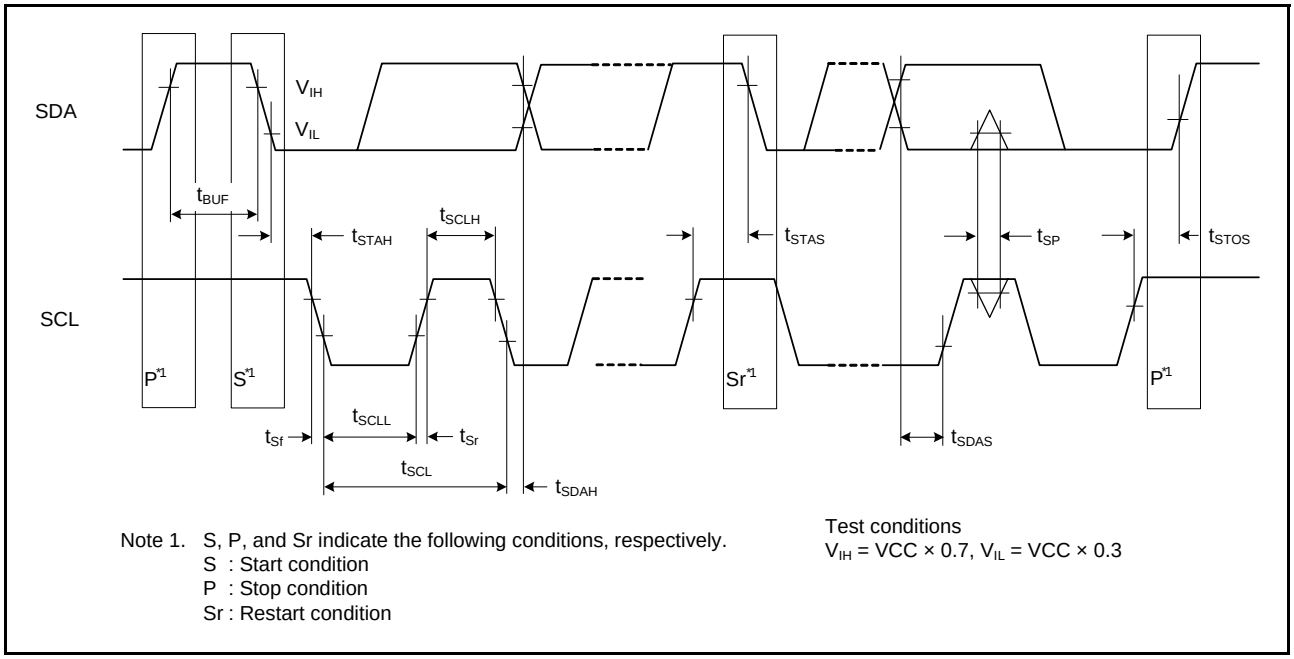



**Figure 5.98 RIIC Bus Interface Input/Output Timing and Simple IIC Bus Interface Input/Output Timing**