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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I²C, SCI, SPI
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	34
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.62V ~ 5.5V
Data Converters	A/D 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f52106bdfl-30

Table 1.4 List of Products Chip Version B: D Version (Ta = –40 to +85°C)

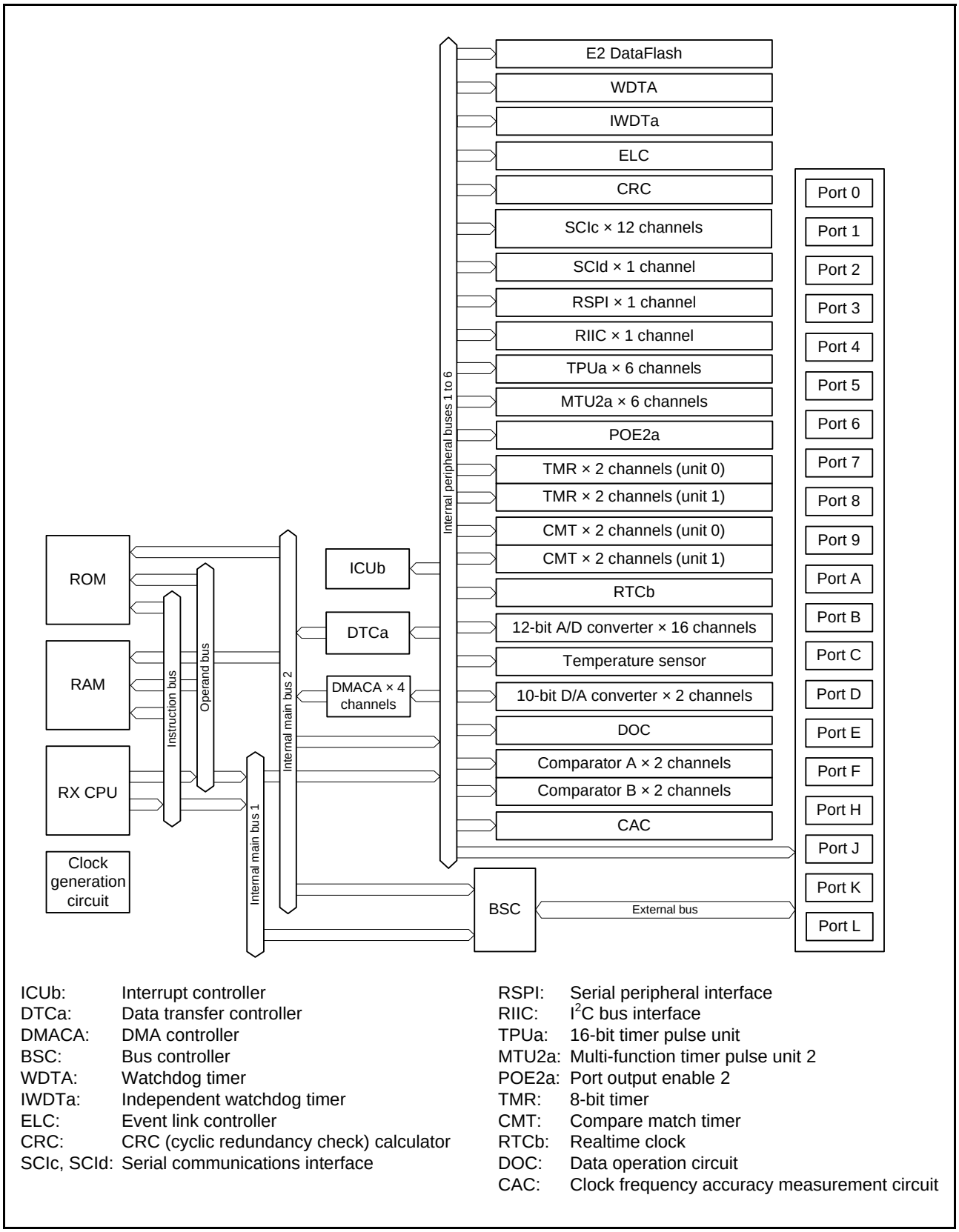
Group	Part No.	Orderable Part No.	Package	ROM Capacity	RAM Capacity	E2 DataFlash	Operating Frequency (Max.)	Operating Temperature
RX210	R5F5210BBDFB	R5F5210BBDFB#30	PLQP0144KA-A	1 Mbytes	96 Kbytes	8 Kbytes	50 MHz	–40 to +85°C
	R5F5210BBDLK	R5F5210BBDLK#U0	PTLG0145KA-A					
	R5F5210BBDFP	R5F5210BBDFP#30	PLQP0100KB-A					
	R5F5210BBDLJ	R5F5210BBDLJ#U0	PTLG0100JA-A					
	R5F5210ABDFB	R5F5210ABDFB#30	PLQP0144KA-A	768 Kbytes				
	R5F5210ABDLK	R5F5210ABDLK#U0	PTLG0145KA-A					
	R5F5210ABDFP	R5F5210ABDFP#30	PLQP0100KB-A					
	R5F5210ABDLJ	R5F5210ABDLJ#U0	PTLG0100JA-A					
	R5F52108BDFB	R5F52108BDFB#30	PLQP0144KA-A	512 Kbytes	64 Kbytes			
	R5F52108BDLK	R5F52108BDLK#U0	PTLG0145KA-A					
	R5F52107BDFB	R5F52107BDFB#30	PLQP0144KA-A	384 Kbytes				
	R5F52107BDLK	R5F52107BDLK#U0	PTLG0145KA-A					
	R5F52106BDFB	R5F52106BDFB#30	PLQP0144KA-A	256 Kbytes	32 Kbytes			
	R5F52106BDLK	R5F52106BDLK#U0	PTLG0145KA-A					
	R5F52106BDFP	R5F52106BDFP#30	PLQP0100KB-A					
	R5F52106BDFN	R5F52106BDFN#30	PLQP0080KB-A					
	R5F52106BDFM	R5F52106BDFM#30	PLQP0064KB-A					
	R5F52106BDFL	R5F52106BDFL#30	PLQP0048KB-A					
	R5F52106BDLJ	R5F52106BDLJ#U0	PTLG0100JA-A					
	R5F52106BDLA	R5F52106BDLA#U0	PTLG0100KA-A					
	R5F52106BDFF	R5F52106BDFF#V0	PLQP0080JA-A					
	R5F52106BDFK	R5F52106BDFK#30	PLQP0064GA-A					
	R5F52106BDLH	R5F52106BDLH#U0	PTLG0064JA-A					
	R5F52106BDBM *1	R5F52106BDBM#W0 *1	SWBG0069LA-A					
	R5F52105BDFB	R5F52105BDFB#30	PLQP0144KA-A	128 Kbytes	20 Kbytes			
	R5F52105BDLK	R5F52105BDLK#U0	PTLG0145KA-A					
	R5F52105BDFP	R5F52105BDFP#30	PLQP0100KB-A					
	R5F52105BDFN	R5F52105BDFN#30	PLQP0080KB-A					
	R5F52105BDFM	R5F52105BDFM#30	PLQP0064KB-A					
	R5F52105BDFL	R5F52105BDFL#30	PLQP0048KB-A					
	R5F52105BDLJ	R5F52105BDLJ#U0	PTLG0100JA-A					
	R5F52105BDLA	R5F52105BDLA#U0	PTLG0100KA-A					
	R5F52105BDFF	R5F52105BDFF#V0	PLQP0080JA-A					
	R5F52105BDFK	R5F52105BDFK#30	PLQP0064GA-A					
	R5F52105BDLH	R5F52105BDLH#U0	PTLG0064JA-A					
	R5F52105BDBM *1	R5F52105BDBM#W0 *1	SWBG0069LA-A					
	R5F52104BDFM	R5F52104BDFM#30	PLQP0064KB-A	96 Kbytes	16 Kbytes			
	R5F52104BDFL	R5F52104BDFL#30	PLQP0048KB-A					
	R5F52104BDFF	R5F52104BDFF#V0	PLQP0080JA-A					
	R5F52104BDLH	R5F52104BDLH#U0	PTLG0064JA-A					
	R5F52103BDFM	R5F52103BDFM#30	PLQP0064KB-A	64 Kbytes	12 Kbytes			
	R5F52103BDFL	R5F52103BDFL#30	PLQP0048KB-A					
	R5F52103BDFF	R5F52103BDFF#V0	PLQP0080JA-A					
	R5F52103BDLH	R5F52103BDLH#U0	PTLG0064JA-A					

Note: • Orderable part numbers are current as of when this manual was published. Please make sure to refer to the relevant product page on the Renesas website for the latest part numbers.

Note 1. These products are available for general consumer equipment only.

1.3 Block Diagram

Figure 1.2 shows a block diagram.

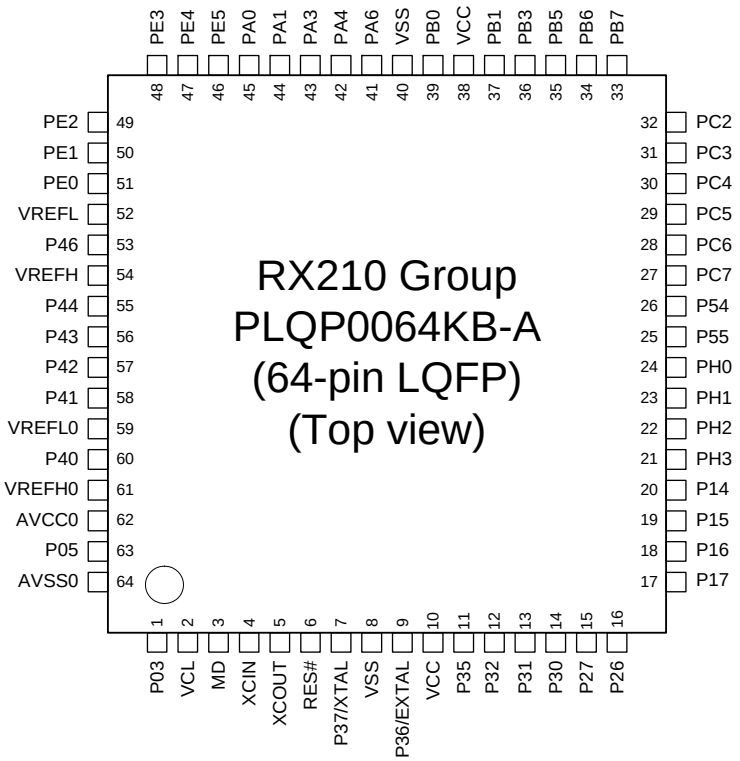


ICUb: Interrupt controller
DTCa: Data transfer controller
DMACA: DMA controller
BSC: Bus controller
WDTA: Watchdog timer
IWDTa: Independent watchdog timer
ELC: Event link controller
CRC: CRC (cyclic redundancy check) calculator
SCIc, SCId: Serial communications interface
RSPI: Serial peripheral interface
RIIC: I^2C bus interface
TPUa: 16-bit timer pulse unit
MTU2a: Multi-function timer pulse unit 2
POE2a: Port output enable 2
TMR: 8-bit timer
CMT: Compare match timer
RTCb: Realtime clock
DOC: Data operation circuit
CAC: Clock frequency accuracy measurement circuit

Figure 1.2 Block Diagram

Table 1.8 Pin Functions (2 / 4)

Classifications	Pin Name	I/O	Description
16-bit timer pulse unit	TIOCA0, TIOCB0 TIOCC0, TIOCD0	I/O	The TGRA0 to TGRD0 input capture input/output compare output/ PWM output pins.
	TIOCA1, TIOCB1	I/O	The TGRA1 and TGRB1 input capture input/output compare output/ PWM output pins.
	TIOCA2, TIOCB2	I/O	The TGRA2 and TGRB2 input capture input/output compare output/ PWM output pins.
	TIOCA3, TIOCB3 TIOCC3, TIOCD3	I/O	The TGRA3 to TGRD3 input capture input/output compare output/ PWM output pins.
	TIOCA4, TIOCB4	I/O	The TGRA4 and TGRB4 input capture input/output compare output/ PWM output pins.
	TIOCA5, TIOCB5	I/O	The TGRA5 and TGRB5 input capture input/output compare output/ PWM output pins.
	TCLKA, TCLKB TCLKC, TCLKD	Input	Input pins for external clock signals.
Multi-function timer pulse unit 2	MTIOC0A, MTIOC0B MTIOC0C, MTIOC0D	I/O	The TGRA0 to TGRD0 input capture input/output compare output/ PWM output pins.
	MTIOC1A, MTIOC1B	I/O	The TGRA1 and TGRB1 input capture input/output compare output/ PWM output pins.
	MTIOC2A, MTIOC2B	I/O	The TGRA2 and TGRB2 input capture input/output compare output/ PWM output pins.
	MTIOC3A, MTIOC3B MTIOC3C, MTIOC3D	I/O	The TGRA3 to TGRD3 input capture input/output compare output/ PWM output pins.
	MTIOC4A, MTIOC4B MTIOC4C, MTIOC4D	I/O	The TGRA4 to TGRD4 input capture input/output compare output/ PWM output pins.
	MTIC5U, MTIC5V, MTIC5W	Input	The TGRU5, TGRV5, and TGRW5 input capture input/external pulse input pins.
	MTCLKA, MTCLKB, MTCLKC, MTCLKD	Input	Input pins for the external clock.
Port output enable 2	POE0# to POE3#, POE8#	Input	Input pins for request signals to place the MTU pins in the high impedance state.
8-bit timer	TMO0 to TMO3	Output	Compare match output pins.
	TMCI0 to TMCI3	Input	Input pins for external clocks to be input to the counter.
	TMRI0 to TMRI3	Input	Input pins for the counter reset.
Realtime clock	RTCOUT	Output	Output pin for 1-Hz clock.
	RTCIC0 to RTCIC2	Input	Time capture event input pins.
Serial communications interface (SCIc)	• Asynchronous mode/clock synchronous mode		
	SCK0 to SCK11	I/O	Input/output pins for the clock
	RXD0 to RXD11	Input	Input pins for received data
	TXD0 to TXD11	Output	Output pins for transmitted data
	CTS0# to CTS11#	Input	Input pins for controlling the start of transmission and reception
	RTS0# to RTS11#	Output	Output pins for controlling the start of transmission and reception
	• Simple I^2C mode		
	SSCL0 to SSCL11	I/O	Input/output pins for the I^2C clock
	SSDA0 to SSDA11	I/O	Input/output pins for the I^2C data
	• Simple SPI mode		
	SCK0 to SCK11	I/O	Input/output pins for the clock
	SMISO0 to SMISO11	I/O	Input/output pins for slave transmission of data
	SMOSI0 to SMOSI11	I/O	Input/output pins for master transmission of data
	SS0# to SS11#	Input	Chip-select input pins



Note: • This figure indicates the power supply pins and I/O port pins. For the pin configuration, see the table “List of Pins and Pin Functions (64-Pin LQFP)”.

Figure 1.10 Pin Assignments of the 64-Pin LQFP

Table 1.9 List of Pins and Pin Functions (145-Pin TFLGA) (1 / 4)

Pin No.	Power Supply, Clock, System Control	I/O Port	External Bus	Timers (MTU, TMR, POE)	Communications (SCIc, SCId, RSPI, RIIC)	Others
A1	AVSS0					
A2		P07				ADTRG0#
A3		P40				AN000
A4		P42				AN002
A5		P45				AN005
A6		P90			TXD7/SMOSI7/SSDA7	
A7		P92			RXD7/SMISO7/SSCL7	
A8		PD2	D2[A2/D2]	MTIOC4D		IRQ2
A9		PD6	D6[A6/D6]	MTIC5V/POE1#		IRQ6
A10		PK3			RXD9/SMISO9/SSCL9	
A11		P62				
A12		PE1	D9[A9/D9]	MTIOC4C	TXD12/TXDX12/SIOX12/ SMOSI12/SSDA12	AN009/CMPB0
A13		PE3	D11[A11/D11]	MTIOC4B/POE8#	CTS12#/RTS12#/SS12#	AN011/CMPA1
B1	VREFH					
B2	AVCC0					
B3		P05				DA1
B4	VREFL0					
B5		P43				AN003
B6		P47				AN007
B7		P91			SCK7	
B8		PD0	D0[A0/D0]			IRQ0
B9		PD4	D4[A4/D4]	POE3#		IRQ4
B10		PK2			TXD9/SMOSI9/SSDA9	
B11		P61			CTS9#/RTS9#/SS9#	
B12		PE2	D10[A10/D10]	MTIOC4A	RXD12/RXDX12/ SMISO12/SSCL12	IRQ7-DS/AN010/ CVREFB0
B13		PE4	D12[A12/D12]	MTIOC4D/MTIOC1A		AN012/CMPA2
C1	VREFL					
C2		P02		TMCI1	SCK6	
C3	VREFH0					
C4		P41				AN001
C5		P46				AN006
C6	VSS					
C7		PD1	D1[A1/D1]	MTIOC4B		IRQ1
C8		PD3	D3[A3/D3]	POE8#		IRQ3
C9		PD7	D7[A7/D7]	MTIC5U/POE0#		IRQ7
C10		P63				
C11		PE0	D8[A8/D8]		SCK12	AN008
C12		P70			SCK4	
C13		PK4			RXD4/SMISO4/SSCL4	
D1		P00		TMRI0	TXD6/SMOSI6/SSDA6	
D2		PF5				IRQ4
D3		P03				DA0
D4		P01		TMCI0	RXD6/SMISO6/SSCL6	
D5	VCC					
D6		P93			CTS7#/RTS7#/SS7#	
D7		PD5	D5[A5/D5]	MTIC5W/POE2#		IRQ5
D8		P60			SCK9	
D9		P64				
D10		PE7	D15[A15/D15]			IRQ7/AN015

Table 1.12 List of Pins and Pin Functions (100-Pin LQFP) (1 / 3)

Pin No.	Power Supply, Clock, System Control	I/O Port	External Bus	Timers (MTU, TMR, POE)	Communications (SCIc, SCId, RSPI, RIIC)	Others
1	VREFH					
2		P03				DA0
3	VREFL					
4		PJ3		MTIOC3C	CTS6#/RTS6#/SS6#	
5	VCL					
6		PJ1		MTIOC3A		
7	MD					FINED
8	XCIN					
9	XCOUT					
10	RES#					
11	XTAL	P37				
12	VSS					
13	EXTAL	P36				
14	VCC					
15		P35				NMI
16		P34		MTIOC0A/TMCI3/ POE2#	SCK6	IRQ4
17		P33		MTIOC0D/TMRI3/ POE3#	RXD6/SMISO6/SSCL6	IRQ3-DS
18		P32		MTIOC0C/TMO3	TXD6/SMOSI6/SSDA6	IRQ2-DS/RTCOUT/ RTCIC2
19		P31		MTIOC4D/TMCI2	CTS1#/RTS1#/SS1#	IRQ1-DS/RTCIC1
20		P30		MTIOC4B/TMRI3/ POE8#	RXD1/SMISO1/SSCL1	IRQ0-DS/RTCIC0
21		P27	CS3#	MTIOC2B/TMCI3	SCK1	
22		P26	CS2#	MTIOC2A/TMO1	TXD1/SMOSI1/SSDA1	
23		P25	CS1#	MTIOC4C/MTCLKB		ADTRG0#
24		P24	CS0#	MTIOC4A/MTCLKA/ TMRI1		
25		P23		MTIOC3D/MTCLKD	CTS0#/RTS0#/SS0#	
26		P22		MTIOC3B/MTCLKC/ TMO0	SCK0	
27		P21		MTIOC1B/TMCI0	RXD0/SMISO0/SSCL0	
28		P20		MTIOC1A/TMRI0	TXD0/SMOSI0/SSDA0	
29		P17		MTIOC3A/MTIOC3B/ TMO1/POE8#	SCK1/MISOA/ SDA-DS	IRQ7
30		P16		MTIOC3C/MTIOC3D/ TMO2	TXD1/SMOSI1/SSDA1/ MOSIA/SCL-DS	IRQ6/RTCOUT/ ADTRG0#
31		P15		MTIOC0B/MTCLKB/ TMCI2	RXD1/SMISO1/SSCL1	IRQ5
32		P14		MTIOC3A/MTCLKA/ TMRI2	CTS1#/RTS1#/SS1#	IRQ4
33		P13		MTIOC0B/TMO3	SDA	IRQ3
34		P12		TMCI1	SCL	IRQ2
35		PH3		TMCI0		
36		PH2		TMRI0		IRQ1
37		PH1		TMO0		IRQ0
38		PH0				CACREF
39		P55	WAIT#	MTIOC4D/TMO3		
40		P54	ALE	MTIOC4B/TMCI1		
41	BCLK	P53				

Table 1.14 List of Pins and Pin Functions (69-Pin WLBGA) (2 / 2)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (MTU, TMR, POE)	Communications (SCIc, SCId, RSPI, RIIC)	Others
G3	NC				
G4		P54	MTIOC4B/TMCI1		
G5		PH1	TMO0		IRQ0
G6		P14	MTIOC3A/MTCLKA/TMRI2	CTS1#/RTS1#/SS1#	IRQ4
G7		P27	MTIOC2B/TMCI3	SCK1	
G8		P32	MTIOC0C/TMO3	TXD6/SMOSI6/SSDA6	IRQ2-DS/RTCOUT/ RTCIC2
G9		P35			NMI
H1		PB7	MTIOC3B	TXD9/SMOSI9/SSDA9	
H2		PC3	MTIOC4D	TXD5/SMOSI5/SSDA5	
H3		PC5	MTIOC3B/MTCLKD/TMRI2	SCK8/RSPCKA	
H4		PC6	MTIOC3C/MTCLKA/TMCI2	RXD8/SMISO8/SSCL8/MOSIA	
H5		P55	MTIOC4D/TMO3		
H6		PH3	TMCI0		
H7		P17	MTIOC3A/MTIOC3B/TMO1/ POE8#	SCK1/MISOA/SDA-DS	IRQ7
H8		P26	MTIOC2A/TMO1	TXD1/SMOSI1/SSDA1	
H9		P30	MTIOC4B/TMRI3/POE8#	RXD1/SMISO1/SSCL1	IRQ0-DS/RTCIC0
J1	NC				
J2		PC2	MTIOC4B	RXD5/SMISO5/SSCL5/SSLA3	
J3		PC4	MTIOC3D/MTCLKC/TMCI1/ POE0#	SCK5/CTS8#/RTS8#/SS8#/ SSLA0	
J4		PC7	MTIOC3A/TMO2/MTCLKB	TXD8/SMOSI8/SSDA8/MISOA	CACREF
J5		PH0			CACREF
J6		PH2	TMRI0		IRQ1
J7		P15	MTIOC0B/MTCLKB/TMCI2	RXD1/SMISO1/SSCL1	IRQ5
J8		P16	MTIOC3C/MTIOC3D/TMO2	TXD1/SMOSI1/SSDA1/ MOSIA/SCL-DS	IRQ6/RTCOUT/ ADTRG0#
J9	NC				

Note: • Pin names to which –DS is appended are for pins that can be used to trigger release from deep software standby mode.
Note: • Leave the NC pin open.

3. Address Space

3.1 Address Space

This LSI has a 4-Gbyte address space, consisting of the range of addresses from 0000 0000h to FFFF FFFFh. That is, linear access to an address space of up to 4 Gbytes is possible, and this contains both program and data areas.
Figure 3.1 shows the memory maps in the respective operating modes. Accessible areas will differ according to the operating mode and states of control bits.

Table 4.1 List of I/O Registers (Address Order) (3 / 29)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles ICLK ≥ PCLK	Number of Access Cycles ICLK < PCLK
0008 3032h	BSC	CS3 mode register	CS3MOD	16	16	1, 2 BCLK	
0008 3034h	BSC	CS3 wait control register 1	CS3WCR1	32	32	1, 2 BCLK	
0008 3038h	BSC	CS3 wait control register 2	CS3WCR2	32	32	1, 2 BCLK	
0008 3802h	BSC	CS0 control register	CS0CR	16	16	1, 2 BCLK	
0008 380Ah	BSC	CS0 recovery cycle register	CS0REC	16	16	1, 2 BCLK	
0008 3812h	BSC	CS1 control register	CS1CR	16	16	1, 2 BCLK	
0008 381Ah	BSC	CS1 recovery cycle register	CS1REC	16	16	1, 2 BCLK	
0008 3822h	BSC	CS2 control register	CS2CR	16	16	1, 2 BCLK	
0008 382Ah	BSC	CS2 recovery cycle register	CS2REC	16	16	1, 2 BCLK	
0008 3832h	BSC	CS3 control register	CS3CR	16	16	1, 2 BCLK	
0008 383Ah	BSC	CS3 recovery cycle register	CS3REC	16	16	1, 2 BCLK	
0008 3880h	BSC	CS recovery cycle insertion enable register	CSRECEN	16	16	1, 2 BCLK	
0008 7010h	ICU	Interrupt request register 016	IR016	8	8	2 ICLK	
0008 7015h	ICU	Interrupt request register 021	IR021	8	8	2 ICLK	
0008 7017h	ICU	Interrupt request register 023	IR023	8	8	2 ICLK	
0008 701Bh	ICU	Interrupt request register 027	IR027	8	8	2 ICLK	
0008 701Ch	ICU	Interrupt request register 028	IR028	8	8	2 ICLK	
0008 701Dh	ICU	Interrupt request register 029	IR029	8	8	2 ICLK	
0008 701Eh	ICU	Interrupt request register 030	IR030	8	8	2 ICLK	
0008 701Fh	ICU	Interrupt request register 031	IR031	8	8	2 ICLK	
0008 7020h	ICU	Interrupt request register 032	IR032	8	8	2 ICLK	
0008 7021h	ICU	Interrupt request register 033	IR033	8	8	2 ICLK	
0008 7022h	ICU	Interrupt request register 034	IR034	8	8	2 ICLK	
0008 702Ch	ICU	Interrupt request register 044	IR044	8	8	2 ICLK	
0008 702Dh	ICU	Interrupt request register 045	IR045	8	8	2 ICLK	
0008 702Eh	ICU	Interrupt request register 046	IR046	8	8	2 ICLK	
0008 702Fh	ICU	Interrupt request register 047	IR047	8	8	2 ICLK	
0008 7039h	ICU	Interrupt request register 057	IR057	8	8	2 ICLK	
0008 703Ah	ICU	Interrupt request register 058	IR058	8	8	2 ICLK	
0008 703Bh	ICU	Interrupt request register 059	IR059	8	8	2 ICLK	
0008 703Fh	ICU	Interrupt request register 063	IR063	8	8	2 ICLK	
0008 7040h	ICU	Interrupt request register 064	IR064	8	8	2 ICLK	
0008 7041h	ICU	Interrupt request register 065	IR065	8	8	2 ICLK	
0008 7042h	ICU	Interrupt request register 066	IR066	8	8	2 ICLK	
0008 7043h	ICU	Interrupt request register 067	IR067	8	8	2 ICLK	
0008 7044h	ICU	Interrupt request register 068	IR068	8	8	2 ICLK	
0008 7045h	ICU	Interrupt request register 069	IR069	8	8	2 ICLK	
0008 7046h	ICU	Interrupt request register 070	IR070	8	8	2 ICLK	
0008 7047h	ICU	Interrupt request register 071	IR071	8	8	2 ICLK	
0008 7058h	ICU	Interrupt request register 088	IR088	8	8	2 ICLK	
0008 7059h	ICU	Interrupt request register 089	IR089	8	8	2 ICLK	
0008 705Ch	ICU	Interrupt request register 092	IR092	8	8	2 ICLK	
0008 705Dh	ICU	Interrupt request register 093	IR093	8	8	2 ICLK	
0008 7066h	ICU	Interrupt request register 102	IR102	8	8	2 ICLK	
0008 7067h	ICU	Interrupt request register 103	IR103	8	8	2 ICLK	
0008 706Ah	ICU	Interrupt request register 106	IR106	8	8	2 ICLK	
0008 706Bh	ICU	Interrupt request register 107	IR107	8	8	2 ICLK	
0008 7072h	ICU	Interrupt request register 114	IR114	8	8	2 ICLK	
0008 7073h	ICU	Interrupt request register 115	IR115	8	8	2 ICLK	
0008 7074h	ICU	Interrupt request register 116	IR116	8	8	2 ICLK	
0008 7075h	ICU	Interrupt request register 117	IR117	8	8	2 ICLK	

Table 4.1 List of I/O Registers (Address Order) (9 / 29)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles ICLK ≥ PCLK	Number of Access Cycles ICLK < PCLK
0008 7301h	ICU	Interrupt source priority register 001	IPR001	8	8	2 ICLK	
0008 7302h	ICU	Interrupt source priority register 002	IPR002	8	8	2 ICLK	
0008 7303h	ICU	Interrupt source priority register 003	IPR003	8	8	2 ICLK	
0008 7304h	ICU	Interrupt source priority register 004	IPR004	8	8	2 ICLK	
0008 7305h	ICU	Interrupt source priority register 005	IPR005	8	8	2 ICLK	
0008 7306h	ICU	Interrupt source priority register 006	IPR006	8	8	2 ICLK	
0008 7307h	ICU	Interrupt source priority register 007	IPR007	8	8	2 ICLK	
0008 7320h	ICU	Interrupt source priority register 032	IPR032	8	8	2 ICLK	
0008 7321h	ICU	Interrupt source priority register 033	IPR033	8	8	2 ICLK	
0008 7322h	ICU	Interrupt source priority register 034	IPR034	8	8	2 ICLK	
0008 732Ch	ICU	Interrupt source priority register 044	IPR044	8	8	2 ICLK	
0008 7339h	ICU	Interrupt source priority register 057	IPR057	8	8	2 ICLK	
0008 733Ah	ICU	Interrupt source priority register 058	IPR058	8	8	2 ICLK	
0008 733Bh	ICU	Interrupt source priority register 059	IPR059	8	8	2 ICLK	
0008 733Fh	ICU	Interrupt source priority register 063	IPR063	8	8	2 ICLK	
0008 7340h	ICU	Interrupt source priority register 064	IPR064	8	8	2 ICLK	
0008 7341h	ICU	Interrupt source priority register 065	IPR065	8	8	2 ICLK	
0008 7342h	ICU	Interrupt source priority register 066	IPR066	8	8	2 ICLK	
0008 7343h	ICU	Interrupt source priority register 067	IPR067	8	8	2 ICLK	
0008 7344h	ICU	Interrupt source priority register 068	IPR068	8	8	2 ICLK	
0008 7345h	ICU	Interrupt source priority register 069	IPR069	8	8	2 ICLK	
0008 7346h	ICU	Interrupt source priority register 070	IPR070	8	8	2 ICLK	
0008 7347h	ICU	Interrupt source priority register 071	IPR071	8	8	2 ICLK	
0008 7358h	ICU	Interrupt source priority register 088	IPR088	8	8	2 ICLK	
0008 7359h	ICU	Interrupt source priority register 089	IPR089	8	8	2 ICLK	
0008 735Ch	ICU	Interrupt source priority register 092	IPR092	8	8	2 ICLK	
0008 735Dh	ICU	Interrupt source priority register 093	IPR093	8	8	2 ICLK	
0008 7366h	ICU	Interrupt source priority register 102	IPR102	8	8	2 ICLK	
0008 7367h	ICU	Interrupt source priority register 103	IPR103	8	8	2 ICLK	
0008 736Ah	ICU	Interrupt source priority register 106	IPR106	8	8	2 ICLK	
0008 736Bh	ICU	Interrupt source priority register 107	IPR107	8	8	2 ICLK	
0008 7372h	ICU	Interrupt source priority register 114	IPR114	8	8	2 ICLK	
0008 7376h	ICU	Interrupt source priority register 118	IPR118	8	8	2 ICLK	
0008 7379h	ICU	Interrupt source priority register 121	IPR121	8	8	2 ICLK	
0008 737Bh	ICU	Interrupt source priority register 123	IPR123	8	8	2 ICLK	
0008 737Dh	ICU	Interrupt source priority register 125	IPR125	8	8	2 ICLK	
0008 737Fh	ICU	Interrupt source priority register 127	IPR127	8	8	2 ICLK	
0008 7381h	ICU	Interrupt source priority register 129	IPR129	8	8	2 ICLK	
0008 7385h	ICU	Interrupt source priority register 133	IPR133	8	8	2 ICLK	
0008 7386h	ICU	Interrupt source priority register 134	IPR134	8	8	2 ICLK	
0008 738Ah	ICU	Interrupt source priority register 138	IPR138	8	8	2 ICLK	
0008 738Bh	ICU	Interrupt source priority register 139	IPR139	8	8	2 ICLK	
0008 738Eh	ICU	Interrupt source priority register 142	IPR142	8	8	2 ICLK	
0008 7392h	ICU	Interrupt source priority register 146	IPR146	8	8	2 ICLK	
0008 7393h	ICU	Interrupt source priority register 147	IPR147	8	8	2 ICLK	
0008 7395h	ICU	Interrupt source priority register 149	IPR149	8	8	2 ICLK	
0008 7397h	ICU	Interrupt source priority register 151	IPR151	8	8	2 ICLK	
0008 7399h	ICU	Interrupt source priority register 153	IPR153	8	8	2 ICLK	
0008 739Bh	ICU	Interrupt source priority register 155	IPR155	8	8	2 ICLK	
0008 739Fh	ICU	Interrupt source priority register 159	IPR159	8	8	2 ICLK	
0008 73A0h	ICU	Interrupt source priority register 160	IPR160	8	8	2 ICLK	

Table 4.1 List of I/O Registers (Address Order) (18 / 29)

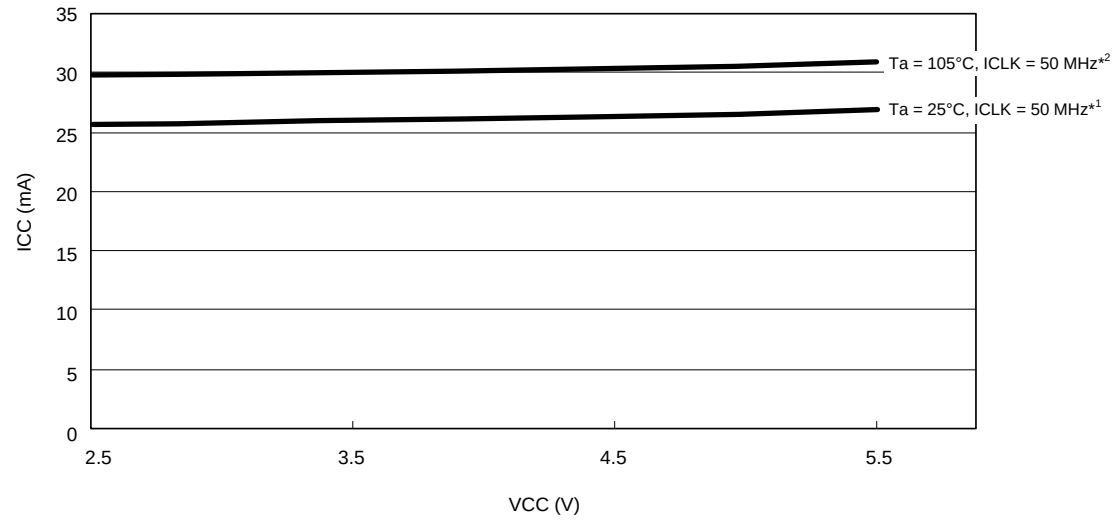
Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles: ICLK ≥ PCLK	Number of Access Cycles: ICLK < PCLK
0008 A064h	SCI3	Serial status register	SSR	8	8	2, 3 PCLKB	2 ICLK
0008 A065h	SCI3	Receive data register	RDR	8	8	2, 3 PCLKB	2 ICLK
0008 A066h	SCI3	Smart card mode register	SCMR	8	8	2, 3 PCLKB	2 ICLK
0008 A067h	SCI3	Serial extended mode register	SEMR	8	8	2, 3 PCLKB	2 ICLK
0008 A068h	SCI3	Noise filter setting register	SNFR	8	8	2, 3 PCLKB	2 ICLK
0008 A069h	SCI3	I^2C mode register 1	SIMR1	8	8	2, 3 PCLKB	2 ICLK
0008 A06Ah	SCI3	I^2C mode register 2	SIMR2	8	8	2, 3 PCLKB	2 ICLK
0008 A06Bh	SCI3	I^2C mode register 3	SIMR3	8	8	2, 3 PCLKB	2 ICLK
0008 A06Ch	SCI3	I^2C status register	SISR	8	8	2, 3 PCLKB	2 ICLK
0008 A06Dh	SCI3	SPI mode register	SPMR	8	8	2, 3 PCLKB	2 ICLK
0008 A080h	SCI4	Serial mode register	SMR	8	8	2, 3 PCLKB	2 ICLK
0008 A081h	SCI4	Bit rate register	BRR	8	8	2, 3 PCLKB	2 ICLK
0008 A082h	SCI4	Serial control register	SCR	8	8	2, 3 PCLKB	2 ICLK
0008 A083h	SCI4	Transmit data register	TDR	8	8	2, 3 PCLKB	2 ICLK
0008 A084h	SCI4	Serial status register	SSR	8	8	2, 3 PCLKB	2 ICLK
0008 A085h	SCI4	Receive data register	RDR	8	8	2, 3 PCLKB	2 ICLK
0008 A086h	SCI4	Smart card mode register	SCMR	8	8	2, 3 PCLKB	2 ICLK
0008 A087h	SCI4	Serial extended mode register	SEMR	8	8	2, 3 PCLKB	2 ICLK
0008 A088h	SCI4	Noise filter setting register	SNFR	8	8	2, 3 PCLKB	2 ICLK
0008 A089h	SCI4	I^2C mode register 1	SIMR1	8	8	2, 3 PCLKB	2 ICLK
0008 A08Ah	SCI4	I^2C mode register 2	SIMR2	8	8	2, 3 PCLKB	2 ICLK
0008 A08Bh	SCI4	I^2C mode register 3	SIMR3	8	8	2, 3 PCLKB	2 ICLK
0008 A08Ch	SCI4	I^2C status register	SISR	8	8	2, 3 PCLKB	2 ICLK
0008 A08Dh	SCI4	SPI mode register	SPMR	8	8	2, 3 PCLKB	2 ICLK
0008 A0A0h	SCI5	Serial mode register	SMR	8	8	2, 3 PCLKB	2 ICLK
0008 A0A1h	SCI5	Bit rate register	BRR	8	8	2, 3 PCLKB	2 ICLK
0008 A0A2h	SCI5	Serial control register	SCR	8	8	2, 3 PCLKB	2 ICLK
0008 A0A3h	SCI5	Transmit data register	TDR	8	8	2, 3 PCLKB	2 ICLK
0008 A0A4h	SCI5	Serial status register	SSR	8	8	2, 3 PCLKB	2 ICLK
0008 A0A5h	SCI5	Receive data register	RDR	8	8	2, 3 PCLKB	2 ICLK
0008 A0A6h	SCI5	Smart card mode register	SCMR	8	8	2, 3 PCLKB	2 ICLK
0008 A0A7h	SCI5	Serial extended mode register	SEMR	8	8	2, 3 PCLKB	2 ICLK
0008 A0A8h	SCI5	Noise filter setting register	SNFR	8	8	2, 3 PCLKB	2 ICLK
0008 A0A9h	SCI5	I^2C mode register 1	SIMR1	8	8	2, 3 PCLKB	2 ICLK
0008 A0AAh	SCI5	I^2C mode register 2	SIMR2	8	8	2, 3 PCLKB	2 ICLK
0008 A0ABh	SCI5	I^2C mode register 3	SIMR3	8	8	2, 3 PCLKB	2 ICLK
0008 A0ACh	SCI5	I^2C status register	SISR	8	8	2, 3 PCLKB	2 ICLK
0008 A0ADh	SCI5	SPI mode register	SPMR	8	8	2, 3 PCLKB	2 ICLK
0008 A0C0h	SCI6	Serial mode register	SMR	8	8	2, 3 PCLKB	2 ICLK
0008 A0C1h	SCI6	Bit rate register	BRR	8	8	2, 3 PCLKB	2 ICLK
0008 A0C2h	SCI6	Serial control register	SCR	8	8	2, 3 PCLKB	2 ICLK
0008 A0C3h	SCI6	Transmit data register	TDR	8	8	2, 3 PCLKB	2 ICLK
0008 A0C4h	SCI6	Serial status register	SSR	8	8	2, 3 PCLKB	2 ICLK
0008 A0C5h	SCI6	Receive data register	RDR	8	8	2, 3 PCLKB	2 ICLK
0008 A0C6h	SCI6	Smart card mode register	SCMR	8	8	2, 3 PCLKB	2 ICLK
0008 A0C7h	SCI6	Serial extended mode register	SEMR	8	8	2, 3 PCLKB	2 ICLK
0008 A0C8h	SCI6	Noise filter setting register	SNFR	8	8	2, 3 PCLKB	2 ICLK
0008 A0C9h	SCI6	I^2C mode register 1	SIMR1	8	8	2, 3 PCLKB	2 ICLK
0008 A0CAh	SCI6	I^2C mode register 2	SIMR2	8	8	2, 3 PCLKB	2 ICLK
0008 A0CBh	SCI6	I^2C mode register 3	SIMR3	8	8	2, 3 PCLKB	2 ICLK
0008 A0CCh	SCI6	I^2C status register	SISR	8	8	2, 3 PCLKB	2 ICLK

[Chip version B with 512 Kbytes or less of flash memory and 144 and 145 pins]

Table 5.19 DC Characteristics (18)

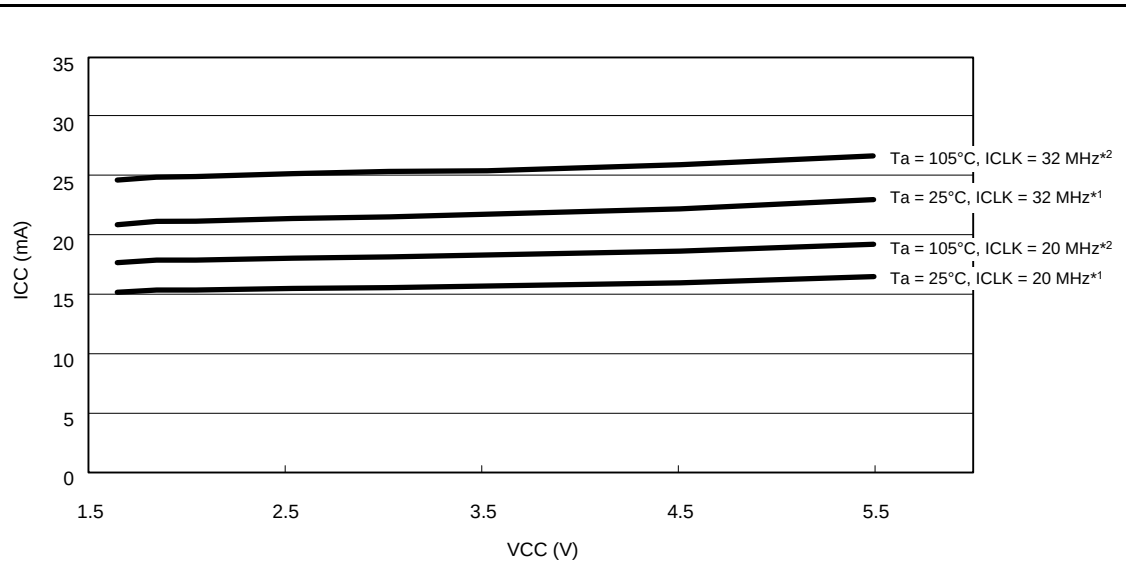
Conditions: VCC = AVCC0 = 1.62 to 5.5 V, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +105°C

Item					Symbol	Typ.	Max.	Unit	Test Conditions
Supply current*1	Middle-speed operating modes 1A and 1B	Normal operating mode	No peripheral operation	ICLK = 32 MHz*2	I_{CC}	5.3	—	mA	
				ICLK = 20 MHz*3		4.6	—		
			All peripheral operation: Normal	ICLK = 32 MHz*4		22.3	—		
				ICLK = 20 MHz*5		15.6	—		
			All peripheral operation: Max.	ICLK = 32 MHz*4		—	35		
				ICLK = 20 MHz*5		—	—		
		Sleep mode	No peripheral operation	ICLK = 32 MHz		3.4	—		
				ICLK = 20 MHz		3.3	—		
			All peripheral operation: Normal	ICLK = 32 MHz		12.8	—		
				ICLK = 20 MHz		9.8	—		
		All-module clock stop mode		ICLK = 32 MHz		3	—		
				ICLK = 20 MHz		3	—		
		Increase during BGO operation*6	Middle-speed operating mode 1A			21	—		
			Middle-speed operating mode 1B			19	—		
	Middle-speed operating modes 2A and 2B	Normal operating mode	No peripheral operation*2	ICLK = 32 MHz		4.7	—		
				ICLK = 16 MHz		3.4	—		
				ICLK = 8 MHz		2.7	—		
			All peripheral operation: Normal*4	ICLK = 32 MHz*3		21.7	—		
				ICLK = 16 MHz*3		12.3	—		
				ICLK = 8 MHz		7.6	—		
			All peripheral operation: Max.*4	ICLK = 32 MHz*3		—	34		
				ICLK = 16 MHz*3		—	—		
				ICLK = 8 MHz		—	—		
		Sleep mode	No peripheral operation	ICLK = 32 MHz		2.9	—		
				ICLK = 16 MHz		2.5	—		
				ICLK = 8 MHz		2.2	—		
			All peripheral operation: Normal	ICLK = 32 MHz		12.3	—		
				ICLK = 16 MHz		7.8	—		
				ICLK = 8 MHz		5.6	—		
		All-module clock stop mode		ICLK = 32 MHz		2.5	—		
				ICLK = 16 MHz		2.2	—		
				ICLK = 8 MHz		2.1	—		
		Increase during BGO operation*6	Middle-speed operating mode 1A			21	—		
			Middle-speed operating mode 1B			19	—		



Note 1. All peripheral operation is normal. This does not include BGO operation.
Average value of the tested middle samples during product evaluation
Note 2. All peripheral operation is maximum. This does not include BGO operation.
Average value of the tested upper-limit samples during product evaluation.

Figure 5.35 Voltage Dependency in High-Speed Operating Mode (Reference Data) for Chip Version B with 512 Kbytes or Less of Flash Memory and 144 and 145 Pins



Note 1. All peripheral operation is normal. This does not include BGO operation.
Average value of the tested middle samples during product evaluation
Note 2. All peripheral operation is maximum. This does not include BGO operation.
Average value of the tested upper-limit samples during product evaluation.

Figure 5.36 Voltage Dependency in Middle-Speed Operating Modes 1A and 1B (Reference Data) for Chip Version B with 512 Kbytes or Less of Flash Memory and 144 and 145 Pins

Table 5.44 Clock Timing

Conditions: VCC = AVCC0 = 1.62 to 5.5 V, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
EXTAL external clock input cycle time		t_{EXcyc}	50	—	—	ns	Figure 5.60
EXTAL external clock input high pulse width		t_{EXH}	20	—	—	ns	
EXTAL external clock input low pulse width		t_{EXL}	20	—	—	ns	
EXTAL external clock rising time		t_{EXr}	—	—	5	ns	
EXTAL external clock falling time		t_{EXf}	—	—	5	ns	
EXTAL external clock input wait time*1		t_{EXWT}	1	—	—	ms	
Main clock oscillator oscillation frequency*2		f_{MAIN}	1	—	20	MHz	
Main clock oscillation stabilization time (crystal)*2		$t_{MAINOSC}$	—	3	—	ms	Figure 5.61
Main clock oscillation stabilization time (ceramic resonator)*2		$t_{MAINOSC}$	—	50		µs	
Main clock oscillation stabilization wait time (crystal)*2		$t_{MAINOSCWT}$	—	6	—	ms	
Main clock oscillation stabilization wait time (ceramic resonator)*2		$t_{MAINOSCWT}$	—	100		µs	
LOCO clock cycle time		t_{cyc}	7.27	8	8.89	µs	
LOCO clock oscillation frequency*6		f_{LOCO}	112.5	125	137.5	kHz	
LOCO clock oscillation stabilization wait time		t_{LOCOWT}	—	—	20	µs	Figure 5.62
HOCO clock oscillation frequency*7		f_{HOCO}	31.680	32	32.320	MHz	Ta = 0 to 50°C
			36.495	36.864	37.233		
			39.600	40	40.400		
			49.500	50	50.500		
			31.520	32	32.480		Ta = -40 to 105°C
			36.311	36.864	37.417		
			39.400	40	40.600		
			49.250	50	50.750		
HOCO clock oscillation stabilization time 1		t_{HOCO1}	—	—	300	µs	Figure 5.63
HOCO clock oscillation stabilization time 2		t_{HOCO2}	—	—	175	µs	Figure 5.64
HOCO clock oscillation stabilization wait time		t_{HOCOWT}	—	—	350	µs	Figure 5.64
HOCO clock power supply stabilization time		t_{HOCOP}	—	—	350	µs	Figure 5.65
PLL input frequency		f_{PLLIN}	4	—	12.5	MHz	
PLL circuit oscillation frequency		f_{PLL}	50	—	100	MHz	
PLL clock oscillation stabilization time	PLL operation started after main clock oscillation has settled	t_{PLL1}	—	—	500	µs	Figure 5.66
PLL clock oscillation stabilization wait time		t_{PLLWT1}	1.5	—	—	ms	
PLL clock oscillation stabilization time*4	PLL operation started before main clock oscillation has settled	t_{PLL2}	—	3.5*3	—	ms	Figure 5.67
PLL clock oscillation stabilization wait time*4		t_{PLLWT2}	—	7	—	ms	
PLL clock power supply stabilization time (for chip version B only)		t_{PLLPW}	—	—	30	µs	Figure 5.68
Sub-clock oscillator oscillation frequency		f_{SUB}	—	32.768	—	kHz	
Sub-clock oscillation stabilization time*5		t_{SUBOSC}	2	—	—	s	Figure 5.69
Sub-clock oscillation stabilization wait time*5		$t_{SUBOSCWT}$	4	—	—	s	

Note 1. The time interval from the time P36 and P37 are configured for input and the main clock oscillator stopping bit (MOSCCR.MOSTP) is set to 0 (operating) until the clock becomes available.

Table 5.51 Bus Timing (3)

Conditions: VCC = AVCC0 = 1.62 to 1.8 V, VSS = AVSS0 = VREFL = VREFL0 = 0 V,
fBCLK ≤ 12 MHz (BCLK pin output frequency ≤ 6 MHz), T_a = –40 to +105°C, V_{OH} = VCC × 0.5,
V_{OL} = VCC × 0.5, I_{OH} = –0.5 mA, I_{OL} = 0.5 mA, C_L = 30 pF
When normal output is selected by the drive capacity register

Item	Symbol	Min.	Max.	Unit	Test Conditions
Address delay time	t_{AD}	—	125	ns	Figure 5.76 to Figure 5.79
Byte control delay time	t_{BCD}	—	125	ns	
CS# delay time	t_{CSD}	—	125	ns	
RD# delay time	t_{RSD}	—	125	ns	
Read data setup time	t_{RDS}	85	—	ns	
Read data hold time	t_{RDH}	0	—	ns	
WR# delay time	t_{WRD}	—	125	ns	
Write data delay time	t_{WDD}	—	125	ns	
Write data hold time	t_{WDH}	0	—	ns	
WAIT# setup time	t_{WTS}	85	—	ns	Figure 5.80
WAIT# hold time	t_{WTH}	0	—	ns	

Item				Symbol	Min.	Max.	Unit*1	Test Conditions
RSPI	Data input setup time	Master	2.7 V ≤ VCC ≤ 5.5 V	t_{SU}	10	—	ns	C = 30pF Figure 5.92 to Figure 5.97
			1.8 V ≤ VCC < 2.7 V		25	—		
			1.62 V ≤ VCC < 1.8 V		30	—		
		Slave			25 – t_{Pcyc}	—		
	Data input hold time	Master	PCLKB set to a division ratio other than divided by 2	t_H	t_{Pcyc}	—	ns	
			PCLKB set to divided by 2*2	t_{HF}	0	—		
		Slave		t_H	20 + 2 × t_{Pcyc}	—		
	SSL setup time	Master		t_{LEAD}	1	8	t_{SPcyc}	
		Slave			4	—	t_{Pcyc}	
	SSL hold time	Master		t_{LAG}	1	8	t_{SPcyc}	
		Slave			4	—	t_{Pcyc}	
	Data output delay time	Master	2.7 V ≤ VCC ≤ 5.5 V	t_{OD}	—	14	ns	
			1.8 V ≤ VCC < 2.7 V		—	20		
			1.62 V ≤ VCC < 1.8 V		—	25		
		Slave	2.7 V ≤ VCC ≤ 5.5 V		—	3 × t_{Pcyc} + 65		
			1.8 V ≤ VCC < 2.7 V		—	3 × tPcyc +85		
			1.62 V ≤ VCC < 1.8 V		—	3 × tPcyc +95		
	Data output hold time	Master		t_{OH}	0	—	ns	
		Slave			0	—		
	Successive transmission delay time	Master		t_{TD}	t_{SPcyc} + 2 × t_{Pcyc}	8 × t_{SPcyc} + 2 × t_{Pcyc}	ns	
		Slave			4 × t_{Pcyc}	—		
	MOSI and MISO rise/fall time	Output	2.7 V ≤ VCC ≤ 5.5 V	t_{Dr}, t_{Df}	—	10	ns	
			1.8 V ≤ VCC < 2.7 V		—	15		
			1.62 V ≤ VCC < 1.8 V		—	20		
		Input			—	1	µs	
	SSL rise/fall time	Output	2.7 V ≤ VCC ≤ 5.5 V	t_{SSLr}, t_{SSLf}	—	10	ns	
			1.8 V ≤ VCC < 2.7 V		—	15		
			1.62 V ≤ VCC < 1.8 V		—	20		
		Input			—	1	µs	
	Slave access time		2.7 V ≤ VCC ≤ 5.5 V	t_{SA}	—	6	t_{Pcyc}	C = 30pF Figure 5.96 and Figure 5.97
			1.8 V ≤ VCC < 2.7 V		—	7		
			1.62 V ≤ VCC < 1.8 V		—	7		
	Slave output release time		2.7 V ≤ VCC ≤ 5.5 V	t_{REL}	—	5	t_{Pcyc}	
			1.8 V ≤ VCC < 2.7 V		—	6		
			1.62 V ≤ VCC < 1.8 V		—	6		

Note 1. t_{Pcyc}: PCLK cycle
Note 2. Divided by 2 can be set only in packages with 768 Kbytes/1 Mbyte of flash memory or 144/145 pins.

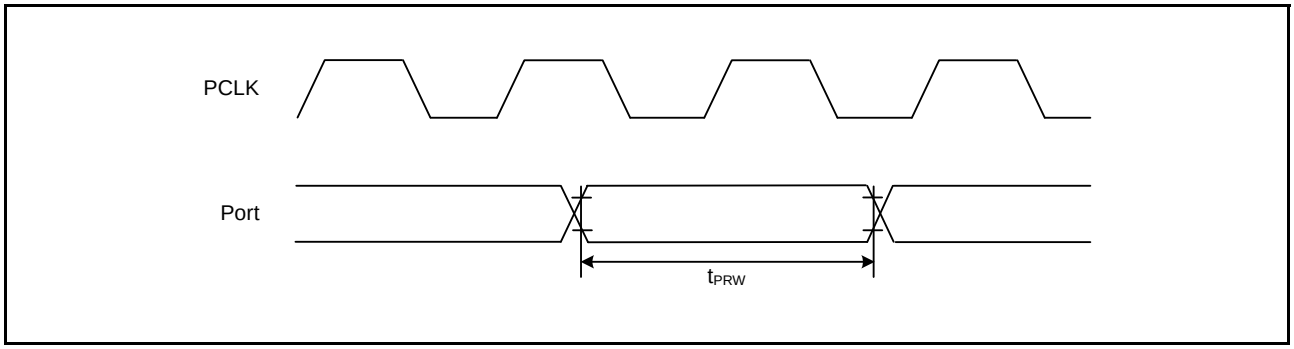


Figure 5.83 I/O Port Input Timing

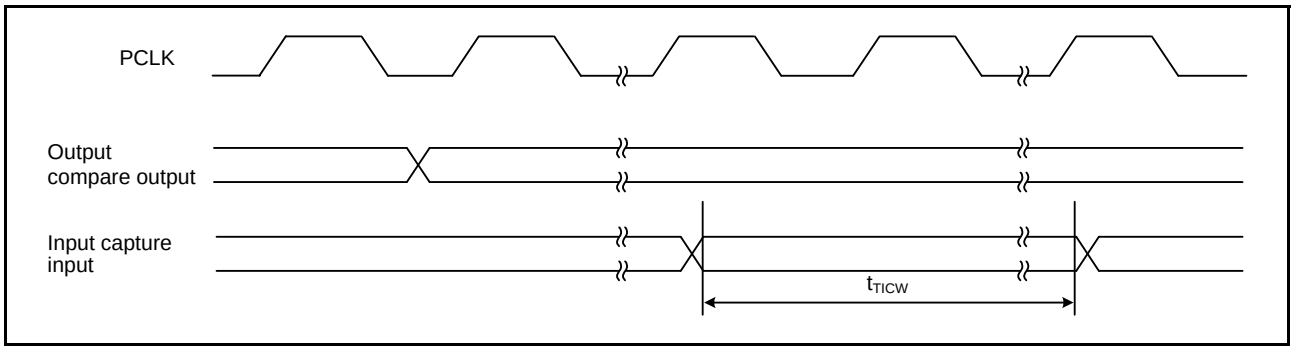


Figure 5.84 MTU/TPU Input/Output Timing

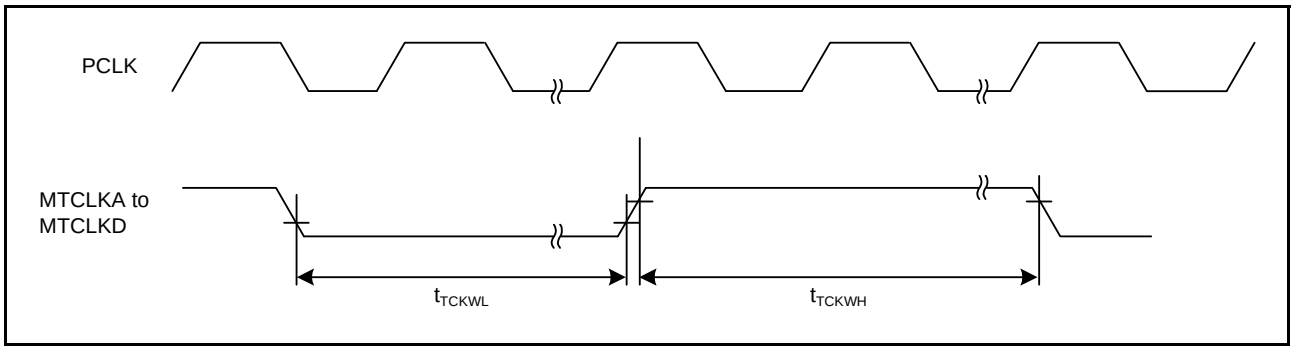


Figure 5.85 MTU/TPU Clock Input Timing

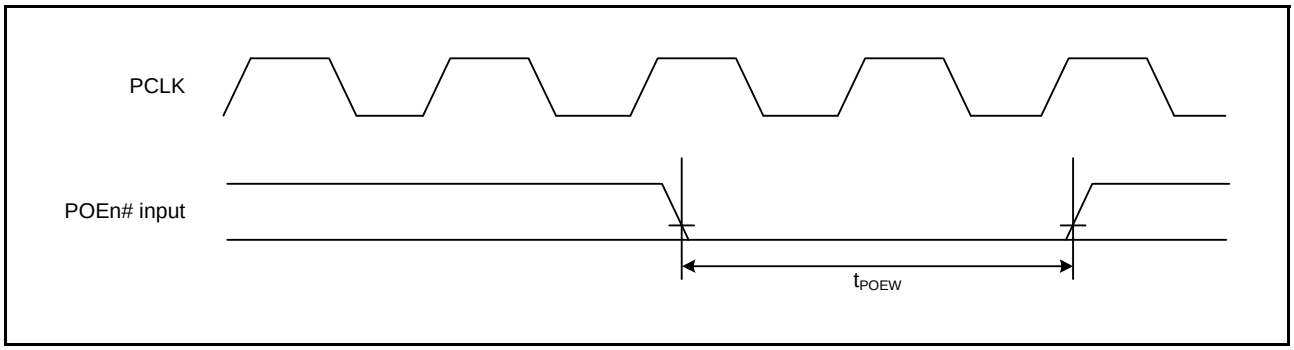


Figure 5.86 POE# Input Timing

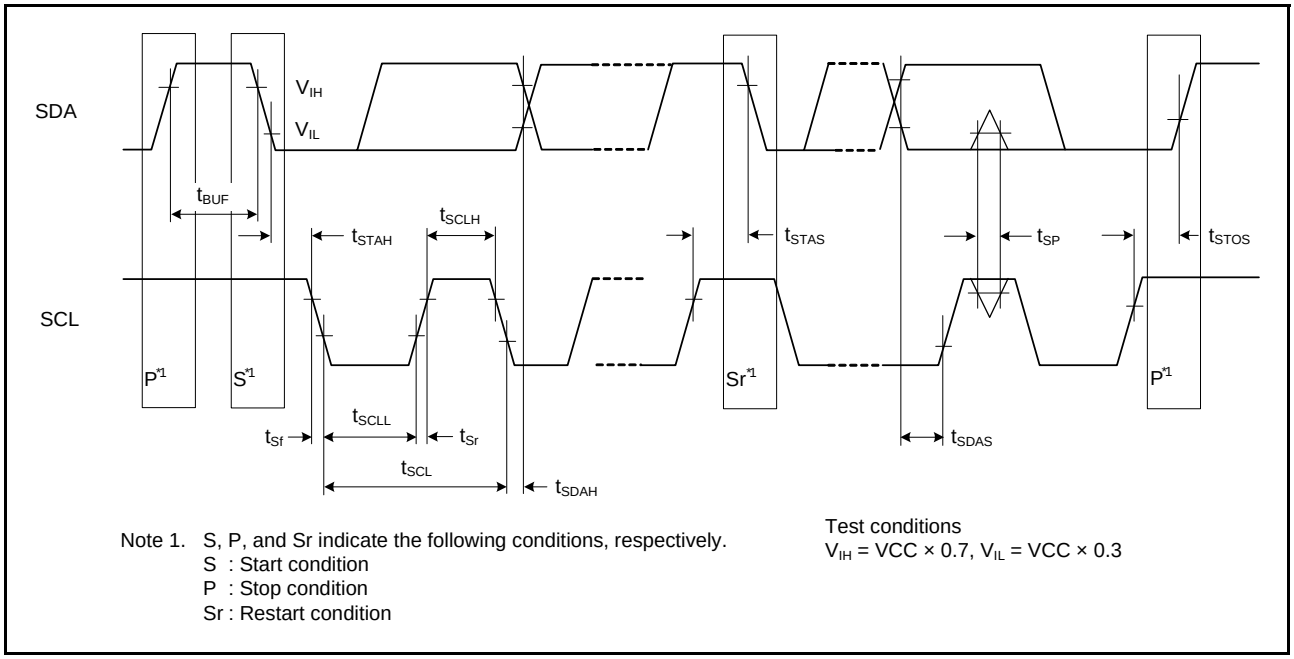


Figure 5.98 RIIC Bus Interface Input/Output Timing and Simple IIC Bus Interface Input/Output Timing

Table 5.66 Sampling Time

Conditions: VCC = AVCC0 = 1.62 to 5.5 V, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +105°C

Item		Symbol	Typ.	Unit	Test Conditions
Sampling time	High-precision channel	Ts	0.2 + 0.14 × R0 (KΩ)	µs	Figure 5.100
	Normal-precision channel		0.35 + 0.14 × R0 (KΩ)		

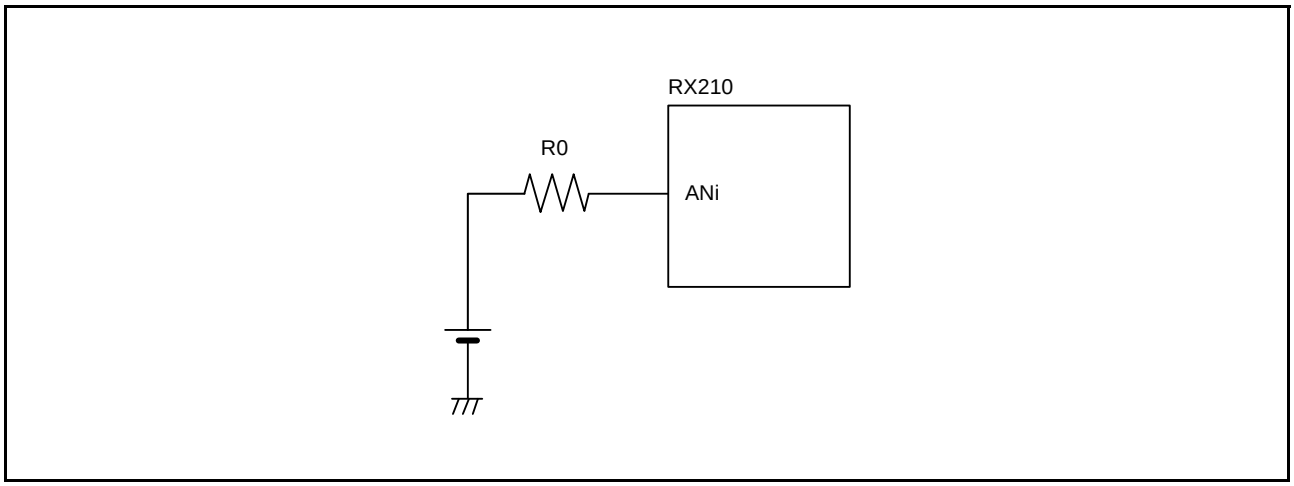


Figure 5.100 Internal Equivalent Circuit of Analog Input Pin

5.5 D/A Conversion Characteristics

Table 5.67 D/A Conversion Characteristics (1)

Conditions: VCC = AVCC0 = 2.7 to 5.5 V, VREFH = 2.7 V to AVCC0,
VSS = AVSS0 = VREFL = VREFL0 = 0 V, fPCLKB = up to 32 MHz, T_a = –40 to +105°C

Item	Min.	Typ.	Max.	Unit	Test Conditions
Resolution	—	—	10	Bit	
Conversion time	—	—	3.0	µs	20-pF capacitive load
Absolute accuracy	—	±3.0	±5.0	LSB	4-MΩ resistive load
	—	—	±4.0	LSB	8-MΩ resistive load
RO output resistance	—	4.1	—	kΩ	

Table 5.68 D/A Conversion Characteristics (2)

Conditions: VCC = AVCC0 = 2.7 to 5.5 V, VREFH =1.8 V to AVCC0,
VSS = AVSS0 = VREFL = VREFL0 = 0 V, fPCLKB = up to 32 MHz, T_a = –40 to +105°C

Item	Min.	Typ.	Max.	Unit	Test Conditions
Resolution	—	—	10	Bit	
Conversion time	—	—	10.0	µs	20-pF capacitive load
Absolute accuracy	—	±5.0	±6.0	LSB	4-MΩ resistive load
	—	—	±5.0	LSB	8-MΩ resistive load
RO output resistance	—	4.1	—	kΩ	

5.6 Temperature Sensor Characteristics

Table 5.69 Temperature Sensor Characteristics

Conditions: VCC = AVCC0 = VREFH0 = 1.8 to 5.5 V, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Relative accuracy		—	—	±1.0	—	°C	
Temperature slope	1.8 ≤ AVCC0 < 2.7	—	—	7.27	—	mV/°C	PGAGAIN = 00b
	2.7 ≤ AVCC0 < 3.6		—	10.46	—		PGAGAIN = 01b
	3.6 ≤ AVCC0 < 4.5		—	13.98	—		PGAGAIN = 10b
	4.5 ≤ AVCC0 ≤ 5.5		—	21.65	—		PGAGAIN = 11b
Output voltage (@ 25°C)		—	—	1.375	—	V	VCC = 3.6 V
Temperature sensor start time		t_{START}	—	—	80	µs	Figure 5.102
Sampling time		—	30	72	300	µs	
PGA restart time		t_{RST_PGA}	—	—	40	µs	