Renesas Electronics America Inc - R5F52106BDFM#30 Datasheet

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I²C, SCI, SPI
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	48
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.62V ~ 5.5V
Data Converters	A/D 12x12b; D/A 2x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LFQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f52106bdfm-30

Table 1.2 Comparison of Functions for Different Packages

Module/Functions		RX210 Group				
		144, 145 Pins	**100 Pins**	**80 Pins**	**64, 69 Pins**	**48 Pins**
External bus	External bus width	16 bits		Not supported		
Interrupt	External interrupts	NMI, IRQ0 to IRQ7			NMI, IRQ0 to IRQ2, IRQ4 to IRQ7	NMI, IRQ0, IRQ1, IRQ4 to IRQ7
DMA	DMA controller	4 channels (DMAC0 to DMAC3)				
	Data transfer controller	Supported				
Timers	16-bit timer pulse unit	6 channels (TPU0 to TPU5)	Not supported			
	Multi-function timer pulse unit 2	6 channels (MTU0 to MTU5)				
	Port output enable 2	POE0# to POE3#, POE8#				
	8-bit timer	2 channels × 2 units				
	Compare match timer	2 channels × 2 units				
	Realtime clock	Supported				Not supported
	Watchdog timer	Supported				
	Independent watchdog timer	Supported				
Communication functions	Serial communications interface (SCIc)	12 channels (SCI0 to 11)	6 channels (SCI0, 1, 5, 6, 8, 9)		5 channels (SCI1, 5, 6, 8, 9)	4 channels (SCI1, 5, 6, 8)
	Serial communications interface (SCId)	1 channel (SCI12)				
	I^2C bus interface	1 channel				
	Serial peripheral interface	1 channel				
12-bit A/D converter		16 channels (AN000 to AN015)		14 channels (AN000 to AN013)	12 channels (AN000 to AN004, AN006, AN008 to AN013)	8 channels (AN000 to AN002, AN006, AN009 to AN012)
Temperature sensor		Supported				
D/A converter		2 channels				Not supported
CRC calculator		Supported				
Event link controller		Supported				
Comparator A		2 channels				
Comparator B		2 channels				
Packages		145-pin TFLGA 144-pin LQFP	100-pin TFLGA 100-pin LQFP	80-pin LQFP	69-pin WLBGA 64-pin TFLGA 64-pin LQFP	48-pin LQFP

1.2 List of Products

Table 1.3 to Table 1.7 are a list of products, and Figure 1.1 shows how to read the product part no., memory capacity, and package type.

Table 1.3 List of Products Chip Version A: D Version (Ta = –40 to +85°C)

Group	Part No.	Orderable Part No.	Package	ROM Capacity	RAM Capacity	E2 DataFlash	Operating Frequency (Max.)	Operating Temperature
RX210	R5F52108ADFP	R5F52108ADFP#V0	PLQP0100KB-A	512 Kbytes	64 Kbytes	8 Kbytes	50 MHz	–40 to +85°C
	R5F52108ADFN	R5F52108ADFN#V0	PLQP0080KB-A					
	R5F52108ADFM	R5F52108ADFM#V0	PLQP0064KB-A					
	R5F52108ADLJ	R5F52108ADLJ#U0	PTLG0100JA-A					
	R5F52107ADFP	R5F52107ADFP#V0	PLQP0100KB-A	384 Kbytes				
	R5F52107ADFN	R5F52107ADFN#V0	PLQP0080KB-A					
	R5F52107ADFM	R5F52107ADFM#V0	PLQP0064KB-A					
	R5F52107ADLJ	R5F52107ADLJ#U0	PTLG0100JA-A					
	R5F52106ADFP	R5F52106ADFP#V0	PLQP0100KB-A	256 Kbytes	32 Kbytes			
	R5F52106ADFN	R5F52106ADFN#V0	PLQP0080KB-A					
	R5F52106ADFM	R5F52106ADFM#V0	PLQP0064KB-A					
	R5F52106ADLJ	R5F52106ADLJ#U0	PTLG0100JA-A					
	R5F52105ADFP	R5F52105ADFP#V0	PLQP0100KB-A	128 Kbytes	20 Kbytes			
	R5F52105ADFN	R5F52105ADFN#V0	PLQP0080KB-A					
	R5F52105ADFM	R5F52105ADFM#V0	PLQP0064KB-A					
	R5F52105ADLJ	R5F52105ADLJ#U0	PTLG0100JA-A					

Note: • Orderable part numbers are current as of when this manual was published. Please make sure to refer to the relevant product page on the Renesas website for the latest part numbers.

1.4 Pin Functions

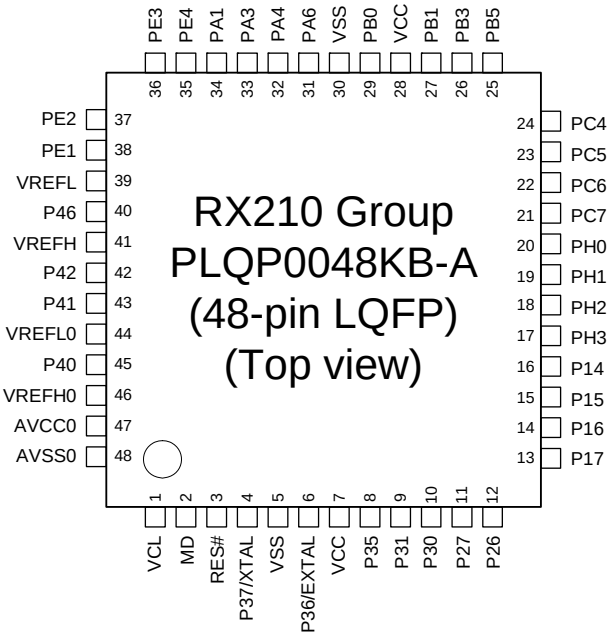
Table 1.8 lists the pin functions.

Table 1.8 Pin Functions (1 / 4)

Classifications	Pin Name	I/O	Description
Power supply	VCC	Input	Power supply pin. Connect it to the system power supply.
	VCL	—	Connect this pin to the VSS pin via the 0.1 µF smoothing capacitor used to stabilize the internal power supply. Place the capacitor close to the pin.
	VSS	Input	Ground pin. Connect it to the system power supply (0 V).
Clock	XTAL	Output	Pins for connecting a crystal resonator. An external clock signal can be input through the EXTAL pin.
	EXTAL	Input	
	BCLK	Output	Outputs the external bus clock for external devices.
	XCIN	Input	Input/output pins for the sub-clock oscillator. Connect a crystal resonator between XCIN and XCOUT.
	XCOUT	Output	
Operating mode control	MD	Input	Pin for setting the operating mode. The signal levels on this pin must not be changed during operation.
System control	RES#	Input	Reset pin. This LSI enters the reset state when this signal goes low.
CAC	CACREF	Input	Input pin for the clock frequency accuracy measurement circuit.
On-chip emulator	FINED	I/O	FINE interface pin.
Address bus	A0 to A23	Output	Output pins for the address.
Data bus	D0 to D15	I/O	Input and output pins for the bidirectional data bus.
Multiplexed bus	A0/D0 to A15/D15	I/O	Address/data multiplexed bus
Bus control	RD#	Output	Strobe signal which indicates that reading from the external bus interface space is in progress.
	WR#	Output	Strobe signal which indicates that writing to the external bus interface space is in progress, in single-write strobe mode.
	WR0#, WR1#	Output	Strobe signals which indicate that either group of data bus pins (D7 to D0, and D15 to D8) is valid in writing to the external bus interface space, in byte strobe mode.
	BC0#, BC1#	Output	Strobe signals which indicate that either group of data bus pins (D7 to D0 and D15 to D8) is valid in access to the external bus interface space, in single-write strobe mode.
	CS0# to CS3#	Output	Select signals for areas 0 to 3.
	WAIT#	Input	Input pin for wait request signals in access to the external space.
	ALE	Output	Address latch signal when address/data multiplexed bus is selected.
Interrupt	NMI	Input	Non-maskable interrupt request pin.
	IRQ0 to IRQ7	Input	Interrupt request pins.

Table 1.8 Pin Functions (4 / 4)

Classifications	Pin Name	I/O	Description
Analog power supply	AVCC0	Input	Analog voltage supply pin for the 12-bit A/D converter. Connect this pin to VCC if the 12-bit A/D converter is not to be used.
	AVSS0	Input	Analog ground pin for the 12-bit A/D converter. Connect this pin to VSS if the 12-bit A/D converter is not to be used.
	VREFH0	Input	Analog reference voltage supply pin for the 12-bit A/D converter. Connect this pin to VCC if the 12-bit A/D converter is not to be used.
	VREFL0	Input	Analog reference ground pin for the 12-bit A/D converter. Connect this pin to VSS if the 12-bit A/D converter is not to be used.
	VREFH	Input	Analog voltage supply pin for the D/A converter. Connect this pin to VCC if the D/A converter is not to be used.
	VREFL	Input	Analog ground pin for the D/A converter. Connect this pin to VSS if the D/A converter is not to be used.
I/O ports	P00 to P03, P05, P07	I/O	6-bit input/output pins.
	P12 to P17	I/O	6-bit input/output pins.
	P20 to P27	I/O	8-bit input/output pins.
	P30 to P37	I/O	8-bit input/output pins. (P35 input pin)
	P40 to P47	I/O	8-bit input/output pins.
	P50 to P56	I/O	7-bit input/output pins.
	P60 to P67	I/O	8-bit input/output pins.
	P70 to P77	I/O	8-bit input/output pins.
	P80 to P83, P86, P87	I/O	6-bit input/output pins.
	P90 to P93	I/O	4-bit input/output pins.
	PA0 to PA7	I/O	8-bit input/output pins.
	PB0 to PB7	I/O	8-bit input/output pins.
	PC0 to PC7	I/O	8-bit input/output pins.
	PD0 to PD7	I/O	8-bit input/output pins.
	PE0 to PE7	I/O	8-bit input/output pins.
	PF5	I/O	1-bit input/output pin.
	PH0 to PH3	I/O	4-bit input/output pins.
	PJ1, PJ3, PJ5	I/O	3-bit input/output pins.
	PK2 to PK5	I/O	4-bit input/output pins.
	PL0, PL1	I/O	2-bit input/output pins.



Note: • This figure indicates the power supply pins and I/O port pins. For the pin configuration, see the table “List of Pins and Pin Functions (48-Pin LQFP)”.

Figure 1.11 Pin Assignments of the 48-Pin LQFP

Table 1.10 List of Pins and Pin Functions (144-Pin LQFP) (4 / 4)

Pin No.	Power Supply, Clock, System Control	I/O Port	External Bus	Timers (MTU, TMR, POE)	Communications (SCIc, SCId, RSPI, RIIC)	Others
122		PD4	D4[A4/D4]	POE3#		IRQ4
123		PD3	D3[A3/D3]	POE8#		IRQ3
124		PD2	D2[A2/D2]	MTIOC4D		IRQ2
125		PD1	D1[A1/D1]	MTIOC4B		IRQ1
126		PD0	D0[A0/D0]			IRQ0
127		P93			CTS7#/RTS7#/SS7#	
128		P92			RXD7/SMISO7/SSCL7	
129		P91			SCK7	
130	VSS					
131		P90			TXD7/SMOSI7/SSDA7	
132	VCC					
133		P47				AN007
134		P46				AN006
135		P45				AN005
136		P44				AN004
137		P43				AN003
138		P42				AN002
139		P41				AN001
140	VREFL0					
141		P40				AN000
142	VREFH0					
143	AVCC0					
144		P07				ADTRG0#

Note: • Pin names to which –DS is appended are for pins that can be used to trigger release from deep software standby mode.
Note: • Leave the NC pin open.

Table 1.16 List of Pins and Pin Functions (64-Pin LQFP) (2 / 2)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (MTU, TMR, POE)	Communication (SCIc, SCId, RSPI, RIIC)	Others
44		PA1	MTIOC0B/MTCLKC	SCK5/SSLA2	CVREFA
45		PA0	MTIOC4A	SSLA1	CACREF
46		PE5	MTIOC4C/MTIOC2B		IRQ5/AN013
47		PE4	MTIOC4D/MTIOC1A		AN012/CMPA2
48		PE3	MTIOC4B/POE8#	CTS12#/RTS12#/SS12#	AN011/CMPA1
49		PE2	MTIOC4A	RXD12/RXDX12/SMISO12/ SSCL12	IRQ7-DS/AN010/ CVREFB0
50		PE1	MTIOC4C	TXD12/TXDX12/SIOX12/ SMOSI12/SSDA12	AN009/CMPB0
51		PE0		SCK12	AN008
52	VREFL				
53		P46			AN006
54	VREFH				
55		P44			AN004
56		P43			AN003
57		P42			AN002
58		P41			AN001
59	VREFL0				
60		P40			AN000
61	VREFH0				
62	AVCC0				
63		P05			DA1
64	AVSS0				

Note: • Pin names to which –DS is appended are for pins that can be used to trigger release from deep software standby mode.

4.1 I/O Register Addresses (Address Order)

Table 4.1 List of I/O Registers (Address Order) (1 / 29)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles: ICLK ≥ PCLK	Number of Access Cycles: ICLK < PCLK
0008 0000h	SYSTEM	Mode monitor register	MDMONR	16	16		3 ICLK
0008 0002h	SYSTEM	Mode status register	MDSR	16	16		3 ICLK
0008 0006h	SYSTEM	System control register 0	SYSCR0	16	16		3 ICLK
0008 0008h	SYSTEM	System control register 1	SYSCR1	16	16		3 ICLK
0008 000Ch	SYSTEM	Standby control register	SBYCR	16	16		3 ICLK
0008 0010h	SYSTEM	Module stop control register A	MSTPCRA	32	32		3 ICLK
0008 0014h	SYSTEM	Module stop control register B	MSTPCRB	32	32		3 ICLK
0008 0018h	SYSTEM	Module stop control register C	MSTPCRC	32	32		3 ICLK
0008 0020h	SYSTEM	System clock control register	SCKCR	32	32		3 ICLK
0008 0026h	SYSTEM	System clock control register 3	SCKCR3	16	16		3 ICLK
0008 0028h	SYSTEM	PLL control register	PLLCR	16	16		3 ICLK
0008 002Ah	SYSTEM	PLL control register 2	PLLCR2	8	8		3 ICLK
0008 0030h	SYSTEM	External bus clock control register	BCKCR	8	8		3 ICLK
0008 0032h	SYSTEM	Main clock oscillator control register	MOSCCR	8	8		3 ICLK
0008 0033h	SYSTEM	Sub-clock oscillator control register	SOSCCR	8	8		3 ICLK
0008 0034h	SYSTEM	Low-speed on-chip oscillator control register	LOCOCR	8	8		3 ICLK
0008 0035h	SYSTEM	IWDT-dedicated on-chip oscillator control register	ILOCOCR	8	8		3 ICLK
0008 0036h	SYSTEM	High-speed on-chip oscillator control register	HOCOCR	8	8		3 ICLK
0008 0037h	SYSTEM	High-speed on-chip oscillator control register 2	HOCOCR2	8	8		3 ICLK
0008 0040h	SYSTEM	Oscillation stop detection control register	OSTDCR	8	8		3 ICLK
0008 0041h	SYSTEM	Oscillation stop detection status register	OSTDSR	8	8		3 ICLK
0008 00A0h	SYSTEM	Operating power control register	OPCCR	8	8		3 ICLK
0008 00A1h	SYSTEM	Sleep mode return clock source switching register	RSTCKCR	8	8		3 ICLK
0008 00A2h	SYSTEM	Main clock oscillator wait control register	MOSCWTCR	8	8		3 ICLK
0008 00A3h	SYSTEM	Sub-clock oscillator wait control register	SOSCWTCR	8	8		3 ICLK
0008 00A6h	SYSTEM	PLL wait control register	PLLWTCR	8	8		3 ICLK
0008 00A9h	SYSTEM	HOCO wait control register 2	HOCOWTCR2	8	8		3 ICLK
0008 00C0h	SYSTEM	Reset status register 2	RSTSR2	8	8		3 ICLK
0008 00C2h	SYSTEM	Software reset register	SWRR	16	16		3 ICLK
0008 00E0h	SYSTEM	Voltage monitoring 1 circuit/comparator A1 control register 1	LVD1CR1	8	8		3 ICLK
0008 00E1h	SYSTEM	Voltage monitoring 1 circuit/comparator A1 status register	LVD1SR	8	8		3 ICLK
0008 00E2h	SYSTEM	Voltage monitoring 2 circuit/comparator A2 control register 1	LVD2CR1	8	8		3 ICLK
0008 00E3h	SYSTEM	Voltage monitoring 2 circuit/comparator A2 status register	LVD2SR	8	8		3 ICLK
0008 0200h	SYSTEM	Voltage regulator control register	VRCR	8	8		3 ICLK
0008 03FEh	SYSTEM	Protect register	PRCR	16	16		3 ICLK
0008 1300h	BSC	Bus error status clear register	BERCLR	8	8		2 ICLK
0008 1304h	BSC	Bus error monitoring enable register	BEREN	8	8		2 ICLK
0008 1308h	BSC	Bus error status register 1	BERSR1	8	8		2 ICLK
0008 130Ah	BSC	Bus error status register 2	BERSR2	16	16		2 ICLK
0008 1310h	BSC	Bus priority control register	BUSPRI	16	16		2 ICLK
0008 2000h	DMAC0	DMA source address register	DMSAR	32	32		2 ICLK
0008 2004h	DMAC0	DMA destination address register	DMDAR	32	32		2 ICLK
0008 2008h	DMAC0	DMA transfer count register	DMCRA	32	32		2 ICLK
0008 200Ch	DMAC0	DMA block transfer count register	DMCRB	16	16		2 ICLK
0008 2010h	DMAC0	DMA transfer mode register	DMTMD	16	16		2 ICLK
0008 2013h	DMAC0	DMA interrupt setting register	DMINT	8	8		2 ICLK
0008 2014h	DMAC0	DMA address mode register	DMAMD	16	16		2 ICLK
0008 2018h	DMAC0	DMA offset register	DMOFR	32	32		2 ICLK
0008 201Ch	DMAC0	DMA transfer enable register	DMCNT	8	8		2 ICLK

Table 4.1 List of I/O Registers (Address Order) (10 / 29)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles: ICLK ≥ PCLK	Number of Access Cycles: ICLK < PCLK
0008 738A2	ICU	Interrupt source priority register 162	IPR162	8	8		2 ICLK
0008 73A4h	ICU	Interrupt source priority register 164	IPR164	8	8		2 ICLK
0008 73A6h	ICU	Interrupt source priority register 166	IPR166	8	8		2 ICLK
0008 73AAh	ICU	Interrupt source priority register 170	IPR170	8	8		2 ICLK
0008 73ABh	ICU	Interrupt source priority register 171	IPR171	8	8		2 ICLK
0008 73AEh	ICU	Interrupt source priority register 174	IPR174	8	8		2 ICLK
0008 73B1h	ICU	Interrupt source priority register 177	IPR177	8	8		2 ICLK
0008 73B4h	ICU	Interrupt source priority register 180	IPR180	8	8		2 ICLK
0008 73B7h	ICU	Interrupt source priority register 183	IPR183	8	8		2 ICLK
0008 73BAh	ICU	Interrupt source priority register 186	IPR186	8	8		2 ICLK
0008 73BEh	ICU	Interrupt source priority register 190	IPR190	8	8		2 ICLK
0008 73C2h	ICU	Interrupt source priority register 194	IPR194	8	8		2 ICLK
0008 73C6h	ICU	Interrupt source priority register 198	IPR198	8	8		2 ICLK
0008 73C7h	ICU	Interrupt source priority register 199	IPR199	8	8		2 ICLK
0008 73C8h	ICU	Interrupt source priority register 200	IPR200	8	8		2 ICLK
0008 73C9h	ICU	Interrupt source priority register 201	IPR201	8	8		2 ICLK
0008 73CEh	ICU	Interrupt source priority register 206	IPR206	8	8		2 ICLK
0008 73D2h	ICU	Interrupt source priority register 210	IPR210	8	8		2 ICLK
0008 73D6h	ICU	Interrupt source priority register 214	IPR214	8	8		2 ICLK
0008 73DAh	ICU	Interrupt source priority register 218	IPR218	8	8		2 ICLK
0008 73DEh	ICU	Interrupt source priority register 222	IPR222	8	8		2 ICLK
0008 73E2h	ICU	Interrupt source priority register 226	IPR226	8	8		2 ICLK
0008 73E6h	ICU	Interrupt source priority register 230	IPR230	8	8		2 ICLK
0008 73EAh	ICU	Interrupt source priority register 234	IPR234	8	8		2 ICLK
0008 73EEh	ICU	Interrupt source priority register 238	IPR238	8	8		2 ICLK
0008 73F2h	ICU	Interrupt source priority register 242	IPR242	8	8		2 ICLK
0008 73F3h	ICU	Interrupt source priority register 243	IPR243	8	8		2 ICLK
0008 73F4h	ICU	Interrupt source priority register 244	IPR244	8	8		2 ICLK
0008 73F5h	ICU	Interrupt source priority register 245	IPR245	8	8		2 ICLK
0008 73F6h	ICU	Interrupt source priority register 246	IPR246	8	8		2 ICLK
0008 73F7h	ICU	Interrupt source priority register 247	IPR247	8	8		2 ICLK
0008 73F8h	ICU	Interrupt source priority register 248	IPR248	8	8		2 ICLK
0008 73F9h	ICU	Interrupt source priority register 249	IPR249	8	8		2 ICLK
0008 73FAh	ICU	Interrupt source priority register 250	IPR250	8	8		2 ICLK
0008 7400h	ICU	DMAC activation request select register 0	DMRSR0	8	8		2 ICLK
0008 7404h	ICU	DMAC activation request select register 1	DMRSR1	8	8		2 ICLK
0008 7408h	ICU	DMAC activation request select register 2	DMRSR2	8	8		2 ICLK
0008 740Ch	ICU	DMAC activation request select register 3	DMRSR3	8	8		2 ICLK
0008 7500h	ICU	IRQ control register 0	IRQCR0	8	8		2 ICLK
0008 7501h	ICU	IRQ control register 1	IRQCR1	8	8		2 ICLK
0008 7502h	ICU	IRQ control register 2	IRQCR2	8	8		2 ICLK
0008 7503h	ICU	IRQ control register 3	IRQCR3	8	8		2 ICLK
0008 7504h	ICU	IRQ control register 4	IRQCR4	8	8		2 ICLK
0008 7505h	ICU	IRQ control register 5	IRQCR5	8	8		2 ICLK
0008 7506h	ICU	IRQ control register 6	IRQCR6	8	8		2 ICLK
0008 7507h	ICU	IRQ control register 7	IRQCR7	8	8		2 ICLK
0008 7510h	ICU	IRQ pin digital filter enable register 0	IRQFLTE0	8	8		2 ICLK
0008 7514h	ICU	IRQ pin digital filter setting register 0	IRQFLTC0	16	16		2 ICLK
0008 7580h	ICU	Non-maskable interrupt status register	NMISR	8	8		2 ICLK
0008 7581h	ICU	Non-maskable interrupt enable register	NMIER	8	8		2 ICLK
0008 7582h	ICU	Non-maskable interrupt clear register	NMICLR	8	8		2 ICLK

Table 4.1 List of I/O Registers (Address Order) (16 / 29)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles: ICLK ≥ PCLK	Number of Access Cycles: ICLK < PCLK
0008 8896h	MTU5	Timer I/O control register V	TIORV	8	8	2, 3 PCLKB	2 ICLK
0008 88A0h	MTU5	Timer counter W	TCNTW	16	16	2, 3 PCLKB	2 ICLK
0008 88A2h	MTU5	Timer general register W	TGRW	16	16	2, 3 PCLKB	2 ICLK
0008 88A4h	MTU5	Timer control register W	TCRW	8	8	2, 3 PCLKB	2 ICLK
0008 88A6h	MTU5	Timer I/O control register W	TIORW	8	8	2, 3 PCLKB	2 ICLK
0008 88B2h	MTU5	Timer interrupt enable register	TIER	8	8	2, 3 PCLKB	2 ICLK
0008 88B4h	MTU5	Timer start register	TSTR	8	8	2, 3 PCLKB	2 ICLK
0008 88B6h	MTU5	Timer compare match clear register	TCNTCMPCLR	8	8	2, 3 PCLKB	2 ICLK
0008 8900h	POE	Input level control/status register 1	ICSR1	16	8, 16	2, 3 PCLKB	2 ICLK
0008 8902h	POE	Output level control/status register 1	OCSR1	16	8, 16	2, 3 PCLKB	2 ICLK
0008 8908h	POE	Input level control/status register 2	ICSR2	16	8, 16	2, 3 PCLKB	2 ICLK
0008 890Ah	POE	Software port output enable register	SPOER	8	8	2, 3 PCLKB	2 ICLK
0008 890Bh	POE	Port output enable control register 1	POECR1	8	8	2, 3 PCLKB	2 ICLK
0008 890Ch	POE	Port output enable control register 2	POECR2	8	8	2, 3 PCLKB	2 ICLK
0008 890Eh	POE	Input level control/status register 3	ICSR3	16	8, 16	2, 3 PCLKB	2 ICLK
0008 9000h	S12AD	A/D control register	ADCSR	16	16	2, 3 PCLKB	2 ICLK
0008 9004h	S12AD	A/D channel select register A	ADANSA	16	16	2, 3 PCLKB	2 ICLK
0008 9008h	S12AD	A/D-converted value addition mode select register	ADADS	16	16	2, 3 PCLKB	2 ICLK
0008 900Ch	S12AD	A/D-converted value addition count select register	ADADC	8	8	2, 3 PCLKB	2 ICLK
0008 900Eh	S12AD	A/D control extended register	ADCER	16	16	2, 3 PCLKB	2 ICLK
0008 9010h	S12AD	A/D start trigger select register	ADSTRGR	16	16	2, 3 PCLKB	2 ICLK
0008 9012h	S12AD	A/D converted extended input control register	ADEXICR	16	16	2, 3 PCLKB	2 ICLK
0008 9014h	S12AD	A/D channel select register B	ADANSB	16	16	2, 3 PCLKB	2 ICLK
0008 9018h	S12AD	A/D double register	ADDBLDR	16	16	2, 3 PCLKB	2 ICLK
0008 901Ah	S12AD	A/D temperature sensor data register	ADTSDR	16	16	2, 3 PCLKB	2 ICLK
0008 901Ch	S12AD	A/D internal reference voltage data register	ADOCDR	16	16	2, 3 PCLKB	2 ICLK
0008 901Eh	S12AD	A/D self-diagnosis data register	ADRD	16	16	2, 3 PCLKB	2 ICLK
0008 9020h	S12AD	A/D data register 0	ADDR0	16	16	2, 3 PCLKB	2 ICLK
0008 9022h	S12AD	A/D data register 1	ADDR1	16	16	2, 3 PCLKB	2 ICLK
0008 9024h	S12AD	A/D data register 2	ADDR2	16	16	2, 3 PCLKB	2 ICLK
0008 9026h	S12AD	A/D data register 3	ADDR3	16	16	2, 3 PCLKB	2 ICLK
0008 9028h	S12AD	A/D data register 4	ADDR4	16	16	2, 3 PCLKB	2 ICLK
0008 902Ah	S12AD	A/D data register 5	ADDR5	16	16	2, 3 PCLKB	2 ICLK
0008 902Ch	S12AD	A/D data register 6	ADDR6	16	16	2, 3 PCLKB	2 ICLK
0008 902Eh	S12AD	A/D data register 7	ADDR7	16	16	2, 3 PCLKB	2 ICLK
0008 9030h	S12AD	A/D data register 8	ADDR8	16	16	2, 3 PCLKB	2 ICLK
0008 9032h	S12AD	A/D data register 9	ADDR9	16	16	2, 3 PCLKB	2 ICLK
0008 9034h	S12AD	A/D data register 10	ADDR10	16	16	2, 3 PCLKB	2 ICLK
0008 9036h	S12AD	A/D data register 11	ADDR11	16	16	2, 3 PCLKB	2 ICLK
0008 9038h	S12AD	A/D data register 12	ADDR12	16	16	2, 3 PCLKB	2 ICLK
0008 903Ah	S12AD	A/D data register 13	ADDR13	16	16	2, 3 PCLKB	2 ICLK
0008 903Ch	S12AD	A/D data register 14	ADDR14	16	16	2, 3 PCLKB	2 ICLK
0008 903Eh	S12AD	A/D data register 15	ADDR15	16	16	2, 3 PCLKB	2 ICLK
0008 9060h	S12AD	A/D sampling state register 0	ADSSTR0	8	8	2, 3 PCLKB	2 ICLK
0008 9061h	S12AD	A/D sampling state register L	ADSSTRL	8	8	2, 3 PCLKB	2 ICLK
0008 9066h	S12AD	A/D sample and hold circuit register	ADSHCR	16	16	2, 3 PCLKB	2 ICLK
0008 9070h	S12AD	A/D sampling state register T	ADSSTRT	8	8	2, 3 PCLKB	2 ICLK
0008 9071h	S12AD	A/D sampling state register O	ADSSTRO	8	8	2, 3 PCLKB	2 ICLK
0008 9073h	S12AD	A/D sampling state register 1	ADSSTR1	8	8	2, 3 PCLKB	2 ICLK
0008 9074h	S12AD	A/D sampling state register 2	ADSSTR2	8	8	2, 3 PCLKB	2 ICLK
0008 9075h	S12AD	A/D sampling state register 3	ADSSTR3	8	8	2, 3 PCLKB	2 ICLK

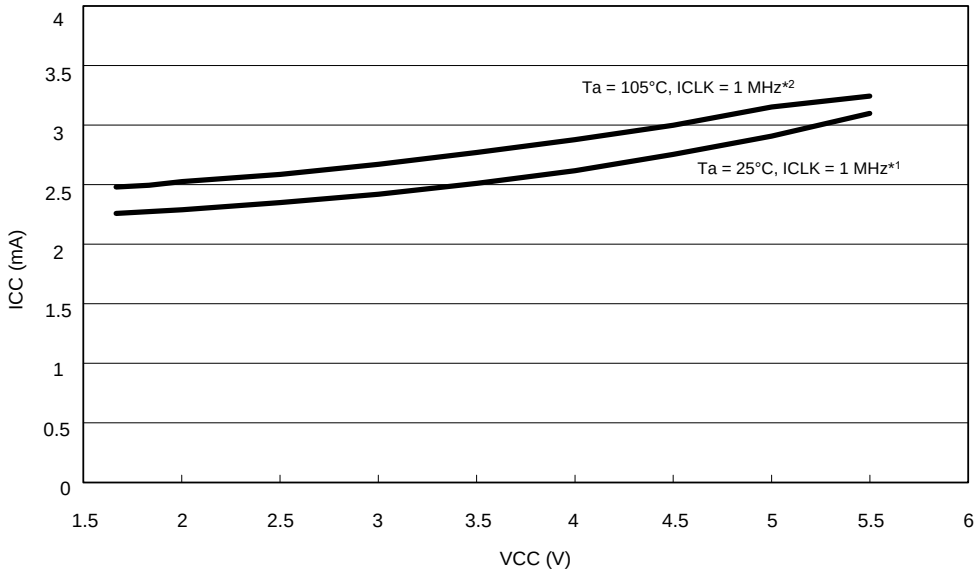
[Chip version A]

Table 5.8 DC Characteristics (7)

Conditions: VCC = AVCC0 = 1.62 to 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

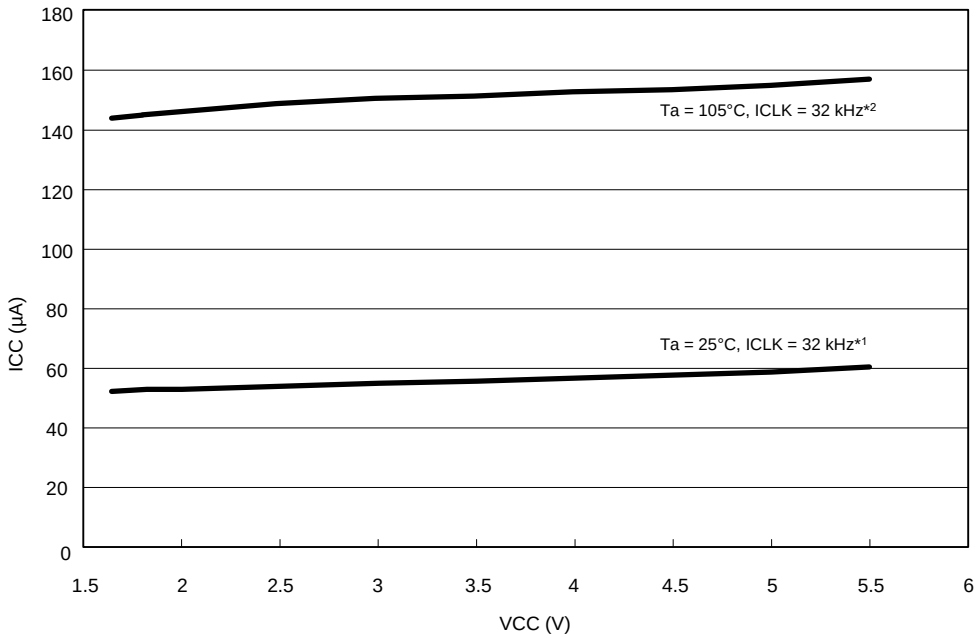
Item				Symbol	Typ.*3	Max.	Unit	Test Conditions
Supply current*1	Software standby mode*2	Flash memory power supplied, HOCO power supplied, POR low power consumption function disabled (SOFTCUT[2:0] bits = 000b)	T_a = 25°C	I_{CC}	175	—	µA	
		Flash memory power supplied, HOCO power not supplied, POR low power consumption function enabled (SOFTCUT[2:0] bits = 110b)	T_a = 25°C		3.0	—		
			T_a = 85°C		—	130		
			T_a = 105°C		—	150		
		Flash memory power not supplied, HOCO power not supplied, POR low power consumption function enabled (SOFTCUT[2:0] bits = 111b)	T_a = 25°C		2.0	—		
			T_a = 85°C		—	120		
			T_a = 105°C		—	140		
	Deep software standby mode*2	Flash memory power not supplied, HOCO power not supplied, POR low power consumption function enabled (DEEPCUT1 bit = 1)	T_a = 25°C		0.45			
			T_a = 85°C		—	20		
			T_a = 105°C		—	25		
	Increments produced by running voltage detection circuits and disabling the POR low power consumption function				1.4	—		
	Increment for RTC operation (low CL)				0.8	—		
	Increment for RTC operation (standard CL)				2.0	—		

Note 1. Supply current values are with all output pins unloaded and all input pull-up MOSs in the off state.
Note 2. The IWDT and LVD are stopped.
Note 3. VCC = 3.3 V.



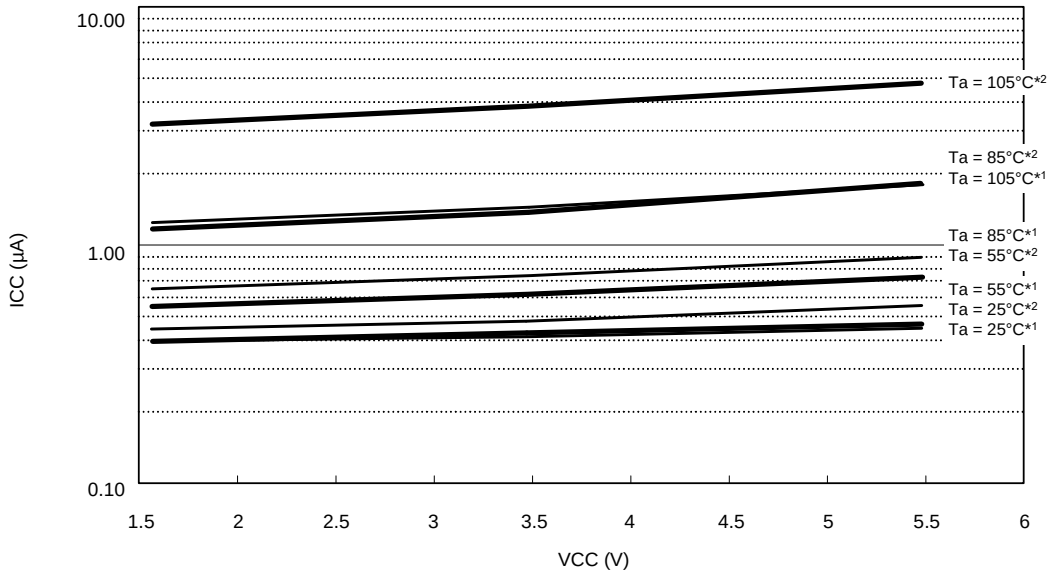
Note 1. All peripheral operation is normal.
Average value of the tested middle samples during product evaluation.
Note 2. All peripheral operation is maximum.
Average value of the tested upper-limit samples during product evaluation.

Figure 5.11 Voltage Dependency in Low-Speed Operating Mode 1 (Reference Data) for Chip Version C



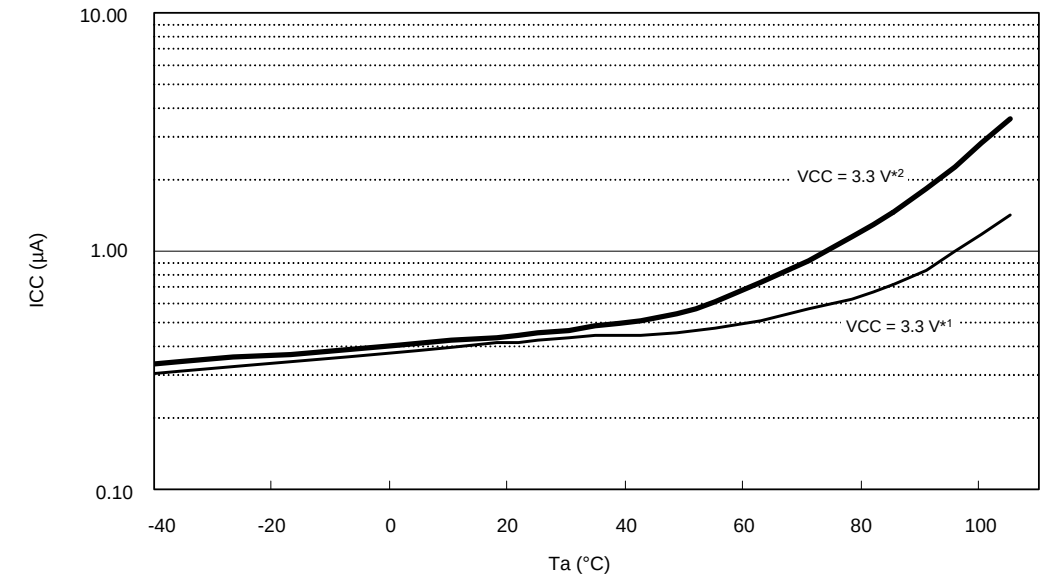
Note 1. All peripheral operation is normal.
Average value of the tested middle samples during product evaluation.
Note 2. All peripheral operation is maximum.
Average value of the tested upper-limit samples during product evaluation.

Figure 5.12 Voltage Dependency in Low-Speed Operating Mode 2 (Reference Data) for Chip Version C



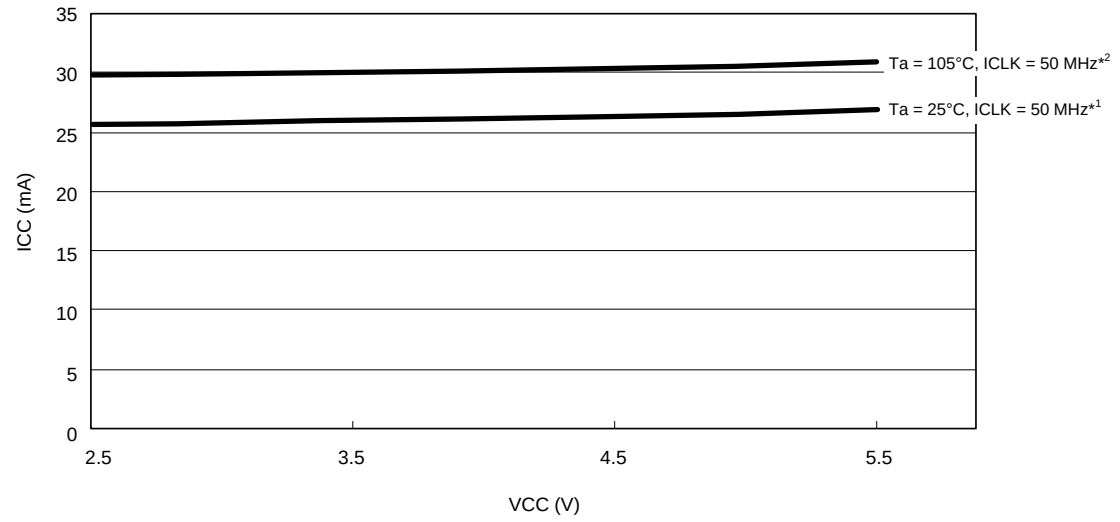
Note 1. Average value of the tested middle samples during product evaluation.
Note 2. Average value of the tested upper-limit samples during product evaluation.

Figure 5.24 Voltage Dependency in Deep Software Standby Mode (DEEPCUT1 Bit = 1) (Reference Data) for Chip Version B with 256 Kbytes or Less of Flash Memory and 48 to 100 Pins



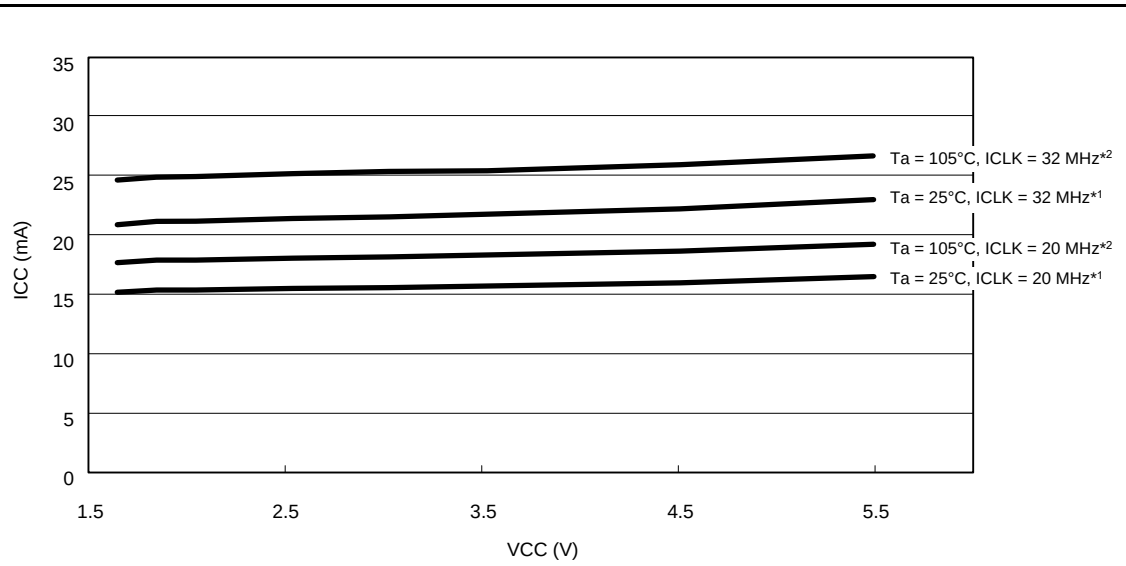
Note 1. Average value of the tested middle samples during product evaluation.
Note 2. Average value of the tested upper-limit samples during product evaluation.

Figure 5.25 Temperature Dependency in Deep Software Standby Mode (DEEPCUT1 Bit = 1) (Reference Data) for Chip Version B with 256 Kbytes or Less of Flash Memory and 48 to 100 Pins



Note 1. All peripheral operation is normal. This does not include BGO operation.
Average value of the tested middle samples during product evaluation
Note 2. All peripheral operation is maximum. This does not include BGO operation.
Average value of the tested upper-limit samples during product evaluation.

Figure 5.35 Voltage Dependency in High-Speed Operating Mode (Reference Data) for Chip Version B with 512 Kbytes or Less of Flash Memory and 144 and 145 Pins



Note 1. All peripheral operation is normal. This does not include BGO operation.
Average value of the tested middle samples during product evaluation
Note 2. All peripheral operation is maximum. This does not include BGO operation.
Average value of the tested upper-limit samples during product evaluation.

Figure 5.36 Voltage Dependency in Middle-Speed Operating Modes 1A and 1B (Reference Data) for Chip Version B with 512 Kbytes or Less of Flash Memory and 144 and 145 Pins

5.2.2 Standard I/O Pin Output Characteristics (2)

Figure 5.50 to Figure 5.54 show the characteristics when high-drive output is selected by the drive capacity control register.

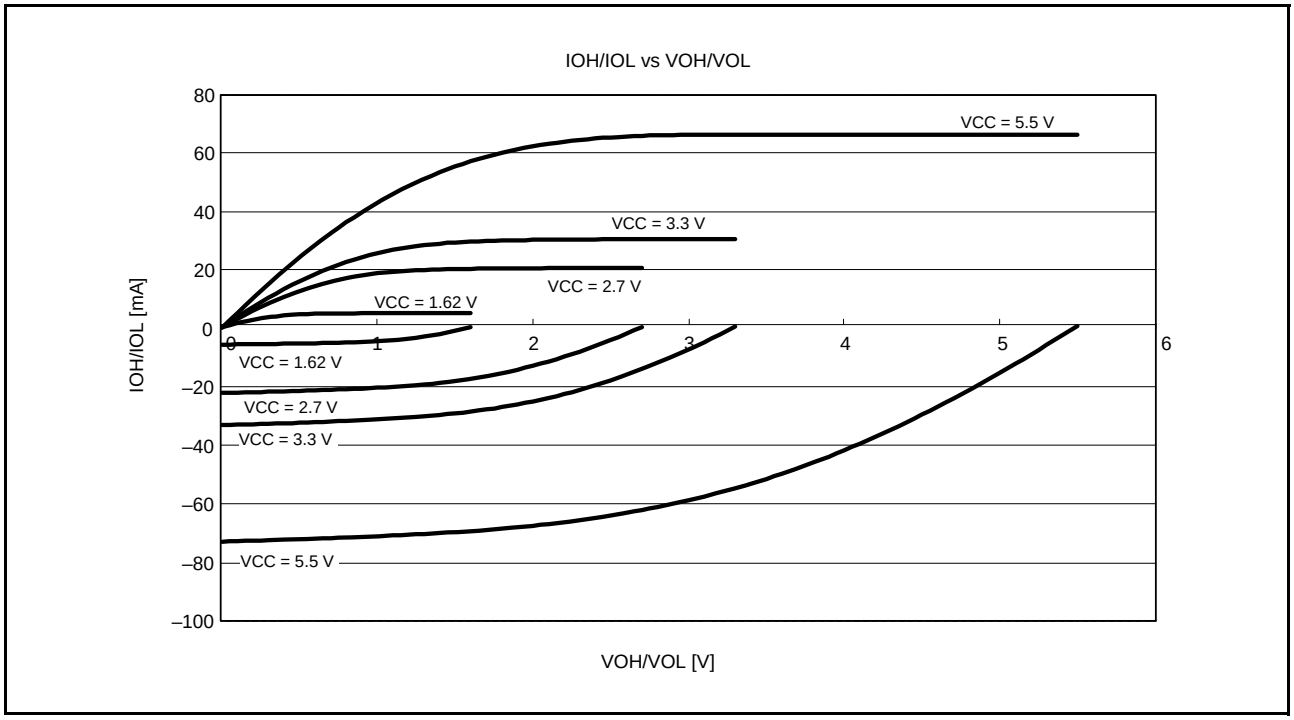


Figure 5.50 VOH/VOL and IOH/IOL Voltage Characteristics at Ta = 25°C when High-Drive Output is Selected (Reference Data)

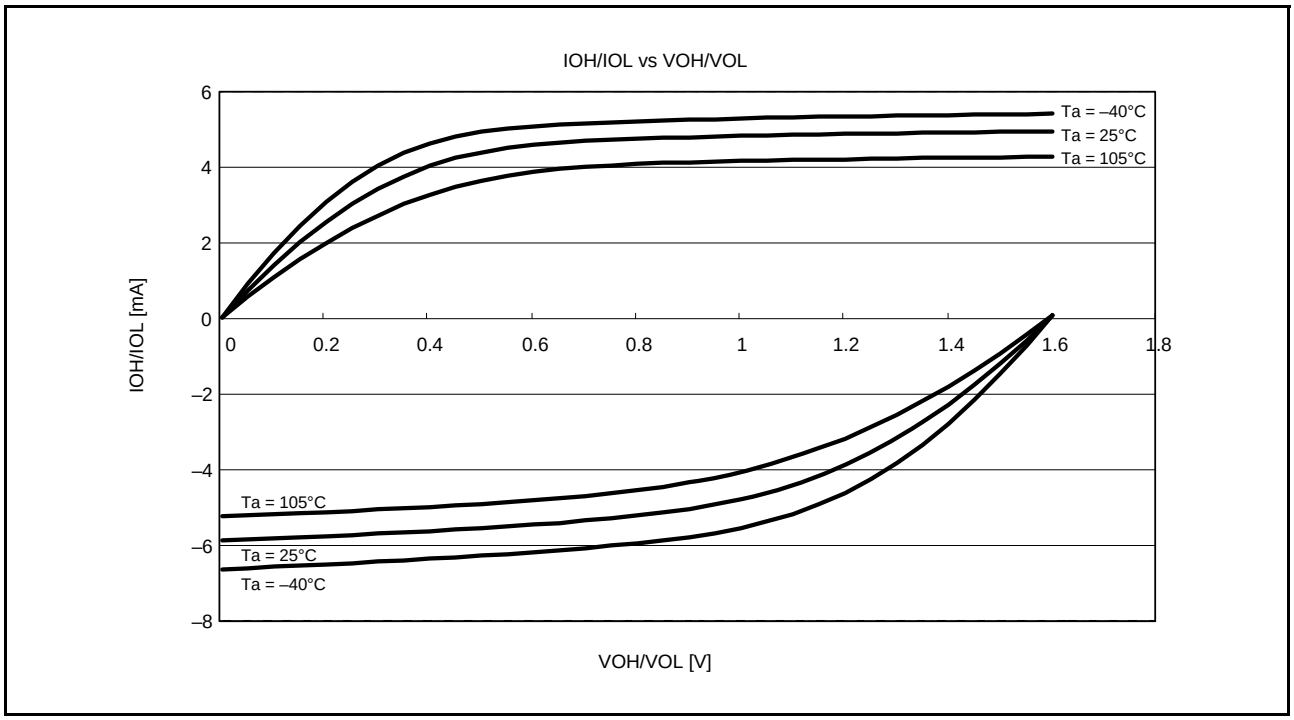


Figure 5.51 VOH/VOL and IOH/IOL Temperature Characteristics at VCC = 1.62 V when High-Drive Output is Selected (Reference Data)

5.3 AC Characteristics

[Chip versions A, B, and C]

Table 5.33 Operation Frequency Value (High-Speed Operating Mode)

Conditions: VCC = AVCC0 = 2.7 to 5.5 V, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +105°C

Item		Symbol	VCC	Unit
			2.7 to 5.5 V	
Maximum operating frequency	System clock (ICLK)	f_{max}	50	MHz
	FlashIF clock (FCLK)*1		32	
	Peripheral module clock (PCLKB)		32	
	Peripheral module clock (PCLKD)*2		50	
	External bus clock (BCLK)		25	
	BCLK pin output		12.5	

Note 1. The lower-limit frequency of FCLK is 4 MHz during programming or erasing of the flash memory.
Note 2. The lower-limit frequency of PCLKD is 1 MHz when the A/D converter is in use.

[Chip versions A, B, and C]

Table 5.34 Operation Frequency Value (MiddleSpeed Operating Mode 1A)

Conditions: VCC = AVCC0 = 1.62 to 5.5 V, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +105°C

Item		Symbol	VCC			Unit
			1.62 to 1.8 V	1.8 to 2.7 V	2.7 to 5.5 V	
Maximum operating frequency	System clock (ICLK)	f_{max}	20	32	32	MHz
	FlashIF clock (FCLK)*1		20	32	32	
	Peripheral module clock (PCLKB)		20	32	32	
	Peripheral module clock (PCLKD)*2		20	32	32	
	External bus clock (BCLK)		12	16	25	
	BCLK pin output		6	8	12.5	

Note 1. The VCC is 2.7 to 5.5 V and the lower-limit frequency of FCLK is 4 MHz during programming or erasing of the flash memory.
Note 2. The lower-limit frequency of PCLKD is 1 MHz when the A/D converter is in use.

[Chip versions A, B, and C]

Table 5.35 Operation Frequency Value (Middle-Speed Operating Mode 1B)

Conditions: VCC = AVCC0 = 1.62 to 5.5 V, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +105°C

Item		Symbol	VCC			Unit
			1.62 to 1.8 V	1.8 to 2.7 V	2.7 to 5.5 V	
Maximum operating frequency	System clock (ICLK)	f_{max}	20	32	32	MHz
	FlashIF clock (FCLK)*1		20	32	32	
	Peripheral module clock (PCLKB)		20	32	32	
	Peripheral module clock (PCLKD)*2		20	32	32	
	External bus clock (BCLK)		12	16	25	
	BCLK pin output		6	8	12.5	

Note 1. The VCC is 1.62 to 3.6 V and the lower-limit frequency of FCLK is 4 MHz during programming or erasing of the flash memory.
Note 2. The lower-limit frequency of PCLKD is 1 MHz when the A/D converter is in use.

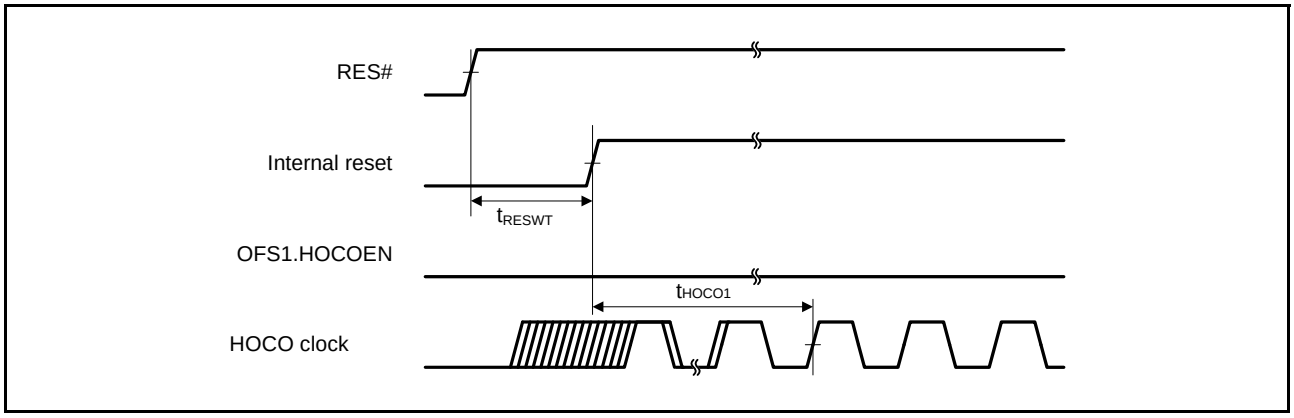


Figure 5.63 HOCO Clock Oscillation Start Timing (After Reset is Canceled by Setting the OFS1.HOCOEN Bit to 0)

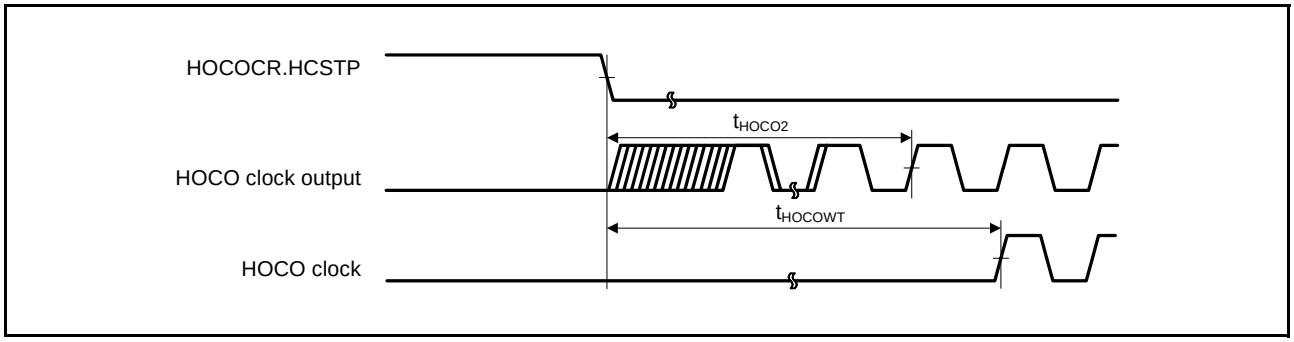


Figure 5.64 HOCO Clock Oscillation Start Timing (Oscillation is Started by Setting the HOCOCR.HCSTP Bit)

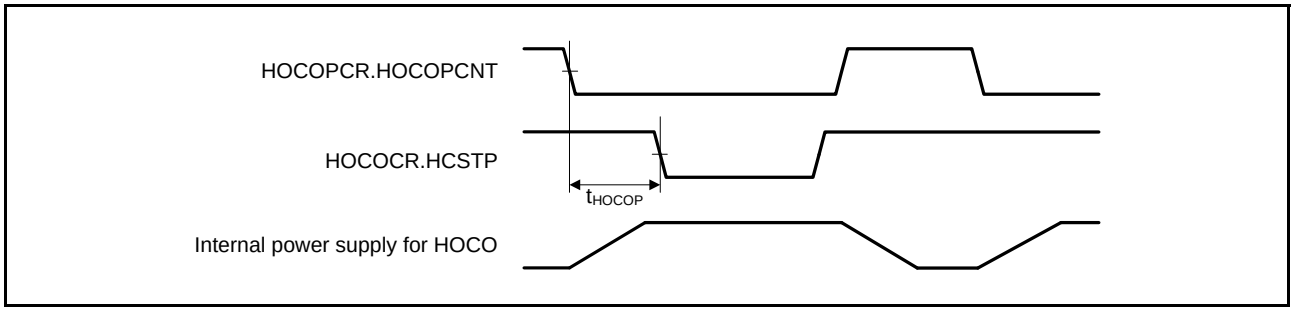


Figure 5.65 HOCO Power Control Timing

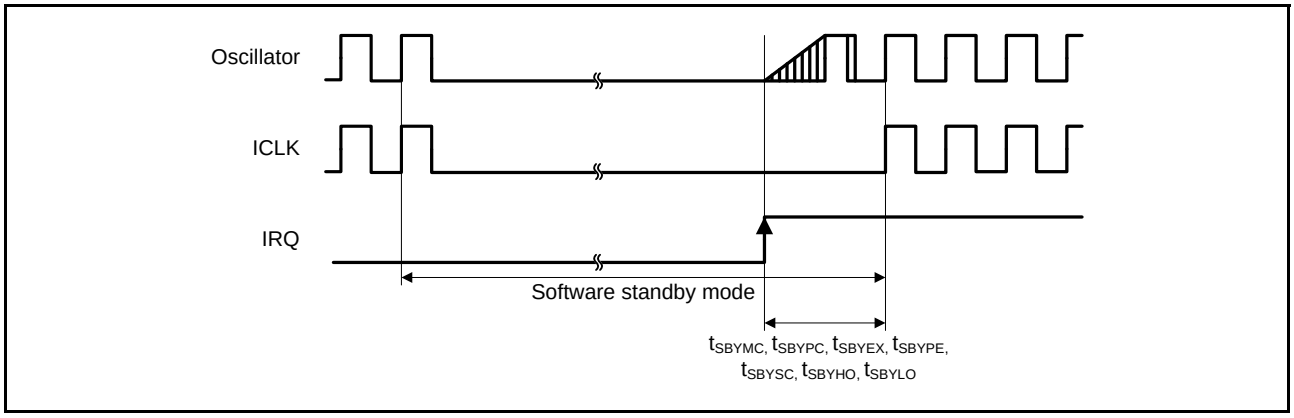


Figure 5.72 Software Standby Mode Cancellation Timing

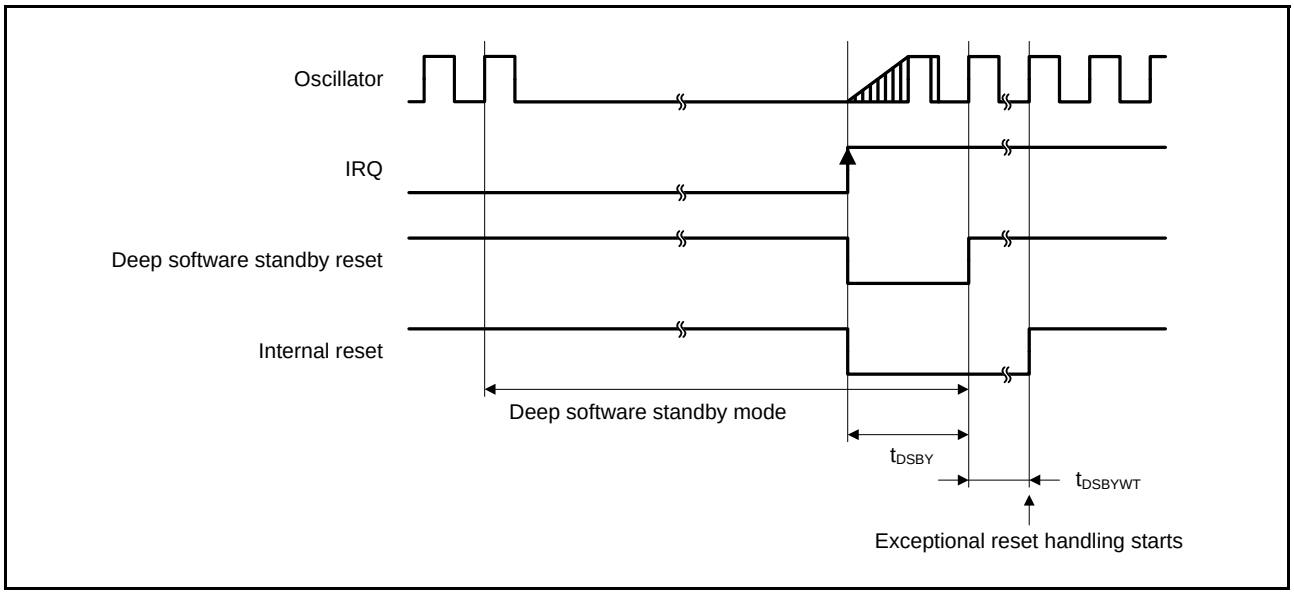


Figure 5.73 Deep Software Standby Mode Cancellation Timing

Table 5.51 Bus Timing (3)

Conditions: VCC = AVCC0 = 1.62 to 1.8 V, VSS = AVSS0 = VREFL = VREFL0 = 0 V,
fBCLK ≤ 12 MHz (BCLK pin output frequency ≤ 6 MHz), T_a = –40 to +105°C, V_{OH} = VCC × 0.5,
V_{OL} = VCC × 0.5, I_{OH} = –0.5 mA, I_{OL} = 0.5 mA, C_L = 30 pF
When normal output is selected by the drive capacity register

Item	Symbol	Min.	Max.	Unit	Test Conditions
Address delay time	t_{AD}	—	125	ns	Figure 5.76 to Figure 5.79
Byte control delay time	t_{BCD}	—	125	ns	
CS# delay time	t_{CSD}	—	125	ns	
RD# delay time	t_{RSD}	—	125	ns	
Read data setup time	t_{RDS}	85	—	ns	
Read data hold time	t_{RDH}	0	—	ns	
WR# delay time	t_{WRD}	—	125	ns	
Write data delay time	t_{WDD}	—	125	ns	
Write data hold time	t_{WDH}	0	—	ns	
WAIT# setup time	t_{WTS}	85	—	ns	Figure 5.80
WAIT# hold time	t_{WTH}	0	—	ns	

Rev.	Date	Description	
		Page	Summary
1.40	Feb 19, 2013	96	Table 5.11 DC Characteristics (10), changed
		105	Table 5.14 DC Characteristics (13), changed
		114	Table 5.17 DC Characteristics (16), changed
		115	Figure 5.31 Voltage Dependency in Software Standby Mode (SOFTCUT[2:0] Bits = 110b) (Reference Data) for Chip Version B with 768 Kbytes/1 Mbyte of Flash Memory and 100 to 145 Pins, changed
		116	Figure 5.32 Temperature Dependency in Software Standby Mode (SOFTCUT[2:0] Bits = 110b) (Reference Data) for Chip Version B with 768 Kbytes/1 Mbyte of Flash Memory and 100 to 145 Pins, changed
		118	Table 5.18 DC Characteristics (17), changed
		119, 120	Table 5.19 DC Characteristics (18), changed
		121 to 123	Figure 5.35 Voltage Dependency in High-Speed Operating Mode (Reference Data) for Chip Version B with 512 Kbytes or Less of Flash Memory and 144 and 145 Pins to Figure 5.39 Voltage Dependency in Low-Speed Operating Mode 2 (Reference Data) for Chip Version B with 512 Kbytes or Less of Flash Memory and 144 and 145 Pins, added
		124	Table 5.20 DC Characteristics (19), changed
		125 to 127	Figure 5.40 Voltage Dependency in Software Standby Mode (SOFTCUT[2:0] Bits = 110b) (Reference Data) for Chip Version B with 512 Kbytes or Less of Flash Memory and 144 and 145 Pins to Figure 5.43 Temperature Dependency in Deep Software Standby Mode (DEEPCUT1 Bit = 1) (Reference Data) for Chip Version B with 512 Kbytes or Less of Flash Memory and 144 and 145 Pins, added
		128	Table 5.22 DC Characteristics (21), changed, Note 2 added
		144	Table 5.44 Clock Timing: Note 5, changed
		154	Table 5.49 Bus Timing (1), Table 5.50 Bus Timing (2), changed
		155	Table 5.51 Bus Timing (3), changed
		160	Table 5.52 Bus Timing (Multiplexed Bus) (1), Table 5.53 Bus Timing (Multiplexed Bus) (2), changed
		161	Table 5.54 Bus Timing (Multiplexed Bus) (3), changed
		164	Table 5.56 Timing of On-Chip Peripheral Modules (2), changed
		166	Table 5.57 Timing of On-Chip Peripheral Modules (3), changed
		177	Table 5.61 A/D Conversion Characteristics (1), Note 3, deleted Figure 5.99 AVCC to AVREFH Voltage Range, added
		179	Table 5.64 A/D Conversion Characteristics (2), Note 3, Table 5.65 A/D Conversion Characteristics (3), Note 3, deleted
		186	Table 5.72 Power-on Reset Circuit and Voltage Detection Circuit Characteristics (2), changed
1.50	Oct 18, 2013	All	69-Pin WLBGA package products, added
		Features	
		1	SWBG0069LA-A 3.91 × 4.26mm, 0.40-mm pitch, ■ Applications, added
		1. Overview	
		2	1.1 Outline of Specifications, changed
		2 to 6	Table 1.1 Outline of Specifications, Note 2, changed
		7	Table 1.2 Comparison of Functions for Different Packages, changed
		8	Table 1.3 List of Products Chip Version A: D Version (Ta = -40 to +85°C), changed, Note, added
		9	Table 1.4 List of Products Chip Version B: D Version (Ta = -40 to +85°C), Note 1, changed, Note added
		10	Table 1.5 List of Products Chip Version B: G Version (Ta = -40 to +105°C), Note, changed, Note 1, deleted
		11	Table 1.6 List of Products Chip Version C: D Version (Ta = -40 to +85°C), Table 1.7 List of Products Chip Version C: G Version (Ta = -40 to +105°C), Note, changed
		12	Figure 1.1 How to Read the Product Part No., Memory Capacity, and Package Type, changed
		23	Figure 1.8 Pin Assignments of the 69-Pin WLBGA, added
		43, 44	Table 1.14 List of Pins and Pin Functions (69-Pin WLBGA), added
		5. Electrical Characteristics	
		134	Table 5.21 DC Characteristics (20) Note, added
		149, 150	Table 5.44 Clock Timing Note 6, Note 7, added
		183	Table 5.61 A/D Conversion Characteristics (1) Note, changed, Note 4, deleted
		184	Table 5.62 Channel Classification for A/D Converter, changed
		185	Table 5.64 A/D Conversion Characteristics (2) Note, changed
		Appendix 1. Package Dimensions	
		211	Figure E 69-Pin WLBGA (SWBG0069LA-A), added