Renesas Electronics America Inc - R5F52106BDFN#30 Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I²C, SCI, SPI
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	64
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.62V ~ 5.5V
Data Converters	A/D 14x12b; D/A 2x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f52106bdfn-30

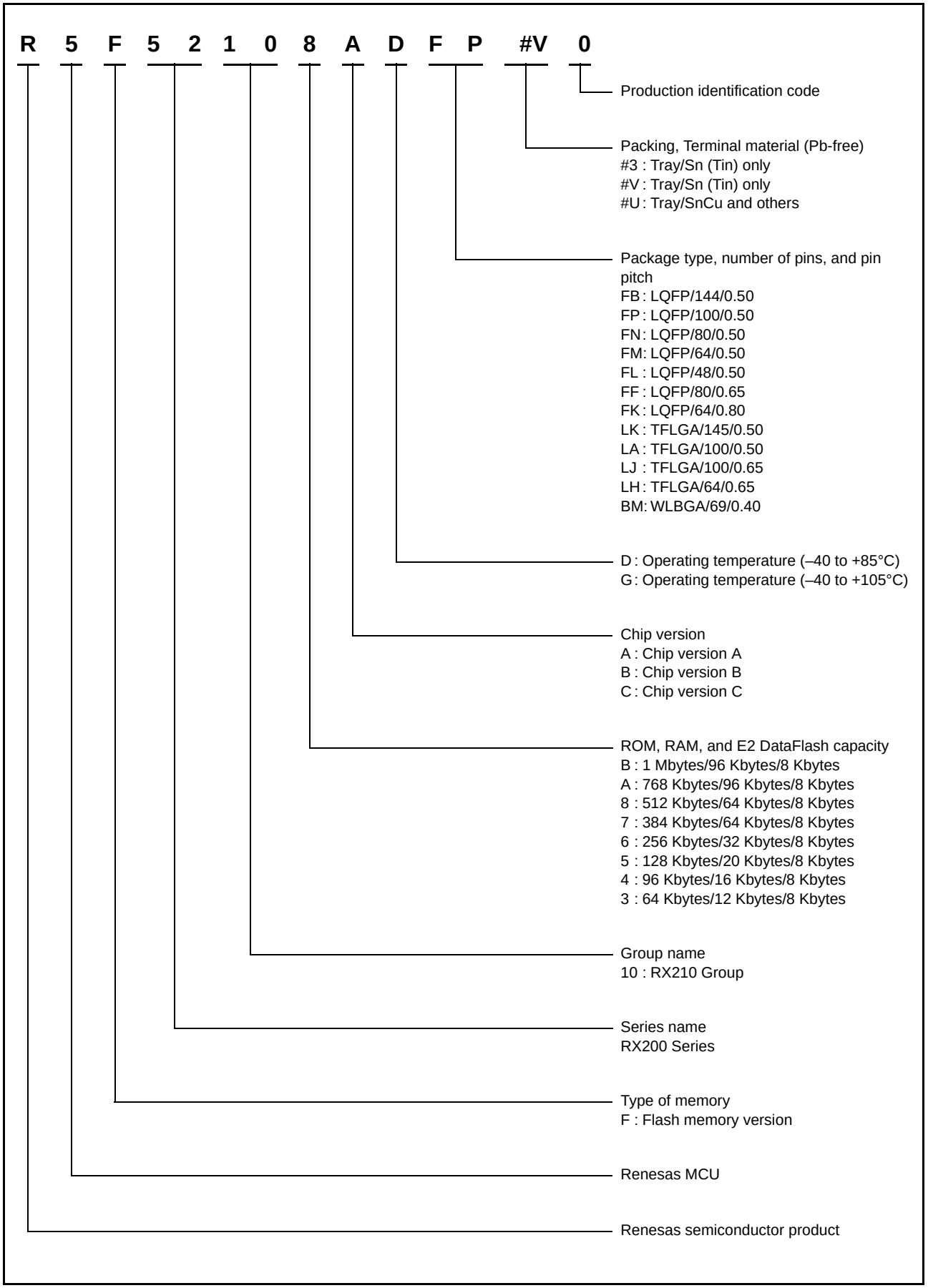
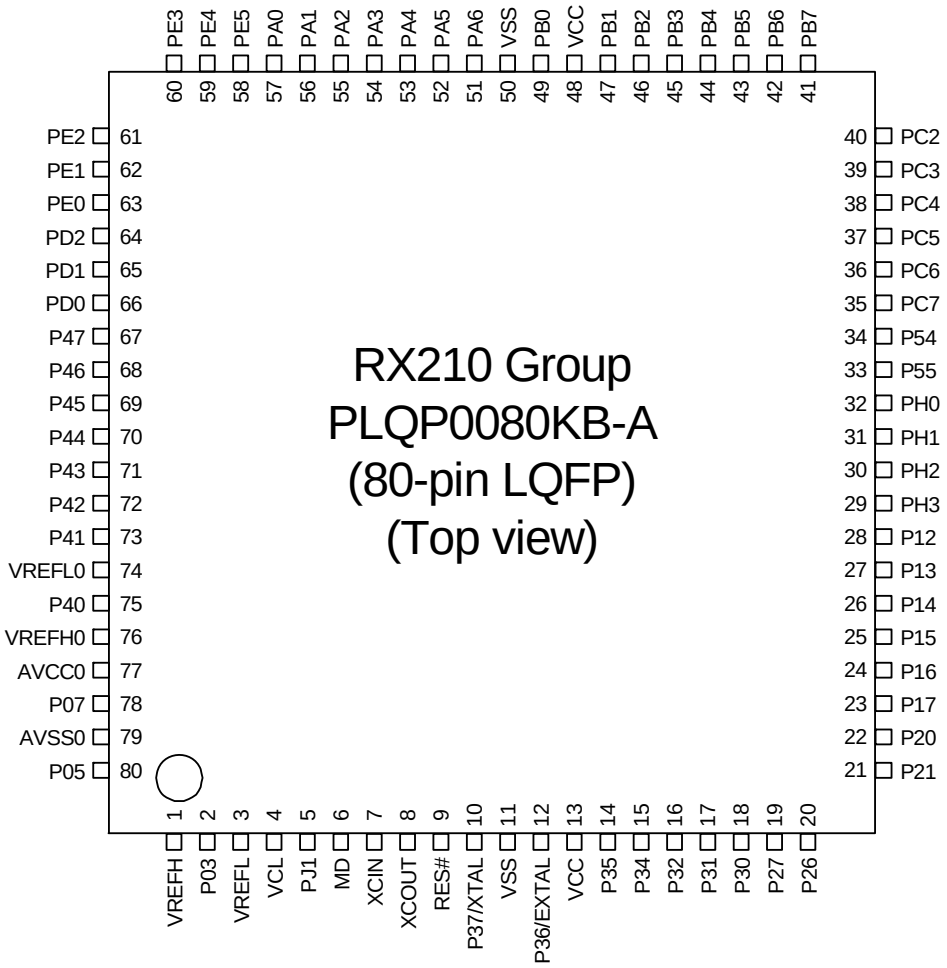


Figure 1.1 How to Read the Product Part No., Memory Capacity, and Package Type



Note: • This figure indicates the power supply pins and I/O port pins. For the pin configuration, see the table “List of Pins and Pin Functions (80-Pin LQFP)”.

Figure 1.7 Pin Assignments of the 80-Pin LQFP

Table 1.10 List of Pins and Pin Functions (144-Pin LQFP) (3 / 4)

Pin No.	Power Supply, Clock, System Control	I/O Port	External Bus	Timers (MTU, TMR, POE)	Communications (SCIc, SCId, RSPI, RIIC)	Others
81		PB4	A12	TIOCA4	CTS9#/RTS9#/SS9#	
82		PB3	A11	MTIOC0A/MTIOC4A/ TMO0/POE3#/ TIOCD3/TCLKD	SCK4/SCK6	
83		PB2	A10	TIOCC3/TCLKC	CTS4#/RTS4#/SS4#/ CTS6#/RTS6#/SS6#	
84		PB1	A9	MTIOC0C/MTIOC4C/ TMCI0/TIOCB3	TXD4/SMOSI4/SSDA4/ TXD6/SMOSI6/SSDA6	IRQ4-DS
85		P72				
86		P71				
87		PB0	A8	MTIC5W/TIOCA3	RXD4/SMISO4/SSCL4/ RXD6/SMISO6/SSCL6/ RSPCKA	
88		PA7	A7	TIOCB2	MISOA	
89		PA6	A6	MTIC5V/MTCLKB/ TMCI3/POE2#/TIOCA2	CTS5#/RTS5#/SS5#/ MOSIA/	
90		PA5	A5	TIOCB1	RSPCKA	
91	VCC					
92		PA4	A4	MTIC5U/MTCLKA/ TMRI0/TIOCA1	TXD5/SMOSI5/SSDA5/ SSLA0	IRQ5-DS/CVREFB1
93	VSS					
94		PA3	A3	MTIOC0D/MTCLKD/ TIOCD0/TCLKB	RXD5/SMISO5/SSCL5	IRQ6-DS/CMPB1
95		PA2	A2		RXD5/SMISO5/SSCL5/ SSLA3	
96		PA1	A1	MTIOC0B/MTCLKC/ TIOCB0	SCK5/SSLA2	CVREFA
97		PA0	A0/BC0#	MTIOC4A/TIOCA0	SSLA1	CACREF
98		P67				
99		P66				
100		P65				
101		PE7	D15[A15/D15]			IRQ7/AN015
102		PE6	D14[A14/D14]		CTS4#/RTS4#/SS4#	IRQ6/AN014
103		PK5			TXD4/SMOSI4/SSDA4	
104		P70			SCK4	
105		PK4			RXD4/SMISO4/SSCL4	
106		PE5	D13[A13/D13]	MTIOC4C/MTIOC2B		IRQ5/AN013
107		PE4	D12[A12/D12]	MTIOC4D/MTIOC1A		AN012/CMPA2
108		PE3	D11[A11/D11]	MTIOC4B/POE8#	CTS12#/RTS12#/SS12#	AN011/CMPA1
109		PE2	D10[A10/D10]	MTIOC4A	RXD12/RXDX12/ SMISO12/SSCL12	IRQ7-DS/AN010/ CVREFB0
110		PE1	D9[A9/D9]	MTIOC4C	TXD12/TXDX12/SIOX12/ SMOSI12/SSDA12	AN009/CMPB0
111		PE0	D8[A8/D8]		SCK12	AN008
112		P64				
113		P63				
114		P62				
115		P61			CTS9#/RTS9#/SS9#	
116		PK3			RXD9/SMISO9/SSCL9	
117		P60			SCK9	
118		PK2			TXD9/SMOSI9/SSDA9	
119		PD7	D7[A7/D7]	MTIC5U/POE0#		IRQ7
120		PD6	D6[A6/D6]	MTIC5V/POE1#		IRQ6
121		PD5	D5[A5/D5]	MTIC5W/POE2#		IRQ5

Table 1.13 List of Pins and Pin Functions (80-Pin LQFP) (2 / 2)

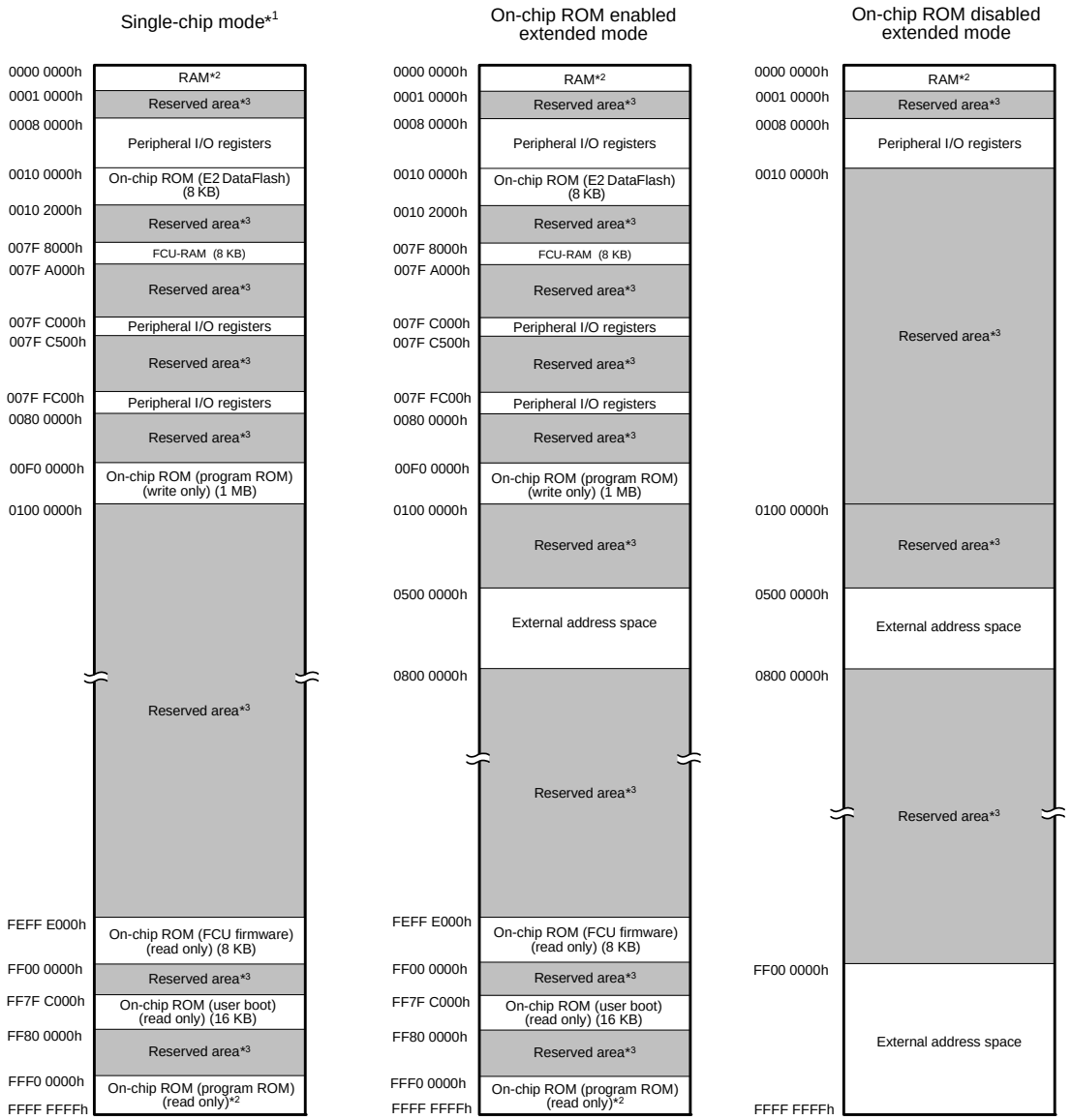
Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (MTU, TMR, POE)	Communications (SCIc, SCId, RSPI, RIIC)	Others
45		PB3	MTIOC0A/MTIOC4A/TMO0/ POE3#	SCK6	
46		PB2		CTS6#/RTS6#/SS6#	
47		PB1	MTIOC0C/MTIOC4C/TMCI0	TXD6/SMOSI6/SSDA6	IRQ4-DS
48	VCC				
49		PB0	MTIC5W	RXD6/SMISO6/SSCL6/RSPCKA	
50	VSS				
51		PA6	MTIC5V/MTCLKB/TMCI3/ POE2#	CTS5#/RTS5#/SS5#/MOSIA	
52		PA5		RSPCKA	
53		PA4	MTIC5U/MTCLKA/TMRI0	TXD5/SMOSI5/SSDA5/SSLA0	IRQ5-DS/CVREFB1
54		PA3	MTIOC0D/MTCLKD	RXD5/SMISO5/SSCL5	IRQ6-DS/CMPB1
55		PA2		RXD5/SMISO5/SSCL5/SSLA3	
56		PA1	MTIOC0B/MTCLKC	SCK5/SSLA2	CVREFA
57		PA0	MTIOC4A	SSLA1	CACREF
58		PE5	MTIOC4C/MTIOC2B		IRQ5/AN013
59		PE4	MTIOC4D/MTIOC1A		AN012/CMPA2
60		PE3	MTIOC4B/POE8#	CTS12#/RTS12#/SS12#	AN011/CMPA1
61		PE2	MTIOC4A	RXD12/RXDX12/SMISO12/ SSCL12	IRQ7-DS/AN010/ CVREFB0
62		PE1	MTIOC4C	TXD12/TXDX12/SIOX12/ SMOSI12/SSDA12	AN009/CMPB0
63		PE0		SCK12	AN008
64		PD2	MTIOC4D		IRQ2
65		PD1	MTIOC4B		IRQ1
66		PD0			IRQ0
67		P47			AN007
68		P46			AN006
69		P45			AN005
70		P44			AN004
71		P43			AN003
72		P42			AN002
73		P41			AN001
74	VREFL0				
75		P40			AN000
76	VREFH0				
77	AVCC0				
78		P07			ADTRG0#
79	AVSS0				
80		P05			DA1

Note: • Pin names to which –DS is appended are for pins that can be used to trigger release from deep software standby mode.

3. Address Space

3.1 Address Space

This LSI has a 4-Gbyte address space, consisting of the range of addresses from 0000 0000h to FFFF FFFFh. That is, linear access to an address space of up to 4 Gbytes is possible, and this contains both program and data areas.
Figure 3.1 shows the memory maps in the respective operating modes. Accessible areas will differ according to the operating mode and states of control bits.



Note 1. The address space in boot mode and user boot mode is the same as the address space in single-chip mode.
Note 2. The capacity of ROM/RAM differs depending on the products.

ROM (bytes)		RAM (bytes)	
Capacity	**Address**	**Capacity**	**Address**
1 M	FFF0 0000h to FFFF FFFFh	96 K	0000 0000h to 0001 7FFFh
768 K	FFF4 0000h to FFFF FFFFh		
512 K	FFF8 0000h to FFFF FFFFh	64 K	0000 0000h to 0000 FFFFh
384 K	FFFA 0000h to FFFF FFFFh		
256 K	FFFC 0000h to FFFF FFFFh	32 K	0000 0000h to 0000 7FFFh
128 K	FFFE 0000h to FFFF FFFFh	20 K	0000 0000h to 0000 4FFFh
96 K	FFFE 8000h to FFFF FFFFh	16 K	0000 0000h to 0000 3FFFh
64 K	FFFF 0000h to FFFF FFFFh	12 K	0000 0000h to 0000 2FFFh

Note:•See Table 1.3 to Table 1.7 List of Products, for the product type name.

Note 3. Reserved areas should not be accessed.

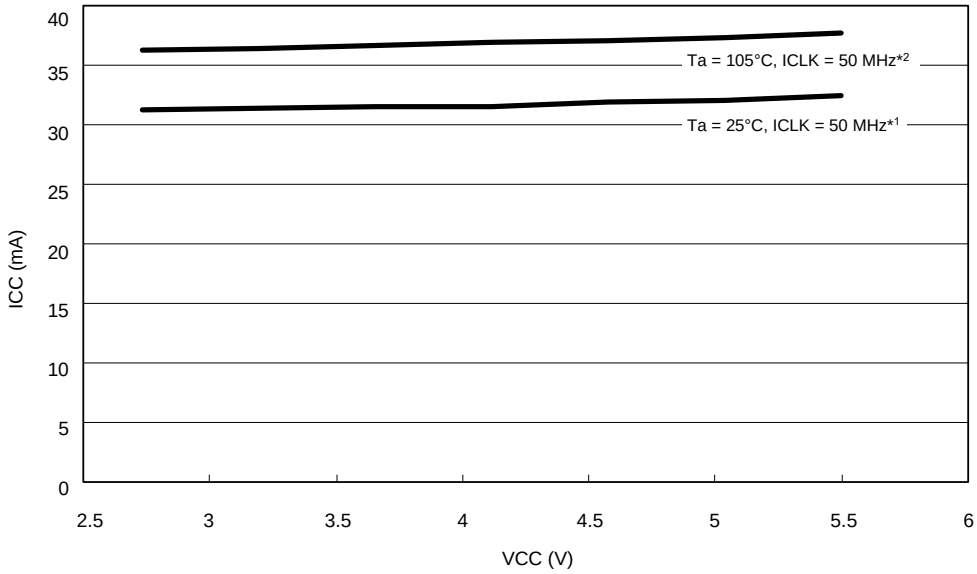
Figure 3.1 Memory Map in Each Operating Mode

Table 4.1 List of I/O Registers (Address Order) (23 / 29)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles: ICLK ≥ PCLK	Number of Access Cycles: ICLK < PCLK
0008 C042h	PORT2	Port input data register	PIDR	8	8	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing	3 ICLK cycles when reading, 2 ICLK cycles when writing
0008 C043h	PORT3	Port input data register	PIDR	8	8	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing	3 ICLK cycles when reading, 2 ICLK cycles when writing
0008 C044h	PORT4	Port input data register	PIDR	8	8	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing	3 ICLK cycles when reading, 2 ICLK cycles when writing
0008 C045h	PORT5	Port input data register	PIDR	8	8	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing	3 ICLK cycles when reading, 2 ICLK cycles when writing
0008 C046h	PORT6	Port input data register	PIDR	8	8	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing	3 ICLK cycles when reading, 2 ICLK cycles when writing
0008 C047h	PORT7	Port input data register	PIDR	8	8	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing	3 ICLK cycles when reading, 2 ICLK cycles when writing
0008 C048h	PORT8	Port input data register	PIDR	8	8	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing	3 ICLK cycles when reading, 2 ICLK cycles when writing
0008 C049h	PORT9	Port input data register	PIDR	8	8	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing	3 ICLK cycles when reading, 2 ICLK cycles when writing
0008 C04Ah	PORTA	Port input data register	PIDR	8	8	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing	3 ICLK cycles when reading, 2 ICLK cycles when writing
0008 C04Bh	PORTB	Port input data register	PIDR	8	8	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing	3 ICLK cycles when reading, 2 ICLK cycles when writing

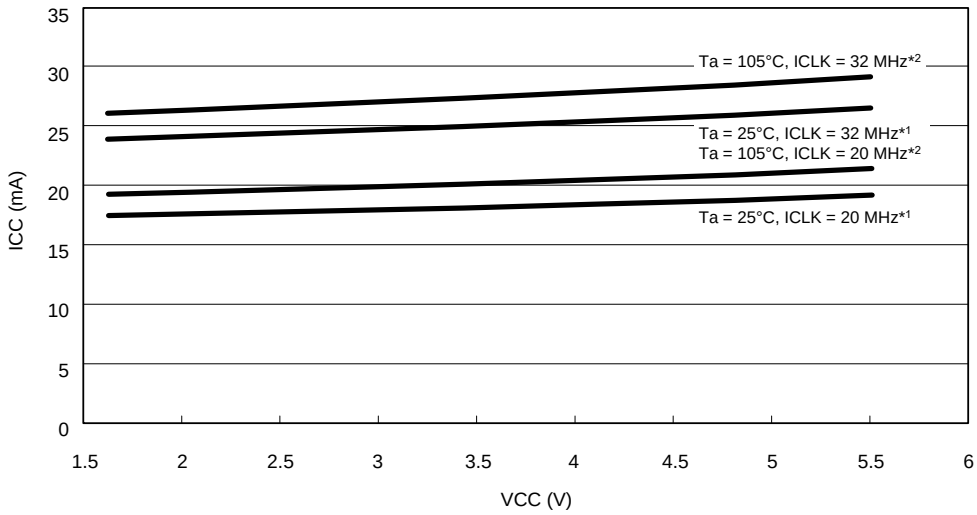
Table 4.1 List of I/O Registers (Address Order) (24 / 29)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles: ICLK ≥ PCLK	Number of Access Cycles: ICLK < PCLK
0008 C04Ch	PORTC	Port input data register	PIDR	8	8	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing	3 ICLK cycles when reading, 2 ICLK cycles when writing
0008 C04Dh	PORTD	Port input data register	PIDR	8	8	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing	3 ICLK cycles when reading, 2 ICLK cycles when writing
0008 C04Eh	PORTE	Port input data register	PIDR	8	8	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing	3 ICLK cycles when reading, 2 ICLK cycles when writing
0008 C04Fh	PORTF	Port input data register	PIDR	8	8	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing	3 ICLK cycles when reading, 2 ICLK cycles when writing
0008 C051h	PORTH	Port input data register	PIDR	8	8	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing	3 ICLK cycles when reading, 2 ICLK cycles when writing
0008 C052h	PORTJ	Port input data register	PIDR	8	8	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing	3 ICLK cycles when reading, 2 ICLK cycles when writing
0008 C053h	PORTK	Port input data register	PIDR	8	8	2, 3 PCLKB	2 ICLK
0008 C054h	PORTL	Port input data register	PIDR	8	8	2, 3 PCLKB	2 ICLK
0008 C060h	PORT0	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK
0008 C061h	PORT1	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK
0008 C062h	PORT2	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK
0008 C063h	PORT3	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK
0008 C064h	PORT4	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK
0008 C065h	PORT5	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK
0008 C066h	PORT6	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK
0008 C067h	PORT7	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK
0008 C068h	PORT8	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK
0008 C069h	PORT9	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK
0008 C06Ah	PORTA	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK
0008 C06Bh	PORTB	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK
0008 C06Ch	PORTC	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK
0008 C06Dh	PORTD	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK
0008 C06Eh	PORTE	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK
0008 C06Fh	PORTF	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK
0008 C071h	PORTH	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK
0008 C072h	PORTJ	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK
0008 C073h	PORTK	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK
0008 C074h	PORTL	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK



Note 1. All peripheral operation is normal. This does not include BGO operation.
Average value of the tested middle samples during product evaluation.
Note 2. All peripheral operation is maximum. This does not include BGO operation.
Average value of the tested upper-limit samples during product evaluation.

Figure 5.9 Voltage Dependency in High-Speed Operating Mode (Reference Data) for Chip Version C

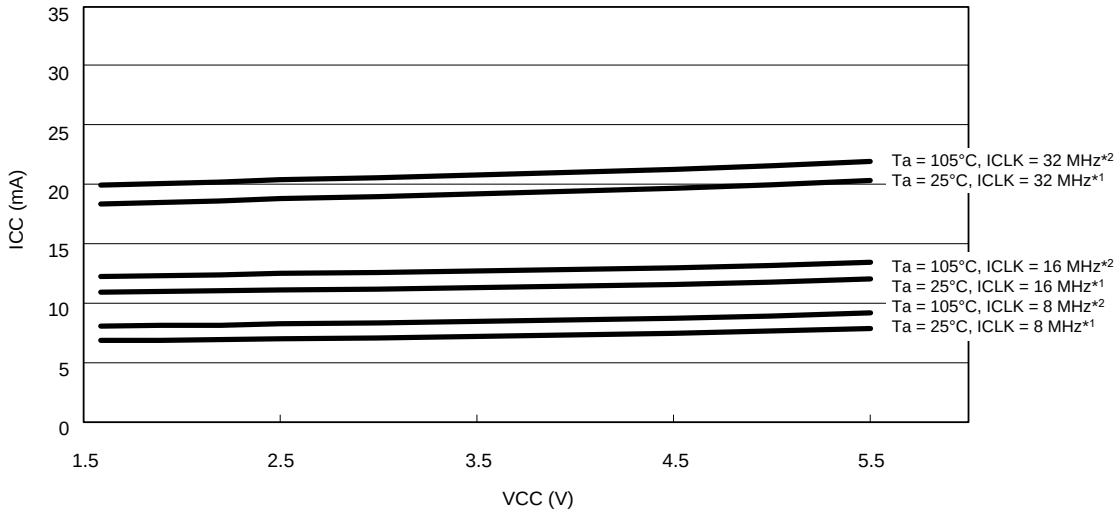


Note 1. All peripheral operation is normal. This does not include BGO operation.
Average value of the tested middle samples during product evaluation.
Note 2. All peripheral operation is maximum. This does not include BGO operation.
Average value of the tested upper-limit samples during product evaluation.

Figure 5.10 Voltage Dependency in Middle-Speed Operating Modes 1A and 1B (Reference Data) for Chip Version C

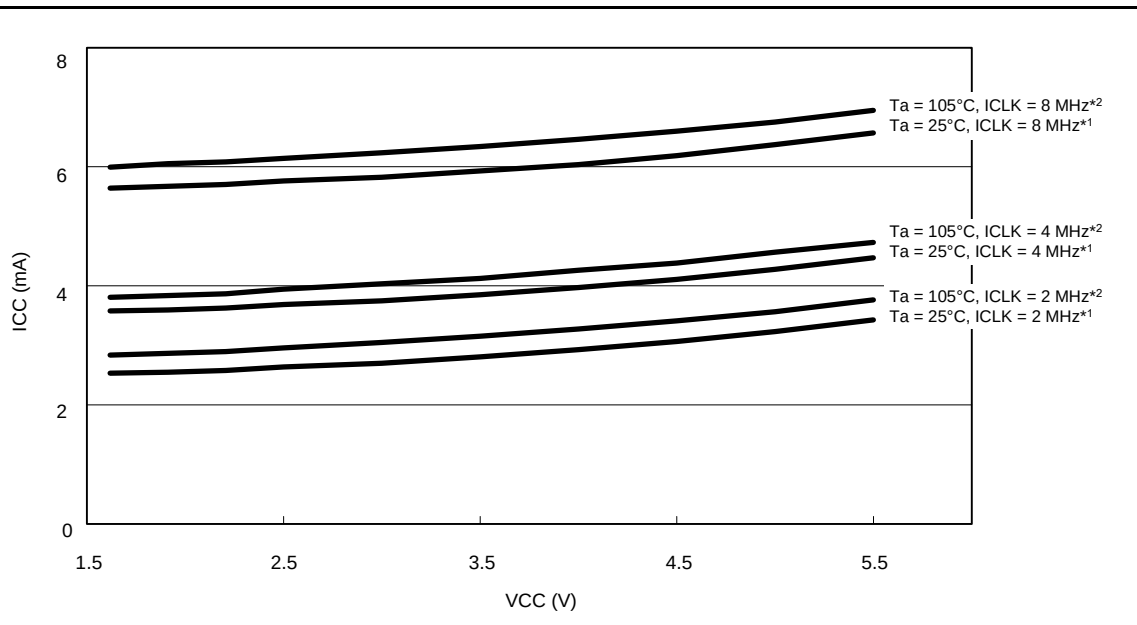
Item					Symbol	Typ.	Max.	Unit	Test Conditions
Supply current*1	Low-speed operating mode 1	Normal operating mode	No peripheral operation*7	ICLK = 8 MHz	I_{CC}	2	—	mA	
				ICLK = 4 MHz		1.6	—		
				ICLK = 2 MHz		1.5	—		
			All peripheral operation: Normal*8	ICLK = 8 MHz		6	—		
				ICLK = 4 MHz		3.8	—		
				ICLK = 2 MHz		2.8	—		
			All peripheral operation: Max.*8	ICLK = 8 MHz		—	12		
				ICLK = 4 MHz		—	—		
				ICLK = 2 MHz		—	—		
		Sleep mode	No peripheral operation	ICLK = 8 MHz		1.5	—		
				ICLK = 4 MHz		1.4	—		
				ICLK = 2 MHz		1.3	—		
			All peripheral operation: Normal	ICLK = 8 MHz		3.6	—		
				ICLK = 4 MHz		2.7	—		
				ICLK = 2 MHz		2.2	—		
		All-module clock stop mode		ICLK = 8 MHz		1.4	—		
				ICLK = 4 MHz		1.3	—		
				ICLK = 2 MHz		1.2	—		
	Low-speed operating mode 2	Normal operating mode	No peripheral operation*9	ICLK = 32 kHz		0.021	—		
			All peripheral operation: Normal*10	ICLK = 32 kHz		0.05	—		
			All peripheral operation: Max.*10	ICLK = 32 kHz		—	3*11		
		Sleep mode	No peripheral operation	ICLK = 32 kHz		0.017	—		
			All peripheral operation: Normal	ICLK = 32 kHz		0.034	—		
		All-module clock stop mode				0.016	—		

Note 1. Supply current values do not include output charge/discharge current from all pins. The values apply when internal pull-up MOSs are in the off state.
Note 2. Clock supply to the peripheral functions is stopped. This does not include BGO operation. The clock source is PLL and the VCO oscillation frequency is 64 MHz. BCLK, FCLK, and PCLK are set to divided by 64.
Note 3. Clock supply to the peripheral functions is stopped. This does not include BGO operation. The clock source is HOCO and the oscillation frequency is 40 MHz. BCLK, FCLK, and PCLK are set to divided by 64.
Note 4. Clocks are supplied to the peripheral functions. This does not include BGO operation. The clock source is PLL and the VCO oscillation frequency is 64 MHz. BCLK, FCLK, and PCLK are ICLK divided by 1.
Note 5. Clocks are supplied to the peripheral functions. This does not include BGO operation. The clock source is HOCO and the oscillation frequency is 40 MHz. BCLK, FCLK, and PCLK are ICLK divided by 1.
Note 6. This is the increase if data is programmed to or erasing from the ROM or E2 DataFlash during program execution.
Note 7. Clock supply to the peripheral functions is stopped. This does not include BGO operation. The clock source is HOCO and the oscillation frequency is 32 MHz. BCLK, FCLK, and PCLK are set to divided by 64.
Note 8. Clocks are supplied to the peripheral functions. This does not include BGO operation. The clock source is HOCO and the oscillation frequency is 32 MHz. BCLK, FCLK, and PCLK are ICLK divided by 1.
Note 9. Clock supply to the peripheral functions is stopped. This does not include BGO operation. The clock source is the sub oscillation circuit. BCLK, FCLK, and PCLK are set to divided by 64.
Note 10. Clocks are supplied to the peripheral functions. This does not include BGO operation. The clock source is the sub oscillation circuit. BCLK, FCLK, and PCLK are ICLK divided by 1.
Note 11. Value when the main clock continues oscillating at 12.5 MHz.



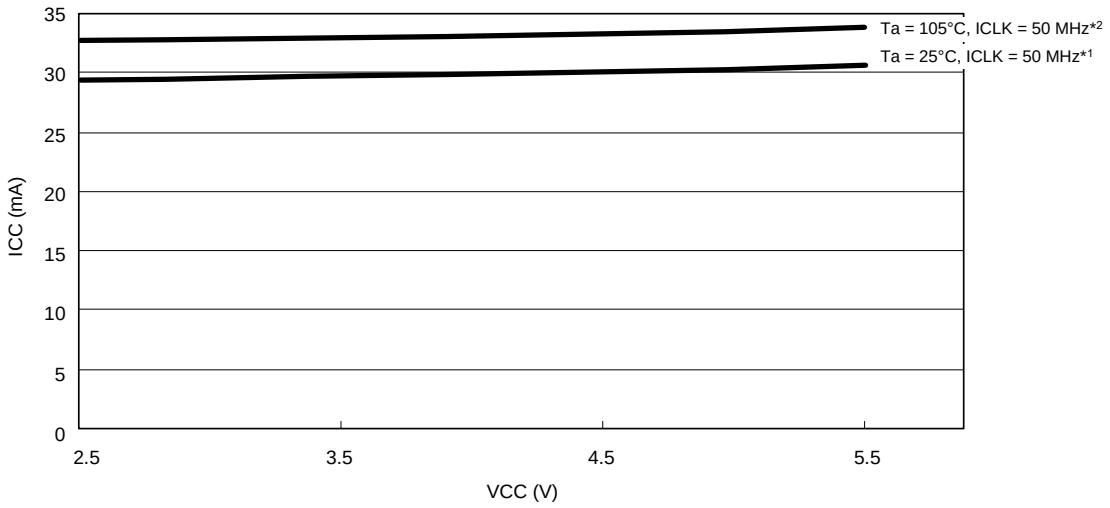
Note 1. All peripheral operation is normal. This does not include BGO operation.
Average value of the tested middle samples during product evaluation.
Note 2. All peripheral operation is maximum. This does not include BGO operation.
Average value of the tested upper-limit samples during product evaluation.

Figure 5.19 Voltage Dependency in Middle-Speed Operating Modes 2A and 2B (Reference Data) for Chip Version B with 256 Kbytes or Less of Flash Memory and 48 to 100 Pins



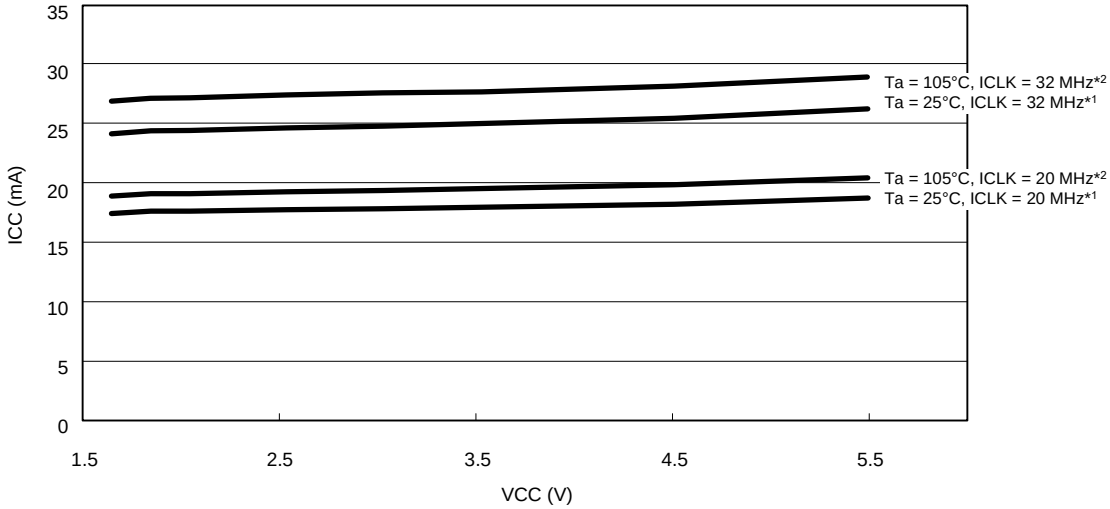
Note 1. All peripheral operation is normal.
Average value of the tested middle samples during product evaluation.
Note 2. All peripheral operation is maximum.
Average value of the tested upper-limit samples during product evaluation.

Figure 5.20 Voltage Dependency in Low-Speed Operating Mode 1 (Reference Data) for Chip Version B with 256 Kbytes or Less of Flash Memory and 48 to 100 Pins



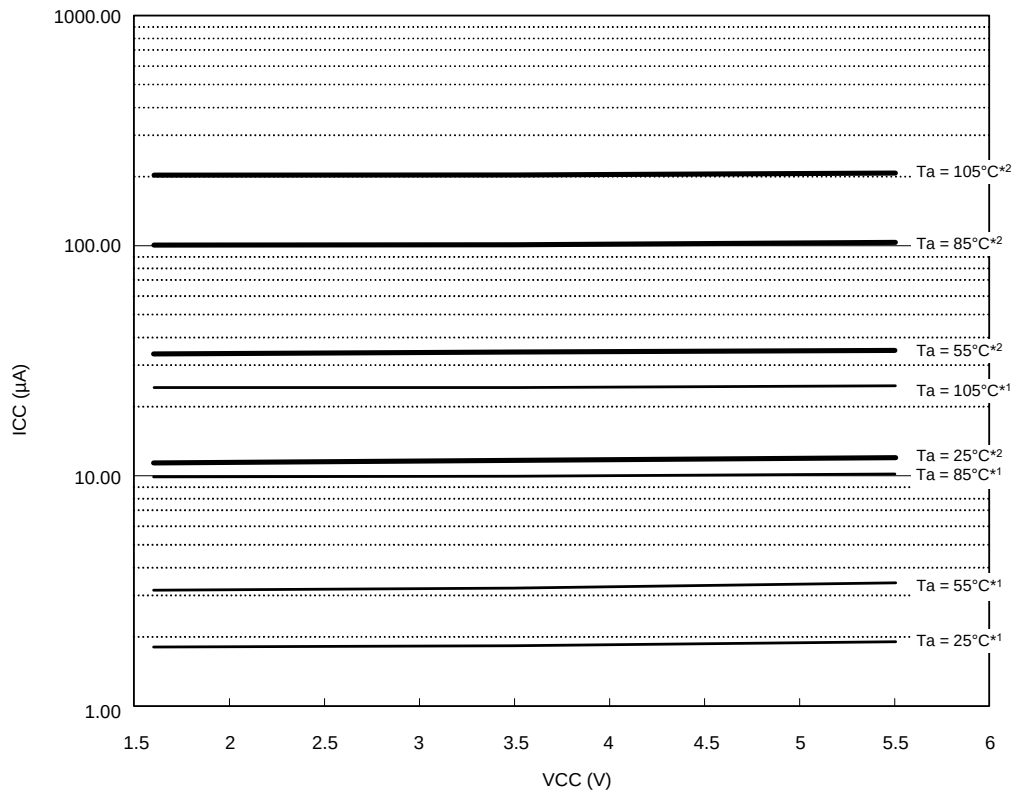
Note 1. All peripheral operation is normal. This does not include BGO operation.
Average value of the tested middle samples during product evaluation.
Note 2. All peripheral operation is maximum. This does not include BGO operation.
Average value of the tested upper-limit samples during product evaluation.

Figure 5.26 Voltage Dependency in High-Speed Operating Mode (Reference Data) for Chip Version B with 768 Kbytes/1 Mbyte of Flash Memory and 100 to 145 Pins



Note 1. All peripheral operation is normal. This does not include BGO operation.
Average value of the tested middle samples during product evaluation.
Note 2. All peripheral operation is maximum. This does not include BGO operation.
Average value of the tested upper-limit samples during product evaluation.

Figure 5.27 Voltage Dependency in Middle-Speed Operating Modes 1A and 1B (Reference Data) for Chip Version B with 768 Kbytes/1 Mbyte of Flash Memory and 100 to 145 Pins



Note 1. Average value of the tested middle samples during product evaluation.
Note 2. Average value of the tested upper-limit samples during product evaluation.

Figure 5.31 Voltage Dependency in Software Standby Mode (SOFTCUT[2:0] Bits = 110b) (Reference Data) for Chip Version B with 768 Kbytes/1 Mbyte of Flash Memory and 100 to 145 Pins

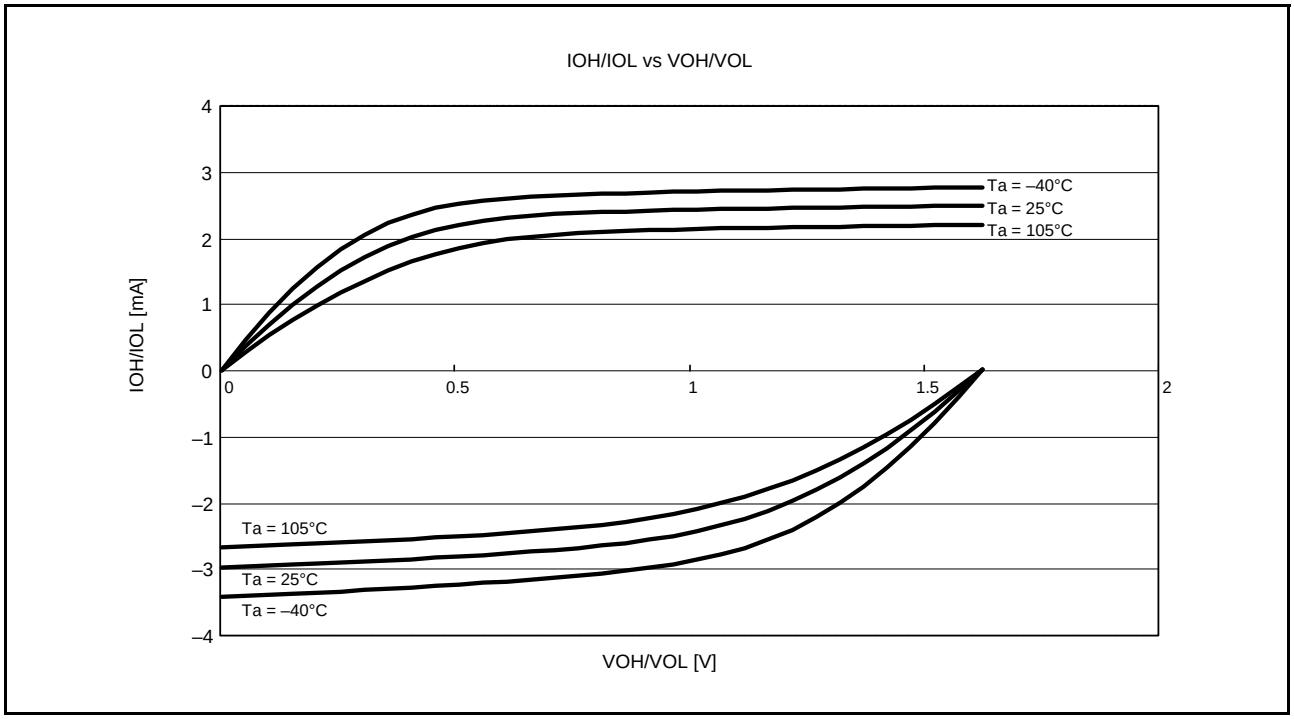


Figure 5.46 VOH/VOL and IOH/IOL Temperature Characteristics at VCC = 1.62 V when Normal Output is Selected (Reference Data)

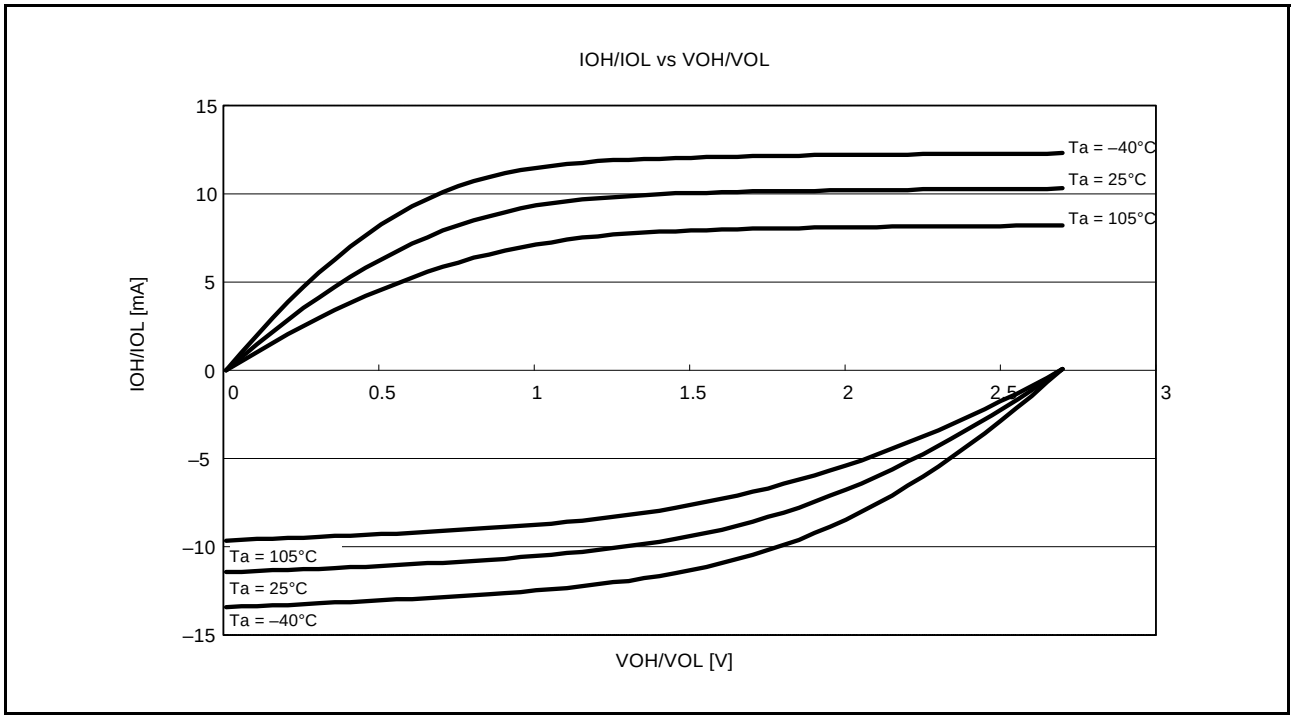


Figure 5.47 VOH/VOL and IOH/IOL Temperature Characteristics at VCC = 2.7 V when Normal Output is Selected (Reference Data)

[Chip version B]

Table 5.39 Operation Frequency Value (Low-Speed Operating Mode 1)

Conditions: VCC = AVCC0 = 1.62 to 5.5 V, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +105°C

Item		Symbol	VCC			Unit
			1.62 to 1.8 V	1.8 to 2.7 V	2.7 to 5.5 V	
Maximum operating frequency	System clock (ICLK)	f_{max}	2	4	8	MHz
	FlashIF clock (FCLK)*1		2	4	8	
	Peripheral module clock (PCLKB)		2	4	8	
	Peripheral module clock (PCLKD)*2		2	4	8	
	External bus clock (BCLK)		2	4	8	
	BCLK pin output		2	4	8	

Note 1. Programming and erasing the flash memory is impossible.
Note 2. The lower-limit frequency of PCLKD is 1 MHz when the A/D converter is in use.

[Chip versions A, B, and C]

Table 5.40 Operation Frequency Value (Low-Speed Operating Mode 2)

Conditions: VCC = AVCC0 = 1.62 to 5.5 V, VSS = AVSS0 = VREFL=VREFL0 = 0 V, T_a = –40 to +105°C

Item		Symbol	VCC			Unit
			1.62 to 1.8 V	1.8 to 2.7 V	2.7 to 5.5 V	
Maximum operating frequency	System clock (ICLK)	f_{max}	32.768	32.768	32.768	kHz
	FlashIF clock (FCLK)*1		32.768	32.768	32.768	
	Peripheral module clock (PCLKB)		32.768	32.768	32.768	
	Peripheral module clock (PCLKD)*2		32.768	32.768	32.768	
	External bus clock (BCLK)		32.768	32.768	32.768	
	BCLK pin output		32.768	32.768	32.768	

Note 1. Programming and erasing the flash memory is impossible.
Note 2. The A/D converter cannot be used.

Table 5.44 Clock Timing

Conditions: VCC = AVCC0 = 1.62 to 5.5 V, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
EXTAL external clock input cycle time		t_{EXcyc}	50	—	—	ns	Figure 5.60
EXTAL external clock input high pulse width		t_{EXH}	20	—	—	ns	
EXTAL external clock input low pulse width		t_{EXL}	20	—	—	ns	
EXTAL external clock rising time		t_{EXr}	—	—	5	ns	
EXTAL external clock falling time		t_{EXf}	—	—	5	ns	
EXTAL external clock input wait time*1		t_{EXWT}	1	—	—	ms	
Main clock oscillator oscillation frequency*2		f_{MAIN}	1	—	20	MHz	
Main clock oscillation stabilization time (crystal)*2		$t_{MAINOSC}$	—	3	—	ms	Figure 5.61
Main clock oscillation stabilization time (ceramic resonator)*2		$t_{MAINOSC}$	—	50		µs	
Main clock oscillation stabilization wait time (crystal)*2		$t_{MAINOSCWT}$	—	6	—	ms	
Main clock oscillation stabilization wait time (ceramic resonator)*2		$t_{MAINOSCWT}$	—	100		µs	
LOCO clock cycle time		t_{cyc}	7.27	8	8.89	µs	
LOCO clock oscillation frequency*6		f_{LOCO}	112.5	125	137.5	kHz	
LOCO clock oscillation stabilization wait time		t_{LOCOWT}	—	—	20	µs	Figure 5.62
HOCO clock oscillation frequency*7		f_{HOCO}	31.680	32	32.320	MHz	Ta = 0 to 50°C
			36.495	36.864	37.233		
			39.600	40	40.400		
			49.500	50	50.500		
			31.520	32	32.480		Ta = -40 to 105°C
			36.311	36.864	37.417		
			39.400	40	40.600		
			49.250	50	50.750		
HOCO clock oscillation stabilization time 1		t_{HOCO1}	—	—	300	µs	Figure 5.63
HOCO clock oscillation stabilization time 2		t_{HOCO2}	—	—	175	µs	Figure 5.64
HOCO clock oscillation stabilization wait time		t_{HOCOWT}	—	—	350	µs	Figure 5.64
HOCO clock power supply stabilization time		t_{HOCOP}	—	—	350	µs	Figure 5.65
PLL input frequency		f_{PLLIN}	4	—	12.5	MHz	
PLL circuit oscillation frequency		f_{PLL}	50	—	100	MHz	
PLL clock oscillation stabilization time	PLL operation started after main clock oscillation has settled	t_{PLL1}	—	—	500	µs	Figure 5.66
PLL clock oscillation stabilization wait time		t_{PLLWT1}	1.5	—	—	ms	
PLL clock oscillation stabilization time*4	PLL operation started before main clock oscillation has settled	t_{PLL2}	—	3.5*3	—	ms	Figure 5.67
PLL clock oscillation stabilization wait time*4		t_{PLLWT2}	—	7	—	ms	
PLL clock power supply stabilization time (for chip version B only)		t_{PLLPW}	—	—	30	µs	Figure 5.68
Sub-clock oscillator oscillation frequency		f_{SUB}	—	32.768	—	kHz	
Sub-clock oscillation stabilization time*5		t_{SUBOSC}	2	—	—	s	Figure 5.69
Sub-clock oscillation stabilization wait time*5		$t_{SUBOSCWT}$	4	—	—	s	

Note 1. The time interval from the time P36 and P37 are configured for input and the main clock oscillator stopping bit (MOSCCR.MOSTP) is set to 0 (operating) until the clock becomes available.

Table 5.54 Bus Timing (Multiplexed Bus) (3)

Conditions: VCC = AVCC0 = 1.62 to 1.8 V, VSS = AVSS0 = VREFL = VREFL0 = 0 V,
fBCLK ≤ 12 MHz (BCLK pin output frequency ≤ 6 MHz), T_a = –40 to +105°C, V_{OH} = VCC × 0.5,
V_{OL} = VCC × 0.5, I_{OH} = –0.5 mA, I_{OL} = 0.5 mA, C_L = 30 pF
When normal output is selected by the drive capacity register

Item	Symbol	Min.	Typ.	Max.	Unit
Address delay time	t_{AD}	—	125	ns	Figure 5.81 and Figure 5.82
Byte control delay time	t_{BCD}	—	125	ns	
CS# delay time	t_{CSD}	—	125	ns	
RD# delay time	t_{RSD}	—	125	ns	
ALE delay time	t_{ALED}	—	125	ns	
Read data setup time	t_{RDS}	85	—	ns	
Read data hold time	t_{RDH}	0	—	ns	
WR# delay time	t_{WRD}	—	125	ns	
Write data delay time	t_{WDD}	—	125	ns	
Write data hold time	t_{WDH}	0	—	ns	
WAIT# setup time	t_{WTS}	85	—	ns	Figure 5.80
WAIT# hold time	t_{WTH}	0	—	ns	

[Chip versions A and C]

Table 5.77 ROM (Flash Memory for Code Storage) Characteristics (4) : middle-speed operating mode 1B

Conditions: VCC = AVCC0 = 1.62 to 3.6 V, VREFH = VREFH0 = AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V
Temperature range for the programming/erasure operation: T_a = –40 to +105°C

Item		Symbol	FCLK = 4 MHz			FCLK = 32 MHz*1			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Programming time when N_{PEC} ≤ 100 times	2 bytes	t_{P2}	—	0.69	6.0	—	0.30	3.5	ms
	8 bytes	t_{P8}	—	0.69	6.0	—	0.30	3.5	
	128 bytes	t_{P128}	—	1.76	14.2	—	0.85	8.3	
Programming time when N_{PEC} > 100 times	2 bytes	t_{P2}	—	0.81	7.1	—	0.35	4.2	ms
	8 bytes	t_{P8}	—	0.81	7.6	—	0.35	4.5	
	128 bytes	t_{P128}	—	1.99	17.5	—	0.96	10	
Erasure time when N_{PEC} ≤ 100 times	2 Kbytes	t_{E2K}	—	24.5	113.7	—	19.0	46	ms
Erasure time when N_{PEC} > 100 times	2 Kbytes	t_{E2K}	—	29.8	225.8	—	23.2	90 (1000 times ≥ N_{PEC} > 100 times), 98 (10000 times ≥ N_{PEC} > 1000 times)	ms
Suspend delay time during programming (in programming/erasure priority mode)		t_{SPD}	—	—	1.7	—	—	1.6	ms
First suspend delay time during programming (in suspend priority mode)		t_{SPSD1}	—	—	220	—	—	120	µs
Second suspend delay time during programming (in suspend priority mode)		t_{SPSD2}	—	—	1.7	—	—	1.6	ms
Suspend delay time during erasing (in programming/erasure priority mode)		t_{SED}	—	—	1.7	—	—	1.6	ms
First suspend delay time during erasing (in suspend priority mode)		t_{SESD1}	—	—	220	—	—	120	µs
Second suspend delay time during erasing (in suspend priority mode)		t_{SESD2}	—	—	1.7	—	—	1.6	ms
FCU reset time		t_{FCUR}	20 µs or longer and FCLK × 6 or greater	—	—	20 µs or longer and FCLK × 6 or greater	—	—	µs

Note 1. The operating frequency is 20 MHz (max.) when the voltage is in the range from 1.62 V to less than 1.8 V.

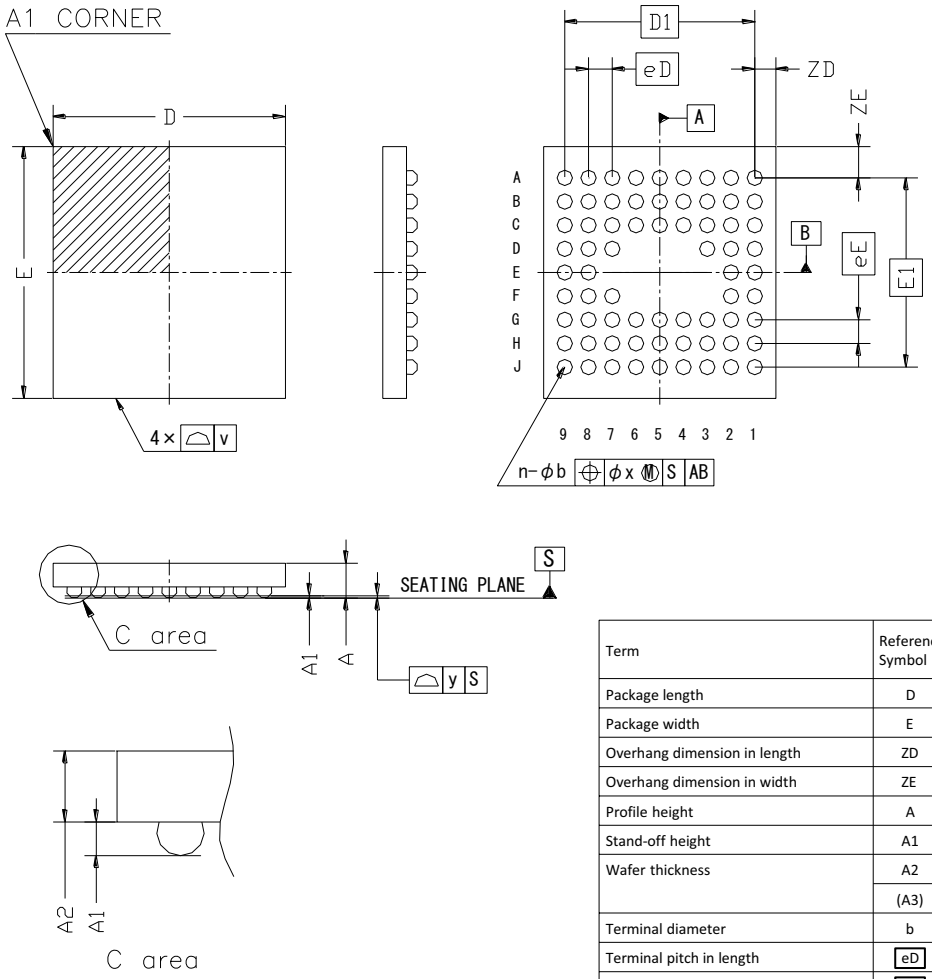
[Chip versions A and C]

Table 5.82 E2 DataFlash Characteristics (3)
: high-speed operating mode, middle-speed operating mode 1A

Conditions: VCC = AVCC0 = 2.7 to 5.5 V, VREFH = VREFH0 = AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V
Temperature range for the programming/erasure operation: T_a = –40 to +105°C

Item		Symbol	FCLK = 4 MHz			FCLK = 32 MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Programming time when N_{DPEC} ≤ 100 times	2 bytes	t_{DP2}	—	0.40	4.4	—	0.16	2.0	ms
	8 bytes	t_{DP8}	—	0.45	5.1	—	0.17	2.2	
Programming time when N_{DPEC} > 100 times	2 bytes	t_{DP2}	—	0.62	6.4	—	0.25	3.0	ms
	8 bytes	t_{DP8}	—	0.69	7.5	—	0.26	3.2	
Erasure time when N_{DPEC} ≤ 100 times	128 bytes	t_{DE128}	—	5.6	27.1	—	2.8	8	ms
Erasure time when N_{DPEC} > 100 times	128 bytes	t_{DE128}	—	6.8	45.1	—	3.4	12	ms
Blank check time	2 bytes	t_{DBC2}	—	—	98	—	—	35	µs
	2 Kbytes	t_{DBC2K}	—	—	16	—	—	2.5	ms
Suspend delay time during programming (in programming/erasure priority mode)		t_{DSPD}	—	—	0.9	—	—	0.8	ms
First suspend delay time during programming (in suspend priority mode)		t_{DSPSD1}	—	—	220	—	—	120	µs
Second suspend delay time during programming (in suspend priority mode)		t_{DSPSD2}	—	—	0.9	—	—	0.8	ms
Suspend delay time during erasing (in programming/erasure priority mode)		t_{DSED}	—	—	0.9	—	—	0.8	ms
First suspend delay time during erasing (in suspend priority mode)		t_{DSESD1}	—	—	220	—	—	120	µs
Second suspend delay time during erasing (in suspend priority mode)		t_{DSESD2}	—	—	0.9	—	—	0.8	ms

JEITA Package code	RENESAS Code	Previous Code	MASS(TYP.)[g]
S-WFBGA69-3.91x4.26-0.40	SWBG0069LA-A	—	0.02



注記:
1. 端子ﾋﾟｯﾁは端子中央部の位置で規定する。
2. ﾃﾞｰﾀﾑA及びBは、ﾎﾞｰﾙｸﾞﾘｯﾄﾞｾﾝﾀを称す。

Note:
1. Ball pitch dimension is specified with the center of balls.
2. Datum A and B are axes defined by the ball grid array, not by the PKG outline.

Dimensions in millimeters

Term	Reference Symbol	Specification		
		Min	Nom	Max
Package length	D	3.86	3.91	3.96
Package width	E	4.21	4.26	4.31
Overhang dimension in length	ZD	0.305	0.355	0.405
Overhang dimension in width	ZE	0.48	0.53	0.58
Profile height	A	—	—	0.70
Stand-off height	A1	0.15	0.19	0.23
Wafer thickness	A2	0.36	0.40	0.44
	(A3)	—	—	—
Terminal diameter	b	0.22	0.27	0.32
Terminal pitch in length	eD		0.4	(BSC)
Terminal pitch in width	eE		0.4	(BSC)
Center terminal position in D-direction	SD		—	(BSC)
Center terminal position in E-direction	SE		—	(BSC)
Edge ball center to center in D-direction	D1		3.2	(BSC)
Edge ball center to center in D-direction	E1		3.2	(BSC)
Number of terminals	n		69	
Tolerance of package lateral profile	v		0.05	
Positional tolerance of terminals	x		0.05	
Coplanarity	y		0.08	

Figure E 69-Pin WLBGA (SWBG0069LA-A)