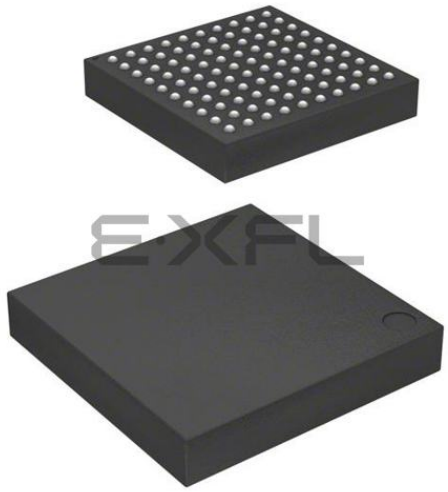
Renesas Electronics America Inc - R5F52106BDLA#U0 Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	EBI/EMI, I²C, SCI, SPI
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	84
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.62V ~ 5.5V
Data Converters	A/D 16x12b; D/A 2x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TFLGA
Supplier Device Package	100-TFLGA (5.5x5.5)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f52106bdla-u0

Table 1.1 Outline of Specifications (3 / 5)

Classification	Module/Function	Description
Timers	16-bit timer pulse unit (TPUa)	• (16 bits × 6 channels) × 1 unit • Maximum of 16 pulse-input/output possible • Select from among seven or eight counter-input clock signals for each channel • Supports the input capture/output compare function • Output of PWM waveforms in up to 15 phases in PWM mode • Support for buffered operation, phase-counting mode (two-phase encoder input) and cascade-connected operation (32 bits × 2 channels) depending on the channel. • Capable of generating conversion start triggers for the A/D converters • Signals from the input capture pins are input via a digital filter • Clock frequency measuring method (Products with 144 or more pins incorporate a TPU.)
	Multi-function timer pulse unit 2 (MTU2a)	• (16 bits × 6 channels) × 1 unit • Up to 16 pulse-input/output lines and three pulse-input lines are available with six 16-bit timer channels • Select from among eight or seven counter-input clock signals for each channel (PCLK/1, PCLK/4, PCLK/16, PCLK/64, PCLK/256, PCLK/1024, MTCLKA, MTCLKB, MTCLKC, MTCLKD) other than channel 5, for which only four signals are available. • Input capture function • 21 output compare/input capture registers • Pulse output mode • Complementary PWM output mode • Reset synchronous PWM mode • Phase-counting mode • Generation of triggers for A/D converter conversion
	Port output enable 2 (POE2a)	Controls the high-impedance state of the MTU's waveform output pins
	8-bit timer (TMR)	• (8 bits × 2 channels) × 2 units • Select from among seven internal clock signals (PCLK1, PCLK/2, PCLK/8, PCLK/32, PCLK/64, PCLK/1024, PCLK/8192) and one external clock signal • Capable of output of pulse trains with desired duty cycles or of PWM signals • The 2 channels of each unit can be cascaded to create a 16-bit timer • Capable of generating baud-rate clocks for SCI5, SCI6, and SCI12
	Compare match timer (CMT)	• (16 bits × 2 channels) × 2 units • Select from among four clock signals (PCLK/8, PCLK/32, PCLK/128, PCLK/512)
	Watchdog timer (WDTA)	• 14 bits × 1 channel • Select from among six counter-input clock signals (PCLK/4, PCLK/64, PCLK/128, PCLK/512, PCLK/2048, PCLK/8192)
	Independent watchdog timer (IWDTa)	• 14 bits × 1 channel • Counter-input clock: IWDT-dedicated on-chip oscillator Frequency divided by 1, 16, 32, 64, 128, or 256
	Realtime clock (RTCb)	• Clock source: Sub-clock • Time/calendar • Interrupt sources: Alarm interrupt, periodic interrupt, and carry interrupt • Time-capture facility for three values

1.2 List of Products

Table 1.3 to Table 1.7 are a list of products, and Figure 1.1 shows how to read the product part no., memory capacity, and package type.

Table 1.3 List of Products Chip Version A: D Version (Ta = –40 to +85°C)

Group	Part No.	Orderable Part No.	Package	ROM Capacity	RAM Capacity	E2 DataFlash	Operating Frequency (Max.)	Operating Temperature
RX210	R5F52108ADFP	R5F52108ADFP#V0	PLQP0100KB-A	512 Kbytes	64 Kbytes	8 Kbytes	50 MHz	–40 to +85°C
	R5F52108ADFN	R5F52108ADFN#V0	PLQP0080KB-A					
	R5F52108ADFM	R5F52108ADFM#V0	PLQP0064KB-A					
	R5F52108ADLJ	R5F52108ADLJ#U0	PTLG0100JA-A					
	R5F52107ADFP	R5F52107ADFP#V0	PLQP0100KB-A	384 Kbytes				
	R5F52107ADFN	R5F52107ADFN#V0	PLQP0080KB-A					
	R5F52107ADFM	R5F52107ADFM#V0	PLQP0064KB-A					
	R5F52107ADLJ	R5F52107ADLJ#U0	PTLG0100JA-A					
	R5F52106ADFP	R5F52106ADFP#V0	PLQP0100KB-A	256 Kbytes	32 Kbytes			
	R5F52106ADFN	R5F52106ADFN#V0	PLQP0080KB-A					
	R5F52106ADFM	R5F52106ADFM#V0	PLQP0064KB-A					
	R5F52106ADLJ	R5F52106ADLJ#U0	PTLG0100JA-A					
	R5F52105ADFP	R5F52105ADFP#V0	PLQP0100KB-A	128 Kbytes	20 Kbytes			
	R5F52105ADFN	R5F52105ADFN#V0	PLQP0080KB-A					
	R5F52105ADFM	R5F52105ADFM#V0	PLQP0064KB-A					
	R5F52105ADLJ	R5F52105ADLJ#U0	PTLG0100JA-A					

Note: • Orderable part numbers are current as of when this manual was published. Please make sure to refer to the relevant product page on the Renesas website for the latest part numbers.

Table 1.12 List of Pins and Pin Functions (100-Pin LQFP) (3 / 3)

Pin No.	Power Supply, Clock, System Control	I/O Port	External Bus	Timers (MTU, TMR, POE)	Communications (SCIc, SCId, RSPI, RIIC)	Others
80		PD6	D6[A6/D6]	MTIC5V/POE1#		IRQ6
81		PD5	D5[A5/D5]	MTIC5W/POE2#		IRQ5
82		PD4	D4[A4/D4]	POE3#		IRQ4
83		PD3	D3[A3/D3]	POE8#		IRQ3
84		PD2	D2[A2/D2]	MTIOC4D		IRQ2
85		PD1	D1[A1/D1]	MTIOC4B		IRQ1
86		PD0	D0[A0/D0]			IRQ0
87		P47				AN007
88		P46				AN006
89		P45				AN005
90		P44				AN004
91		P43				AN003
92		P42				AN002
93		P41				AN001
94	VREFL0					
95		P40				AN000
96	VREFH0					
97	AVCC0					
98		P07				ADTRG0#
99	AVSS0					
100		P05				DA1

Note: • Pin names to which –DS is appended are for pins that can be used to trigger release from deep software standby mode.

Table 4.1 List of I/O Registers (Address Order) (12 / 29)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles: ICLK ≥ PCLK	Number of Access Cycles: ICLK < PCLK
0008 8122h	TPU1	Timer I/O control register	TIOR	8	8	2, 3 PCLKB	2 ICLK
0008 8124h	TPU1	Timer interrupt enable register	TIER	8	8	2, 3 PCLKB	2 ICLK
0008 8125h	TPU1	Timer status register	TSR	8	8	2, 3 PCLKB	2 ICLK
0008 8126h	TPU1	Timer counter	TCNT	16	16	2, 3 PCLKB	2 ICLK
0008 8128h	TPU1	Timer general register A	TGRA	16	16	2, 3 PCLKB	2 ICLK
0008 812Ah	TPU1	Timer general register B	TGRB	16	16	2, 3 PCLKB	2 ICLK
0008 8130h	TPU2	Timer control register	TCR	8	8	2, 3 PCLKB	2 ICLK
0008 8131h	TPU2	Timer mode register	TMDR	8	8	2, 3 PCLKB	2 ICLK
0008 8132h	TPU2	Timer I/O control register	TIOR	8	8	2, 3 PCLKB	2 ICLK
0008 8134h	TPU2	Timer interrupt enable register	TIER	8	8	2, 3 PCLKB	2 ICLK
0008 8135h	TPU2	Timer status register	TSR	8	8	2, 3 PCLKB	2 ICLK
0008 8136h	TPU2	Timer counter	TCNT	16	16	2, 3 PCLKB	2 ICLK
0008 8138h	TPU2	Timer general register A	TGRA	16	16	2, 3 PCLKB	2 ICLK
0008 813Ah	TPU2	Timer general register B	TGRB	16	16	2, 3 PCLKB	2 ICLK
0008 8140h	TPU3	Timer control register	TCR	8	8	2, 3 PCLKB	2 ICLK
0008 8141h	TPU3	Timer mode register	TMDR	8	8	2, 3 PCLKB	2 ICLK
0008 8142h	TPU3	Timer I/O control register H	TIORH	8	8	2, 3 PCLKB	2 ICLK
0008 8143h	TPU3	Timer I/O control register L	TIORL	8	8	2, 3 PCLKB	2 ICLK
0008 8144h	TPU3	Timer interrupt enable register	TIER	8	8	2, 3 PCLKB	2 ICLK
0008 8145h	TPU3	Timer status register	TSR	8	8	2, 3 PCLKB	2 ICLK
0008 8146h	TPU3	Timer counter	TCNT	16	16	2, 3 PCLKB	2 ICLK
0008 8148h	TPU3	Timer general register A	TGRA	16	16	2, 3 PCLKB	2 ICLK
0008 814Ah	TPU3	Timer general register B	TGRB	16	16	2, 3 PCLKB	2 ICLK
0008 814Ch	TPU3	Timer general register C	TGRC	16	16	2, 3 PCLKB	2 ICLK
0008 814Eh	TPU3	Timer general register D	TGRD	16	16	2, 3 PCLKB	2 ICLK
0008 8150h	TPU4	Timer control register	TCR	8	8	2, 3 PCLKB	2 ICLK
0008 8151h	TPU4	Timer mode register	TMDR	8	8	2, 3 PCLKB	2 ICLK
0008 8152h	TPU4	Timer I/O control register	TIOR	8	8	2, 3 PCLKB	2 ICLK
0008 8154h	TPU4	Timer interrupt enable register	TIER	8	8	2, 3 PCLKB	2 ICLK
0008 8155h	TPU4	Timer status register	TSR	8	8	2, 3 PCLKB	2 ICLK
0008 8156h	TPU4	Timer counter	TCNT	16	16	2, 3 PCLKB	2 ICLK
0008 8158h	TPU4	Timer general register A	TGRA	16	16	2, 3 PCLKB	2 ICLK
0008 815Ah	TPU4	Timer general register B	TGRB	16	16	2, 3 PCLKB	2 ICLK
0008 8160h	TPU5	Timer control register	TCR	8	8	2, 3 PCLKB	2 ICLK
0008 8161h	TPU5	Timer mode register	TMDR	8	8	2, 3 PCLKB	2 ICLK
0008 8162h	TPU5	Timer I/O control register	TIOR	8	8	2, 3 PCLKB	2 ICLK
0008 8164h	TPU5	Timer interrupt enable register	TIER	8	8	2, 3 PCLKB	2 ICLK
0008 8165h	TPU5	Timer status register	TSR	8	8	2, 3 PCLKB	2 ICLK
0008 8166h	TPU5	Timer counter	TCNT	16	16	2, 3 PCLKB	2 ICLK
0008 8168h	TPU5	Timer general register A	TGRA	16	16	2, 3 PCLKB	2 ICLK
0008 816Ah	TPU5	Timer general register B	TGRB	16	16	2, 3 PCLKB	2 ICLK
0008 8200h	TMR0	Timer control register	TCR	8	8	2, 3 PCLKB	2 ICLK
0008 8201h	TMR1	Timer counter control register	TCR	8	8	2, 3 PCLKB	2 ICLK
0008 8202h	TMR0	Timer control/status register	TCSR	8	8	2, 3 PCLKB	2 ICLK
0008 8203h	TMR1	Timer control/status register	TCSR	8	8	2, 3 PCLKB	2 ICLK
0008 8204h	TMR0	Time constant register A	TCORA	8	8	2, 3 PCLKB	2 ICLK
0008 8205h	TMR1	Time constant register A	TCORA	8	8*1	2, 3 PCLKB	2 ICLK
0008 8206h	TMR0	Time constant register B	TCORB	8	8	2, 3 PCLKB	2 ICLK
0008 8207h	TMR1	Time constant register B	TCORB	8	8*1	2, 3 PCLKB	2 ICLK
0008 8208h	TMR0	Timer counter	TCNT	8	8	2, 3 PCLKB	2 ICLK
0008 8209h	TMR1	Timer counter	TCNT	8	8*1	2, 3 PCLKB	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (15 / 29)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles: ICLK ≥ PCLK	Number of Access Cycles: ICLK < PCLK
0008 8648h	MTU4	Timer A/D converter start request cycle set buffer register A	TADCOBRA	16	16	2, 3 PCLKB	2 ICLK
0008 864Ah	MTU4	Timer A/D converter start request cycle set buffer register B	TADCOBRB	16	16	2, 3 PCLKB	2 ICLK
0008 8660h	MTU	Timer waveform control register	TWCR	8	8, 16	2, 3 PCLKB	2 ICLK
0008 8680h	MTU	Timer start register	TSTR	8	8, 16	2, 3 PCLKB	2 ICLK
0008 8681h	MTU	Timer synchronous register	TSYR	8	8, 16	2, 3 PCLKB	2 ICLK
0008 8684h	MTU	Timer read/write enable register	TRWER	8	8, 16	2, 3 PCLKB	2 ICLK
0008 8690h	MTU0	Noise filter control register	NFCR	8	8, 16	2, 3 PCLKB	2 ICLK
0008 8691h	MTU1	Noise filter control register	NFCR	8	8, 16	2, 3 PCLKB	2 ICLK
0008 8692h	MTU2	Noise filter control register	NFCR	8	8, 16	2, 3 PCLKB	2 ICLK
0008 8693h	MTU3	Noise filter control register	NFCR	8	8, 16	2, 3 PCLKB	2 ICLK
0008 8694h	MTU4	Noise filter control register	NFCR	8	8, 16	2, 3 PCLKB	2 ICLK
0008 8695h	MTU5	Noise filter control register	NFCR	8	8, 16	2, 3 PCLKB	2 ICLK
0008 8700h	MTU0	Timer control register	TCR	8	8	2, 3 PCLKB	2 ICLK
0008 8701h	MTU0	Timer mode register	TMDR	8	8	2, 3 PCLKB	2 ICLK
0008 8702h	MTU0	Timer I/O control register H	TIORH	8	8	2, 3 PCLKB	2 ICLK
0008 8703h	MTU0	Timer I/O control register L	TIORL	8	8	2, 3 PCLKB	2 ICLK
0008 8704h	MTU0	Timer interrupt enable register	TIER	8	8	2, 3 PCLKB	2 ICLK
0008 8705h	MTU0	Timer status register	TSR	8	8	2, 3 PCLKB	2 ICLK
0008 8706h	MTU0	Timer counter	TCNT	16	16	2, 3 PCLKB	2 ICLK
0008 8708h	MTU0	Timer general register A	TGRA	16	16	2, 3 PCLKB	2 ICLK
0008 870Ah	MTU0	Timer general register B	TGRB	16	16	2, 3 PCLKB	2 ICLK
0008 870Ch	MTU0	Timer general register C	TGRC	16	16	2, 3 PCLKB	2 ICLK
0008 870Eh	MTU0	Timer general register D	TGRD	16	16	2, 3 PCLKB	2 ICLK
0008 8720h	MTU0	Timer general register E	TGRE	16	16	2, 3 PCLKB	2 ICLK
0008 8722h	MTU0	Timer general register F	TGRF	16	16	2, 3 PCLKB	2 ICLK
0008 8724h	MTU0	Timer interrupt enable register 2	TIER2	8	8	2, 3 PCLKB	2 ICLK
0008 8726h	MTU0	Timer buffer operation transfer mode register	TBTM	8	8	2, 3 PCLKB	2 ICLK
0008 8780h	MTU1	Timer control register	TCR	8	8	2, 3 PCLKB	2 ICLK
0008 8781h	MTU1	Timer mode register	TMDR	8	8	2, 3 PCLKB	2 ICLK
0008 8782h	MTU1	Timer I/O control register	TIOR	8	8	2, 3 PCLKB	2 ICLK
0008 8784h	MTU1	Timer interrupt enable register	TIER	8	8	2, 3 PCLKB	2 ICLK
0008 8785h	MTU1	Timer status register	TSR	8	8	2, 3 PCLKB	2 ICLK
0008 8786h	MTU1	Timer counter	TCNT	16	16	2, 3 PCLKB	2 ICLK
0008 8788h	MTU1	Timer general register A	TGRA	16	16	2, 3 PCLKB	2 ICLK
0008 878Ah	MTU1	Timer general register B	TGRB	16	16	2, 3 PCLKB	2 ICLK
0008 8790h	MTU1	Timer input capture control register	TICCR	8	8	2, 3 PCLKB	2 ICLK
0008 8800h	MTU2	Timer control register	TCR	8	8	2, 3 PCLKB	2 ICLK
0008 8801h	MTU2	Timer mode register	TMDR	8	8	2, 3 PCLKB	2 ICLK
0008 8802h	MTU2	Timer I/O control register	TIOR	8	8	2, 3 PCLKB	2 ICLK
0008 8804h	MTU2	Timer interrupt enable register	TIER	8	8	2, 3 PCLKB	2 ICLK
0008 8805h	MTU2	Timer status register	TSR	8	8	2, 3 PCLKB	2 ICLK
0008 8806h	MTU2	Timer counter	TCNT	16	16	2, 3 PCLKB	2 ICLK
0008 8808h	MTU2	Timer general register A	TGRA	16	16	2, 3 PCLKB	2 ICLK
0008 880Ah	MTU2	Timer general register B	TGRB	16	16	2, 3 PCLKB	2 ICLK
0008 8880h	MTU5	Timer counter U	TCNTU	16	16	2, 3 PCLKB	2 ICLK
0008 8882h	MTU5	Timer general register U	TGRU	16	16	2, 3 PCLKB	2 ICLK
0008 8884h	MTU5	Timer control register U	TCRU	8	8	2, 3 PCLKB	2 ICLK
0008 8886h	MTU5	Timer I/O control register U	TIORU	8	8	2, 3 PCLKB	2 ICLK
0008 8890h	MTU5	Timer counter V	TCNTV	16	16	2, 3 PCLKB	2 ICLK
0008 8892h	MTU5	Timer general register V	TGRV	16	16	2, 3 PCLKB	2 ICLK
0008 8894h	MTU5	Timer control register V	TCRV	8	8	2, 3 PCLKB	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (24 / 29)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles: ICLK ≥ PCLK	Number of Access Cycles: ICLK < PCLK
0008 C04Ch	PORTC	Port input data register	PIDR	8	8	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing	3 ICLK cycles when reading, 2 ICLK cycles when writing
0008 C04Dh	PORTD	Port input data register	PIDR	8	8	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing	3 ICLK cycles when reading, 2 ICLK cycles when writing
0008 C04Eh	PORTE	Port input data register	PIDR	8	8	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing	3 ICLK cycles when reading, 2 ICLK cycles when writing
0008 C04Fh	PORTF	Port input data register	PIDR	8	8	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing	3 ICLK cycles when reading, 2 ICLK cycles when writing
0008 C051h	PORTH	Port input data register	PIDR	8	8	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing	3 ICLK cycles when reading, 2 ICLK cycles when writing
0008 C052h	PORTJ	Port input data register	PIDR	8	8	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing	3 ICLK cycles when reading, 2 ICLK cycles when writing
0008 C053h	PORTK	Port input data register	PIDR	8	8	2, 3 PCLKB	2 ICLK
0008 C054h	PORTL	Port input data register	PIDR	8	8	2, 3 PCLKB	2 ICLK
0008 C060h	PORT0	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK
0008 C061h	PORT1	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK
0008 C062h	PORT2	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK
0008 C063h	PORT3	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK
0008 C064h	PORT4	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK
0008 C065h	PORT5	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK
0008 C066h	PORT6	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK
0008 C067h	PORT7	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK
0008 C068h	PORT8	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK
0008 C069h	PORT9	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK
0008 C06Ah	PORTA	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK
0008 C06Bh	PORTB	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK
0008 C06Ch	PORTC	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK
0008 C06Dh	PORTD	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK
0008 C06Eh	PORTE	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK
0008 C06Fh	PORTF	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK
0008 C071h	PORTH	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK
0008 C072h	PORTJ	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK
0008 C073h	PORTK	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK
0008 C074h	PORTL	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK

5.2 DC Characteristics

Table 5.2 DC Characteristics (1)

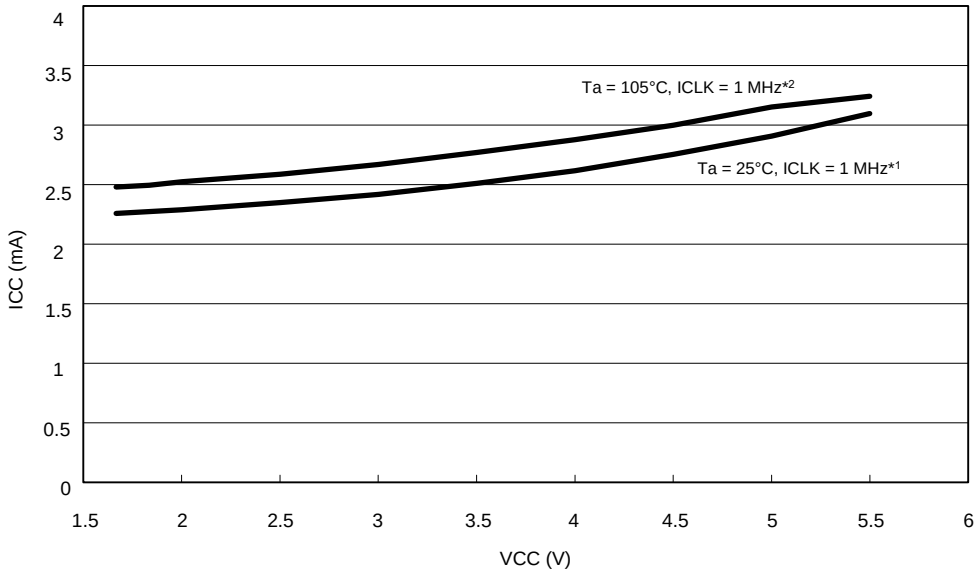
Conditions: VCC = AVCC0 = 2.7 to 5.5 V, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Schmitt trigger input voltage	RIIC input pin (except for SMBus, 5 V tolerant)	V_{IH}	VCC × 0.7	—	5.8	V	
	Ports 12, 13, 16, and 17 (5 V tolerant)		VCC × 0.8	—	5.8		
	Ports 0, 14, 15, 2 to 9, A to L, and RES#		VCC × 0.8	—	VCC + 0.3		
	RIIC input pin (except for SMBus)	V_{IL}	–0.3	—	VCC × 0.3		
	Other than RIIC input pin		–0.3	—	VCC × 0.2		
	RIIC input pin (except for SMBus)	ΔV_T	VCC × 0.05	—	—		
	Other than RIIC input pin		VCC × 0.1	—	—		
Input level voltage (except for Schmitt trigger input pins)	MD pin	V_{IH}	VCC × 0.9	—	VCC + 0.3	V	
	EXTAL, WAIT#		VCC × 0.8	—	VCC + 0.3		
	D0 to D15		VCC × 0.7	—	VCC + 0.3		
	RIIC input pin (SMBus)		2.1	—	VCC + 0.3		
	MD pin	V_{IL}	–0.3	—	VCC × 0.1		
	EXTAL, WAIT#		–0.3	—	VCC × 0.2		
	D0 to D15		–0.3	—	VCC × 0.3		
	RIIC input pin (SMBus)		–0.3	—	0.8		

Table 5.3 DC Characteristics (2)

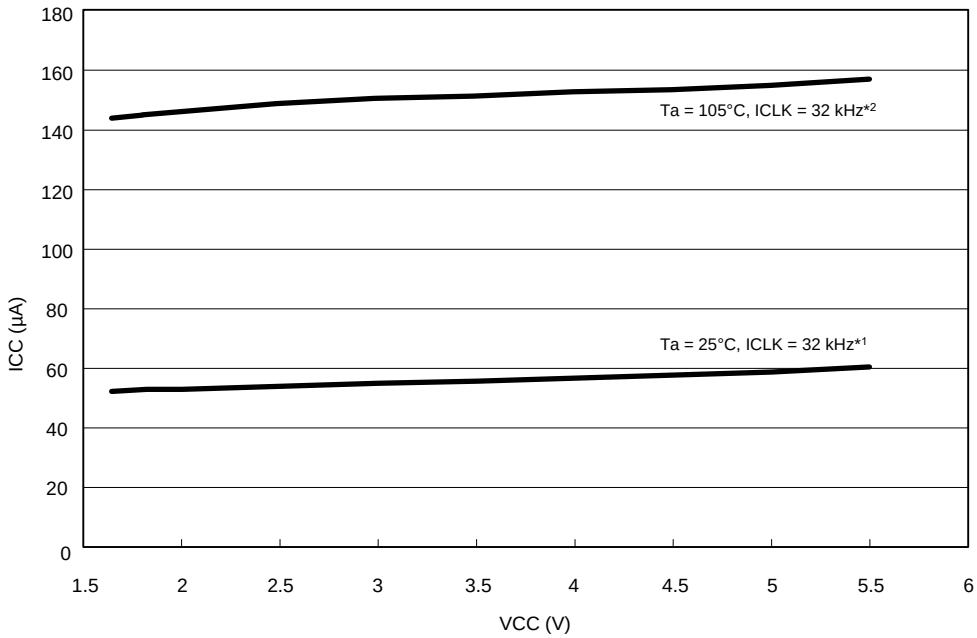
Conditions: VCC = AVCC0 = 1.62 to 2.7 V, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +105°C

Item			Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Schmitt trigger input voltage	Ports 12, 13, 16, and 17 (5 V tolerant)		V_{IH}	VCC × 0.8	—	5.8	V	
	Ports 0, 14, 15, 2 to 9, A to L, and RES#			VCC × 0.8	—	VCC + 0.3		
	All input pins		V_{IL}	–0.3	—	VCC × 0.2		
	Ports 0 to 9, A to L	VCC ≥ 2.2V	ΔV_T	VCC × 0.05	—	—		
		VCC < 2.2V		VCC × 0.01				
	RES#			VCC × 0.1				
Input level voltage (except for Schmitt trigger input pins)	MD pin		V_{IH}	VCC × 0.9	—	VCC + 0.3	V	
	EXTAL, WAIT#			VCC × 0.8	—	VCC + 0.3		
	D0 to D15			VCC × 0.7	—	VCC + 0.3		
	MD pin		V_{IL}	–0.3	—	VCC × 0.1		
	EXTAL, WAIT#			–0.3	—	VCC × 0.2		
	D0 to D15			–0.3	—	VCC × 0.3		



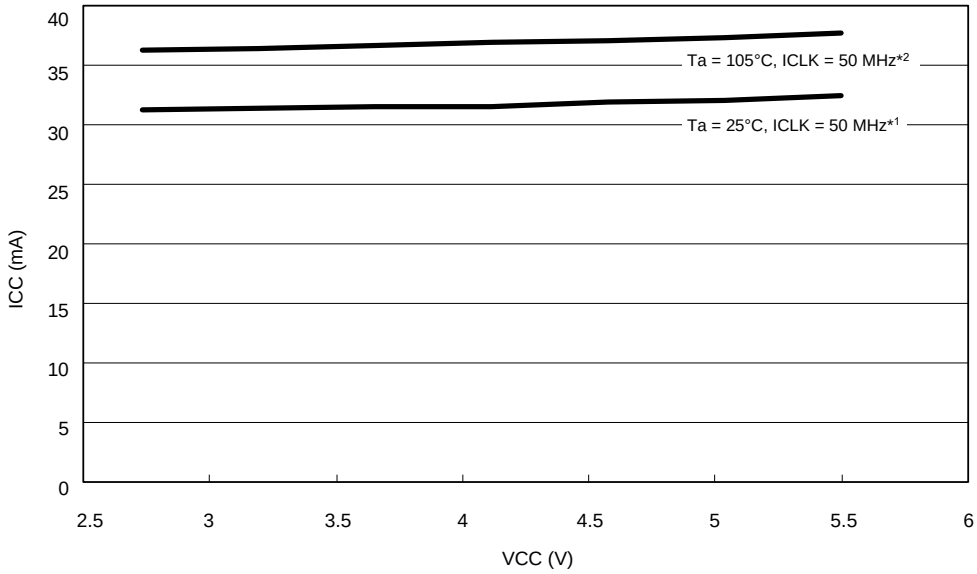
Note 1. All peripheral operation is normal.
Average value of the tested middle samples during product evaluation.
Note 2. All peripheral operation is maximum.
Average value of the tested upper-limit samples during product evaluation.

Figure 5.3 Voltage Dependency in Low-Speed Operating Mode 1 (Reference Data) for Chip Version A



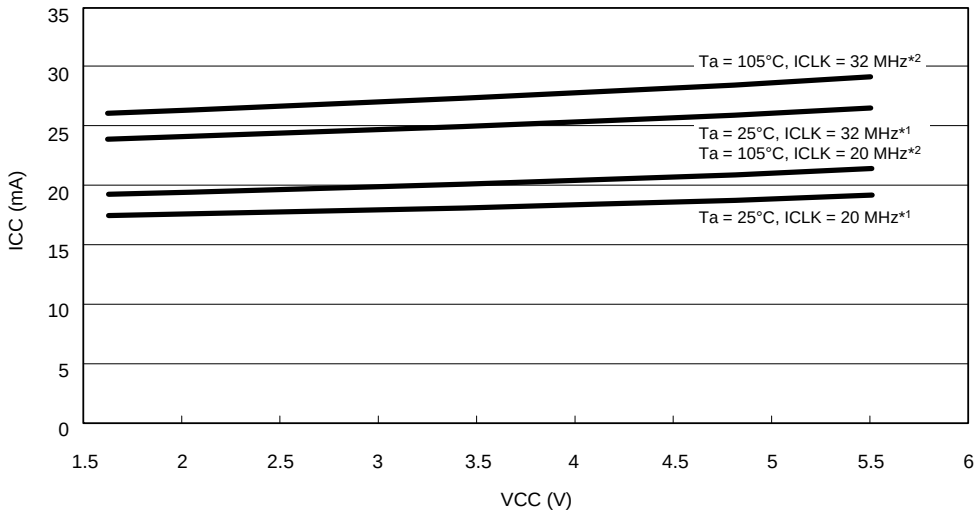
Note 1. All peripheral operation is normal.
Average value of the tested middle samples during product evaluation.
Note 2. All peripheral operation is maximum.
Average value of the tested upper-limit samples during product evaluation.

Figure 5.4 Voltage Dependency in Low-Speed Operating Mode 2 (Reference Data) for Chip Version A



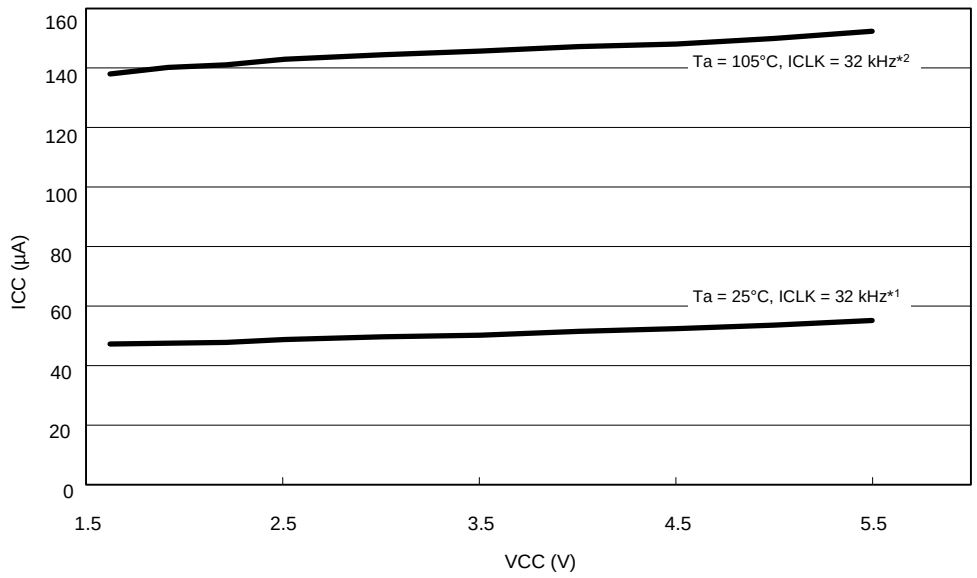
Note 1. All peripheral operation is normal. This does not include BGO operation.
Average value of the tested middle samples during product evaluation.
Note 2. All peripheral operation is maximum. This does not include BGO operation.
Average value of the tested upper-limit samples during product evaluation.

Figure 5.9 Voltage Dependency in High-Speed Operating Mode (Reference Data) for Chip Version C



Note 1. All peripheral operation is normal. This does not include BGO operation.
Average value of the tested middle samples during product evaluation.
Note 2. All peripheral operation is maximum. This does not include BGO operation.
Average value of the tested upper-limit samples during product evaluation.

Figure 5.10 Voltage Dependency in Middle-Speed Operating Modes 1A and 1B (Reference Data) for Chip Version C



Note 1. All peripheral operation is normal.
Average value of the tested middle samples during product evaluation.
Note 2. All peripheral operation is maximum.
Average value of the tested upper-limit samples during product evaluation.

Figure 5.21 Voltage Dependency in Low-Speed Operating Mode 2 (Reference Data) for Chip Version B with 256 Kbytes or Less of Flash Memory and 48 to 100 Pins

[Chip version B with 768 Kbytes/1 Mbyte of flash memory and 100 to 145 pins]

Table 5.15 DC Characteristics (14)

Conditions: VCC = AVCC0 = 2.7 to 5.5 V, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +105°C

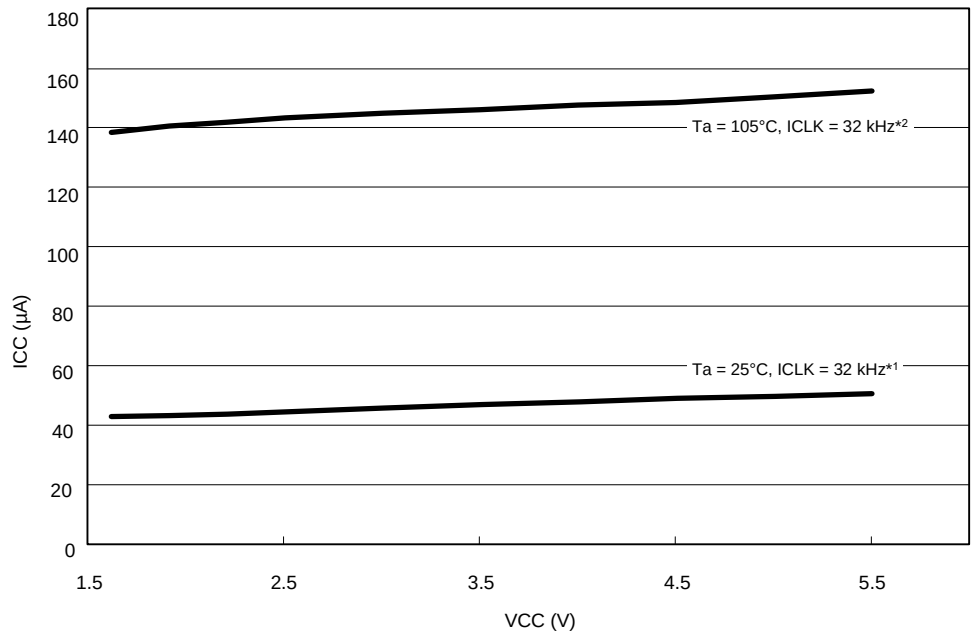
Item					Symbol	Typ.	Max.	Unit	Test Conditions
Supply current*1	High-speed operating mode	Normal operating mode	No peripheral operation*2	ICLK = 50 MHz	I_{CC}	7.8	—	mA	
			All peripheral operation: Normal*3	ICLK = 50 MHz		29.8	—		
			All peripheral operation: Max.*3	ICLK = 50 MHz		—	45		
		Sleep mode	No peripheral operation	ICLK = 50 MHz		4.3	—		
			All peripheral operation: Normal	ICLK = 50 MHz		13.5	—		
		All-module clock stop mode				3.7	—		
		Increase during BGO operation*4				23	—		

Note 1. Supply current values do not include output charge/discharge current from all pins. The values apply when internal pull-up MOSs are in the off state.

Note 2. Clock supply to the peripheral functions is stopped. This does not include BGO operation. The clock source is PLL and the VCO oscillation frequency is 100 MHz. BCLK, FCLK, and PCLK are set to divided by 64.

Note 3. Clocks are supplied to the peripheral functions. This does not include BGO operation. The clock source is PLL and the VCO oscillation frequency is 100 MHz. BCLK, FCLK, and PCLK are ICLK divided by 2.

Note 4. This is the increase if data is programmed to or erasing from the ROM or E2 DataFlash during program execution.



Note 1. All peripheral operation is normal.
Average value of the tested middle samples during product evaluation.
Note 2. All peripheral operation is maximum.
Average value of the tested upper-limit samples during product evaluation.

Figure 5.39 Voltage Dependency in Low-Speed Operating Mode 2 (Reference Data) for Chip Version B with 512 Kbytes or Less of Flash Memory and 144 and 145 Pins

[Chip version B with 512 Kbytes or less of flash memory and 144 and 145 pins]

Table 5.20 DC Characteristics (19)

Conditions: VCC = AVCC0 = 1.62 to 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item				Symbol	Typ.*3	Max.	Unit	Test Conditions
Supply current*1	Software standby mode*2	Flash memory power supplied, HOCO power supplied, POR low power consumption function disabled (SOFTCUT[2:0] bits = 000b)	T_a = 25°C	I_{CC}	10	18	µA	
			T_a = 55°C		13	52		
			T_a = 85°C		20	101		
			T_a = 105°C		34	173		
		Flash memory power supplied, HOCO power not supplied, POR low power consumption function enabled (SOFTCUT[2:0] bits = 110b)	T_a = 25°C		1.8	7.7		
			T_a = 55°C		3.3	30		
			T_a = 85°C		9.2	75		
			T_a = 105°C		20	139		
	Deep software standby mode*2	Flash memory power not supplied, HOCO power not supplied, POR low power consumption function enabled (DEEPCUT1 bit = 1)	T_a = 25°C		0.4	0.8		
			T_a = 55°C		0.5	1.0		
			T_a = 85°C		0.7	2.5		
			T_a = 105°C		1.4	6.3		
	Increments produced by running voltage detection circuits and disabling the POR low power consumption function				1.4	—		
	Increment for RTC operation (low CL)				0.8	—		
	Increment for RTC operation (standard CL)				2.0	—		

Note 1. Supply current values are with all output pins unloaded and all input pull-up MOSs in the off state.
Note 2. The IWDT and LVD are stopped.
Note 3. VCC = 3.3 V.

Table 5.21 DC Characteristics (20)

Conditions: VCC = AVCC0 = 1.62 to 5.5 V, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +105°C

Item	Symbol	Typ.	Max.	Unit	Test Conditions
Permissible total consumption power*1	Pd	—	350	mW	Ta = –40 to 85°C
		—	150		85°C < Ta ≤ 105°C

Note: • Please contact Renesas Electronics sales office for derating of operation under Ta = +85°C to +105°C. Derating is the systematic reduction of load for the sake of improved reliability.
Note 1. Total power dissipated by the entire chip (including output currents)

Table 5.22 DC Characteristics (21)

Conditions: VCC = AVCC0 = 1.62 to 5.5 V, VREFH = 1.8 to AVCC0, VREFH0 = 1.62 to AVCC0,
VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Analog power supply current	During A/D conversion	I_{AVCC0}	—	1.0	3.2	mA	
	Temperature sensor operating, waiting for A/D conversion		—	60	200	µA	
	During D/A conversion (per channel)	I_{VREFH}*1	—	0.25	0.75	mA	
	Waiting for A/D, D/A conversion (all units)*2	—	—	0.2	5.0	µA	
Reference power supply current	During A/D conversion	I_{VREFH0}	—	0.1	0.2	mA	
	Waiting for A/D conversion		—	0.2	0.4	µA	

Note: • The values for A/D conversion apply when the sample and hold circuit is not in use.
Note 1. The reference power supply current is included in the power supply current value for D/A conversion.
Note 2. The value is the total value of I_{AVCC0} and I_{VREFH}.

Table 5.23 DC Characteristics (22)

Conditions: VCC = AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +105°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
RAM standby voltage	V_{RAM}	1.62	—	—	V	

Table 5.24 DC Characteristics (23)

Conditions: VCC = AVCC0 = 0 to 5.5 V, VREFH = VREFH0 = 0 to AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V,
T_a = –40 to +105°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
VCC rising gradient	SrVCC	0.02	—	20	ms/V	At cold start

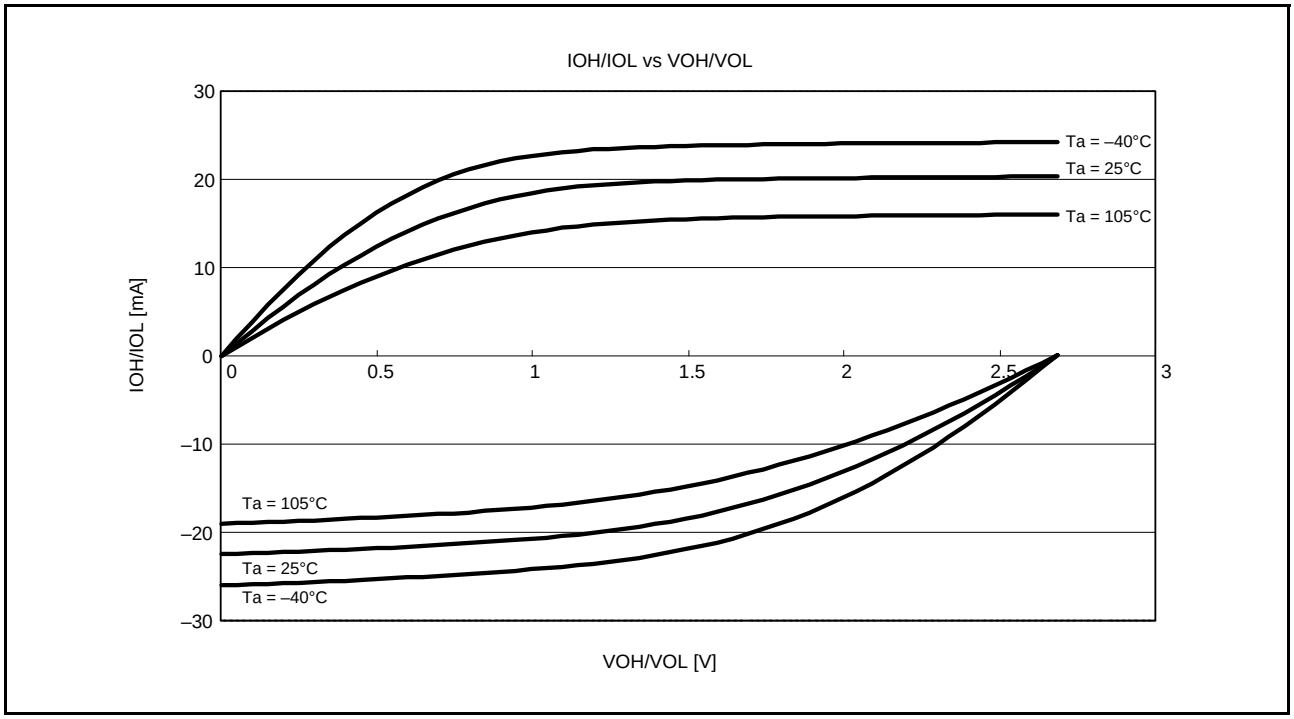


Figure 5.52 VOH/VOL and IOH/IOL Temperature Characteristics at VCC = 2.7 V when High-Drive Output is Selected (Reference Data)

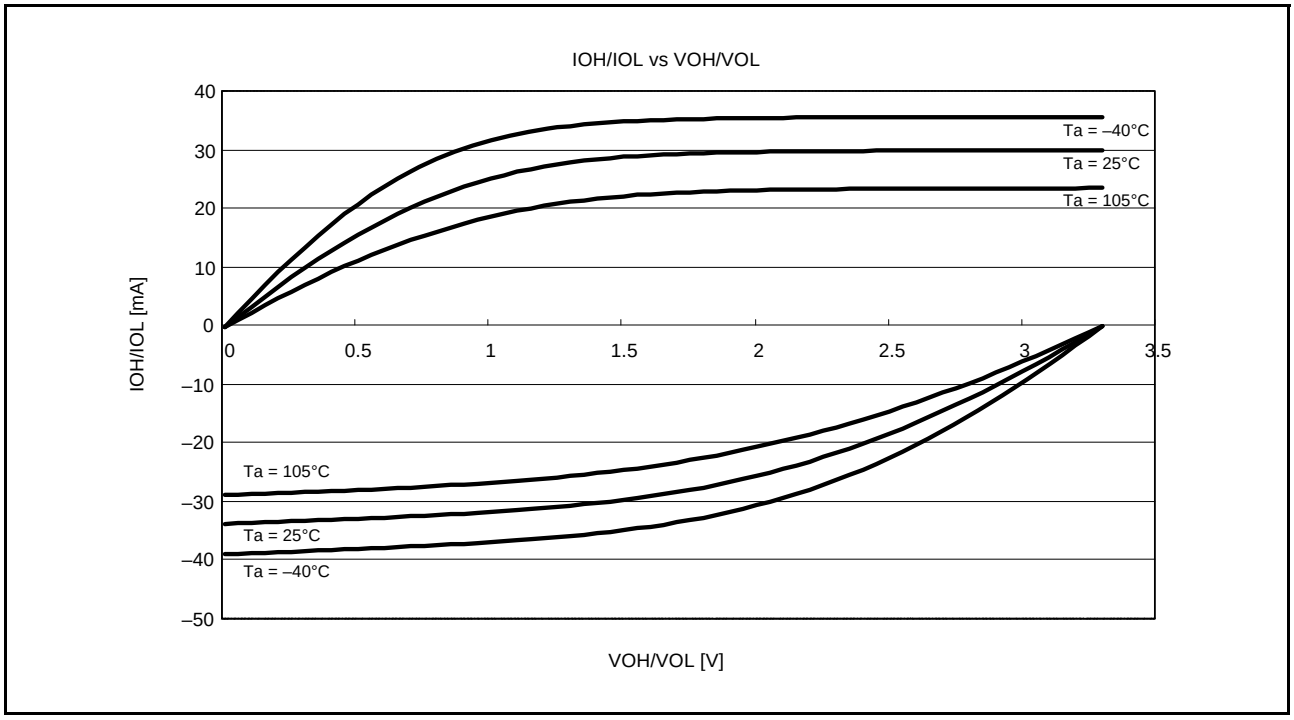


Figure 5.53 VOH/VOL and IOH/IOL Temperature Characteristics at VCC = 3.3 V when High-Drive Output is Selected (Reference Data)

[Chip version B]

Table 5.36 Operation Frequency Value (Middle-Speed Operating Mode 2A)

Conditions: VCC = AVCC0 = 1.62 to 5.5 V, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +105°C

Item		Symbol	VCC			Unit
			1.62 to 1.8 V	1.8 to 2.7 V	2.7 to 5.5 V	
Maximum operating frequency	System clock (ICLK)	f_{max}	8	16	32	MHz
	FlashIF clock (FCLK)*1		8	16	32	
	Peripheral module clock (PCLKB)		8	16	32	
	Peripheral module clock (PCLKD)*2		8	16	32	
	External bus clock (BCLK)		8	16	25	
	BCLK pin output		8	8	12.5	

Note 1. The VCC is 2.7 to 5.5 V and the lower-limit frequency of FCLK is 4 MHz during programming or erasing of the flash memory.
Note 2. The lower-limit frequency of PCLKD is 1 MHz when the A/D converter is in use.

[Chip version B]

Table 5.37 Operation Frequency Value (Middle-Speed Operating Mode 2B)

Conditions: VCC = AVCC0 = 1.62 to 5.5 V, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +105°C

Item		Symbol	VCC			Unit
			1.62 to 1.8 V	1.8 to 2.7 V	2.7 to 5.5 V	
Maximum operating frequency	System clock (ICLK)	f_{max}	8	16	32	MHz
	FlashIF clock (FCLK)*1		8	16	32	
	Peripheral module clock (PCLKB)		8	16	32	
	Peripheral module clock (PCLKD)*2		8	16	32	
	External bus clock (BCLK)		8	16	25	
	BCLK pin output		8	8	12.5	

Note 1. The VCC is 1.62 to 3.6 V and the lower-limit frequency of FCLK is 4 MHz during programming or erasing of the flash memory.
Note 2. The lower-limit frequency of PCLKD is 1 MHz when the A/D converter is in use.

[Chip versions A and C]

Table 5.38 Operation Frequency Value (Low-Speed Operating Mode 1)

Conditions: VCC = AVCC0 = 1.62 to 5.5 V, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +105°C

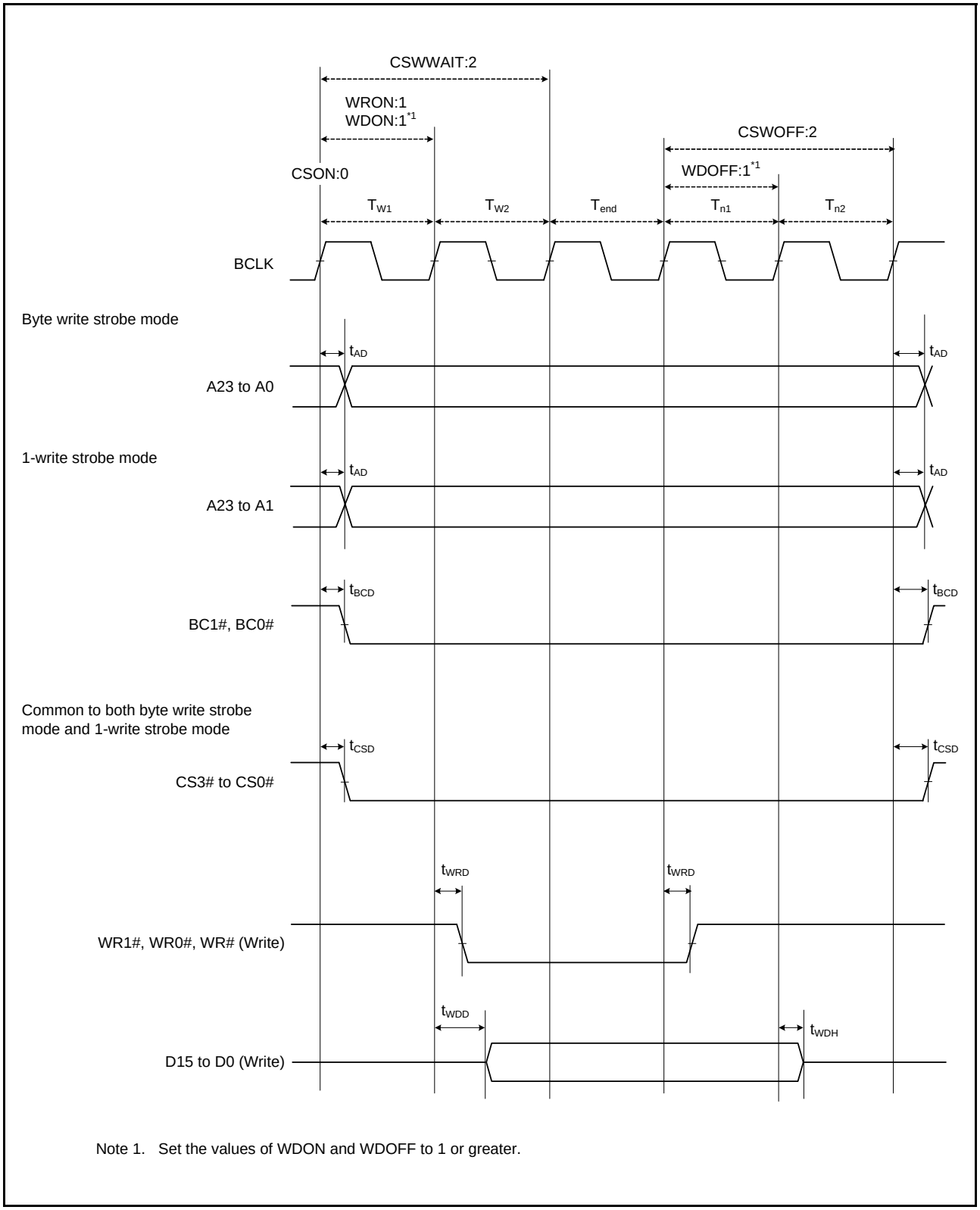
Item		Symbol	VCC			Unit
			1.62 to 1.8 V	1.8 to 2.7 V	2.7 to 5.5 V	
Maximum operating frequency	System clock (ICLK)	f_{max}	1	1	1	MHz
	FlashIF clock (FCLK)*1		1	1	1	
	Peripheral module clock (PCLKB)		1	1	1	
	Peripheral module clock (PCLKD)*2		1	1	1	
	External bus clock (BCLK)		1	1	1	
	BCLK pin output		1	1	1	

Note 1. Programming and erasing the flash memory is impossible.
Note 2. The lower-limit frequency of PCLKD is 1 MHz when the A/D converter is in use.

Table 5.51 Bus Timing (3)

Conditions: VCC = AVCC0 = 1.62 to 1.8 V, VSS = AVSS0 = VREFL = VREFL0 = 0 V,
fBCLK ≤ 12 MHz (BCLK pin output frequency ≤ 6 MHz), T_a = –40 to +105°C, V_{OH} = VCC × 0.5,
V_{OL} = VCC × 0.5, I_{OH} = –0.5 mA, I_{OL} = 0.5 mA, C_L = 30 pF
When normal output is selected by the drive capacity register

Item	Symbol	Min.	Max.	Unit	Test Conditions
Address delay time	t_{AD}	—	125	ns	Figure 5.76 to Figure 5.79
Byte control delay time	t_{BCD}	—	125	ns	
CS# delay time	t_{CSD}	—	125	ns	
RD# delay time	t_{RSD}	—	125	ns	
Read data setup time	t_{RDS}	85	—	ns	
Read data hold time	t_{RDH}	0	—	ns	
WR# delay time	t_{WRD}	—	125	ns	
Write data delay time	t_{WDD}	—	125	ns	
Write data hold time	t_{WDH}	0	—	ns	
WAIT# setup time	t_{WTS}	85	—	ns	Figure 5.80
WAIT# hold time	t_{WTH}	0	—	ns	



Note 1. Set the values of WDON and WDOFF to 1 or greater.

Figure 5.77 External Bus Timing/Normal Write Cycle (Bus Clock Synchronized)

5.9 Oscillation Stop Detection Timing

Table 5.73 Oscillation Stop Detection Circuit Characteristics

Conditions: VCC = AVCC0 = 1.62 to 5.5 V, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +105°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Detection time	t_{dr}	—	—	1	ms	Figure 5.108

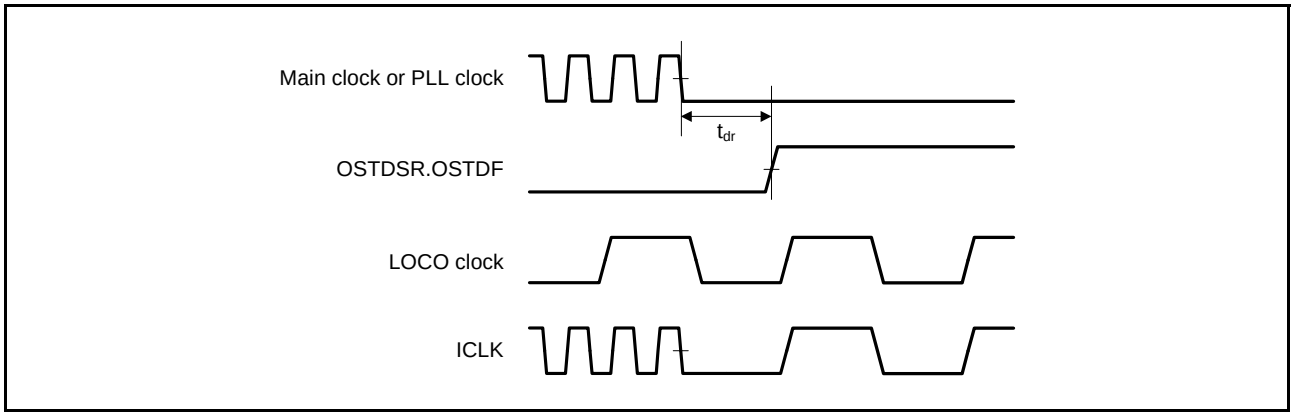


Figure 5.108 Oscillation Stop Detection Timing

[Chip versions A and C]

Table 5.82 E2 DataFlash Characteristics (3)
: high-speed operating mode, middle-speed operating mode 1A

Conditions: VCC = AVCC0 = 2.7 to 5.5 V, VREFH = VREFH0 = AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V
Temperature range for the programming/erasure operation: T_a = –40 to +105°C

Item		Symbol	FCLK = 4 MHz			FCLK = 32 MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Programming time when N_{DPEC} ≤ 100 times	2 bytes	t_{DP2}	—	0.40	4.4	—	0.16	2.0	ms
	8 bytes	t_{DP8}	—	0.45	5.1	—	0.17	2.2	
Programming time when N_{DPEC} > 100 times	2 bytes	t_{DP2}	—	0.62	6.4	—	0.25	3.0	ms
	8 bytes	t_{DP8}	—	0.69	7.5	—	0.26	3.2	
Erasure time when N_{DPEC} ≤ 100 times	128 bytes	t_{DE128}	—	5.6	27.1	—	2.8	8	ms
Erasure time when N_{DPEC} > 100 times	128 bytes	t_{DE128}	—	6.8	45.1	—	3.4	12	ms
Blank check time	2 bytes	t_{DBC2}	—	—	98	—	—	35	µs
	2 Kbytes	t_{DBC2K}	—	—	16	—	—	2.5	ms
Suspend delay time during programming (in programming/erasure priority mode)		t_{DSPD}	—	—	0.9	—	—	0.8	ms
First suspend delay time during programming (in suspend priority mode)		t_{DSPSD1}	—	—	220	—	—	120	µs
Second suspend delay time during programming (in suspend priority mode)		t_{DSPSD2}	—	—	0.9	—	—	0.8	ms
Suspend delay time during erasing (in programming/erasure priority mode)		t_{DSED}	—	—	0.9	—	—	0.8	ms
First suspend delay time during erasing (in suspend priority mode)		t_{DSESD1}	—	—	220	—	—	120	µs
Second suspend delay time during erasing (in suspend priority mode)		t_{DSESD2}	—	—	0.9	—	—	0.8	ms