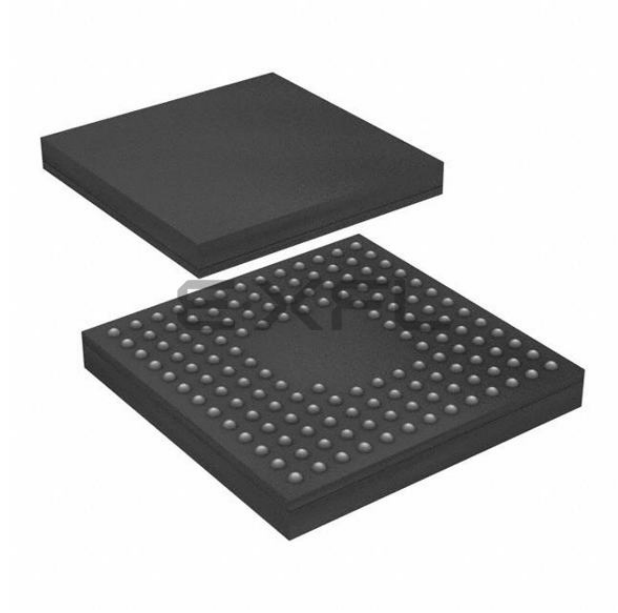
Renesas Electronics America Inc - R5F52106BDLK#U0 Datasheet



Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	EBI/EMI, I²C, SCI, SPI
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	122
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.62V ~ 5.5V
Data Converters	A/D 16x12b; D/A 2x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	145-TFLGA
Supplier Device Package	145-TFLGA (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f52106bdlk-u0

1.Overview

1.1 Outline of Specifications

Table 1.1 lists the specifications in outline, and Table 1.2 gives a comparison of the functions of products in different packages.
Table 1.1 is for products with the greatest number of functions, so numbers of peripheral modules and channels will differ in accord with the package. For details, see Table 1.2, Comparison of Functions for Different Packages.
This product includes chip version A (part no.: R5F5210xAxxx), chip version B (part no.: R5F5210xBxxx), and chip version C (part no: R5F5210xCxxx).
For the specification differences between chip versions A, B, and C, see Table 1, Specification Differences Depending on Chip Versions.

Table 1.1 Outline of Specifications (1 / 5)

Classification	Module/Function	Description
CPU	CPU	• Maximum operating frequency: 50 MHz • 32-bit RX CPU • Minimum instruction execution time: One instruction per state (cycle of the system clock) • Address space: 4-Gbyte linear • Register General purpose: Sixteen 32-bit registers Control: Eight 32-bit registers Accumulator: One 64-bit register • Basic instructions: 73 • DSP instructions: 9 • Addressing modes: 10 • Data arrangement Instructions: Little endian Data: Selectable as little endian or big endian • On-chip 32-bit multiplier: 32 × 32 → 64 bits • On-chip divider: 32 / 32 → 32 bits • Barrel shifter: 32 bits
Memory	ROM	• Capacity: 64 K/96 K/128 K/256 K/384 K/512 K/768 Kbytes/1 Mbyte • 50 MHz, no-wait memory access • On-board programming: 3 types Off-board programming
	RAM	• Capacity: 12 K/16 K/20 K/32 K/64 K/96 Kbytes • 50 MHz, no-wait memory access
	E2 DataFlash	• Capacity: 8 Kbytes • Number of times for programming/erasing: 100,000
MCU operating mode		Single-chip mode, on-chip ROM enabled expansion mode, and on-chip ROM disabled expansion mode (software switching)
Clock	Clock generation circuit	• Main clock oscillator, sub-clock oscillator, low-speed on-chip oscillator, high-speed on-chip oscillator, PLL frequency synthesizer, and IWDT-dedicated on-chip oscillator • Oscillation stop detection • Measuring circuit for accuracy of clock frequency (clock-accuracy check: CAC) • Independent settings for the system clock (ICLK), peripheral module clock (PCLK), external bus clock (BCLK), and FlashIF clock (FCLK) The CPU and system sections such as other bus masters run in synchronization with the system clock (ICLK): 50 MHz (at max.) Peripheral modules run in synchronization with the peripheral module clock (PCLK): 32 MHz (at max.) Devices connected to the external bus run in synchronization with the external bus clock (BCLK): 12.5 MHz (at max.) The flash peripheral circuit runs in synchronization with the FlashIF clock (FCLK): 32 MHz (at max.)
Reset		RES# pin reset, power-on reset, voltage monitoring reset, watchdog timer reset, independent watchdog timer reset, deep software standby reset, and software reset
Voltage detection	Voltage detection circuit (LVDAa)	• When the voltage on VCC falls below the voltage detection level, an internal reset or internal interrupt is generated. Voltage detection circuit 0 is capable of selecting the detection voltage from 4 levels Voltage detection circuit 1 is capable of selecting the detection voltage from 16 levels Voltage detection circuit 2 is capable of selecting the detection voltage from 16 levels

Table 1.1 Outline of Specifications (2 / 5)

Classification	Module/Function	Description
Low power consumption	Low power consumption facilities	• Module stop function • Four low power consumption modes Sleep mode, all-module clock stop mode, software standby mode, and deep software standby mode
	Function for lower operating power consumption	• Operating power control modes [Chip versions A and C] High-speed operating mode, middle-speed operating mode 1A, middle-speed operating mode 1B, low-speed operating mode 1, low-speed operating mode 2 [Chip version B] High-speed operating mode, middle-speed operating mode 1A, middle-speed operating mode 1B, middle-speed operating mode 2A, middle-speed operating mode 2B, low-speed operating mode 1, low-speed operating mode 2
Interrupt	Interrupt controller (ICUb)	• Interrupt vectors: 167 • External interrupts: 9 (NMI, IRQ0 to IRQ7 pins) • Non-maskable interrupts: 6 (the NMI pin, oscillation stop detection interrupt, voltage monitoring 1 interrupt, voltage monitoring 2 interrupt, WDT interrupt, and IWDT interrupt) • 16 levels specifiable for the order of priority
External bus extension		• The external address space can be divided into four areas (CS0 to CS3), each with independent control of access settings. Capacity of each area: 16 Mbytes (CS0 to CS3) A chip-select signal (CS0# to CS3#) can be output for each area. Each area is specifiable as an 8-bit or 16-bit bus space The data arrangement in each area is selectable as little or big endian (only for data). Bus format: Separate bus, multiplex bus • Wait control • Write buffer facility
DMA	DMA controller (DMACA)	• 4 channels • Three transfer modes: Normal transfer, repeat transfer, and block transfer • Activation sources: Software trigger, external interrupts, and interrupt requests from peripheral functions
	Data transfer controller (DTCa)	• Three transfer modes: Normal transfer, repeat transfer, and block transfer • Activation sources: Interrupts • Chain transfer function
I/O ports	General I/O ports	145-pin/144-pin/100-pin/80-pin/69-pin/64-pin/48-pin • I/O: 122/122/84/64/48/48/34 • Input: 1/1/1/1/1/1/1 • Pull-up resistors: 122/122/84/64/48/48/34 • Open-drain outputs: 76/76/54/44/35/35/26 • 5-V tolerance:4/4/4/4/2/2*1/2
Event link controller (ELC)		• Event signals of 59 types can be directly connected to the module • Operations of timer modules are selectable at event input • Capable of event link operation for ports B and E
Multi-function pin controller (MPC)		• Capable of selecting input/output function from multiple pins

1.2 List of Products

Table 1.3 to Table 1.7 are a list of products, and Figure 1.1 shows how to read the product part no., memory capacity, and package type.

Table 1.3 List of Products Chip Version A: D Version (Ta = –40 to +85°C)

Group	Part No.	Orderable Part No.	Package	ROM Capacity	RAM Capacity	E2 DataFlash	Operating Frequency (Max.)	Operating Temperature
RX210	R5F52108ADFP	R5F52108ADFP#V0	PLQP0100KB-A	512 Kbytes	64 Kbytes	8 Kbytes	50 MHz	–40 to +85°C
	R5F52108ADFN	R5F52108ADFN#V0	PLQP0080KB-A					
	R5F52108ADFM	R5F52108ADFM#V0	PLQP0064KB-A					
	R5F52108ADLJ	R5F52108ADLJ#U0	PTLG0100JA-A					
	R5F52107ADFP	R5F52107ADFP#V0	PLQP0100KB-A	384 Kbytes				
	R5F52107ADFN	R5F52107ADFN#V0	PLQP0080KB-A					
	R5F52107ADFM	R5F52107ADFM#V0	PLQP0064KB-A					
	R5F52107ADLJ	R5F52107ADLJ#U0	PTLG0100JA-A					
	R5F52106ADFP	R5F52106ADFP#V0	PLQP0100KB-A	256 Kbytes	32 Kbytes			
	R5F52106ADFN	R5F52106ADFN#V0	PLQP0080KB-A					
	R5F52106ADFM	R5F52106ADFM#V0	PLQP0064KB-A					
	R5F52106ADLJ	R5F52106ADLJ#U0	PTLG0100JA-A					
	R5F52105ADFP	R5F52105ADFP#V0	PLQP0100KB-A	128 Kbytes	20 Kbytes			
	R5F52105ADFN	R5F52105ADFN#V0	PLQP0080KB-A					
	R5F52105ADFM	R5F52105ADFM#V0	PLQP0064KB-A					
	R5F52105ADLJ	R5F52105ADLJ#U0	PTLG0100JA-A					

Note: • Orderable part numbers are current as of when this manual was published. Please make sure to refer to the relevant product page on the Renesas website for the latest part numbers.

Table 1.10 List of Pins and Pin Functions (144-Pin LQFP) (3 / 4)

Pin No.	Power Supply, Clock, System Control	I/O Port	External Bus	Timers (MTU, TMR, POE)	Communications (SCIc, SCId, RSPI, RIIC)	Others
81		PB4	A12	TIOCA4	CTS9#/RTS9#/SS9#	
82		PB3	A11	MTIOC0A/MTIOC4A/ TMO0/POE3#/ TIOCD3/TCLKD	SCK4/SCK6	
83		PB2	A10	TIOCC3/TCLKC	CTS4#/RTS4#/SS4#/ CTS6#/RTS6#/SS6#	
84		PB1	A9	MTIOC0C/MTIOC4C/ TMCI0/TIOCB3	TXD4/SMOSI4/SSDA4/ TXD6/SMOSI6/SSDA6	IRQ4-DS
85		P72				
86		P71				
87		PB0	A8	MTIC5W/TIOCA3	RXD4/SMISO4/SSCL4/ RXD6/SMISO6/SSCL6/ RSPCKA	
88		PA7	A7	TIOCB2	MISOA	
89		PA6	A6	MTIC5V/MTCLKB/ TMCI3/POE2#/TIOCA2	CTS5#/RTS5#/SS5#/ MOSIA/	
90		PA5	A5	TIOCB1	RSPCKA	
91	VCC					
92		PA4	A4	MTIC5U/MTCLKA/ TMRI0/TIOCA1	TXD5/SMOSI5/SSDA5/ SSLA0	IRQ5-DS/CVREFB1
93	VSS					
94		PA3	A3	MTIOC0D/MTCLKD/ TIOCD0/TCLKB	RXD5/SMISO5/SSCL5	IRQ6-DS/CMPB1
95		PA2	A2		RXD5/SMISO5/SSCL5/ SSLA3	
96		PA1	A1	MTIOC0B/MTCLKC/ TIOCB0	SCK5/SSLA2	CVREFA
97		PA0	A0/BC0#	MTIOC4A/TIOCA0	SSLA1	CACREF
98		P67				
99		P66				
100		P65				
101		PE7	D15[A15/D15]			IRQ7/AN015
102		PE6	D14[A14/D14]		CTS4#/RTS4#/SS4#	IRQ6/AN014
103		PK5			TXD4/SMOSI4/SSDA4	
104		P70			SCK4	
105		PK4			RXD4/SMISO4/SSCL4	
106		PE5	D13[A13/D13]	MTIOC4C/MTIOC2B		IRQ5/AN013
107		PE4	D12[A12/D12]	MTIOC4D/MTIOC1A		AN012/CMPA2
108		PE3	D11[A11/D11]	MTIOC4B/POE8#	CTS12#/RTS12#/SS12#	AN011/CMPA1
109		PE2	D10[A10/D10]	MTIOC4A	RXD12/RXDX12/ SMISO12/SSCL12	IRQ7-DS/AN010/ CVREFB0
110		PE1	D9[A9/D9]	MTIOC4C	TXD12/TXDX12/SIOX12/ SMOSI12/SSDA12	AN009/CMPB0
111		PE0	D8[A8/D8]		SCK12	AN008
112		P64				
113		P63				
114		P62				
115		P61			CTS9#/RTS9#/SS9#	
116		PK3			RXD9/SMISO9/SSCL9	
117		P60			SCK9	
118		PK2			TXD9/SMOSI9/SSDA9	
119		PD7	D7[A7/D7]	MTIC5U/POE0#		IRQ7
120		PD6	D6[A6/D6]	MTIC5V/POE1#		IRQ6
121		PD5	D5[A5/D5]	MTIC5W/POE2#		IRQ5

Table 1.10 List of Pins and Pin Functions (144-Pin LQFP) (4 / 4)

Pin No.	Power Supply, Clock, System Control	I/O Port	External Bus	Timers (MTU, TMR, POE)	Communications (SCIc, SCId, RSPI, RIIC)	Others
122		PD4	D4[A4/D4]	POE3#		IRQ4
123		PD3	D3[A3/D3]	POE8#		IRQ3
124		PD2	D2[A2/D2]	MTIOC4D		IRQ2
125		PD1	D1[A1/D1]	MTIOC4B		IRQ1
126		PD0	D0[A0/D0]			IRQ0
127		P93			CTS7#/RTS7#/SS7#	
128		P92			RXD7/SMISO7/SSCL7	
129		P91			SCK7	
130	VSS					
131		P90			TXD7/SMOSI7/SSDA7	
132	VCC					
133		P47				AN007
134		P46				AN006
135		P45				AN005
136		P44				AN004
137		P43				AN003
138		P42				AN002
139		P41				AN001
140	VREFL0					
141		P40				AN000
142	VREFH0					
143	AVCC0					
144		P07				ADTRG0#

Note: • Pin names to which –DS is appended are for pins that can be used to trigger release from deep software standby mode.
Note: • Leave the NC pin open.

Table 1.15 List of Pins and Pin Functions (64-Pin TFLGA) (1 / 2)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (MTU, TMR, POE)	Communication (SCIc, SCId, RSPI, RIIC)	Others
A1		P05			DA1
A2	AVCC0				
A3	VREFH0				
A4	VREFL0				
A5	VREFH				
A6	VREFL				
A7		PE2	MTIOC4A	RXD12/RXDX12/SMISO12/ SSCL12	IRQ7-DS/AN010/ CVREFB0
A8		PE3	MTIOC4B/POE8#	CTS12#/RTS12#/SS12#	AN011/CMPA1
B1	VCL				
B2	AVSS0				
B3		P40			AN000
B4		P42			AN002
B5		P44			AN004
B6		P46			AN006
B7		PE1	MTIOC4C	TXD12/TXDX12/SIOX12/ SMOSI12/SSDA12	AN009/CMPB0
B8		PE4	MTIOC4D/MTIOC1A		AN012/CMPA2
C1	XCIN				
C2	MD				FINED
C3		P03			DA0
C4		P41			AN001
C5		P43			AN003
C6		PE0		SCK12	AN008
C7		PE5	MTIOC4C/MTIOC2B		IRQ5/AN013
C8		PA0	MTIOC4A	SSLA1	CACREF
D1	XCOUT				
D2	RES#				
D3		P27	MTIOC2B/TMCI3	SCK1	
D4		P14	MTIOC3A/MTCLKA/TMRI2	CTS1#/RTS1#/SS1#	IRQ4
D5		PA6	MTIC5V/MTCLKB/TMCI3/ POE2#	CTS5#/RTS5#/SS5#/MOSIA	
D6		PA4	MTIC5U/MTCLKA/TMRI0	TXD5/SMOSI5/SSDA5/SSLA0	IRQ5-DS/CVREFB1
D7		PA1	MTIOC0B/MTCLKC	SCK5/SSLA2	CVREFA
D8		PA3	MTIOC0D/MTCLKD	RXD5/SMISO5/SSCL5	IRQ6-DS/CMPB1
E1	VSS				
E2		P32	MTIOC0C/TMO3	TXD6/SMOSI6/SSDA6	IRQ2-DS/RTCOUT/ RTCIC2
E3		P30	MTIOC4B/TMRI3/POE8#	RXD1/SMISO1/SSCL1	IRQ0-DS/RTCIC0
E4		P16	MTIOC3C/MTIOC3D/TMO2	TXD1/SMOSI1/SSDA1/MOSIA/ SCL-DS	IRQ6/RTCOUT/ ADTRG0#
E5		PC4	MTIOC3D/MTCLKC/TMCI1/ POE0#	SCK5/CTS8#/RTS8#/SS8#/ SSLA0	
E6	VCC				
E7	VSS				
E8		PB0	MTIC5W	RXD6/SMISO6/SSCL6/RSPCKA	
F1	VCC				
F2		P35			NMI
F3		P31	MTIOC4D/TMCI2	CTS1#/RTS1#/SS1#	IRQ1-DS/RTCIC1
F4		PC5	MTIOC3B/MTCLKD/TMRI2	SCK8/RSPCKA	

Table 4.1 List of I/O Registers (Address Order) (3 / 29)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles ICLK ≥ PCLK	Number of Access Cycles ICLK < PCLK
0008 3032h	BSC	CS3 mode register	CS3MOD	16	16	1, 2 BCLK	
0008 3034h	BSC	CS3 wait control register 1	CS3WCR1	32	32	1, 2 BCLK	
0008 3038h	BSC	CS3 wait control register 2	CS3WCR2	32	32	1, 2 BCLK	
0008 3802h	BSC	CS0 control register	CS0CR	16	16	1, 2 BCLK	
0008 380Ah	BSC	CS0 recovery cycle register	CS0REC	16	16	1, 2 BCLK	
0008 3812h	BSC	CS1 control register	CS1CR	16	16	1, 2 BCLK	
0008 381Ah	BSC	CS1 recovery cycle register	CS1REC	16	16	1, 2 BCLK	
0008 3822h	BSC	CS2 control register	CS2CR	16	16	1, 2 BCLK	
0008 382Ah	BSC	CS2 recovery cycle register	CS2REC	16	16	1, 2 BCLK	
0008 3832h	BSC	CS3 control register	CS3CR	16	16	1, 2 BCLK	
0008 383Ah	BSC	CS3 recovery cycle register	CS3REC	16	16	1, 2 BCLK	
0008 3880h	BSC	CS recovery cycle insertion enable register	CSRECEN	16	16	1, 2 BCLK	
0008 7010h	ICU	Interrupt request register 016	IR016	8	8	2 ICLK	
0008 7015h	ICU	Interrupt request register 021	IR021	8	8	2 ICLK	
0008 7017h	ICU	Interrupt request register 023	IR023	8	8	2 ICLK	
0008 701Bh	ICU	Interrupt request register 027	IR027	8	8	2 ICLK	
0008 701Ch	ICU	Interrupt request register 028	IR028	8	8	2 ICLK	
0008 701Dh	ICU	Interrupt request register 029	IR029	8	8	2 ICLK	
0008 701Eh	ICU	Interrupt request register 030	IR030	8	8	2 ICLK	
0008 701Fh	ICU	Interrupt request register 031	IR031	8	8	2 ICLK	
0008 7020h	ICU	Interrupt request register 032	IR032	8	8	2 ICLK	
0008 7021h	ICU	Interrupt request register 033	IR033	8	8	2 ICLK	
0008 7022h	ICU	Interrupt request register 034	IR034	8	8	2 ICLK	
0008 702Ch	ICU	Interrupt request register 044	IR044	8	8	2 ICLK	
0008 702Dh	ICU	Interrupt request register 045	IR045	8	8	2 ICLK	
0008 702Eh	ICU	Interrupt request register 046	IR046	8	8	2 ICLK	
0008 702Fh	ICU	Interrupt request register 047	IR047	8	8	2 ICLK	
0008 7039h	ICU	Interrupt request register 057	IR057	8	8	2 ICLK	
0008 703Ah	ICU	Interrupt request register 058	IR058	8	8	2 ICLK	
0008 703Bh	ICU	Interrupt request register 059	IR059	8	8	2 ICLK	
0008 703Fh	ICU	Interrupt request register 063	IR063	8	8	2 ICLK	
0008 7040h	ICU	Interrupt request register 064	IR064	8	8	2 ICLK	
0008 7041h	ICU	Interrupt request register 065	IR065	8	8	2 ICLK	
0008 7042h	ICU	Interrupt request register 066	IR066	8	8	2 ICLK	
0008 7043h	ICU	Interrupt request register 067	IR067	8	8	2 ICLK	
0008 7044h	ICU	Interrupt request register 068	IR068	8	8	2 ICLK	
0008 7045h	ICU	Interrupt request register 069	IR069	8	8	2 ICLK	
0008 7046h	ICU	Interrupt request register 070	IR070	8	8	2 ICLK	
0008 7047h	ICU	Interrupt request register 071	IR071	8	8	2 ICLK	
0008 7058h	ICU	Interrupt request register 088	IR088	8	8	2 ICLK	
0008 7059h	ICU	Interrupt request register 089	IR089	8	8	2 ICLK	
0008 705Ch	ICU	Interrupt request register 092	IR092	8	8	2 ICLK	
0008 705Dh	ICU	Interrupt request register 093	IR093	8	8	2 ICLK	
0008 7066h	ICU	Interrupt request register 102	IR102	8	8	2 ICLK	
0008 7067h	ICU	Interrupt request register 103	IR103	8	8	2 ICLK	
0008 706Ah	ICU	Interrupt request register 106	IR106	8	8	2 ICLK	
0008 706Bh	ICU	Interrupt request register 107	IR107	8	8	2 ICLK	
0008 7072h	ICU	Interrupt request register 114	IR114	8	8	2 ICLK	
0008 7073h	ICU	Interrupt request register 115	IR115	8	8	2 ICLK	
0008 7074h	ICU	Interrupt request register 116	IR116	8	8	2 ICLK	
0008 7075h	ICU	Interrupt request register 117	IR117	8	8	2 ICLK	

Table 4.1 List of I/O Registers (Address Order) (8 / 29)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles	
						ICLK ≥ PCLK	ICLK < PCLK
0008 71D0h	ICU	DTC activation enable register 208	DTCER208	8	8	2 ICLK	
0008 71D3h	ICU	DTC activation enable register 211	DTCER211	8	8	2 ICLK	
0008 71D4h	ICU	DTC activation enable register 212	DTCER212	8	8	2 ICLK	
0008 71D7h	ICU	DTC activation enable register 215	DTCER215	8	8	2 ICLK	
0008 71D8h	ICU	DTC activation enable register 216	DTCER216	8	8	2 ICLK	
0008 71DBh	ICU	DTC activation enable register 219	DTCER219	8	8	2 ICLK	
0008 71DCh	ICU	DTC activation enable register 220	DTCER220	8	8	2 ICLK	
0008 71DFh	ICU	DTC activation enable register 223	DTCER223	8	8	2 ICLK	
0008 71E0h	ICU	DTC activation enable register 224	DTCER224	8	8	2 ICLK	
0008 71E3h	ICU	DTC activation enable register 227	DTCER227	8	8	2 ICLK	
0008 71E4h	ICU	DTC activation enable register 228	DTCER228	8	8	2 ICLK	
0008 71E7h	ICU	DTC activation enable register 231	DTCER231	8	8	2 ICLK	
0008 71E8h	ICU	DTC activation enable register 232	DTCER232	8	8	2 ICLK	
0008 71EBh	ICU	DTC activation enable register 235	DTCER235	8	8	2 ICLK	
0008 71ECh	ICU	DTC activation enable register 236	DTCER236	8	8	2 ICLK	
0008 71EFh	ICU	DTC activation enable register 239	DTCER239	8	8	2 ICLK	
0008 71F0h	ICU	DTC activation enable register 240	DTCER240	8	8	2 ICLK	
0008 71F7h	ICU	DTC activation enable register 247	DTCER247	8	8	2 ICLK	
0008 71F8h	ICU	DTC activation enable register 248	DTCER248	8	8	2 ICLK	
0008 71FBh	ICU	DTC activation enable register 251	DTCER251	8	8	2 ICLK	
0008 71FCh	ICU	DTC activation enable register 252	DTCER252	8	8	2 ICLK	
0008 7202h	ICU	Interrupt request enable register 02	IER02	8	8	2 ICLK	
0008 7203h	ICU	Interrupt request enable register 03	IER03	8	8	2 ICLK	
0008 7204h	ICU	Interrupt request enable register 04	IER04	8	8	2 ICLK	
0008 7205h	ICU	Interrupt request enable register 05	IER05	8	8	2 ICLK	
0008 7207h	ICU	Interrupt request enable register 07	IER07	8	8	2 ICLK	
0008 7208h	ICU	Interrupt request enable register 08	IER08	8	8	2 ICLK	
0008 720Bh	ICU	Interrupt request enable register 0B	IER0B	8	8	2 ICLK	
0008 720Ch	ICU	Interrupt request enable register 0C	IER0C	8	8	2 ICLK	
0008 720Dh	ICU	Interrupt request enable register 0D	IER0D	8	8	2 ICLK	
0008 720Eh	ICU	Interrupt request enable register 0E	IER0E	8	8	2 ICLK	
0008 720Fh	ICU	Interrupt request enable register 0F	IER0F	8	8	2 ICLK	
0008 7210h	ICU	Interrupt request enable register 10	IER10	8	8	2 ICLK	
0008 7211h	ICU	Interrupt request enable register 11	IER11	8	8	2 ICLK	
0008 7212h	ICU	Interrupt request enable register 12	IER12	8	8	2 ICLK	
0008 7213h	ICU	Interrupt request enable register 13	IER13	8	8	2 ICLK	
0008 7214h	ICU	Interrupt request enable register 14	IER14	8	8	2 ICLK	
0008 7215h	ICU	Interrupt request enable register 15	IER15	8	8	2 ICLK	
0008 7216h	ICU	Interrupt request enable register 16	IER16	8	8	2 ICLK	
0008 7217h	ICU	Interrupt request enable register 17	IER17	8	8	2 ICLK	
0008 7218h	ICU	Interrupt request enable register 18	IER18	8	8	2 ICLK	
0008 7219h	ICU	Interrupt request enable register 19	IER19	8	8	2 ICLK	
0008 721Ah	ICU	Interrupt request enable register 1A	IER1A	8	8	2 ICLK	
0008 721Bh	ICU	Interrupt request enable register 1B	IER1B	8	8	2 ICLK	
0008 721Ch	ICU	Interrupt request enable register 1C	IER1C	8	8	2 ICLK	
0008 721Dh	ICU	Interrupt request enable register 1D	IER1D	8	8	2 ICLK	
0008 721Eh	ICU	Interrupt request enable register 1E	IER1E	8	8	2 ICLK	
0008 721Fh	ICU	Interrupt request enable register 1F	IER1F	8	8	2 ICLK	
0008 72E0h	ICU	Software interrupt activation register	SWINTR	8	8	2 ICLK	
0008 72F0h	ICU	Fast interrupt set register	FIR	16	16	2 ICLK	
0008 7300h	ICU	Interrupt source priority register 000	IPR000	8	8	2 ICLK	

Table 4.1 List of I/O Registers (Address Order) (17 / 29)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles: ICLK ≥ PCLK	Number of Access Cycles: ICLK < PCLK
0008 9076h	S12AD	A/D sampling state register 4	ADSSTR4	8	8	2, 3 PCLKB	2 ICLK
0008 9077h	S12AD	A/D sampling state register 5	ADSSTR5	8	8	2, 3 PCLKB	2 ICLK
0008 9078h	S12AD	A/D sampling state register 6	ADSSTR6	8	8	2, 3 PCLKB	2 ICLK
0008 9079h	S12AD	A/D sampling state register 7	ADSSTR7	8	8	2, 3 PCLKB	2 ICLK
0008 907Ah	S12AD	A/D disconnecting detection control register	ADDISCR	8	8	2, 3 PCLKB	2 ICLK
0008 A000h	SCI0	Serial mode register	SMR	8	8	2, 3 PCLKB	2 ICLK
0008 A001h	SCI0	Bit rate register	BRR	8	8	2, 3 PCLKB	2 ICLK
0008 A002h	SCI0	Serial control register	SCR	8	8	2, 3 PCLKB	2 ICLK
0008 A003h	SCI0	Transmit data register	TDR	8	8	2, 3 PCLKB	2 ICLK
0008 A004h	SCI0	Serial status register	SSR	8	8	2, 3 PCLKB	2 ICLK
0008 A005h	SCI0	Receive data register	RDR	8	8	2, 3 PCLKB	2 ICLK
0008 A006h	SCI0	Smart card mode register	SCMR	8	8	2, 3 PCLKB	2 ICLK
0008 A007h	SCI0	Serial extended mode register	SEMR	8	8	2, 3 PCLKB	2 ICLK
0008 A008h	SCI0	Noise filter setting register	SNFR	8	8	2, 3 PCLKB	2 ICLK
0008 A009h	SCI0	I^2C mode register 1	SIMR1	8	8	2, 3 PCLKB	2 ICLK
0008 A00Ah	SCI0	I^2C mode register 2	SIMR2	8	8	2, 3 PCLKB	2 ICLK
0008 A00Bh	SCI0	I^2C mode register 3	SIMR3	8	8	2, 3 PCLKB	2 ICLK
0008 A00Ch	SCI0	I^2C status register	SISR	8	8	2, 3 PCLKB	2 ICLK
0008 A00Dh	SCI0	SPI mode register	SPMR	8	8	2, 3 PCLKB	2 ICLK
0008 A020h	SCI1	Serial mode register	SMR	8	8	2, 3 PCLKB	2 ICLK
0008 A021h	SCI1	Bit rate register	BRR	8	8	2, 3 PCLKB	2 ICLK
0008 A022h	SCI1	Serial control register	SCR	8	8	2, 3 PCLKB	2 ICLK
0008 A023h	SCI1	Transmit data register	TDR	8	8	2, 3 PCLKB	2 ICLK
0008 A024h	SCI1	Serial status register	SSR	8	8	2, 3 PCLKB	2 ICLK
0008 A025h	SCI1	Receive data register	RDR	8	8	2, 3 PCLKB	2 ICLK
0008 A026h	SCI1	Smart card mode register	SCMR	8	8	2, 3 PCLKB	2 ICLK
0008 A027h	SCI1	Serial extended mode register	SEMR	8	8	2, 3 PCLKB	2 ICLK
0008 A028h	SCI1	Noise filter setting register	SNFR	8	8	2, 3 PCLKB	2 ICLK
0008 A029h	SCI1	I^2C mode register 1	SIMR1	8	8	2, 3 PCLKB	2 ICLK
0008 A02Ah	SCI1	I^2C mode register 2	SIMR2	8	8	2, 3 PCLKB	2 ICLK
0008 A02Bh	SCI1	I^2C mode register 3	SIMR3	8	8	2, 3 PCLKB	2 ICLK
0008 A02Ch	SCI1	I^2C status register	SISR	8	8	2, 3 PCLKB	2 ICLK
0008 A02Dh	SCI1	SPI mode register	SPMR	8	8	2, 3 PCLKB	2 ICLK
0008 A040h	SCI2	Serial mode register	SMR	8	8	2, 3 PCLKB	2 ICLK
0008 A041h	SCI2	Bit rate register	BRR	8	8	2, 3 PCLKB	2 ICLK
0008 A042h	SCI2	Serial control register	SCR	8	8	2, 3 PCLKB	2 ICLK
0008 A043h	SCI2	Transmit data register	TDR	8	8	2, 3 PCLKB	2 ICLK
0008 A044h	SCI2	Serial status register	SSR	8	8	2, 3 PCLKB	2 ICLK
0008 A045h	SCI2	Receive data register	RDR	8	8	2, 3 PCLKB	2 ICLK
0008 A046h	SCI2	Smart card mode register	SCMR	8	8	2, 3 PCLKB	2 ICLK
0008 A047h	SCI2	Serial extended mode register	SEMR	8	8	2, 3 PCLKB	2 ICLK
0008 A048h	SCI2	Noise filter setting register	SNFR	8	8	2, 3 PCLKB	2 ICLK
0008 A049h	SCI2	I^2C mode register 1	SIMR1	8	8	2, 3 PCLKB	2 ICLK
0008 A04Ah	SCI2	I^2C mode register 2	SIMR2	8	8	2, 3 PCLKB	2 ICLK
0008 A04Bh	SCI2	I^2C mode register 3	SIMR3	8	8	2, 3 PCLKB	2 ICLK
0008 A04Ch	SCI2	I^2C status register	SISR	8	8	2, 3 PCLKB	2 ICLK
0008 A04Dh	SCI2	SPI mode register	SPMR	8	8	2, 3 PCLKB	2 ICLK
0008 A060h	SCI3	Serial mode register	SMR	8	8	2, 3 PCLKB	2 ICLK
0008 A061h	SCI3	Bit rate register	BRR	8	8	2, 3 PCLKB	2 ICLK
0008 A062h	SCI3	Serial control register	SCR	8	8	2, 3 PCLKB	2 ICLK
0008 A063h	SCI3	Transmit data register	TDR	8	8	2, 3 PCLKB	2 ICLK

Table 5.4 DC Characteristics (3)

Conditions: VCC = AVCC0 = 1.62 to 5.5 V, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Input leakage current	RES#, MD pin, P35/NMI	$\lvert I_{in} \rvert$	—	—	1.0	µA	V_{in} = 0 V, VCC
Three-state leakage current (off-state)	Port 4	$\lvert I_{TSI} \rvert$	—	—	1.0	µA	V_{in} = 0 V, VCC
	Other pins except for ports for 5 V tolerant and port 4		—	—	0.2		
	Ports for 5 V tolerant		—	—	1.0		V_{in} = 0 V, 5.8 V
Input capacitance	All input pins (except for ports 12, 13, 16, 17, 4, A1, A3, A4, and E)	C_{in}	—	—	15	pF	V_{in} = 0 V, f = 1 MHz, T_a = 25°C
	Ports 12, 13, 16, 17, 4, A1, A3, A4, and E		—	—	30		

Table 5.5 DC Characteristics (4)

Conditions: VCC = AVCC0 = 1.62 to 5.5 V, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +105°C

Item		Symbol	VCC						Unit	Test Conditions
			1.62 to 2.7 V		2.7 to 4.0 V		4.0 to 5.5 V			
			Min.	Max.	Min.	Max.	Min.	Max.		
Input pull-up MOS current	All ports (except for port 35)	I_p	–150	–5	–200	–10	–400	–50	µA	V_{in} = 0 V

[Chip version A]

Table 5.6 DC Characteristics (5)

Conditions: VCC = AVCC0 = 2.7 to 5.5 V, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +105°C

Item					Symbol	Typ.	Max.	Unit	Test Conditions
Supply current*1	High-speed operating mode	Normal operating mode	No peripheral operation*2	ICLK = 50 MHz	I_{CC}	10	—	mA	
			All peripheral operation: Normal*3	ICLK = 50 MHz		31.5	—		
			All peripheral operation: Max.*3	ICLK = 50 MHz		—	55		
		Sleep mode	No peripheral operation	ICLK = 50 MHz		7.5	—		
			All peripheral operation: Normal	ICLK = 50 MHz		17.5	—		
		All-module clock stop mode		ICLK = 50 MHz		6.7	—		
		Increase during BGO operation*4				25	—		

Note 1. Supply current values do not include output charge/discharge current from all pins. The values apply when internal pull-up MOSs are in the off state.

Note 2. Clock supply to the peripheral functions is stopped. This does not include BGO operation. The clock source is PLL and the VCO oscillation frequency is 100 MHz. BCLK, FCLK, and PCLK are set to divided by 64.

Note 3. Clocks are supplied to the peripheral functions. This does not include BGO operation. The clock source is PLL and the VCO oscillation frequency is 100 MHz. BCLK, FCLK, and PCLK are ICLK divided by 2.

Note 4. This is the increase if data is programmed to or erasing from the ROM or E2 DataFlash during program execution.

[Chip version B with 256 Kbytes or less of flash memory and 48 to 100 pins]

Table 5.13 DC Characteristics (12)

Conditions: VCC = AVCC0 = 1.62 to 5.5 V, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +105°C

Item					Symbol	Typ.	Max.	Unit	Test Conditions
Supply current*1	Middle-speed operating modes 1A and 1B	Normal operating mode	No peripheral operation	ICLK = 32 MHz*2	I_{CC}	5.3	—	mA	
				ICLK = 20 MHz*3		4.6	—		
			All peripheral operation: Normal	ICLK = 32 MHz*4		20.1	—		
				ICLK = 20 MHz*5		14.3	—		
			All peripheral operation: Max.	ICLK = 32 MHz*4		—	35		
				ICLK = 20 MHz*5		—	—		
		Sleep mode	No peripheral operation	ICLK = 32 MHz		3.4	—		
				ICLK = 20 MHz		3.3	—		
			All peripheral operation: Normal	ICLK = 32 MHz		11.5	—		
				ICLK = 20 MHz		9	—		
		All-module clock stop mode		ICLK = 32 MHz		3	—		
				ICLK = 20 MHz		3	—		
		Increase during BGO operation*6	Middle-speed operating mode 1A			17	—		
			Middle-speed operating mode 1B			17	—		
	Middle-speed operating modes 2A and 2B	Normal operating mode	No peripheral operation*2	ICLK = 32 MHz		4.7	—		
				ICLK = 16 MHz		3.4	—		
				ICLK = 8 MHz		2.7	—		
			All peripheral operation: Normal*4	ICLK = 32 MHz		19.6	—		
				ICLK =16 MHz		11.3	—		
				ICLK = 8 MHz		7.2	—		
			All peripheral operation: Max.*4	ICLK = 32 MHz		—	34		
				ICLK = 16 MHz		—	—		
				ICLK = 8 MHz		—	—		
		Sleep mode	No peripheral operation	ICLK = 32 MHz		2.8	—		
				ICLK = 16 MHz		2.5	—		
				ICLK = 8 MHz		2.2	—		
			All peripheral operation: Normal	ICLK = 32 MHz		11	—		
				ICLK = 16 MHz		7.2	—		
				ICLK = 8 MHz		5.3	—		
		All-module clock stop mode		ICLK = 32 MHz		2.4	—		
				ICLK = 16 MHz		2.2	—		
				ICLK = 8 MHz		2.1	—		
		Increase during BGO operation*6	Middle-speed operating mode 1A			17	—		
			Middle-speed operating mode 1B			17	—		

Table 5.21 DC Characteristics (20)

Conditions: VCC = AVCC0 = 1.62 to 5.5 V, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +105°C

Item	Symbol	Typ.	Max.	Unit	Test Conditions
Permissible total consumption power*1	Pd	—	350	mW	Ta = –40 to 85°C
		—	150		85°C < Ta ≤ 105°C

Note: • Please contact Renesas Electronics sales office for derating of operation under Ta = +85°C to +105°C. Derating is the systematic reduction of load for the sake of improved reliability.
Note 1. Total power dissipated by the entire chip (including output currents)

Table 5.22 DC Characteristics (21)

Conditions: VCC = AVCC0 = 1.62 to 5.5 V, VREFH = 1.8 to AVCC0, VREFH0 = 1.62 to AVCC0,
VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Analog power supply current	During A/D conversion	I_{AVCC0}	—	1.0	3.2	mA	
	Temperature sensor operating, waiting for A/D conversion		—	60	200	µA	
	During D/A conversion (per channel)	I_{VREFH}*1	—	0.25	0.75	mA	
	Waiting for A/D, D/A conversion (all units)*2	—	—	0.2	5.0	µA	
Reference power supply current	During A/D conversion	I_{VREFH0}	—	0.1	0.2	mA	
	Waiting for A/D conversion		—	0.2	0.4	µA	

Note: • The values for A/D conversion apply when the sample and hold circuit is not in use.
Note 1. The reference power supply current is included in the power supply current value for D/A conversion.
Note 2. The value is the total value of I_{AVCC0} and I_{VREFH}.

Table 5.23 DC Characteristics (22)

Conditions: VCC = AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +105°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
RAM standby voltage	V_{RAM}	1.62	—	—	V	

Table 5.24 DC Characteristics (23)

Conditions: VCC = AVCC0 = 0 to 5.5 V, VREFH = VREFH0 = 0 to AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V,
T_a = –40 to +105°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
VCC rising gradient	SrVCC	0.02	—	20	ms/V	At cold start

[Chip versions B and C]

Table 5.31 Output Values of Voltage (4)

Conditions: VCC = AVCC0 = 2.7 to 4.0 V, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +105°C

Item			Symbol	Min.	Max.	Unit	Test Conditions
Output low	All output pins (other than RIIC)	Normal output mode	V_{OL}	—	0.5	V	I_{OL} = 1.0 mA
		High-drive output mode		—	0.5		I_{OL} = 2.0 mA
	RIIC pins			—	0.4		I_{OL} = 3.0 mA
				—	0.6		I_{OL} = 6.0 mA
Output high	All output pins	Normal output mode	V_{OH}	VCC – 0.5	—	V	I_{OH} = –1.0 mA
		High-drive output mode		VCC – 0.5	—		I_{OH} = –2.0 mA

[Chip versions B and C]

Table 5.32 Output Values of Voltage (5)

Conditions: VCC = AVCC0 = 4.0 to 5.5 V, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +105°C

Item			Symbol	Min.	Max.	Unit	Test Conditions
Output low	All output pins (other than RIIC)	Normal output mode	V_{OL}	—	0.8	V	I_{OL} = 2.0 mA
		High-drive output mode		—	0.8		I_{OL} = 4.0 mA
	RIIC pins			—	0.4		I_{OL} = 3.0 mA
				—	0.6		I_{OL} = 6.0 mA
Output high	All output pins	Normal output mode	V_{OH}	VCC – 0.8	—	V	I_{OH} = –2.0 mA
		High-drive output mode		VCC – 0.8	—		I_{OH} = –4.0 mA

5.2.1 Standard I/O Pin Output Characteristics (1)

Figure 5.45 to Figure 5.49 show the characteristics when normal output is selected by the drive capacity control register.

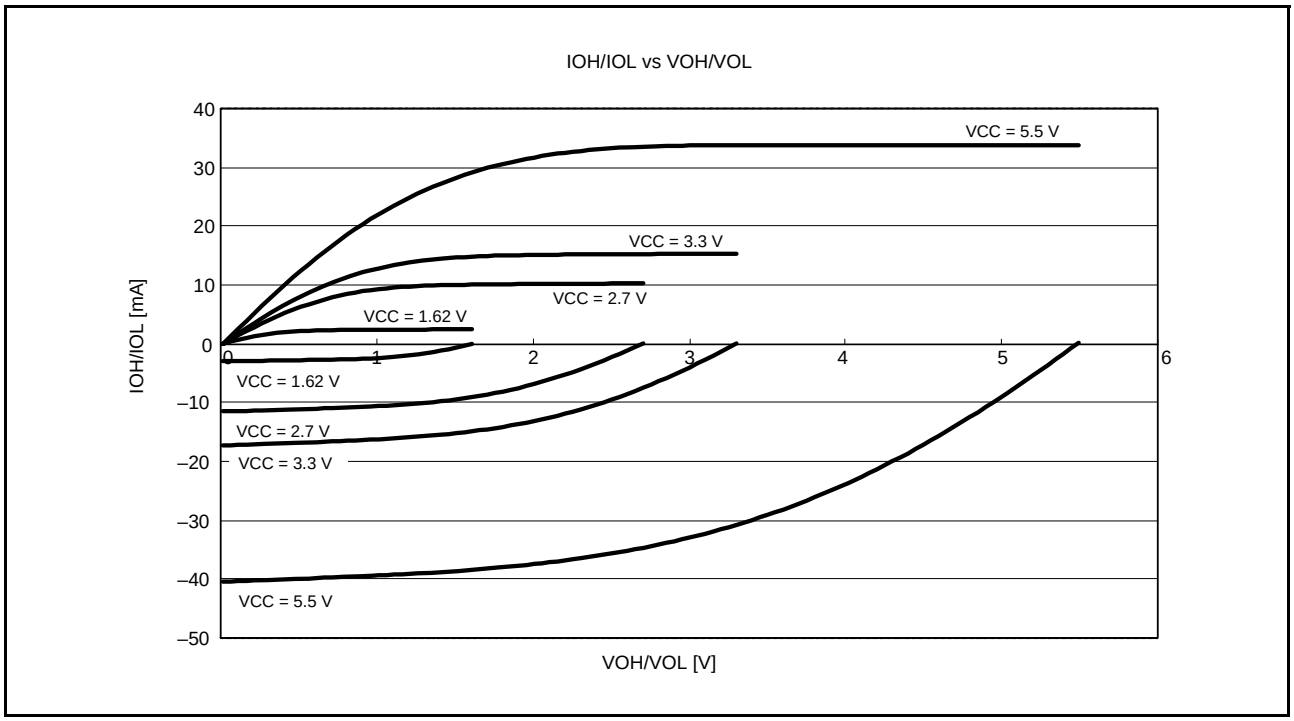


Figure 5.45 VOH/VOL and IOH/IOL Voltage Characteristics at Ta = 25°C when Normal Output is Selected (Reference Data)

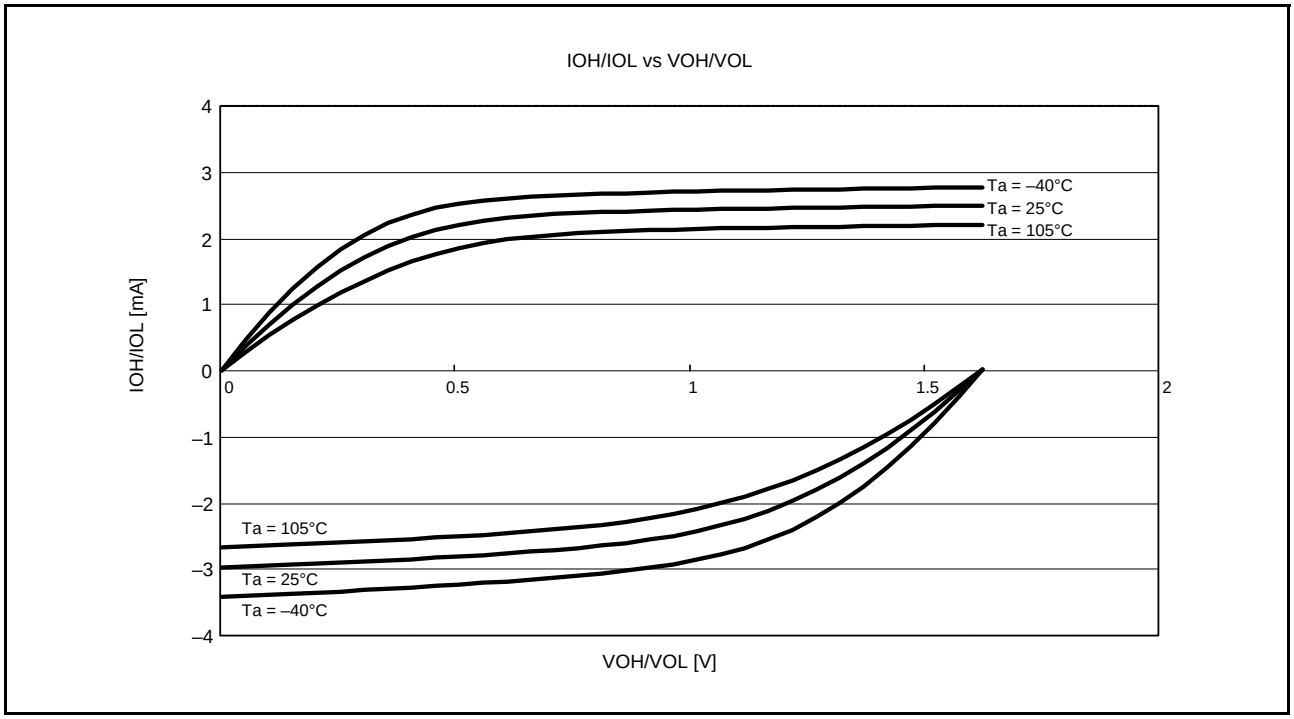


Figure 5.46 VOH/VOL and IOH/IOL Temperature Characteristics at VCC = 1.62 V when Normal Output is Selected (Reference Data)

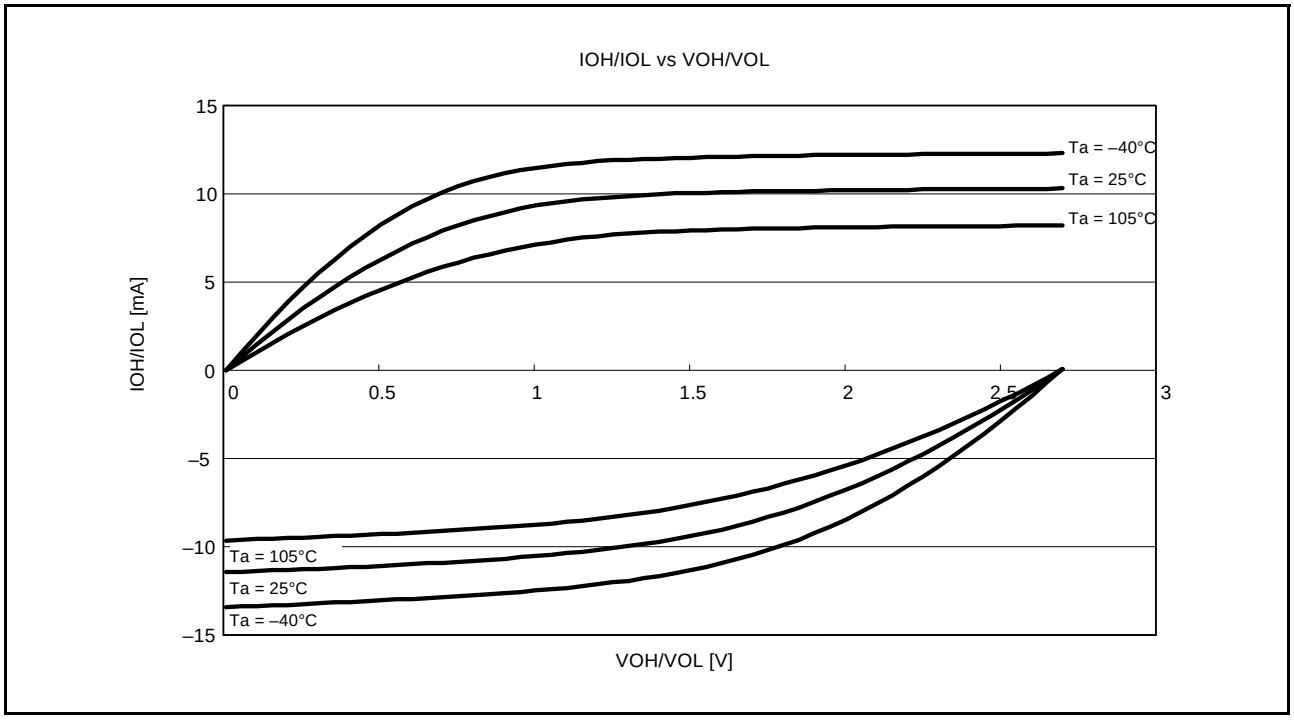


Figure 5.47 VOH/VOL and IOH/IOL Temperature Characteristics at VCC = 2.7 V when Normal Output is Selected (Reference Data)

[Chip version B]

Table 5.36 Operation Frequency Value (Middle-Speed Operating Mode 2A)

Conditions: VCC = AVCC0 = 1.62 to 5.5 V, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +105°C

Item		Symbol	VCC			Unit
			1.62 to 1.8 V	1.8 to 2.7 V	2.7 to 5.5 V	
Maximum operating frequency	System clock (ICLK)	f_{max}	8	16	32	MHz
	FlashIF clock (FCLK)*1		8	16	32	
	Peripheral module clock (PCLKB)		8	16	32	
	Peripheral module clock (PCLKD)*2		8	16	32	
	External bus clock (BCLK)		8	16	25	
	BCLK pin output		8	8	12.5	

Note 1. The VCC is 2.7 to 5.5 V and the lower-limit frequency of FCLK is 4 MHz during programming or erasing of the flash memory.
Note 2. The lower-limit frequency of PCLKD is 1 MHz when the A/D converter is in use.

[Chip version B]

Table 5.37 Operation Frequency Value (Middle-Speed Operating Mode 2B)

Conditions: VCC = AVCC0 = 1.62 to 5.5 V, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +105°C

Item		Symbol	VCC			Unit
			1.62 to 1.8 V	1.8 to 2.7 V	2.7 to 5.5 V	
Maximum operating frequency	System clock (ICLK)	f_{max}	8	16	32	MHz
	FlashIF clock (FCLK)*1		8	16	32	
	Peripheral module clock (PCLKB)		8	16	32	
	Peripheral module clock (PCLKD)*2		8	16	32	
	External bus clock (BCLK)		8	16	25	
	BCLK pin output		8	8	12.5	

Note 1. The VCC is 1.62 to 3.6 V and the lower-limit frequency of FCLK is 4 MHz during programming or erasing of the flash memory.
Note 2. The lower-limit frequency of PCLKD is 1 MHz when the A/D converter is in use.

[Chip versions A and C]

Table 5.38 Operation Frequency Value (Low-Speed Operating Mode 1)

Conditions: VCC = AVCC0 = 1.62 to 5.5 V, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +105°C

Item		Symbol	VCC			Unit
			1.62 to 1.8 V	1.8 to 2.7 V	2.7 to 5.5 V	
Maximum operating frequency	System clock (ICLK)	f_{max}	1	1	1	MHz
	FlashIF clock (FCLK)*1		1	1	1	
	Peripheral module clock (PCLKB)		1	1	1	
	Peripheral module clock (PCLKD)*2		1	1	1	
	External bus clock (BCLK)		1	1	1	
	BCLK pin output		1	1	1	

Note 1. Programming and erasing the flash memory is impossible.
Note 2. The lower-limit frequency of PCLKD is 1 MHz when the A/D converter is in use.

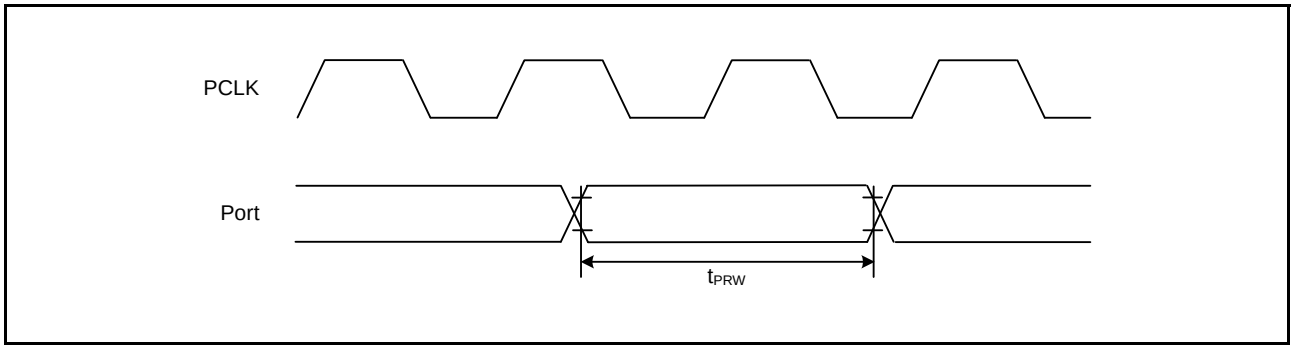


Figure 5.83 I/O Port Input Timing

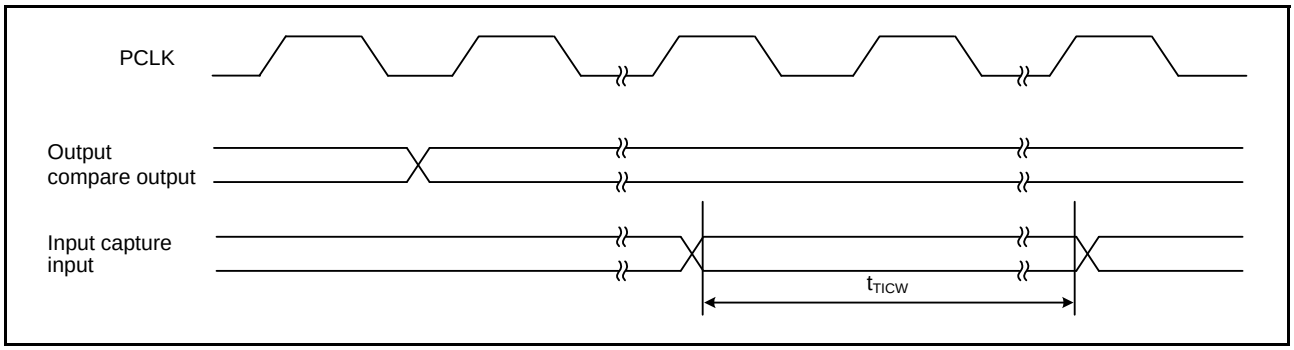


Figure 5.84 MTU/TPU Input/Output Timing

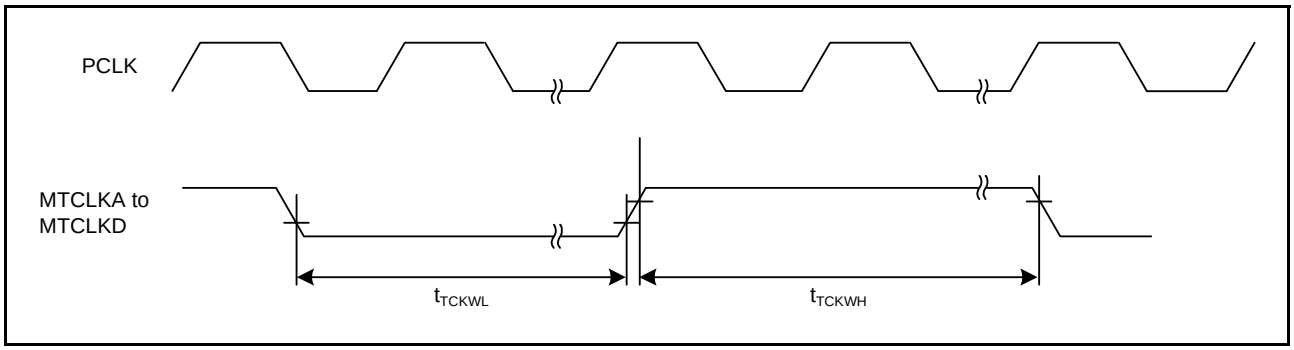


Figure 5.85 MTU/TPU Clock Input Timing

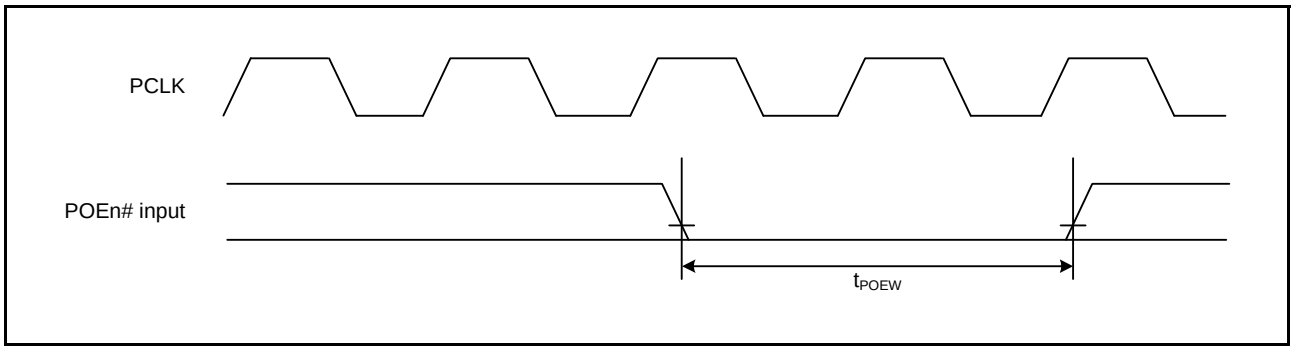


Figure 5.86 POE# Input Timing

[Chip version B]

Table 5.79 ROM (Flash Memory for Code Storage) Characteristics (6) : middle-speed operating modes 1B and 2B

Conditions: VCC = AVCC0 = 1.62 to 3.6 V, VREFH = VREFH0 = AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V
Temperature range for the programming/erasure operation: T_a = –40 to +105°C

Item		Symbol	FCLK = 4 MHz			FCLK = 32 MHz*1			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Programming time when N_{PEC} ≤ 100 times	2 bytes	t_{P2}	—	0.25	5.0	—	0.21	2.8	ms
	8 bytes	t_{P8}	—	0.25	5.3	—	0.21	3.0	
	128 bytes	t_{P128}	—	0.92	14.0	—	0.65	8.3	
Programming time when N_{PEC} > 100 times	2 bytes	t_{P2}	—	0.31	6.2	—	0.26	3.5	ms
	8 bytes	t_{P8}	—	0.31	6.6	—	0.26	3.7	
	128 bytes	t_{P128}	—	1.09	17.5	—	0.77	10.0	
Erasure time when N_{PEC} ≤ 100 times	2 Kbytes	t_{E2K}	—	21.0	113.7	—	18.5	46	ms
Erasure time when N_{PEC} > 100 times	2 Kbytes	t_{E2K}	—	25.6	220.6	—	22.5	90 (1000 times ≥ N_{PEC} > 100 times), 98 (10000 times ≥ N_{PEC} > 1000 times)	ms
Suspend delay time during programming (in programming/erasure priority mode)		t_{SPD}	—	—	1.7	—	—	1.6	ms
First suspend delay time during programming (in suspend priority mode)		t_{SPSD1}	—	—	220	—	—	120	µs
Second suspend delay time during programming (in suspend priority mode)		t_{SPSD2}	—	—	1.7	—	—	1.6	ms
Suspend delay time during erasing (in programming/erasure priority mode)		t_{SED}	—	—	1.7	—	—	1.6	ms
First suspend delay time during erasing (in suspend priority mode)		t_{SESD1}	—	—	220	—	—	120	µs
Second suspend delay time during erasing (in suspend priority mode)		t_{SESD2}	—	—	1.7	—	—	1.6	ms
FCU reset time		t_{FCUR}	20 µs or longer and FCLK × 6 or greater	—	—	20 µs or longer and FCLK × 6 or greater	—	—	µs

Note 1. The operating frequency is 20 MHz (max.) when the voltage is in the range from 1.62 V to less than 1.8 V.

5.11 E2 DataFlash Characteristics

[Chip version A]

Table 5.80 E2 DataFlash Characteristics (1)

Item	Symbol	Min.	Typ.	Max.	Unit	Conditions
Reprogramming/erasure cycle*1	N_{DPEC}	100000	—	—	Times	
Data hold time	t_{DRP}	10*2	—	—	Year	

Note 1. The reprogram/erase cycle is the number of erasing for each block. When the reprogram/erase cycle is n times (n = 100000), erasing can be performed n times for each block. For instance, when 8-byte programming is performed 16 times for different addresses in 128-byte block and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address for several times as one erasing is not enabled (overwriting is prohibited).

Note 2. This result is obtained from reliability testing.

[Chip versions B and C]

Table 5.81 E2 DataFlash Characteristics (2)

Item		Symbol	Min.	Typ.	Max.	Unit	Conditions
Reprogramming/erasure cycle*1		N_{DPEC}	100000	—	—	Times	
Data hold time	After 100000 times of N_{DPEC}	t_{DRP}	30*2	—	—	Year	Ta = +85°C

Note 1. The reprogram/erase cycle is the number of erasing for each block. When the reprogram/erase cycle is n times (n = 100000), erasing can be performed n times for each block. For instance, when 8-byte programming is performed 16 times for different addresses in 128-byte block and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address for several times as one erasing is not enabled (overwriting is prohibited).

Note 2. This result is obtained from reliability testing.

[Chip version B]

Table 5.85 E2 DataFlash Characteristics (6)
: middle-speed operating modes 1B and 2B

Conditions: VCC = AVCC0 = 1.62 to 3.6 V, VREFH = VREFH0 = AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V
Temperature range for the programming/erasure operation: T_a = –40 to +105°C

Item		Symbol	FCLK = 4 MHz			FCLK = 32 MHz*1			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Programming time when N_{DPEC} ≤ 100 times	2 bytes	t_{DP2}	—	0.28	5.1	—	0.20	2.8	ms
	8 bytes	t_{DP8}	—	0.32	6.0	—	0.22	3.2	
Programming time when N_{DPEC} > 100 times	2 bytes	t_{DP2}	—	0.36	7.6	—	0.25	4.2	ms
	8 bytes	t_{DP8}	—	0.40	8.8	—	0.28	4.5	
Erasure time when N_{DPEC} ≤ 100 times	128 bytes	t_{DE128}	—	4.8	32.4	—	4.1	12	ms
Erasure time when N_{DPEC} > 100 times	128 bytes	t_{DE128}	—	5.8	51.4	—	4.9	17	ms
Blank check time	2 bytes	t_{DBC2}	—	—	110	—	—	40	µs
	2 Kbytes	t_{DBC2K}	—	—	16.3	—	—	2.6	ms
Suspend delay time during programming (in programming/erasure priority mode)		t_{DSPD}	—	—	1.7	—	—	1.6	ms
First suspend delay time during programming (in suspend priority mode)		t_{DSPSD1}	—	—	220	—	—	120	µs
Second suspend delay time during programming (in suspend priority mode)		t_{DSPSD2}	—	—	1.7	—	—	1.6	ms
Suspend delay time during erasing (in programming/erasure priority mode)		t_{DSED}	—	—	1.7	—	—	1.6	ms
First suspend delay time during erasing (in suspend priority mode)		t_{DSESD1}	—	—	220	—	—	120	µs
Second suspend delay time during erasing (in suspend priority mode)		t_{DSESD2}	—	—	1.7	—	—	1.6	ms

Note 1. The operating frequency is 20 MHz (max.) when the voltage is in the range from 1.62 V to less than 1.8 V.

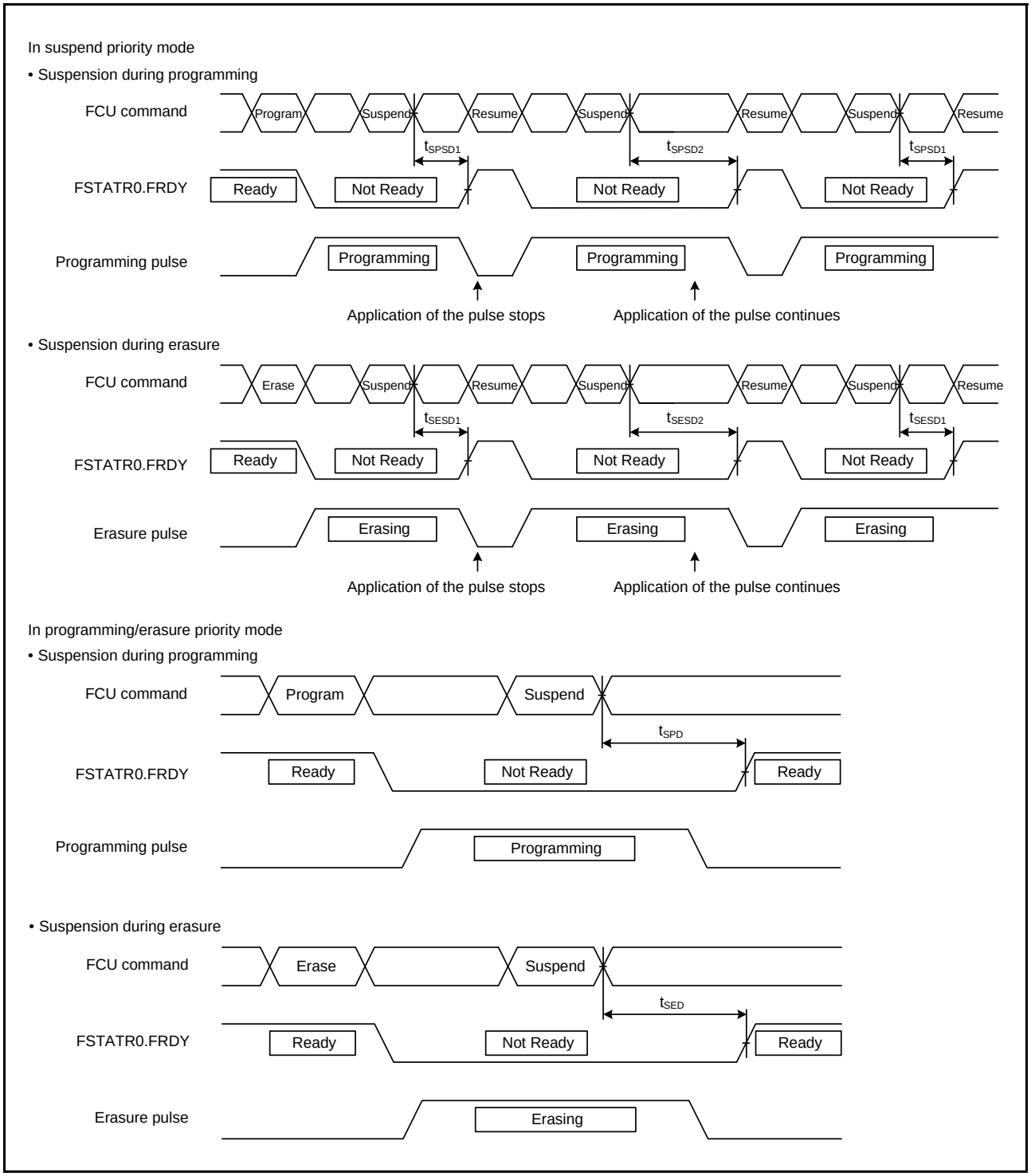


Figure 5.109 Flash Memory Program/Erase Suspend Timing