Renesas Electronics America Inc - R5F52107CDFF#V0 Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I²C, SCI, SPI
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	64
Program Memory Size	384KB (384K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	1.62V ~ 5.5V
Data Converters	A/D 14x12b; D/A 2x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f52107cdff-v0

1.4 Pin Functions

Table 1.8 lists the pin functions.

Table 1.8 Pin Functions (1 / 4)

Classifications	Pin Name	I/O	Description
Power supply	VCC	Input	Power supply pin. Connect it to the system power supply.
	VCL	—	Connect this pin to the VSS pin via the 0.1 µF smoothing capacitor used to stabilize the internal power supply. Place the capacitor close to the pin.
	VSS	Input	Ground pin. Connect it to the system power supply (0 V).
Clock	XTAL	Output	Pins for connecting a crystal resonator. An external clock signal can be input through the EXTAL pin.
	EXTAL	Input	
	BCLK	Output	Outputs the external bus clock for external devices.
	XCIN	Input	Input/output pins for the sub-clock oscillator. Connect a crystal resonator between XCIN and XCOUT.
	XCOUT	Output	
Operating mode control	MD	Input	Pin for setting the operating mode. The signal levels on this pin must not be changed during operation.
System control	RES#	Input	Reset pin. This LSI enters the reset state when this signal goes low.
CAC	CACREF	Input	Input pin for the clock frequency accuracy measurement circuit.
On-chip emulator	FINED	I/O	FINE interface pin.
Address bus	A0 to A23	Output	Output pins for the address.
Data bus	D0 to D15	I/O	Input and output pins for the bidirectional data bus.
Multiplexed bus	A0/D0 to A15/D15	I/O	Address/data multiplexed bus
Bus control	RD#	Output	Strobe signal which indicates that reading from the external bus interface space is in progress.
	WR#	Output	Strobe signal which indicates that writing to the external bus interface space is in progress, in single-write strobe mode.
	WR0#, WR1#	Output	Strobe signals which indicate that either group of data bus pins (D7 to D0, and D15 to D8) is valid in writing to the external bus interface space, in byte strobe mode.
	BC0#, BC1#	Output	Strobe signals which indicate that either group of data bus pins (D7 to D0 and D15 to D8) is valid in access to the external bus interface space, in single-write strobe mode.
	CS0# to CS3#	Output	Select signals for areas 0 to 3.
	WAIT#	Input	Input pin for wait request signals in access to the external space.
	ALE	Output	Address latch signal when address/data multiplexed bus is selected.
Interrupt	NMI	Input	Non-maskable interrupt request pin.
	IRQ0 to IRQ7	Input	Interrupt request pins.

Table 1.11 List of Pins and Pin Functions (100-Pin TFLGA) (1 / 3)

Pin No.	Power Supply, Clock, System Control	I/O Port	External Bus	Timers (MTU, TMR, POE)	Communications (SCIc, SCId, RSPI, RIIC)	Others
A1		P05				DA1
A2	VREFH					
A3		P07				ADTRG0#
A4	VREFL0					
A5		P43				AN003
A6		PD0	D0[A0/D0]			IRQ0
A7		PD4	D4[A4/D4]	POE3#		IRQ4
A8		PE0	D8[A8/D8]		SCK12	AN008
A9		PE1	D9[A9/D9]	MTIOC4C	TXD12/TXDX12/SIOX12/ SMOSI12/SSDA12	AN009/CMPB0
A10		PE2	D10[A10/D10]	MTIOC4A	RXD12/RXDX12/ SMISO12/SSCL12	IRQ7-DS/AN010/ CVREFB0
B1		P03				DA0
B2	AVSS0					
B3	AVCC0					
B4		P40				AN000
B5		P44				AN004
B6		PD1	D1[A1/D1]	MTIOC4B		IRQ1
B7		PD3	D3[A3/D3]	POE8#		IRQ3
B8		PD6	D6[A6/D6]	MTIC5V/POE1#		IRQ6
B9		PD7	D7[A7/D7]	MTIC5U/POE0#		IRQ7
B10		PE3	D11[A11/D11]	MTIOC4B/POE8#	CTS12#/RTS12#/SS12#	AN011/CMPA1
C1	VCL					
C2	VREFL					
C3		PJ3		MTIOC3C	CTS6#/RTS6#/SS6#	
C4	VREFH0					
C5		P42				AN002
C6		P47				AN007
C7		PD2	D2[A2/D2]	MTIOC4D		IRQ2
C8		PD5	D5[A5/D5]	MTIC5W/POE2#		IRQ5
C9		PE5	D13[A13/D13]	MTIOC4C/MTIOC2B		IRQ5/AN013
C10		PE4	D12[A12/D12]	MTIOC4D/MTIOC1A		AN012/CMPA2
D1	XCIN					
D2	XCOUT					
D3	MD					FINED
D4		PJ1		MTIOC3A		
D5		P45				AN005
D6		P46				AN006
D7		PE6	D14[A14/D14]			IRQ6/AN014
D8		PE7	D15[A15/D15]			IRQ7/AN015
D9		PA1	A1	MTIOC0B/MTCLKC	SCK5/SSLA2	CVREFA
D10		PA0	A0/BC0#	MTIOC4A	SSLA1	CACREF
E1	XTAL	P37				
E2	VSS					
E3	RES#					
E4		P34		MTIOC0A/TMCI3/ POE2#	SCK6	IRQ4
E5		P41				AN001

Table 1.11 List of Pins and Pin Functions (100-Pin TFLGA) (3 / 3)

Pin No.	Power Supply, Clock, System Control	I/O Port	External Bus	Timers (MTU, TMR, POE)	Communications (SCIc, SCId, RSPI, RIIC)	Others
J4		P13		MTIOC0B/TMO3	SDA	IRQ3
J5		PH0				CACREF
J6		PH3		TMCI0		
J7		P50	WR0#/WR#			
J8		PC4	A20/CS3#	MTIOC3D/MTCLKC/ TMCI1/POE0#	SCK5/CTS8#/RTS8#/ SS8#/SSLA0	
J9		PC0	A16	MTIOC3C	CTS5#/RTS5#/SS5#/ SSLA1	
J10		PC1	A17	MTIOC3A	SCK5/SSLA2	
K1		P23		MTIOC3D/MTCLKD	CTS0#/RTS0#/SS0#	
K2		P22		MTIOC3B/MTCLKC/ TMO0	SCK0	
K3		P20		MTIOC1A/TMRI0	TXD0/SMOSI0/SSDA0	
K4		P14		MTIOC3A/MTCLKA/ TMRI2	CTS1#/RTS1#/SS1#	IRQ4
K5		PH2		TMRI0		IRQ1
K6		PH1		TMO0		IRQ0
K7		P51	WR1#/BC1#/WAIT#			
K8		PC5	A21/CS2#/WAIT#	MTIOC3B/MTCLKD/ TMRI2	SCK8/RSPCKA	
K9		PC3	A19	MTIOC4D	TXD5/SMOSI5/SSDA5	
K10		PC2	A18	MTIOC4B	RXD5/SMISO5/SSCL5/ SSLA3	

Note: • Pin names to which –DS is appended are for pins that can be used to trigger release from deep software standby mode.

Table 1.16 List of Pins and Pin Functions (64-Pin LQFP) (2 / 2)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (MTU, TMR, POE)	Communication (SCIc, SCId, RSPI, RIIC)	Others
44		PA1	MTIOC0B/MTCLKC	SCK5/SSLA2	CVREFA
45		PA0	MTIOC4A	SSLA1	CACREF
46		PE5	MTIOC4C/MTIOC2B		IRQ5/AN013
47		PE4	MTIOC4D/MTIOC1A		AN012/CMPA2
48		PE3	MTIOC4B/POE8#	CTS12#/RTS12#/SS12#	AN011/CMPA1
49		PE2	MTIOC4A	RXD12/RXDX12/SMISO12/ SSCL12	IRQ7-DS/AN010/ CVREFB0
50		PE1	MTIOC4C	TXD12/TXDX12/SIOX12/ SMOSI12/SSDA12	AN009/CMPB0
51		PE0		SCK12	AN008
52	VREFL				
53		P46			AN006
54	VREFH				
55		P44			AN004
56		P43			AN003
57		P42			AN002
58		P41			AN001
59	VREFL0				
60		P40			AN000
61	VREFH0				
62	AVCC0				
63		P05			DA1
64	AVSS0				

Note: • Pin names to which –DS is appended are for pins that can be used to trigger release from deep software standby mode.

Table 4.1 List of I/O Registers (Address Order) (3 / 29)

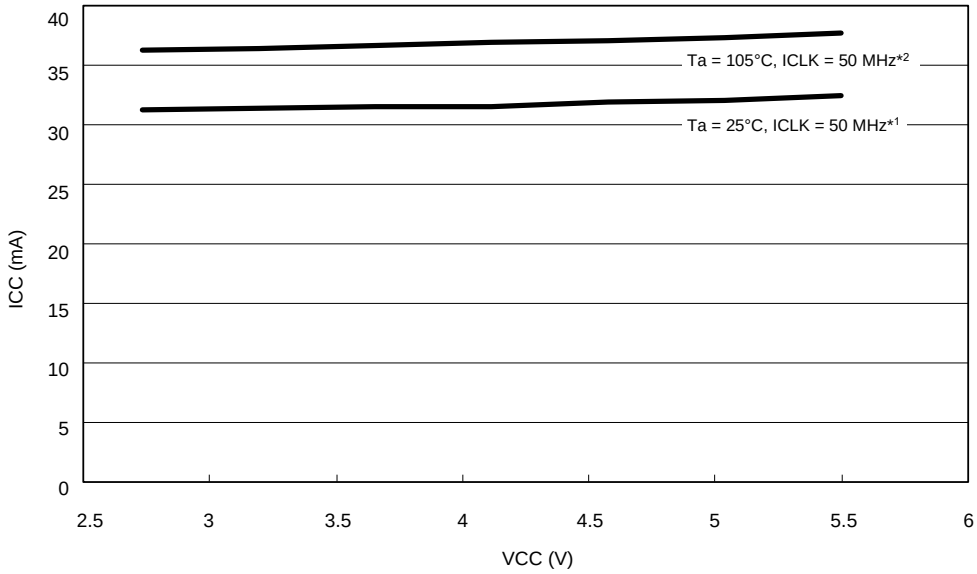
Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles ICLK ≥ PCLK	Number of Access Cycles ICLK < PCLK
0008 3032h	BSC	CS3 mode register	CS3MOD	16	16	1, 2 BCLK	
0008 3034h	BSC	CS3 wait control register 1	CS3WCR1	32	32	1, 2 BCLK	
0008 3038h	BSC	CS3 wait control register 2	CS3WCR2	32	32	1, 2 BCLK	
0008 3802h	BSC	CS0 control register	CS0CR	16	16	1, 2 BCLK	
0008 380Ah	BSC	CS0 recovery cycle register	CS0REC	16	16	1, 2 BCLK	
0008 3812h	BSC	CS1 control register	CS1CR	16	16	1, 2 BCLK	
0008 381Ah	BSC	CS1 recovery cycle register	CS1REC	16	16	1, 2 BCLK	
0008 3822h	BSC	CS2 control register	CS2CR	16	16	1, 2 BCLK	
0008 382Ah	BSC	CS2 recovery cycle register	CS2REC	16	16	1, 2 BCLK	
0008 3832h	BSC	CS3 control register	CS3CR	16	16	1, 2 BCLK	
0008 383Ah	BSC	CS3 recovery cycle register	CS3REC	16	16	1, 2 BCLK	
0008 3880h	BSC	CS recovery cycle insertion enable register	CSRECEN	16	16	1, 2 BCLK	
0008 7010h	ICU	Interrupt request register 016	IR016	8	8	2 ICLK	
0008 7015h	ICU	Interrupt request register 021	IR021	8	8	2 ICLK	
0008 7017h	ICU	Interrupt request register 023	IR023	8	8	2 ICLK	
0008 701Bh	ICU	Interrupt request register 027	IR027	8	8	2 ICLK	
0008 701Ch	ICU	Interrupt request register 028	IR028	8	8	2 ICLK	
0008 701Dh	ICU	Interrupt request register 029	IR029	8	8	2 ICLK	
0008 701Eh	ICU	Interrupt request register 030	IR030	8	8	2 ICLK	
0008 701Fh	ICU	Interrupt request register 031	IR031	8	8	2 ICLK	
0008 7020h	ICU	Interrupt request register 032	IR032	8	8	2 ICLK	
0008 7021h	ICU	Interrupt request register 033	IR033	8	8	2 ICLK	
0008 7022h	ICU	Interrupt request register 034	IR034	8	8	2 ICLK	
0008 702Ch	ICU	Interrupt request register 044	IR044	8	8	2 ICLK	
0008 702Dh	ICU	Interrupt request register 045	IR045	8	8	2 ICLK	
0008 702Eh	ICU	Interrupt request register 046	IR046	8	8	2 ICLK	
0008 702Fh	ICU	Interrupt request register 047	IR047	8	8	2 ICLK	
0008 7039h	ICU	Interrupt request register 057	IR057	8	8	2 ICLK	
0008 703Ah	ICU	Interrupt request register 058	IR058	8	8	2 ICLK	
0008 703Bh	ICU	Interrupt request register 059	IR059	8	8	2 ICLK	
0008 703Fh	ICU	Interrupt request register 063	IR063	8	8	2 ICLK	
0008 7040h	ICU	Interrupt request register 064	IR064	8	8	2 ICLK	
0008 7041h	ICU	Interrupt request register 065	IR065	8	8	2 ICLK	
0008 7042h	ICU	Interrupt request register 066	IR066	8	8	2 ICLK	
0008 7043h	ICU	Interrupt request register 067	IR067	8	8	2 ICLK	
0008 7044h	ICU	Interrupt request register 068	IR068	8	8	2 ICLK	
0008 7045h	ICU	Interrupt request register 069	IR069	8	8	2 ICLK	
0008 7046h	ICU	Interrupt request register 070	IR070	8	8	2 ICLK	
0008 7047h	ICU	Interrupt request register 071	IR071	8	8	2 ICLK	
0008 7058h	ICU	Interrupt request register 088	IR088	8	8	2 ICLK	
0008 7059h	ICU	Interrupt request register 089	IR089	8	8	2 ICLK	
0008 705Ch	ICU	Interrupt request register 092	IR092	8	8	2 ICLK	
0008 705Dh	ICU	Interrupt request register 093	IR093	8	8	2 ICLK	
0008 7066h	ICU	Interrupt request register 102	IR102	8	8	2 ICLK	
0008 7067h	ICU	Interrupt request register 103	IR103	8	8	2 ICLK	
0008 706Ah	ICU	Interrupt request register 106	IR106	8	8	2 ICLK	
0008 706Bh	ICU	Interrupt request register 107	IR107	8	8	2 ICLK	
0008 7072h	ICU	Interrupt request register 114	IR114	8	8	2 ICLK	
0008 7073h	ICU	Interrupt request register 115	IR115	8	8	2 ICLK	
0008 7074h	ICU	Interrupt request register 116	IR116	8	8	2 ICLK	
0008 7075h	ICU	Interrupt request register 117	IR117	8	8	2 ICLK	

Table 4.1 List of I/O Registers (Address Order) (10 / 29)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles: ICLK ≥ PCLK	Number of Access Cycles: ICLK < PCLK
0008 738A2	ICU	Interrupt source priority register 162	IPR162	8	8		2 ICLK
0008 73A4h	ICU	Interrupt source priority register 164	IPR164	8	8		2 ICLK
0008 73A6h	ICU	Interrupt source priority register 166	IPR166	8	8		2 ICLK
0008 73AAh	ICU	Interrupt source priority register 170	IPR170	8	8		2 ICLK
0008 73ABh	ICU	Interrupt source priority register 171	IPR171	8	8		2 ICLK
0008 73AEh	ICU	Interrupt source priority register 174	IPR174	8	8		2 ICLK
0008 73B1h	ICU	Interrupt source priority register 177	IPR177	8	8		2 ICLK
0008 73B4h	ICU	Interrupt source priority register 180	IPR180	8	8		2 ICLK
0008 73B7h	ICU	Interrupt source priority register 183	IPR183	8	8		2 ICLK
0008 73BAh	ICU	Interrupt source priority register 186	IPR186	8	8		2 ICLK
0008 73BEh	ICU	Interrupt source priority register 190	IPR190	8	8		2 ICLK
0008 73C2h	ICU	Interrupt source priority register 194	IPR194	8	8		2 ICLK
0008 73C6h	ICU	Interrupt source priority register 198	IPR198	8	8		2 ICLK
0008 73C7h	ICU	Interrupt source priority register 199	IPR199	8	8		2 ICLK
0008 73C8h	ICU	Interrupt source priority register 200	IPR200	8	8		2 ICLK
0008 73C9h	ICU	Interrupt source priority register 201	IPR201	8	8		2 ICLK
0008 73CEh	ICU	Interrupt source priority register 206	IPR206	8	8		2 ICLK
0008 73D2h	ICU	Interrupt source priority register 210	IPR210	8	8		2 ICLK
0008 73D6h	ICU	Interrupt source priority register 214	IPR214	8	8		2 ICLK
0008 73DAh	ICU	Interrupt source priority register 218	IPR218	8	8		2 ICLK
0008 73DEh	ICU	Interrupt source priority register 222	IPR222	8	8		2 ICLK
0008 73E2h	ICU	Interrupt source priority register 226	IPR226	8	8		2 ICLK
0008 73E6h	ICU	Interrupt source priority register 230	IPR230	8	8		2 ICLK
0008 73EAh	ICU	Interrupt source priority register 234	IPR234	8	8		2 ICLK
0008 73EEh	ICU	Interrupt source priority register 238	IPR238	8	8		2 ICLK
0008 73F2h	ICU	Interrupt source priority register 242	IPR242	8	8		2 ICLK
0008 73F3h	ICU	Interrupt source priority register 243	IPR243	8	8		2 ICLK
0008 73F4h	ICU	Interrupt source priority register 244	IPR244	8	8		2 ICLK
0008 73F5h	ICU	Interrupt source priority register 245	IPR245	8	8		2 ICLK
0008 73F6h	ICU	Interrupt source priority register 246	IPR246	8	8		2 ICLK
0008 73F7h	ICU	Interrupt source priority register 247	IPR247	8	8		2 ICLK
0008 73F8h	ICU	Interrupt source priority register 248	IPR248	8	8		2 ICLK
0008 73F9h	ICU	Interrupt source priority register 249	IPR249	8	8		2 ICLK
0008 73FAh	ICU	Interrupt source priority register 250	IPR250	8	8		2 ICLK
0008 7400h	ICU	DMAC activation request select register 0	DMRSR0	8	8		2 ICLK
0008 7404h	ICU	DMAC activation request select register 1	DMRSR1	8	8		2 ICLK
0008 7408h	ICU	DMAC activation request select register 2	DMRSR2	8	8		2 ICLK
0008 740Ch	ICU	DMAC activation request select register 3	DMRSR3	8	8		2 ICLK
0008 7500h	ICU	IRQ control register 0	IRQCR0	8	8		2 ICLK
0008 7501h	ICU	IRQ control register 1	IRQCR1	8	8		2 ICLK
0008 7502h	ICU	IRQ control register 2	IRQCR2	8	8		2 ICLK
0008 7503h	ICU	IRQ control register 3	IRQCR3	8	8		2 ICLK
0008 7504h	ICU	IRQ control register 4	IRQCR4	8	8		2 ICLK
0008 7505h	ICU	IRQ control register 5	IRQCR5	8	8		2 ICLK
0008 7506h	ICU	IRQ control register 6	IRQCR6	8	8		2 ICLK
0008 7507h	ICU	IRQ control register 7	IRQCR7	8	8		2 ICLK
0008 7510h	ICU	IRQ pin digital filter enable register 0	IRQFLTE0	8	8		2 ICLK
0008 7514h	ICU	IRQ pin digital filter setting register 0	IRQFLTC0	16	16		2 ICLK
0008 7580h	ICU	Non-maskable interrupt status register	NMISR	8	8		2 ICLK
0008 7581h	ICU	Non-maskable interrupt enable register	NMIER	8	8		2 ICLK
0008 7582h	ICU	Non-maskable interrupt clear register	NMICLR	8	8		2 ICLK

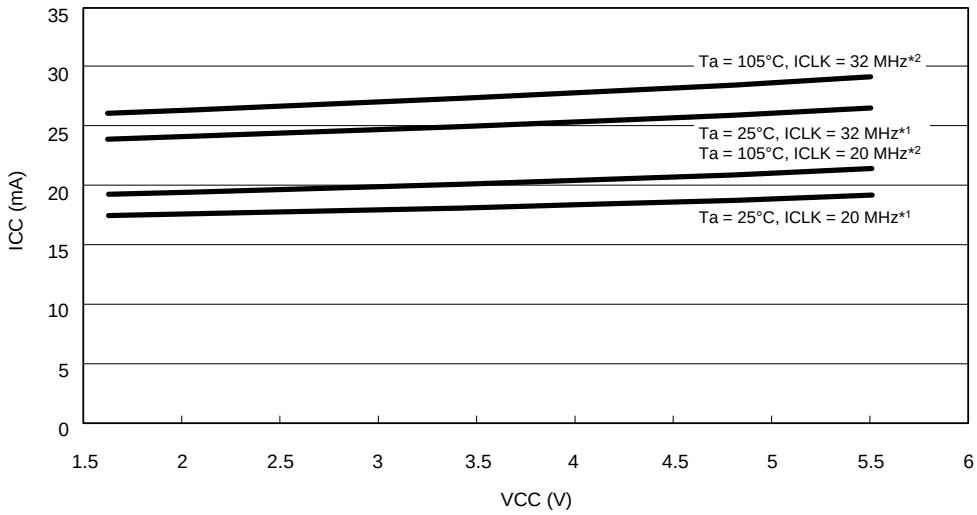
Table 4.1 List of I/O Registers (Address Order) (27 / 29)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles: ICLK ≥ PCLK	Number of Access Cycles: ICLK < PCLK
0008 C16Dh	MPC	P55 pin function control register	P55PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C16Eh	MPC	P56 pin function control register	P56PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C170h	MPC	P60 pin function control register	P60PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C171h	MPC	P61 pin function control register	P61PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C178h	MPC	P70 pin function control register	P70PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C17Ch	MPC	P74 pin function control register	P74PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C17Dh	MPC	P75 pin function control register	P75PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C17Eh	MPC	P76 pin function control register	P76PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C17Fh	MPC	P77 pin function control register	P77PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C180h	MPC	P80 pin function control register	P80PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C181h	MPC	P81 pin function control register	P81PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C182h	MPC	P82 pin function control register	P82PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C183h	MPC	P83 pin function control register	P83PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C186h	MPC	P86 pin function control register	P865PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C187h	MPC	P87 pin function control register	P87PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C188h	MPC	P90 pin function control register	P90PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C189h	MPC	P91 pin function control register	P91PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C18Ah	MPC	P92 pin function control register	P92PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C18Bh	MPC	P93 pin function control register	P93PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C190h	MPC	PA0 pin function control register	PA0PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C191h	MPC	PA1 pin function control register	PA1PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C192h	MPC	PA2 pin function control register	PA2PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C193h	MPC	PA3 pin function control register	PA3PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C194h	MPC	PA4 pin function control register	PA4PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C195h	MPC	PA5 pin function control register	PA5PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C196h	MPC	PA6 pin function control register	PA6PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C197h	MPC	PA7 pin function control register	PA7PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C198h	MPC	PB0 pin function control register	PB0PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C199h	MPC	PB1 pin function control register	PB1PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C19Ah	MPC	PB2 pin function control register	PB2PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C19Bh	MPC	PB3 pin function control register	PB3PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C19Ch	MPC	PB4 pin function control register	PB4PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C19Dh	MPC	PB5 pin function control register	PB5PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C19Eh	MPC	PB6 pin function control register	PB6PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C19Fh	MPC	PB7 pin function control register	PB7PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C1A0h	MPC	PC0 pin function control register	PC0PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C1A1h	MPC	PC1 pin function control register	PC1PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C1A2h	MPC	PC2 pin function control register	PC2PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C1A3h	MPC	PC3 pin function control register	PC3PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C1A4h	MPC	PC4 pin function control register	PC4PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C1A5h	MPC	PC5 pin function control register	PC5PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C1A6h	MPC	PC6 pin function control register	PC6PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C1A7h	MPC	PC7 pin function control register	PC7PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C1A8h	MPC	PD0 pin function control register	PD0PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C1A9h	MPC	PD1 pin function control register	PD1PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C1AAh	MPC	PD2 pin function control register	PD2PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C1ABh	MPC	PD3 pin function control register	PD3PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C1ACh	MPC	PD4 pin function control register	PD4PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C1ADh	MPC	PD5 pin function control register	PD5PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C1AEh	MPC	PD6 pin function control register	PD6PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C1AFh	MPC	PD7 pin function control register	PD7PFS	8	8	2, 3 PCLKB	2 ICLK



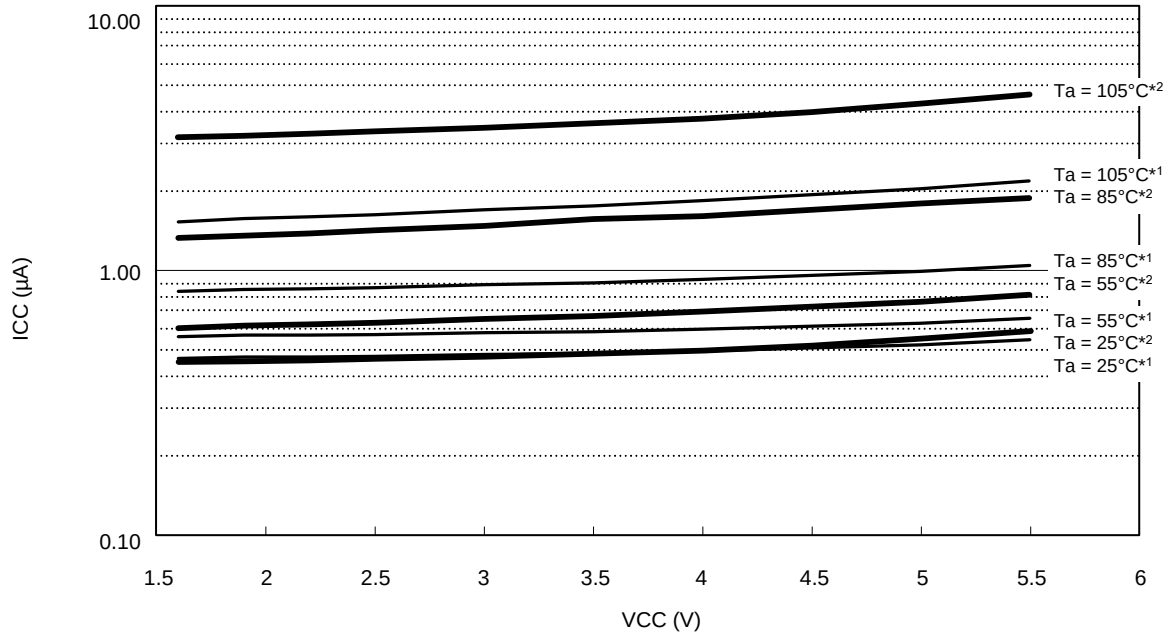
Note 1. All peripheral operation is normal. This does not include BGO operation.
Average value of the tested middle samples during product evaluation.
Note 2. All peripheral operation is maximum. This does not include BGO operation.
Average value of the tested upper-limit samples during product evaluation.

Figure 5.1 Voltage Dependency in High-Speed Operating Mode (Reference Data) for Chip Version A



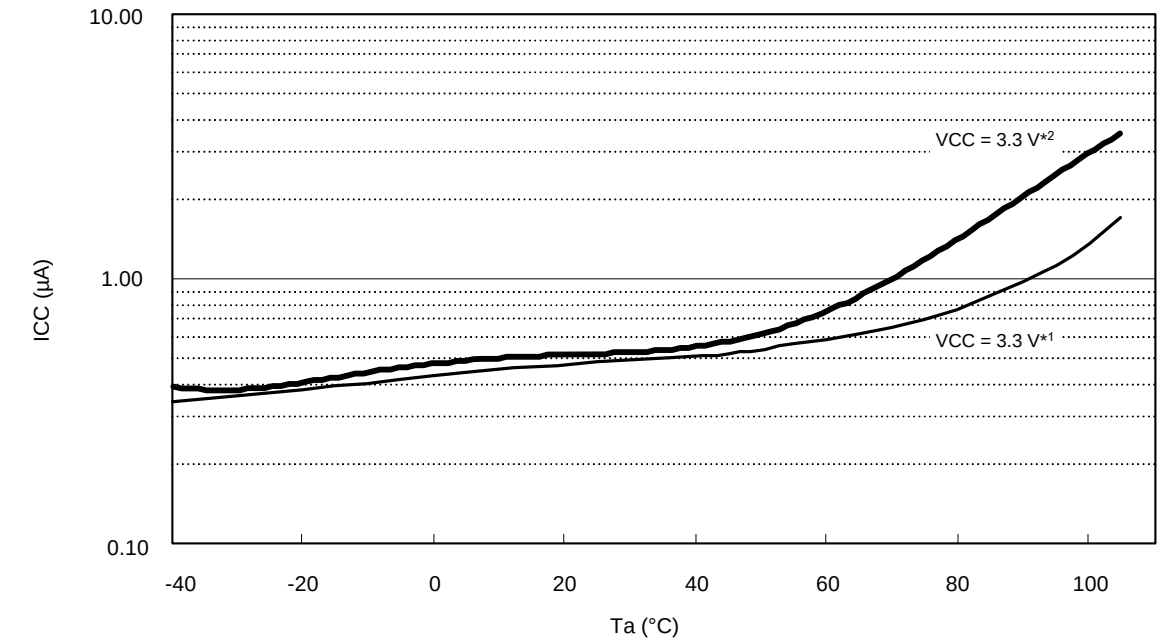
Note 1. All peripheral operation is normal. This does not include BGO operation.
Average value of the tested middle samples during product evaluation.
Note 2. All peripheral operation is maximum. This does not include BGO operation.
Average value of the tested upper-limit samples during product evaluation.

Figure 5.2 Voltage Dependency in Middle-Speed Operating Modes 1A and 1B (Reference Data) for Chip Version A



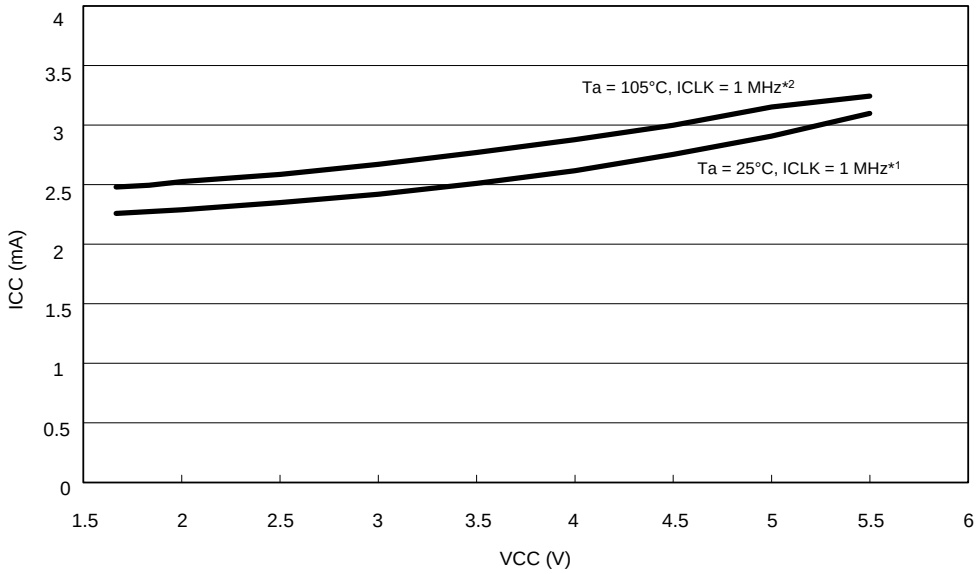
Note 1. Average value of the tested middle samples during product evaluation.
Note 2. Average value of the tested upper-limit samples during product evaluation.

Figure 5.7 Voltage Dependency in Deep Software Standby Mode (DEEPCUT1 Bit = 1) (Reference Data) for Chip Version A



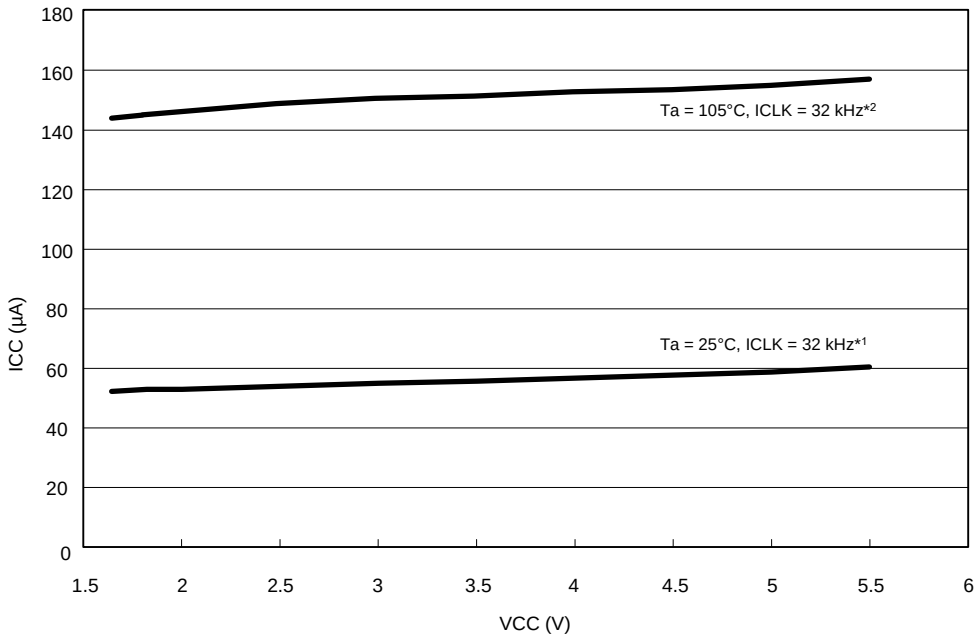
Note 1. Average value of the tested middle samples during product evaluation.
Note 2. Average value of the tested upper-limit samples during product evaluation.

Figure 5.8 Temperature Dependency in Deep Software Standby Mode (DEEPCUT1 Bit = 1) (Reference Data) for Chip Version A



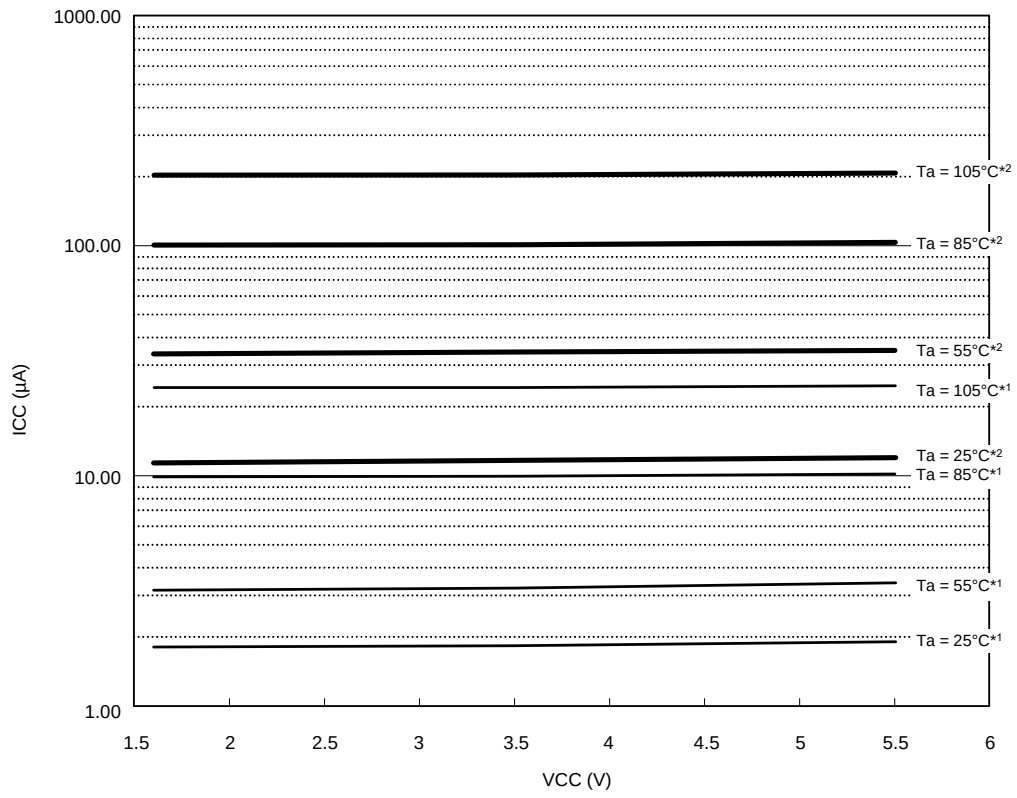
Note 1. All peripheral operation is normal.
Average value of the tested middle samples during product evaluation.
Note 2. All peripheral operation is maximum.
Average value of the tested upper-limit samples during product evaluation.

Figure 5.11 Voltage Dependency in Low-Speed Operating Mode 1 (Reference Data) for Chip Version C



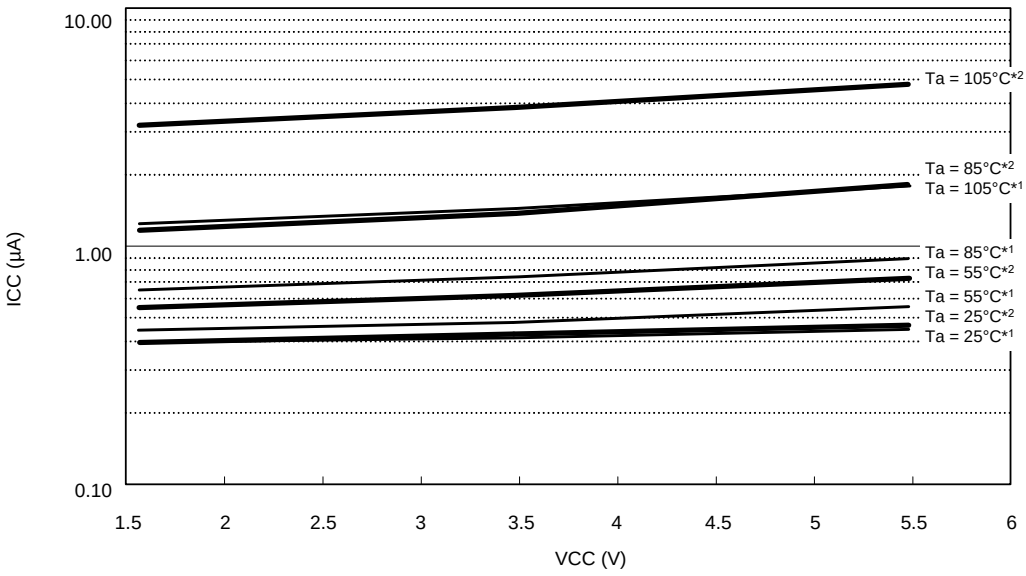
Note 1. All peripheral operation is normal.
Average value of the tested middle samples during product evaluation.
Note 2. All peripheral operation is maximum.
Average value of the tested upper-limit samples during product evaluation.

Figure 5.12 Voltage Dependency in Low-Speed Operating Mode 2 (Reference Data) for Chip Version C



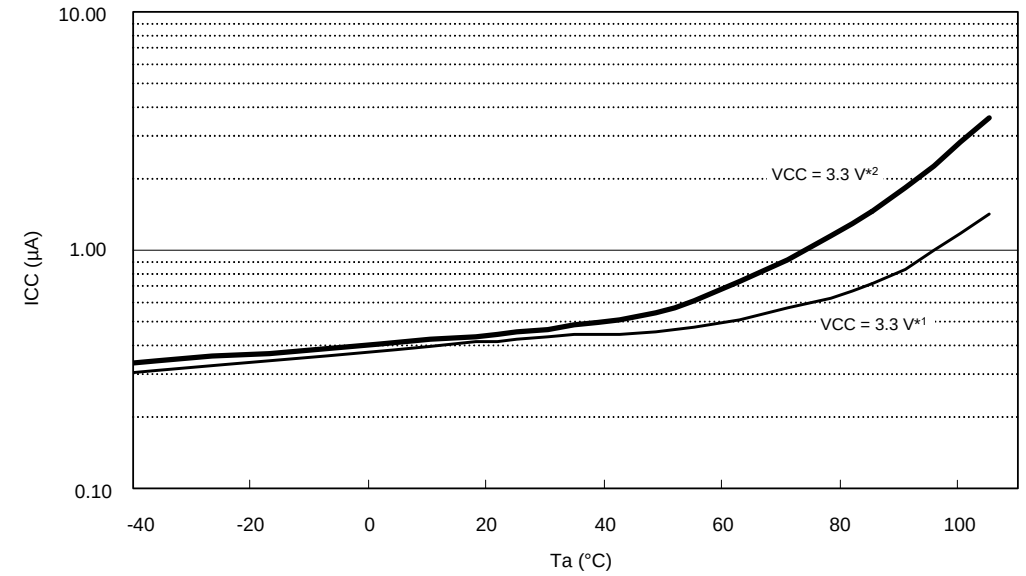
Note 1. Average value of the tested middle samples during product evaluation.
Note 2. Average value of the tested upper-limit samples during product evaluation.

Figure 5.31 Voltage Dependency in Software Standby Mode (SOFTCUT[2:0] Bits = 110b) (Reference Data) for Chip Version B with 768 Kbytes/1 Mbyte of Flash Memory and 100 to 145 Pins



Note 1. Average value of the tested middle samples during product evaluation.
Note 2. Average value of the tested upper-limit samples during product evaluation.

Figure 5.33 Voltage Dependency in Deep Software Standby Mode (DEEPCUT1 Bit = 1) (Reference Data) for Chip Version B with 768 Kbytes/1 Mbyte of Flash Memory and 100 to 145 Pins



Note 1. Average value of the tested middle samples during product evaluation.
Note 2. Average value of the tested upper-limit samples during product evaluation.

Figure 5.34 Temperature Dependency in Deep Software Standby Mode (DEEPCUT1 Bit = 1) (Reference Data) for Chip Version B with 768 Kbytes/1 Mbyte of Flash Memory and 100 to 145 Pins

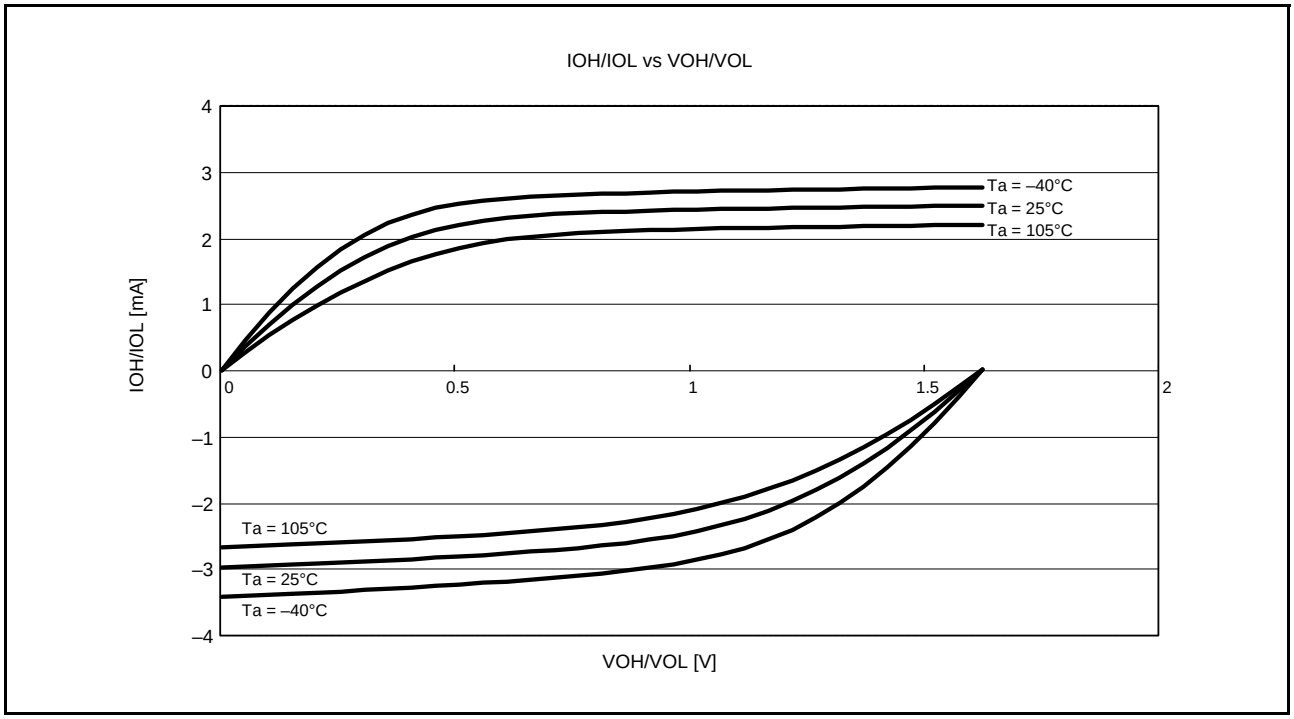


Figure 5.46 VOH/VOL and IOH/IOL Temperature Characteristics at VCC = 1.62 V when Normal Output is Selected (Reference Data)

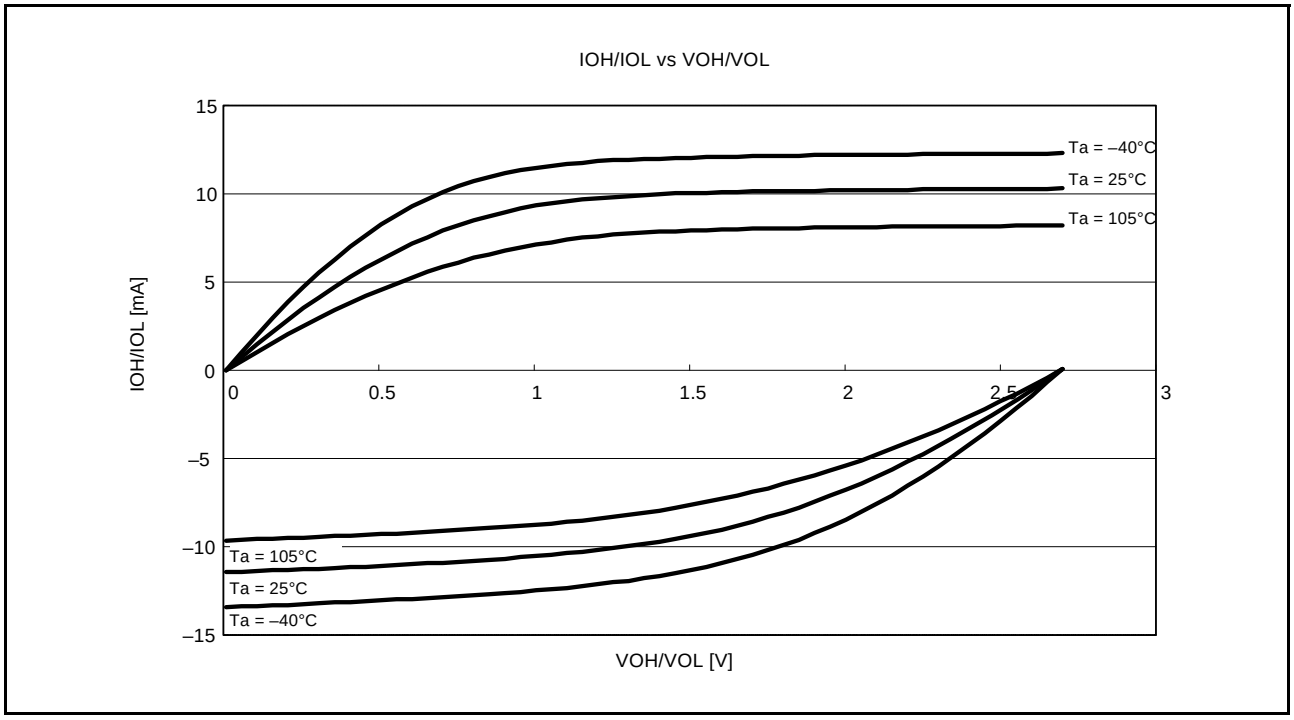


Figure 5.47 VOH/VOL and IOH/IOL Temperature Characteristics at VCC = 2.7 V when Normal Output is Selected (Reference Data)

5.2.3 RIIC Pin Output Characteristics

Figure 5.55 to Figure 5.58 show the output characteristics of the RIIC pin.

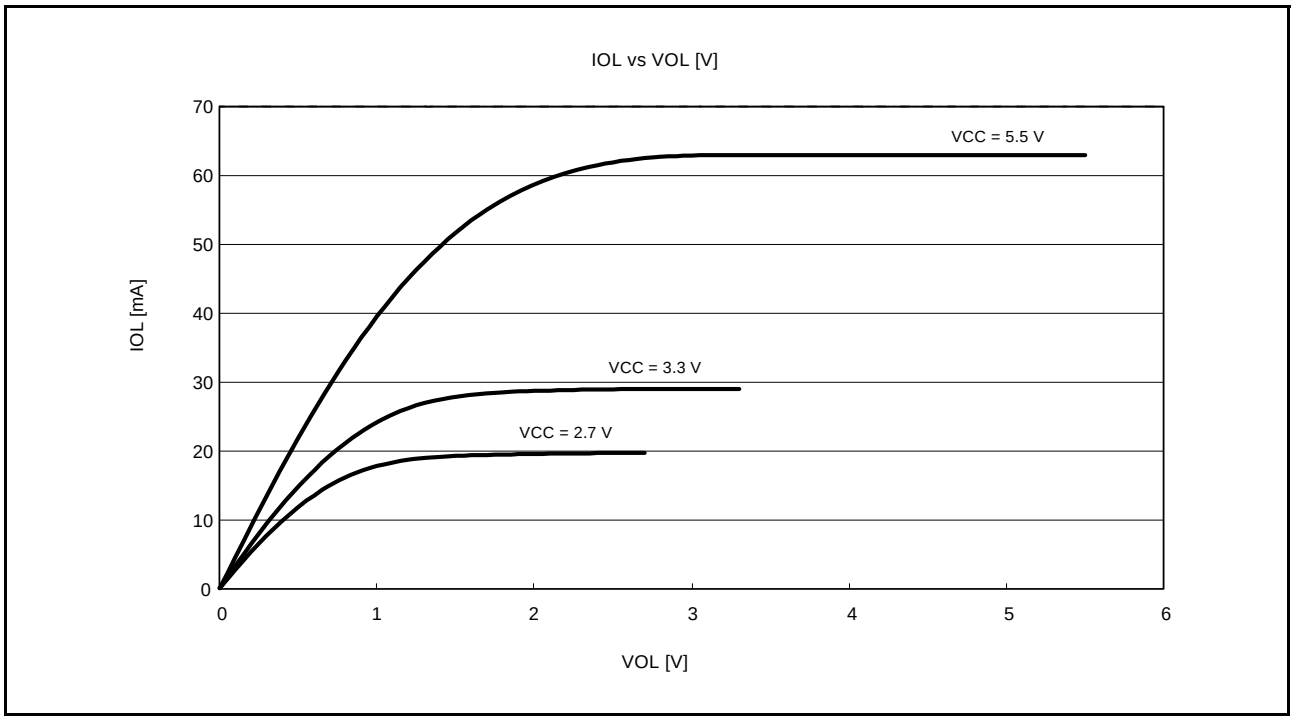


Figure 5.55 VOL and IOL Voltage Characteristics of RIIC Output Pin at Ta = 25°C (Reference Data)

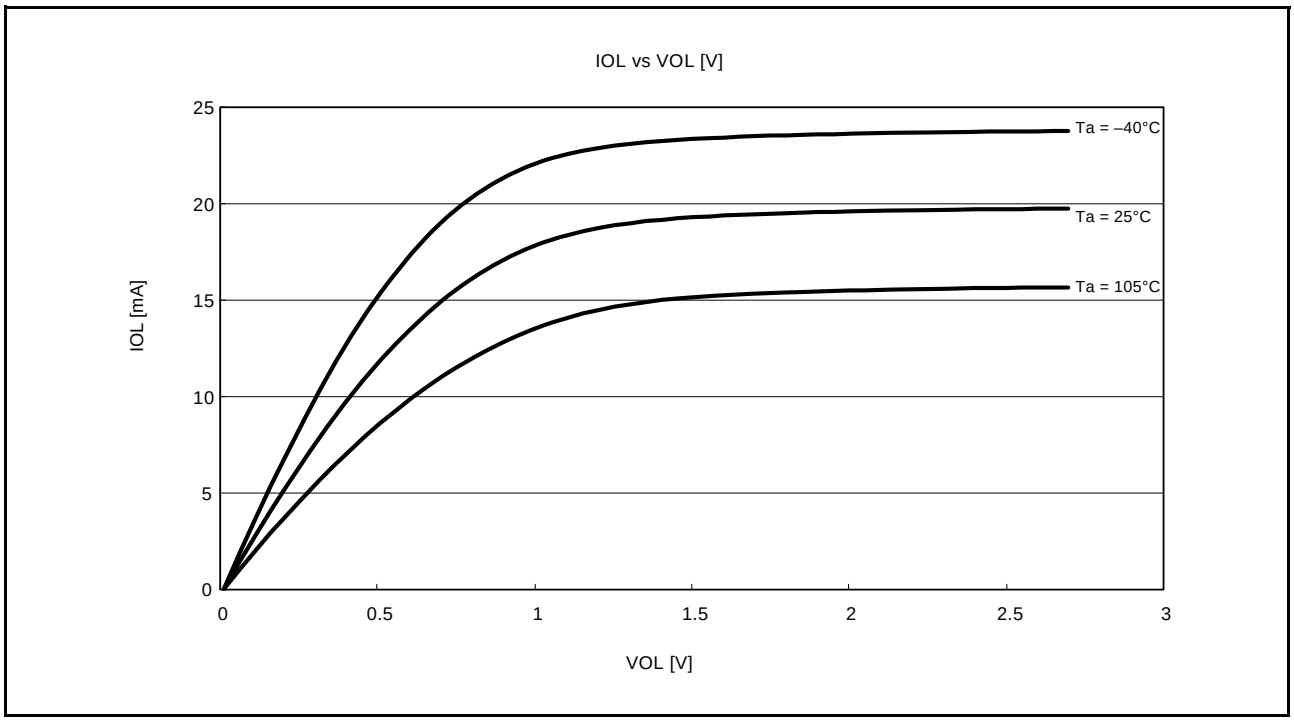


Figure 5.56 VOL and IOL Temperature Characteristics of RIIC Output Pin at VCC = 2.7 V (Reference Data)

5.3.1 Clock Timing

Table 5.41 BCLK Timing (1)

Conditions: VCC = AVCC0 = 2.7 to 5.5 V, VSS = AVSS0 = VREFL = VREFL0 = 0 V,
fBCLK = up to 25 MHz (BCLK pin output frequency = up to 12.5 MHz), T_a = –40 to +105°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
BCLK pin output cycle time	t_{Bcyc}	80	—	—	ns	Figure 5.59
BCLK pin output high pulse width*1	t_{CH}	20	—	—	ns	
BCLK pin output low pulse width*1	t_{CL}	20	—	—	ns	
BCLK pin output rising time	t_{Cr}	—	—	15	ns	
BCLK pin output falling time	t_{Cf}	—	—	15	ns	

Note 1. When the EXTAL external clock input is used with divided by 1 (SCKCR.BCK[3:0] bits = 0000b and BCKCR.BCLKDIV bit = 0) to output from the BCLK pin, the above should be satisfied with a duty cycle of 45 to 55%.

Table 5.42 BCLK Timing (2)

Conditions: VCC = AVCC0 = 1.8 to 2.7 V, VSS = AVSS0 = VREFL = VREFL0 = 0 V,
fBCLK = up to 16 MHz (BCLK pin output frequency= up to 8 MHz), T_a = –40 to +105°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
BCLK pin output cycle time	t_{Bcyc}	125	—	—	ns	Figure 5.59
BCLK pin output high pulse width*1	t_{CH}	30	—	—	ns	
BCLK pin output low pulse width*1	t_{CL}	30	—	—	ns	
BCLK pin output rising time	t_{Cr}	—	—	25	ns	
BCLK pin output falling time	t_{Cf}	—	—	25	ns	

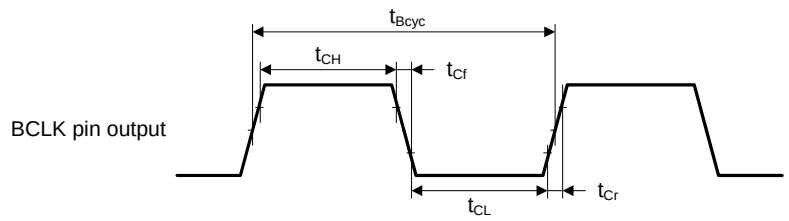
Note 1. When the EXTAL external clock input is used with divided by 1 (SCKCR.BCK[3:0] bits = 0000b and BCKCR.BCLKDIV bit = 0) to output from the BCLK pin, the above should be satisfied with a duty cycle of 45 to 55%.

Table 5.43 BCLK Timing (3)

Conditions: VCC = AVCC0 = 1.62 to 1.8 V, VSS = AVSS0 = VREFL=VREFL0 = 0 V,
fBCLK = up to 12 MHz (BCLK pin output frequency = up to 6 MHz), T_a = –40 to +105°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
BCLK pin output cycle time	t_{Bcyc}	166.6	—	—	ns	Figure 5.59
BCLK pin output high pulse width*1	t_{CH}	42	—	—	ns	
BCLK pin output low pulse width*1	t_{CL}	42	—	—	ns	
BCLK pin output rising time	t_{Cr}	—	—	35	ns	
BCLK pin output falling time	t_{Cf}	—	—	35	ns	

Note: • Set high driving ability for the output port pin to be used for the BCLK pin function.
Note 1. When the EXTAL external clock input is used with divided by 1 (SCKCR.BCK[3:0] bits = 0000b and BCKCR.BCLKDIV bit = 0) to output from the BCLK pin, the above should be satisfied with a duty cycle of 45 to 55%.



Test conditions: VOH = VCC × 0.7, VOL = VCC × 0.3, IOH = –1.0 mA, IOL = 1.0 mA, C = 30 pF

Figure 5.59 BCLK Pin Output Timing

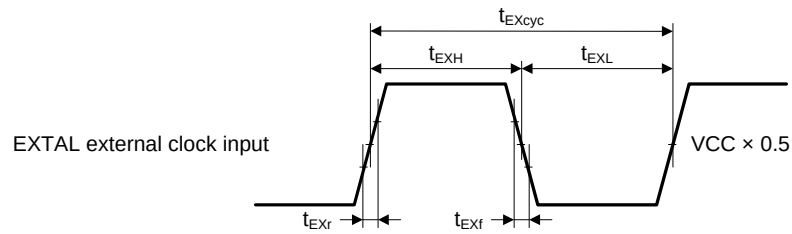


Figure 5.60 EXTAL External Clock Input Timing

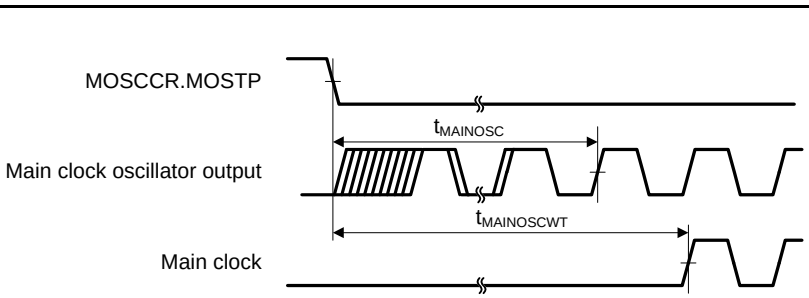


Figure 5.61 Main Clock Oscillation Start Timing

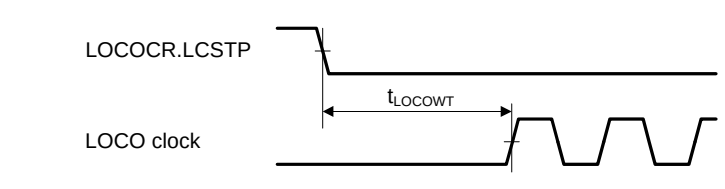


Figure 5.62 LOCO Clock Oscillation Start Timing

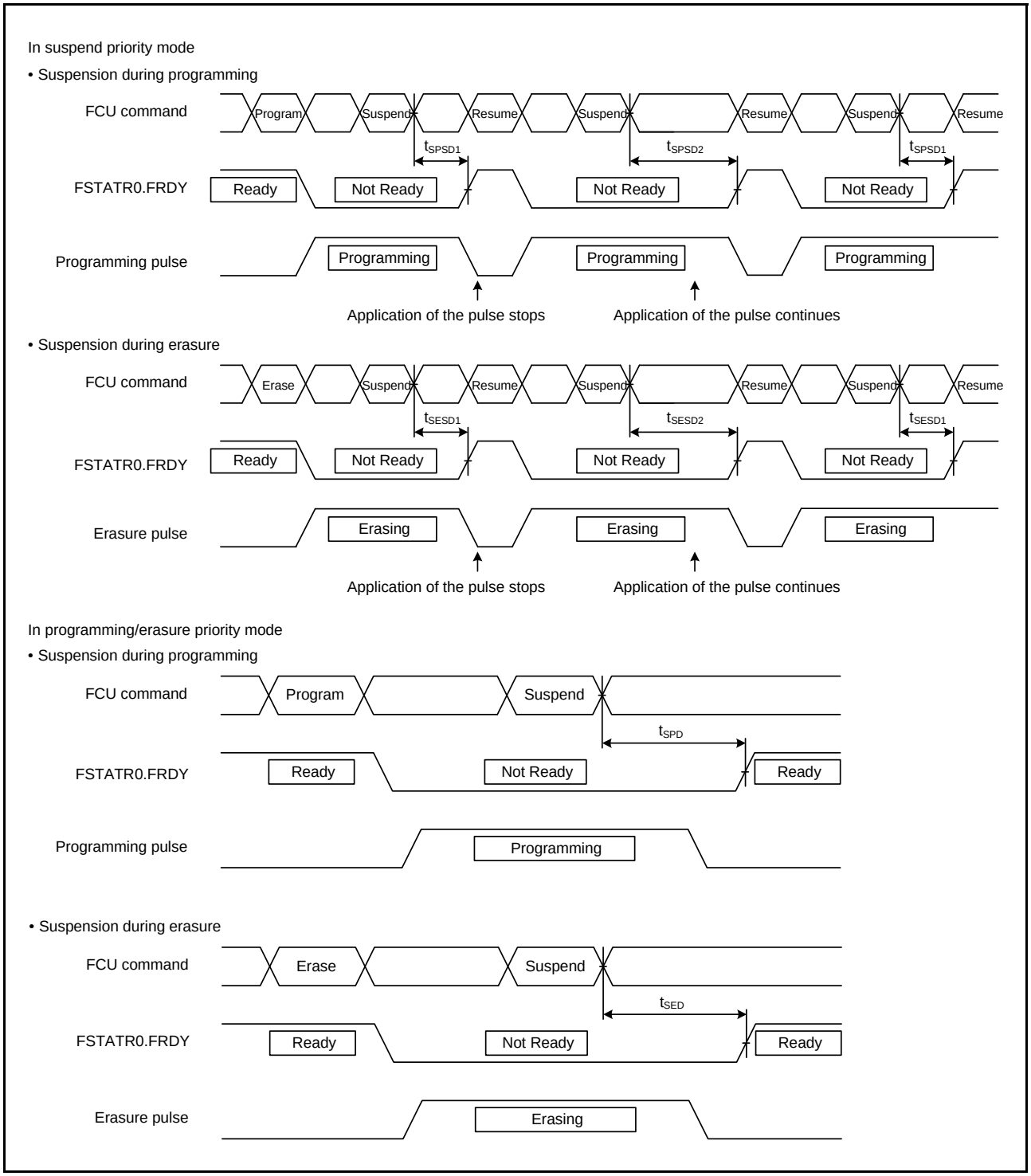
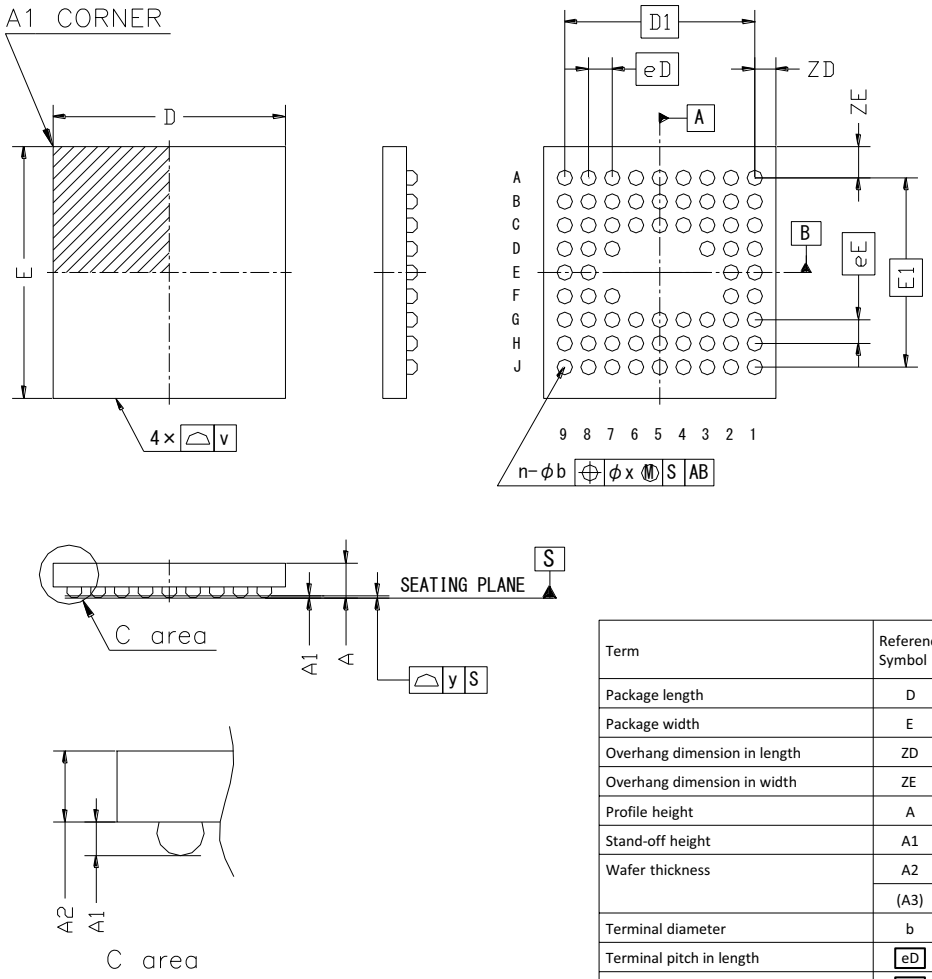


Figure 5.109 Flash Memory Program/Erase Suspend Timing

JEITA Package code	RENESAS Code	Previous Code	MASS(TYP.)[g]
S-WFBGA69-3.91x4.26-0.40	SWBG0069LA-A	—	0.02



注記:
1. 端子ﾋﾟｯﾁは端子中央部の位置で規定する。
2. ﾃﾞｰﾀﾑA及びBは、ﾎﾞｰﾙｸﾞﾘｯﾄﾞｾﾝﾀを称す。

Note:
1. Ball pitch dimension is specified with the center of balls.
2. Datum A and B are axes defined by the ball grid array, not by the PKG outline.

Dimensions in millimeters

Term	Reference Symbol	Specification		
		Min	Nom	Max
Package length	D	3.86	3.91	3.96
Package width	E	4.21	4.26	4.31
Overhang dimension in length	ZD	0.305	0.355	0.405
Overhang dimension in width	ZE	0.48	0.53	0.58
Profile height	A	—	—	0.70
Stand-off height	A1	0.15	0.19	0.23
Wafer thickness	A2	0.36	0.40	0.44
	(A3)	—	—	—
Terminal diameter	b	0.22	0.27	0.32
Terminal pitch in length	eD		0.4	(BSC)
Terminal pitch in width	eE		0.4	(BSC)
Center terminal position in D-direction	SD		—	(BSC)
Center terminal position in E-direction	SE		—	(BSC)
Edge ball center to center in D-direction	D1		3.2	(BSC)
Edge ball center to center in D-direction	E1		3.2	(BSC)
Number of terminals	n		69	
Tolerance of package lateral profile	v		0.05	
Positional tolerance of terminals	x		0.05	
Coplanarity	y		0.08	

Figure E 69-Pin WLBGA (SWBG0069LA-A)

REVISION HISTORY	RX210 Group Datasheet

Rev.	Date	Description	
		Page	Summary
0.50	Apr.15, 2011	—	First edition, issued
0.90	Aug.10, 2011	1. Overview	
		4	Table 1.1 Outline of Specifications: Power supply voltage/ Operating frequency, changed
		17, 21, 24, 26	Table 1.5 to Table 1.8 List of Pins and Pin Functions (Pin name: LVCMP2 → CMPA2), changed
		2. CPU	
		51	Table 2.14 Instructions that are Converted into Multiple Micro-Operations (multiplier: 32 × 32 → 64 bits), (memory source operand), added
		4. I/O Registers	
		63	Table 5.1 List of I/O Registers (Address Order), SOSCWTCR, LOCOWTCR2, HOCOWTCR2, added
		114 to 116	Table 5.1 List of I/O Registers (Address Order): Interrupt source priority register, changed
		5. Electrical Characteristics	
		85 to 137	Newly added
1.20	Nov 28, 2012	All	Information on chip versions A, B, and C, corresponding descriptions and notes, added 48-pin products added, PLQP0080JA-A 14 × 14 mm, 0.65-mm pitch, package deleted
		Features	
		1	Description changed
		1. Overview	
		2	1.1 Outline of Specifications: Description, changed
		2 to 5	Table 1.1 Outline of Specifications, changed Note 1, added
		6	Table 1.2 Comparison of Functions for Different Packages, changed
		7	Table 1.3 List of Products, changed
		8 to 10	Tables 1.4 to 1.7 List of Products, added
		11	Figure 1.1 How to Read the Product Part No., Memory Capacity, and Package Type: G item added
		12	Figure 1.2 Block Diagram, changed
		13	Table 1.8 Pin Functions: Power supply and On-chip emulator, changed
		13	Table 1.8 Pin Functions: Multiplexed bus, added
		18	Figure 1.4 Pin Assignments of the 100-Pin LQFP, changed
		21	Figure 1.7 Pin Assignments of the 48-Pin LQFP, added
		23	Table 1.9 List of Pins and Pin Functions (100-Pin TFLGA): Pin No. G4, changed
		25	Table 1.10 List of Pins and Pin Functions (100-Pin LQFP): Pin No. 21, changed
		28	Table 1.11 List of Pins and Pin Functions (80-Pin LQFP): Pin No. 19, changed
		30	Table 1.12 List of Pins and Pin Functions (64-Pin LQFP): Pin No. 15, changed
		3. Address Space	
		37	Figure 3.1 Memory Map in Each Operating Mode: Note 2, changed
		4. I/O Registers	
		41 to 63	Table 4.1 List of I/O Registers (Address Order): Number of Access, changed Voltage regulator control register, Timeout internal counter L, Timeout internal counter U, and PLL power control register, added
		63	Table 4.1 List of I/O Registers (Address Order): Notes 1 and 2, added
		—	Table 4.1 List of I/O Registers (Address Order): LOCO Wait Control Register 2 (LOCOWTCR2), deleted
		5. Electrical Characteristics	
		64 to 152	Description added
1.30	Jan 22, 2013	Features	
		1	On-chip flash memory for code, no wait states, On-chip SRAM, no wait states, Real-time clock, Up to 15 communications channels, Up to 20 extended-function timers, changed
		1.Overview	
		2 to 6	Table 1.1 Outline of Specifications, changed
		7	Table 1.2 Comparison of Functions for Different Packages, changed
		9	Table 1.4 List of Products Chip Version B: D Version (Ta = -40 to +85°C), changed
		10	Table 1.5 List of Products Chip Version B: G Version (Ta = -40 to +105°C), changed

Rev.	Date	Description	
		Page	Summary
1.40	Feb 19, 2013	96	Table 5.11 DC Characteristics (10), changed
		105	Table 5.14 DC Characteristics (13), changed
		114	Table 5.17 DC Characteristics (16), changed
		115	Figure 5.31 Voltage Dependency in Software Standby Mode (SOFTCUT[2:0] Bits = 110b) (Reference Data) for Chip Version B with 768 Kbytes/1 Mbyte of Flash Memory and 100 to 145 Pins, changed
		116	Figure 5.32 Temperature Dependency in Software Standby Mode (SOFTCUT[2:0] Bits = 110b) (Reference Data) for Chip Version B with 768 Kbytes/1 Mbyte of Flash Memory and 100 to 145 Pins, changed
		118	Table 5.18 DC Characteristics (17), changed
		119, 120	Table 5.19 DC Characteristics (18), changed
		121 to 123	Figure 5.35 Voltage Dependency in High-Speed Operating Mode (Reference Data) for Chip Version B with 512 Kbytes or Less of Flash Memory and 144 and 145 Pins to Figure 5.39 Voltage Dependency in Low-Speed Operating Mode 2 (Reference Data) for Chip Version B with 512 Kbytes or Less of Flash Memory and 144 and 145 Pins, added
		124	Table 5.20 DC Characteristics (19), changed
		125 to 127	Figure 5.40 Voltage Dependency in Software Standby Mode (SOFTCUT[2:0] Bits = 110b) (Reference Data) for Chip Version B with 512 Kbytes or Less of Flash Memory and 144 and 145 Pins to Figure 5.43 Temperature Dependency in Deep Software Standby Mode (DEEPCUT1 Bit = 1) (Reference Data) for Chip Version B with 512 Kbytes or Less of Flash Memory and 144 and 145 Pins, added
		128	Table 5.22 DC Characteristics (21), changed, Note 2 added
		144	Table 5.44 Clock Timing: Note 5, changed
		154	Table 5.49 Bus Timing (1), Table 5.50 Bus Timing (2), changed
		155	Table 5.51 Bus Timing (3), changed
		160	Table 5.52 Bus Timing (Multiplexed Bus) (1), Table 5.53 Bus Timing (Multiplexed Bus) (2), changed
		161	Table 5.54 Bus Timing (Multiplexed Bus) (3), changed
		164	Table 5.56 Timing of On-Chip Peripheral Modules (2), changed
		166	Table 5.57 Timing of On-Chip Peripheral Modules (3), changed
		177	Table 5.61 A/D Conversion Characteristics (1), Note 3, deleted Figure 5.99 AVCC to AVREFH Voltage Range, added
		179	Table 5.64 A/D Conversion Characteristics (2), Note 3, Table 5.65 A/D Conversion Characteristics (3), Note 3, deleted
		186	Table 5.72 Power-on Reset Circuit and Voltage Detection Circuit Characteristics (2), changed
1.50	Oct 18, 2013	All	69-Pin WLBGA package products, added
		Features	
		1	SWBG0069LA-A 3.91 × 4.26mm, 0.40-mm pitch, ■ Applications, added
		1. Overview	
		2	1.1 Outline of Specifications, changed
		2 to 6	Table 1.1 Outline of Specifications, Note 2, changed
		7	Table 1.2 Comparison of Functions for Different Packages, changed
		8	Table 1.3 List of Products Chip Version A: D Version (Ta = -40 to +85°C), changed, Note, added
		9	Table 1.4 List of Products Chip Version B: D Version (Ta = -40 to +85°C), Note 1, changed, Note added
		10	Table 1.5 List of Products Chip Version B: G Version (Ta = -40 to +105°C), Note, changed, Note 1, deleted
		11	Table 1.6 List of Products Chip Version C: D Version (Ta = -40 to +85°C), Table 1.7 List of Products Chip Version C: G Version (Ta = -40 to +105°C), Note, changed
		12	Figure 1.1 How to Read the Product Part No., Memory Capacity, and Package Type, changed
		23	Figure 1.8 Pin Assignments of the 69-Pin WLBGA, added
		43, 44	Table 1.14 List of Pins and Pin Functions (69-Pin WLBGA), added
		5. Electrical Characteristics	
		134	Table 5.21 DC Characteristics (20) Note, added
		149, 150	Table 5.44 Clock Timing Note 6, Note 7, added
		183	Table 5.61 A/D Conversion Characteristics (1) Note, changed, Note 4, deleted
		184	Table 5.62 Channel Classification for A/D Converter, changed
		185	Table 5.64 A/D Conversion Characteristics (2) Note, changed
		Appendix 1. Package Dimensions	
		211	Figure E 69-Pin WLBGA (SWBG0069LA-A), added