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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Discontinued at Digi-Key |
| Core Processor | RX |
| Core Size | 32-Bit Single-Core |
| Speed | 50MHz |
| Connectivity | I²C, SCI, SPI |
| Peripherals | DMA, LVD, POR, PWM, WDT |
| Number of I/O | 64 |
| Program Memory Size | 384KB (384K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | 8K x 8 |
| RAM Size | 64K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.62V ~ 5.5V |
| Data Converters | A/D 14x12b; D/A 2x10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 80-LQFP |
| Supplier Device Package | 80-LQFP (12x12) |
| Purchase URL | https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f52107cdfn-30 |

**Table 1.1 Outline of Specifications (4 / 5)**

| Classification | Module/Function | Description |
|---|---|---|
| Communication functions | Serial communications interfaces (SCIc, SCId) | • 13 channels (channel 0 to 11: SCIc, channel 12: SCId)<br>• Serial communications modes:<br>Asynchronous, clock synchronous, and smart-card interface<br>• On-chip baud rate generator allows selection of the desired bit rate<br>• Choice of LSB-first or MSB-first transfer<br>• Average transfer rate clock can be input from TMR timers (SCI5, SCI6, and SCI12)<br>• Simple IIC<br>• Simple SPI<br>• Master/slave mode supported (SCId only)<br>• Start frame and information frame are included (SCId only) |
| | $I^2C$ bus interface (RIIC) | • 1 channel<br>• Communications formats:<br>$I^2C$ bus format/SMBus format<br>• Master/slave selectable<br>• Supports the fast mode |
| | Serial peripheral interface (RSPI) | • 1 channel<br>• Transfer facility<br>Using the MOSI (master out, slave in), MISO (master in, slave out), SSL (slave select), and RSPI clock (RSPCK) signals enables serial transfer through SPI operation (four lines) or clock-synchronous operation (three lines)<br>• Capable of handling serial transfer as a master or slave<br>• Data formats<br>• Choice of LSB-first or MSB-first transfer<br>The number of bits in each transfer can be changed to any number of bits from 8 to 16, 20, 24, or 32 bits.<br>128-bit buffers for transmission and reception<br>Up to four frames can be transmitted or received in a single transfer operation (with each frame having up to 32 bits)<br>• Double buffers for both transmission and reception |
| 12-bit A/D converter (S12ADb) | | • 12 bits (16 channels × 1 unit)<br>• 12-bit resolution<br>• Minimum conversion time: 1.0 μs per channel (in operation with ADCLK at 50 MHz)<br>• Operating modes<br>Scan mode (single scan mode, continuous scan mode, and group scan mode)<br>• Sample-and-hold function<br>• Self-diagnosis for the A/D converter<br>• Assistance in detecting disconnected analog inputs<br>• Double-trigger mode (duplication of A/D conversion data)<br>• A/D conversion start conditions<br>A software trigger, a trigger from a timer (MTU), an external trigger signal, or ELC |
| Temperature sensor (TEMPSa) | | • Outputs the voltage that changes depending on the temperature<br>• PGA gain switchable: Four levels according to the voltage range |
| D/A converter (DA) | | • 2 channels<br>• 10-bit resolution<br>• Output voltage: 0 V to VREFH |
| CRC calculator (CRC) | | • CRC code generation for arbitrary amounts of data in 8-bit units<br>• Select any of three generating polynomials:<br>$X^8 + X^2 + X + 1$, $X^{16} + X^{15} + X^2 + 1$, or $X^{16} + X^{12} + X^5 + 1$<br>• Generation of CRC codes for use with LSB-first or MSB-first communications is selectable. |
| Comparator A (CMPA) | | • 2 channels<br>• Comparison of reference voltage and analog input voltage |
| Comparator B (CMPB) | | • 2 channels<br>• Comparison of reference voltage and analog input voltage |
| Data Operation Circuit (DOC) | | Comparison, addition, and subtraction of 16-bit data |
| Power supply voltage/Operating frequency | | VCC = 1.62 to 1.8 V: 20 MHz, VCC = 1.8 to 2.7 V: 32 MHz, VCC = 2.7 to 5.5 V: 50 MHz |
| Operating temperature | | D version: −40 to +85°C, G version: −40 to +105°C*2 |

**Table 1.1 Outline of Specifications (5 / 5)**

| Classification | Module/Function | Description |
|---|---|---|
| Packages | Chip version A | 100-pin TFLGA (PTLG0100JA-A) 7 × 7 mm, 0.65-mm pitch<br>100-pin LQFP (PLQP0100KB-A) 14 × 14 mm, 0.5-mm pitch<br>80-pin LQFP (PLQP0080KB-A) 12 × 12 mm, 0.5-mm pitch<br>64-pin LQFP (PLQP0064KB-A) 10 × 10 mm, 0.5-mm pitch |
| | Chip version B | 145-pin TFLGA (PTLG0145KA-A) 7 × 7 mm, 0.5-mm pitch<br>100-pin TFLGA (PTLG0100JA-A) 7 × 7 mm, 0.65-mm pitch<br>100-pin TFLGA (PTLG0100KA-A) 5.5 × 5.5 mm, 0.5-mm pitch<br>64-pin TFLGA (PTLG0064JA-A) 6 × 6 mm, 0.65-mm pitch<br>144-pin LQFP (PLQP0144KA-A) 20 × 20 mm, 0.5-mm pitch<br>100-pin LQFP (PLQP0100KB-A) 14 × 14 mm, 0.5-mm pitch<br>80-pin LQFP (PLQP0080KB-A) 12 × 12 mm, 0.5-mm pitch<br>80-pin LQFP (PLQP0080JA-A) 14 × 14 mm, 0.65-mm pitch<br>64-pin LQFP (PLQP0064KB-A) 10 × 10 mm, 0.5-mm pitch<br>64-pin LQFP (PLQP0064GA-A) 14 × 14 mm, 0.8-mm pitch<br>48-pin LQFP (PLQP0048KB-A) 7 × 7 mm, 0.5-mm pitch<br>69-pin WLBGA (SWBG0069LA-A) 3.91 × 4.26mm, 0.40-mm pitch |
| | Chip version C | 100-pin TFLGA (PTLG0100JA-A) 7 × 7 mm, 0.65-mm pitch<br>100-pin LQFP (PLQP0100KB-A) 14 × 14 mm, 0.5-mm pitch<br>80-pin LQFP (PLQP0080KB-A) 12 × 12 mm, 0.5-mm pitch<br>80-pin LQFP (PLQP0080JA-A) 14 × 14 mm, 0.65-mm pitch<br>64-pin LQFP (PLQP0064KB-A) 10 × 10 mm, 0.5-mm pitch<br>64-pin LQFP (PLQP0064GA-A) 14 × 14 mm, 0.8-mm pitch |
| On-chip debugging system | | E1 emulator (FINE interface) |

Note 1. In chip version A of the part numbers below, port P17 is not 5 V tolerant. Therefore there is only one port in these products.
R5F52108ADFM, R5F52107ADFM, R5F52106ADFM, and R5F52105ADFM

Note 2. Please contact Renesas Electronics sales office for derating of operation under Ta = +85°C to +105°C. Derating is the systematic reduction of load for the sake of improved reliability.

**Table 1.8 Pin Functions (4 / 4)**

| Classifications | Pin Name | I/O | Description |
|---|---|---|---|
| Analog power supply | AVCC0 | Input | Analog voltage supply pin for the 12-bit A/D converter. Connect this pin to VCC if the 12-bit A/D converter is not to be used. |
| | AVSS0 | Input | Analog ground pin for the 12-bit A/D converter. Connect this pin to VSS if the 12-bit A/D converter is not to be used. |
| | VREFH0 | Input | Analog reference voltage supply pin for the 12-bit A/D converter. Connect this pin to VCC if the 12-bit A/D converter is not to be used. |
| | VREFL0 | Input | Analog reference ground pin for the 12-bit A/D converter. Connect this pin to VSS if the 12-bit A/D converter is not to be used. |
| | VREFH | Input | Analog voltage supply pin for the D/A converter. Connect this pin to VCC if the D/A converter is not to be used. |
| | VREFL | Input | Analog ground pin for the D/A converter. Connect this pin to VSS if the D/A converter is not to be used. |
| I/O ports | P00 to P03, P05, P07 | I/O | 6-bit input/output pins. |
| | P12 to P17 | I/O | 6-bit input/output pins. |
| | P20 to P27 | I/O | 8-bit input/output pins. |
| | P30 to P37 | I/O | 8-bit input/output pins. (P35 input pin) |
| | P40 to P47 | I/O | 8-bit input/output pins. |
| | P50 to P56 | I/O | 7-bit input/output pins. |
| | P60 to P67 | I/O | 8-bit input/output pins. |
| | P70 to P77 | I/O | 8-bit input/output pins. |
| | P80 to P83, P86, P87 | I/O | 6-bit input/output pins. |
| | P90 to P93 | I/O | 4-bit input/output pins. |
| | PA0 to PA7 | I/O | 8-bit input/output pins. |
| | PB0 to PB7 | I/O | 8-bit input/output pins. |
| | PC0 to PC7 | I/O | 8-bit input/output pins. |
| | PD0 to PD7 | I/O | 8-bit input/output pins. |
| | PE0 to PE7 | I/O | 8-bit input/output pins. |
| | PF5 | I/O | 1-bit input/output pin. |
| | PH0 to PH3 | I/O | 4-bit input/output pins. |
| | PJ1, PJ3, PJ5 | I/O | 3-bit input/output pins. |
| | PK2 to PK5 | I/O | 4-bit input/output pins. |
| | PL0, PL1 | I/O | 2-bit input/output pins. |

**Table 1.15 List of Pins and Pin Functions (64-Pin TFLGA) (2 / 2)**

| Pin No. | Power Supply, Clock, System Control | I/O Port | Timers (MTU, TMR, POE) | Communication (SCIc, SCId, RSPI, RIIC) | Others |
|---|---|---|---|---|---|
| F5 | | P15 | MTIOC0B/MTCLKB/TMCI2 | RXD1/SMISO1/SSCL1 | IRQ5 |
| F6 | | PB1 | MTIOC0C/MTIOC4C/TMCI0 | TXD6/SMOSI6/SSDA6 | IRQ4-DS |
| F7 | | PB5 | MTIOC2A/MTIOC1B/TMRI1/ POE1# | SCK9 | |
| F8 | | PB3 | MTIOC0A/MTIOC4A/TMO0/ POE3# | SCK6 | |
| G1 | EXTAL | P36 | | | |
| G2 | | P26 | MTIOC2A/TMO1 | TXD1/SMOSI1/SSDA1 | |
| G3 | | PH3 | TMCI0 | | |
| G4 | | PH0 | | | CACREF |
| G5 | | PC7 | MTIOC3A/TMO2/MTCLKB | TXD8/SMOSI8/SSDA8/MISOA | CACREF |
| G6 | | PC6 | MTIOC3C/MTCLKA/TMCI2 | RXD8/SMISO8/SSCL8/MOSIA | |
| G7 | | PC3 | MTIOC4D | TXD5/SMOSI5/SSDA5 | |
| G8 | | PB6 | MTIOC3D | RXD9/SMISO9/SSCL9 | |
| H1 | XTAL | P37 | | | |
| H2 | | P17 | MTIOC3A/MTIOC3B/TMO1/ POE8# | SCK1/MISOA/SDA-DS | IRQ7 |
| H3 | | PH2 | TMRI0 | | IRQ1 |
| H4 | | PH1 | TMO0 | | IRQ0 |
| H5 | | P55 | MTIOC4D/TMO3 | | |
| H6 | | P54 | MTIOC4B/TMCI1 | | |
| H7 | | PC2 | MTIOC4B | RXD5/SMISO5/SSCL5/SSLA3 | |
| H8 | | PB7 | MTIOC3B | TXD9/SMOSI9/SSDA9 | |

Note: • Pin names to which -DS is appended are for pins that can be used to trigger release from deep software standby mode.

## 2.1 General-Purpose Registers (R0 to R15)

This CPU has sixteen general-purpose registers (R0 to R15). R1 to R15 can be used as data registers or address registers. R0, a general-purpose register, also functions as the stack pointer (SP). The stack pointer is switched to operate as the interrupt stack pointer (ISP) or user stack pointer (USP) by the value of the stack pointer select bit (U) in the processor status word (PSW).

## 2.2 Control Registers

### (1) Interrupt Stack Pointer (ISP)/User Stack Pointer (USP)

The stack pointer (SP) can be either of two types, the interrupt stack pointer (ISP) or the user stack pointer (USP). Whether the stack pointer operates as the ISP or USP depends on the value of the stack pointer select bit (U) in the processor status word (PSW).
Set the ISP or USP to a multiple of four, as this reduces the numbers of cycles required to execute interrupt sequences and instructions entailing stack manipulation.

### (2) Interrupt Table Register (INTB)

The interrupt table register (INTB) specifies the address where the relocatable vector table starts.

### (3) Program Counter (PC)

The program counter (PC) indicates the address of the instruction being executed.

### (4) Processor Status Word (PSW)

The processor status word (PSW) indicates the results of instruction execution or the state of the CPU.

### (5) Backup PC (BPC)

The backup PC (BPC) is provided to speed up response to interrupts.
After a fast interrupt has been generated, the contents of the program counter (PC) are saved in the BPC register.

### (6) Backup PSW (BPSW)

The backup PSW (BPSW) is provided to speed up response to interrupts.
After a fast interrupt has been generated, the contents of the processor status word (PSW) are saved in the BPSW. The allocation of bits in the BPSW corresponds to that in the PSW.

### (7) Fast Interrupt Vector Register (FINTV)

The fast interrupt vector register (FINTV) is provided to speed up response to interrupts.
The FINTV register specifies a branch destination address when a fast interrupt has been generated.

## 2.3 Register Associated with DSP Instructions

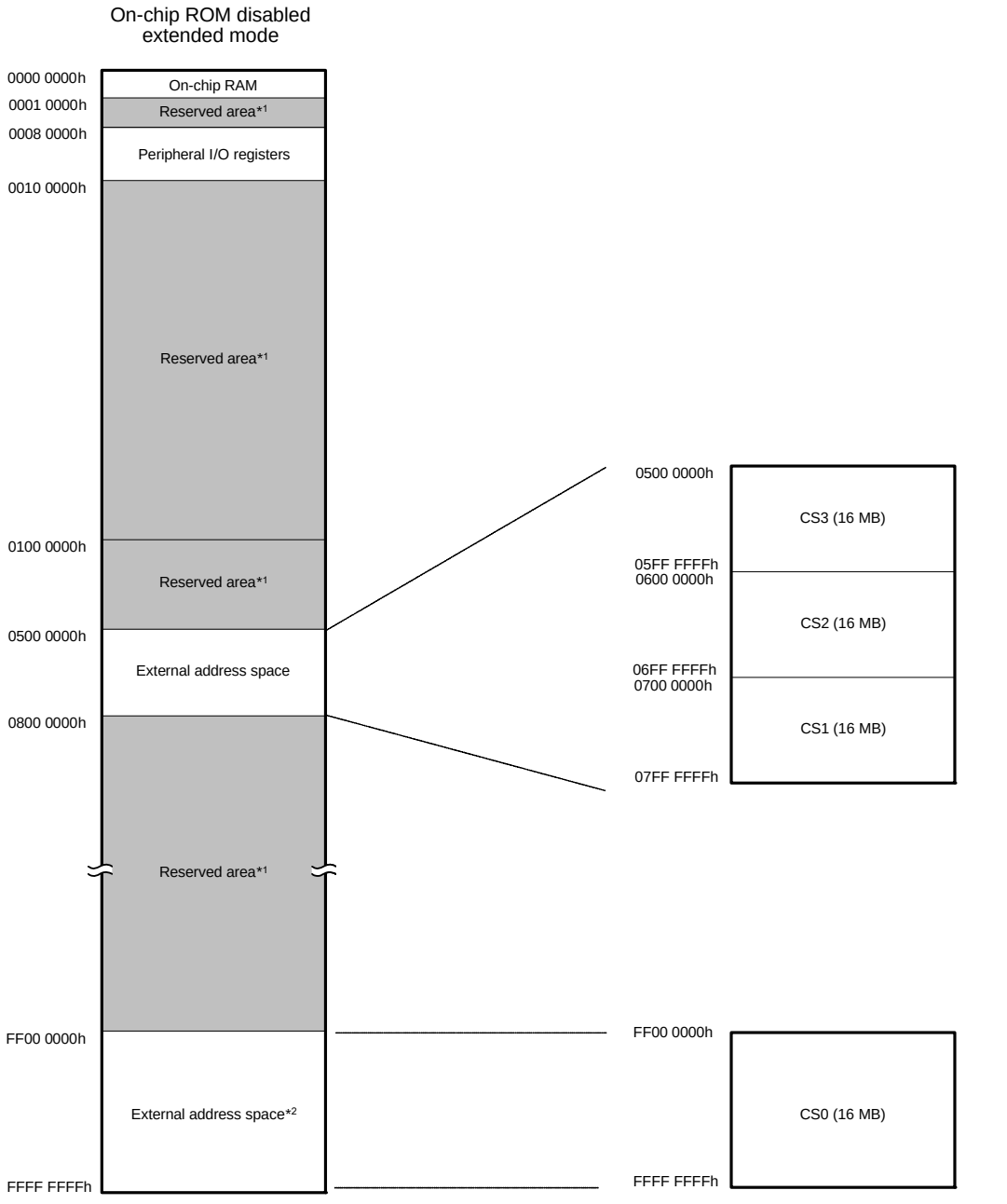
### (1) Accumulator (ACC)

The accumulator (ACC) is a 64-bit register used for DSP instructions. The accumulator is also used for the multiply and multiply-and-accumulate instructions; EMUL, EMULU, MUL, and RMPA, in which case the prior value in the accumulator is modified by execution of the instruction.
Use the MVTACHI and MVTACLO instructions for writing to the accumulator. The MVTACHI and MVTACLO instructions write data to the higher-order 32 bits (bits 63 to 32) and the lower-order 32 bits (bits 31 to 0), respectively.
Use the MVFACHI and MVFACMI instructions for reading data from the accumulator. The MVFACHI and MVFACMI instructions read data from the higher-order 32 bits (bits 63 to 32) and the middle 32 bits (bits 47 to 16), respectively.

## 3.2 External Address Space

The external address space is divided into up to four CS areas (CS0 to CS3), each corresponding to the CSn# signal output from a CSn# (n = 0 to 3) pin.

Figure 3.2 shows the address ranges corresponding to the individual CS areas (CS0 to CS3) in on-chip ROM disabled extended mode.




Note 1. Reserved areas should not be accessed.

Note 2. The CS0 area is disabled in on-chip ROM enabled extended mode. In this mode, the address space for addresses above 0800 0000h is as shown in figure on this section “Memory Map in Each Operating Mode”.

**Figure 3.2 Correspondence between External Address Spaces and CS Areas (In On-Chip ROM Disabled Extended Mode)**

**Table 4.1 List of I/O Registers (Address Order) (2 / 29)**

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles ICLK ≥ PCLK | Number of Access Cycles ICLK < PCLK |
|---|---|---|---|---|---|---|---|
| 0008 201Dh | DMAC0 | DMA software start register | DMREQ | 8 | 8 | 2 ICLK | |
| 0008 201Eh | DMAC0 | DMA status register | DMSTS | 8 | 8 | 2 ICLK | |
| 0008 201Fh | DMAC0 | DMA activation source flag control register | DMCSL | 8 | 8 | 2 ICLK | |
| 0008 2040h | DMAC1 | DMA source address register | DMSAR | 32 | 32 | 2 ICLK | |
| 0008 2044h | DMAC1 | DMA destination address register | DMDAR | 32 | 32 | 2 ICLK | |
| 0008 2048h | DMAC1 | DMA transfer count register | DMCRA | 32 | 32 | 2 ICLK | |
| 0008 204Ch | DMAC1 | DMA block transfer count register | DMCRB | 16 | 16 | 2 ICLK | |
| 0008 2050h | DMAC1 | DMA transfer mode register | DMTMD | 16 | 16 | 2 ICLK | |
| 0008 2053h | DMAC1 | DMA interrupt setting register | DMINT | 8 | 8 | 2 ICLK | |
| 0008 2054h | DMAC1 | DMA address mode register | DMAMD | 16 | 16 | 2 ICLK | |
| 0008 205Ch | DMAC1 | DMA transfer enable register | DMCNT | 8 | 8 | 2 ICLK | |
| 0008 205Dh | DMAC1 | DMA software start register | DMREQ | 8 | 8 | 2 ICLK | |
| 0008 205Eh | DMAC1 | DMA status register | DMSTS | 8 | 8 | 2 ICLK | |
| 0008 205Fh | DMAC1 | DMA activation source flag control register | DMCSL | 8 | 8 | 2 ICLK | |
| 0008 2080h | DMAC2 | DMA source address register | DMSAR | 32 | 32 | 2 ICLK | |
| 0008 2084h | DMAC2 | DMA destination address register | DMDAR | 32 | 32 | 2 ICLK | |
| 0008 2088h | DMAC2 | DMA transfer count register | DMCRA | 32 | 32 | 2 ICLK | |
| 0008 208Ch | DMAC2 | DMA block transfer count register | DMCRB | 16 | 16 | 2 ICLK | |
| 0008 2090h | DMAC2 | DMA transfer mode register | DMTMD | 16 | 16 | 2 ICLK | |
| 0008 2093h | DMAC2 | DMA interrupt setting register | DMINT | 8 | 8 | 2 ICLK | |
| 0008 2094h | DMAC2 | DMA address mode register | DMAMD | 16 | 16 | 2 ICLK | |
| 0008 209Ch | DMAC2 | DMA transfer enable register | DMCNT | 8 | 8 | 2 ICLK | |
| 0008 209Dh | DMAC2 | DMA software start register | DMREQ | 8 | 8 | 2 ICLK | |
| 0008 209Eh | DMAC2 | DMA status register | DMSTS | 8 | 8 | 2 ICLK | |
| 0008 209Fh | DMAC2 | DMA activation source flag control register | DMCSL | 8 | 8 | 2 ICLK | |
| 0008 20C0h | DMAC3 | DMA source address register | DMSAR | 32 | 32 | 2 ICLK | |
| 0008 20C4h | DMAC3 | DMA destination address register | DMDAR | 32 | 32 | 2 ICLK | |
| 0008 20C8h | DMAC3 | DMA transfer count register | DMCRA | 32 | 32 | 2 ICLK | |
| 0008 20CCh | DMAC3 | DMA block transfer count register | DMCRB | 16 | 16 | 2 ICLK | |
| 0008 20D0h | DMAC3 | DMA transfer mode register | DMTMD | 16 | 16 | 2 ICLK | |
| 0008 20D3h | DMAC3 | DMA interrupt setting register | DMINT | 8 | 8 | 2 ICLK | |
| 0008 20D4h | DMAC3 | DMA address mode register | DMAMD | 16 | 16 | 2 ICLK | |
| 0008 20DCh | DMAC3 | DMA transfer enable register | DMCNT | 8 | 8 | 2 ICLK | |
| 0008 20DDh | DMAC3 | DMA software start register | DMREQ | 8 | 8 | 2 ICLK | |
| 0008 20DEh | DMAC3 | DMA status register | DMSTS | 8 | 8 | 2 ICLK | |
| 0008 20DFh | DMAC3 | DMA activation source flag control register | DMCSL | 8 | 8 | 2 ICLK | |
| 0008 2200h | DMAC | DMA module activation register | DMAST | 8 | 8 | 2 ICLK | |
| 0008 2400h | DTC | DTC control register | DTCCR | 8 | 8 | 2 ICLK | |
| 0008 2404h | DTC | DTC vector base register | DTCVBR | 32 | 32 | 2 ICLK | |
| 0008 2408h | DTC | DTC address mode register | DTCADMOD | 8 | 8 | 2 ICLK | |
| 0008 240Ch | DTC | DTC module start register | DTCST | 8 | 8 | 2 ICLK | |
| 0008 240Eh | DTC | DTC status register | DTCSTS | 16 | 16 | 2 ICLK | |
| 0008 3002h | BSC | CS0 mode register | CS0MOD | 16 | 16 | 1, 2 BCLK | |
| 0008 3004h | BSC | CS0 wait control register 1 | CS0WCR1 | 32 | 32 | 1, 2 BCLK | |
| 0008 3008h | BSC | CS0 wait control register 2 | CS0WCR2 | 32 | 32 | 1, 2 BCLK | |
| 0008 3012h | BSC | CS1 mode register | CS1MOD | 16 | 16 | 1, 2 BCLK | |
| 0008 3014h | BSC | CS1 wait control register 1 | CS1WCR1 | 32 | 32 | 1, 2 BCLK | |
| 0008 3018h | BSC | CS1 wait control register 2 | CS1WCR2 | 32 | 32 | 1, 2 BCLK | |
| 0008 3022h | BSC | CS2 mode register | CS2MOD | 16 | 16 | 1, 2 BCLK | |
| 0008 3024h | BSC | CS2 wait control register 1 | CS2WCR1 | 32 | 32 | 1, 2 BCLK | |
| 0008 3028h | BSC | CS2 wait control register 2 | CS2WCR2 | 32 | 32 | 1, 2 BCLK | |

**Table 4.1 List of I/O Registers (Address Order) (24 / 29)**

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles: ICLK ≥ PCLK | Number of Access Cycles: ICLK < PCLK |
|---|---|---|---|---|---|---|---|
| 0008 C04Ch | PORTC | Port input data register | PIDR | 8 | 8 | 3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing | 3 ICLK cycles when reading, 2 ICLK cycles when writing |
| 0008 C04Dh | PORTD | Port input data register | PIDR | 8 | 8 | 3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing | 3 ICLK cycles when reading, 2 ICLK cycles when writing |
| 0008 C04Eh | PORTE | Port input data register | PIDR | 8 | 8 | 3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing | 3 ICLK cycles when reading, 2 ICLK cycles when writing |
| 0008 C04Fh | PORTF | Port input data register | PIDR | 8 | 8 | 3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing | 3 ICLK cycles when reading, 2 ICLK cycles when writing |
| 0008 C051h | PORTH | Port input data register | PIDR | 8 | 8 | 3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing | 3 ICLK cycles when reading, 2 ICLK cycles when writing |
| 0008 C052h | PORTJ | Port input data register | PIDR | 8 | 8 | 3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing | 3 ICLK cycles when reading, 2 ICLK cycles when writing |
| 0008 C053h | PORTK | Port input data register | PIDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 C054h | PORTL | Port input data register | PIDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 C060h | PORT0 | Port mode register | PMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 C061h | PORT1 | Port mode register | PMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 C062h | PORT2 | Port mode register | PMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 C063h | PORT3 | Port mode register | PMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 C064h | PORT4 | Port mode register | PMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 C065h | PORT5 | Port mode register | PMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 C066h | PORT6 | Port mode register | PMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 C067h | PORT7 | Port mode register | PMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 C068h | PORT8 | Port mode register | PMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 C069h | PORT9 | Port mode register | PMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 C06Ah | PORTA | Port mode register | PMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 C06Bh | PORTB | Port mode register | PMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 C06Ch | PORTC | Port mode register | PMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 C06Dh | PORTD | Port mode register | PMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 C06Eh | PORTE | Port mode register | PMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 C06Fh | PORTF | Port mode register | PMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 C071h | PORTH | Port mode register | PMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 C072h | PORTJ | Port mode register | PMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 C073h | PORTK | Port mode register | PMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 C074h | PORTL | Port mode register | PMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |

[Chip version B with 256 Kbytes or less of flash memory and 48 to 100 pins]

**Table 5.14 DC Characteristics (13)**

Conditions: VCC = AVCC0 = 1.62 to 5.5 V, VSS = AVSS0 = 0 V, $T_a$ = –40 to +105°C

| Item | | | | Symbol | Typ.*3 | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|---|
| Supply current*1 | Software standby mode*2 | Flash memory power supplied, HOCO power supplied, POR low power consumption function disabled (SOFTCUT[2:0] bits = 000b) | $T_a$ = 25°C | $I_{CC}$ | 10 | 18 | µA | |
| | | | $T_a$ = 55°C | | 13 | 35 | | |
| | | | $T_a$ = 85°C | | 20 | 81 | | |
| | | | $T_a$ = 105°C | | 34 | 154 | | |
| | | Flash memory power supplied, HOCO power not supplied, POR low power consumption function enabled (SOFTCUT[2:0] bits = 110b) | $T_a$ = 25°C | | 1.8 | 7.7 | | |
| | | | $T_a$ = 55°C | | 3.3 | 20 | | |
| | | | $T_a$ = 85°C | | 9.2 | 60 | | |
| | | | $T_a$ = 105°C | | 20 | 124 | | |
| | Deep software standby mode*2 | Flash memory power not supplied, HOCO power not supplied, POR low power consumption function enabled (DEEPCUT1 bit = 1) | $T_a$ = 25°C | | 0.4 | 0.8 | | |
| | | | $T_a$ = 55°C | | 0.5 | 1.0 | | |
| | | | $T_a$ = 85°C | | 0.7 | 2.5 | | |
| | | | $T_a$ = 105°C | | 1.4 | 6.3 | | |
| | Increments produced by running voltage detection circuits and disabling the POR low power consumption function | | | | 1.4 | — | | |
| | Increment for RTC operation (low CL) | | | | 0.8 | — | | |
| | Increment for RTC operation (standard CL) | | | | 2.0 | — | | |

Note 1. Supply current values are with all output pins unloaded and all input pull-up MOSs in the off state.
Note 2. The IWDT and LVD are stopped.
Note 3. VCC = 3.3 V.

## 5.3.4 Control Signal Timing

**Table 5.48 Control Signal Timing**

Conditions: VCC = AVCC0 = 1.62 to 5.5 V, VSS = AVSS0 = VREFL = VREFL0 = 0 V, $T_a$ = –40 to +105°C

| Item | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| NMI pulse width | $t_{NMIW}$ | 200 | — | — | ns | $t_{c(PCLKB)}$ × 2 ≤ 200 ns, Figure 5.74 |
| | | $t_{c(PCLKB)}$ × 2 | — | — | ns | $t_{c(PCLKB)}$ × 2 > 200 ns, Figure 5.74 |
| IRQ pulse width | $t_{IRQW}$ | 200 | — | — | ns | $t_{c(PCLKB)}$ × 2 ≤ 200 ns, Figure 5.75 |
| | | $t_{c(PCLKB)}$ × 2 | — | — | ns | $t_{c(PCLKB)}$ × 2 > 200 ns, Figure 5.75 |

Note: • 200 ns minimum in deep software standby and software standby modes.

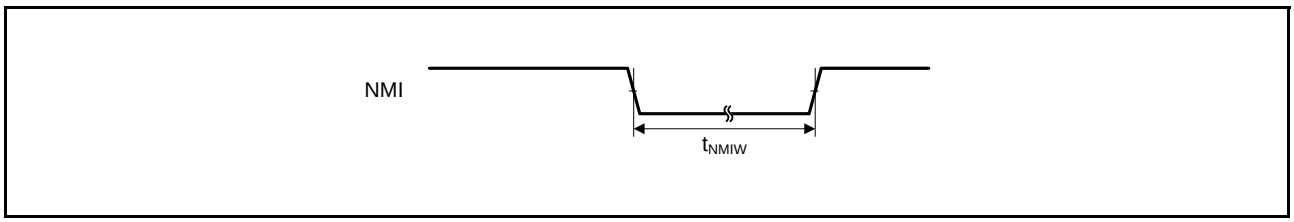



**Figure 5.74 NMI Interrupt Input Timing**

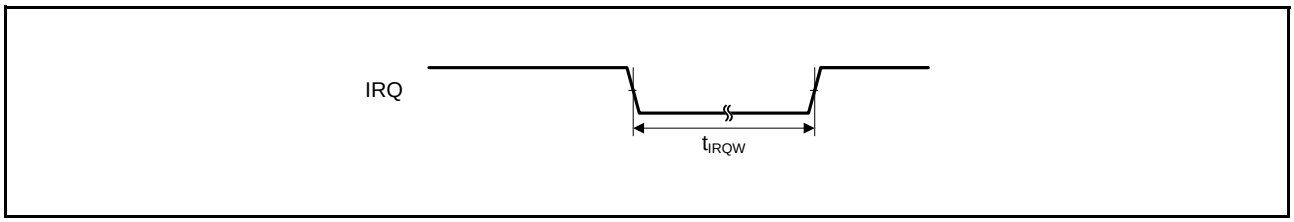



**Figure 5.75 IRQ Interrupt Input Timing**

### Table 5.52 Bus Timing (Multiplexed Bus) (1)

Conditions: VCC = AVCC0 = 2.7 to 5.5 V, VSS = AVSS0 = VREFL = VREFL0 = 0 V,
fBCLK ≤ 25 MHz (BCLK pin output frequency ≤ 12.5 MHz), $T_a$ = –40 to +105°C, $V_{OH}$ = VCC × 0.5,
$V_{OL}$ = VCC × 0.5, $I_{OH}$ = –1.0 mA, $I_{OL}$ = 1.0 mA, $C_L$ = 30 pF
When normal output is selected by the drive capacity register

| Item | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| Address delay time | $t_{AD}$ | — | 60 | ns | Figure 5.81 and Figure 5.82 |
| Byte control delay time | $t_{BCD}$ | — | 60 | ns | |
| CS# delay time | $t_{CSD}$ | — | 60 | ns | |
| RD# delay time | $t_{RSD}$ | — | 60 | ns | |
| ALE delay time | $t_{ALED}$ | — | 60 | ns | |
| Read data setup time | $t_{RDS}$ | 40 | — | ns | |
| Read data hold time | $t_{RDH}$ | 0 | — | ns | |
| WR# delay time | $t_{WRD}$ | — | 60 | ns | |
| Write data delay time | $t_{WDD}$ | — | 60 | ns | |
| Write data hold time | $t_{WDH}$ | 0 | — | ns | |
| WAIT# setup time | $t_{WTS}$ | 40 | — | ns | Figure 5.80 |
| WAIT# hold time | $t_{WTH}$ | 0 | — | ns | |

### Table 5.53 Bus Timing (Multiplexed Bus) (2)

Conditions: VCC = AVCC0 = 1.8 to 2.7 V, VSS = AVSS0 = VREFL = VREFL0 = 0 V,
fBCLK ≤ 16 MHz (BCLK pin output frequency ≤ 8 MHz), $T_a$ = –40 to +105°C, $V_{OH}$ = VCC × 0.5,
$V_{OL}$ = VCC × 0.5, $I_{OH}$ = –1.0 mA, $I_{OL}$ = 1.0 mA, $C_L$ = 30 pF
When normal output is selected by the drive capacity register

| Item | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| Address delay time | $t_{AD}$ | — | 90 | ns | Figure 5.81 and Figure 5.82 |
| Byte control delay time | $t_{BCD}$ | — | 90 | ns | |
| CS# delay time | $t_{CSD}$ | — | 90 | ns | |
| RD# delay time | $t_{RSD}$ | — | 90 | ns | |
| ALE delay time | $t_{ALED}$ | — | 90 | ns | |
| Read data setup time | $t_{RDS}$ | 60 | — | ns | |
| Read data hold time | $t_{RDH}$ | 0 | — | ns | |
| WR# delay time | $t_{WRD}$ | — | 90 | ns | |
| Write data delay time | $t_{WDD}$ | — | 90 | ns | |
| Write data hold time | $t_{WDH}$ | 0 | — | ns | |
| WAIT# setup time | $t_{WTS}$ | 60 | — | ns | Figure 5.80 |
| WAIT# hold time | $t_{WTH}$ | 0 | — | ns | |

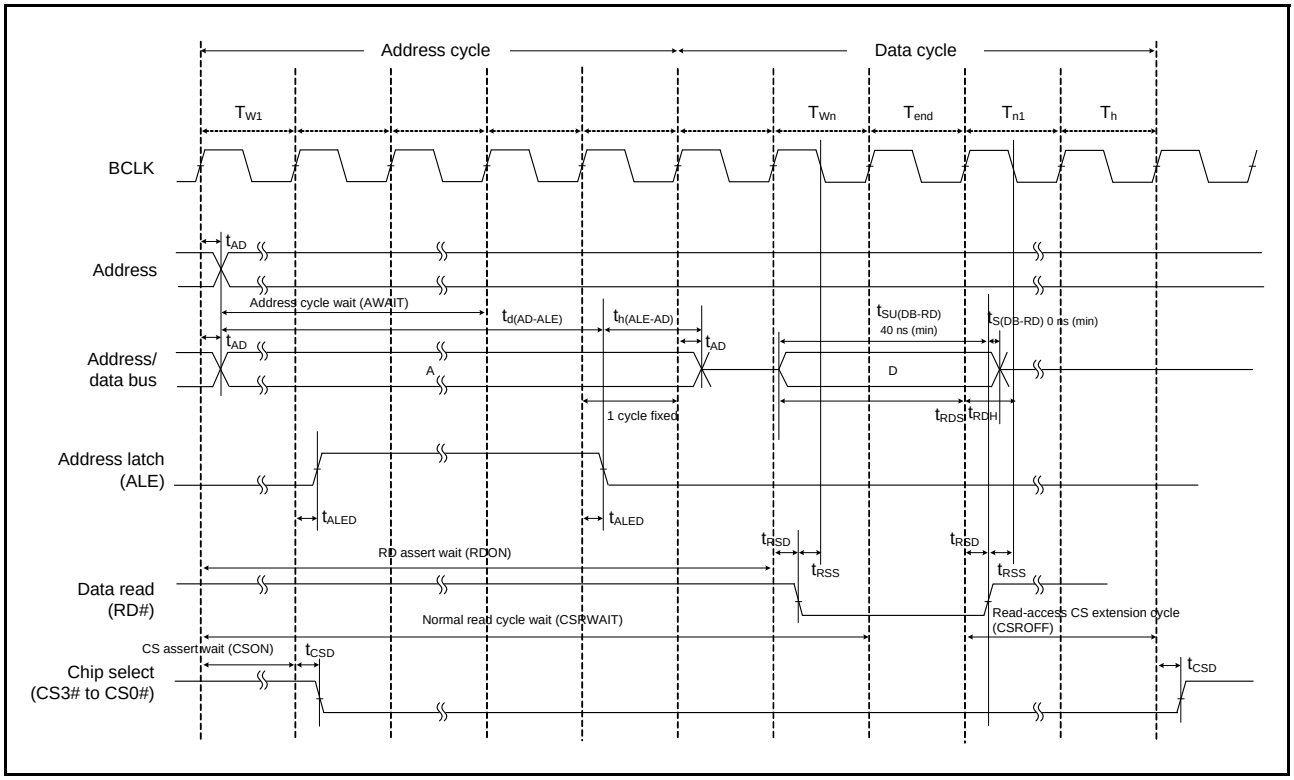



**Figure 5.81 Example of Operation in Read Access over the External Bus (Multiplexed)**

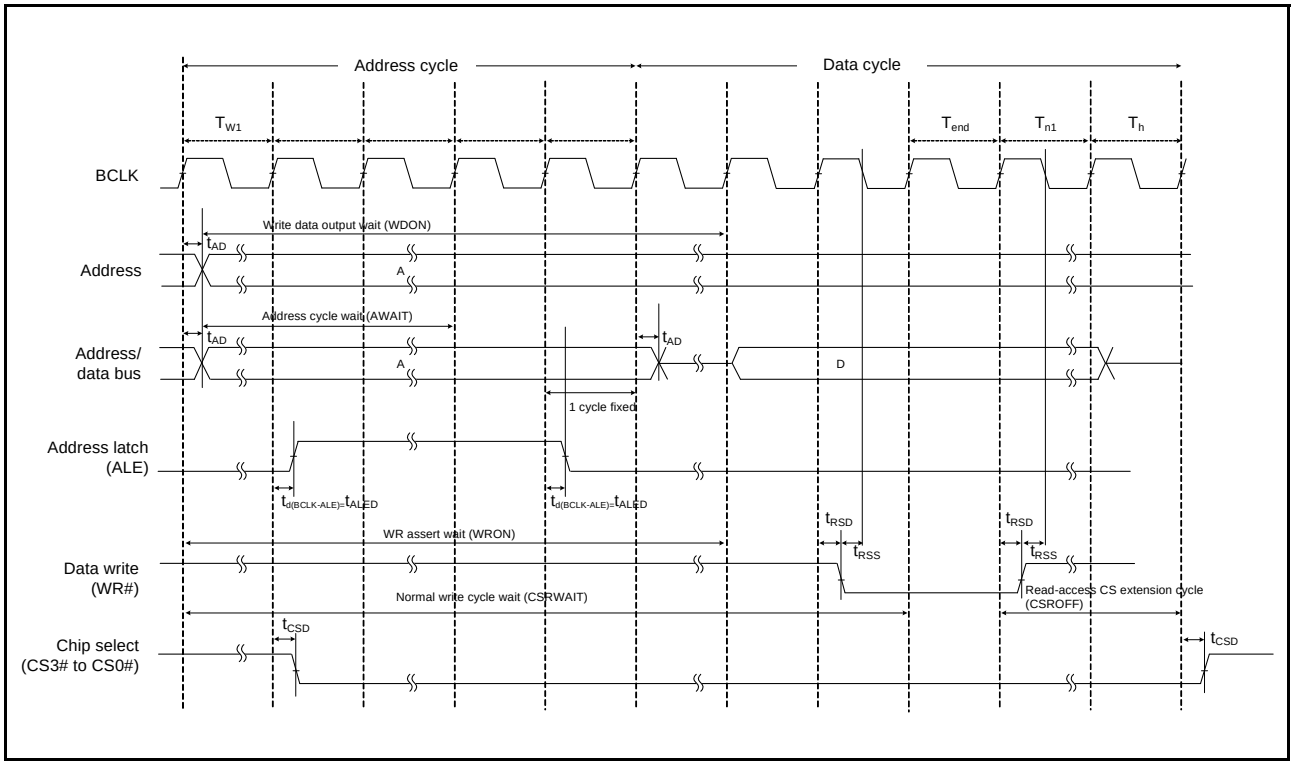



**Figure 5.82 Example of Operation in Write Access over the External Bus (Multiplexed)**

| Item | | | | Symbol | Min. | Max. | Unit*1 | Test Conditions |
|---|---|---|---|---|---|---|---|---|
| RSPI | MOSI and MISO rise/fall time | Output | | $t_{Dr}$, $t_{Df}$ | — | 20 | ns | C = 30 pF Figure 5.92 to Figure 5.97 |
| | | Input | | | — | 1 | μs | |
| | SSL rise/fall time | Output | | $t_{SSLr}$, $t_{SSLf}$ | — | 20 | ns | |
| | | Input | | | — | 1 | μs | |
| | Slave access time | | 2.7 V ≤ VCC ≤ 5.5 V | $t_{SA}$ | — | 6 | $t_{Pcyc}$ | C = 30 pF Figure 5.96 and Figure 5.97 |
| | | | 1.8 V ≤ VCC < 2.7 V | | — | 7 | | |
| | | | 1.62 V ≤ VCC < 1.8 V | | — | 7 | | |
| | Slave output release time | | 2.7 V ≤ VCC ≤ 5.5 V | $t_{REL}$ | — | 5 | $t_{Pcyc}$ | |
| | | | 1.8 V ≤ VCC < 2.7 V | | — | 6 | | |
| | | | 1.62 V ≤ VCC < 1.8 V | | — | 6 | | |

Note 1. $t_{Pcyc}$: PCLK cycle

[768 Kbytes/1 Mbyte of flash memory or 144/145 pins]

**Table 5.57 Timing of On-Chip Peripheral Modules (3)**

Conditions: VCC = AVCC0 = 1.62 to 5.5 V, VSS = AVSS0 = VREFL = VREFL0 = 0 V, $T_a$ = –40 to +105°C
When high-drive output is selected by the drive capacity register

| Item | | | | Symbol | Min. | Max. | Unit*1 | Test Conditions |
|---|---|---|---|---|---|---|---|---|
| RSPI | RSPCK clock cycle | Master | | $t_{SPcyc}$ | 2 | 4096 | $t_{Pcyc}$ | C = 30pF Figure 5.91 |
| | | Slave | | | 8 | 4096 | | |
| | RSPCK clock high pulse width | Master | 2.7 V ≤ VCC ≤ 5.5 V | $t_{SPCKWH}$ | $(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2 - 3$ | — | ns | |
| | | | 1.8 V ≤ VCC < 2.7 V | | $(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2 - 3$ | — | | |
| | | | 1.62 V ≤ VCC < 1.8 V | | $(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2 - 10$ | — | | |
| | | Slave | | | $(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2$ | — | | |
| | RSPCK clock low pulse width | Master | 2.7 V ≤ VCC ≤ 5.5 V | $t_{SPCKWL}$ | $(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2 - 3$ | — | ns | |
| | | | 1.8 V ≤ VCC < 2.7 V | | $(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2 - 3$ | — | | |
| | | | 1.62 V ≤ VCC < 1.8 V | | $(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2 - 10$ | — | | |
| | | Slave | | | $(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2$ | — | | |
| | RSPCK clock rise/fall time | Output | 2.7 V ≤ VCC ≤ 5.5 V | $t_{SPCKr}$, $t_{SPCKf}$ | — | 10 | ns | |
| | | | 1.8 V ≤ VCC < 2.7 V | | — | 15 | | |
| | | | 1.62 V ≤ VCC < 1.8 V | | — | 20 | | |
| | | Input | | | — | 1 | μs | |

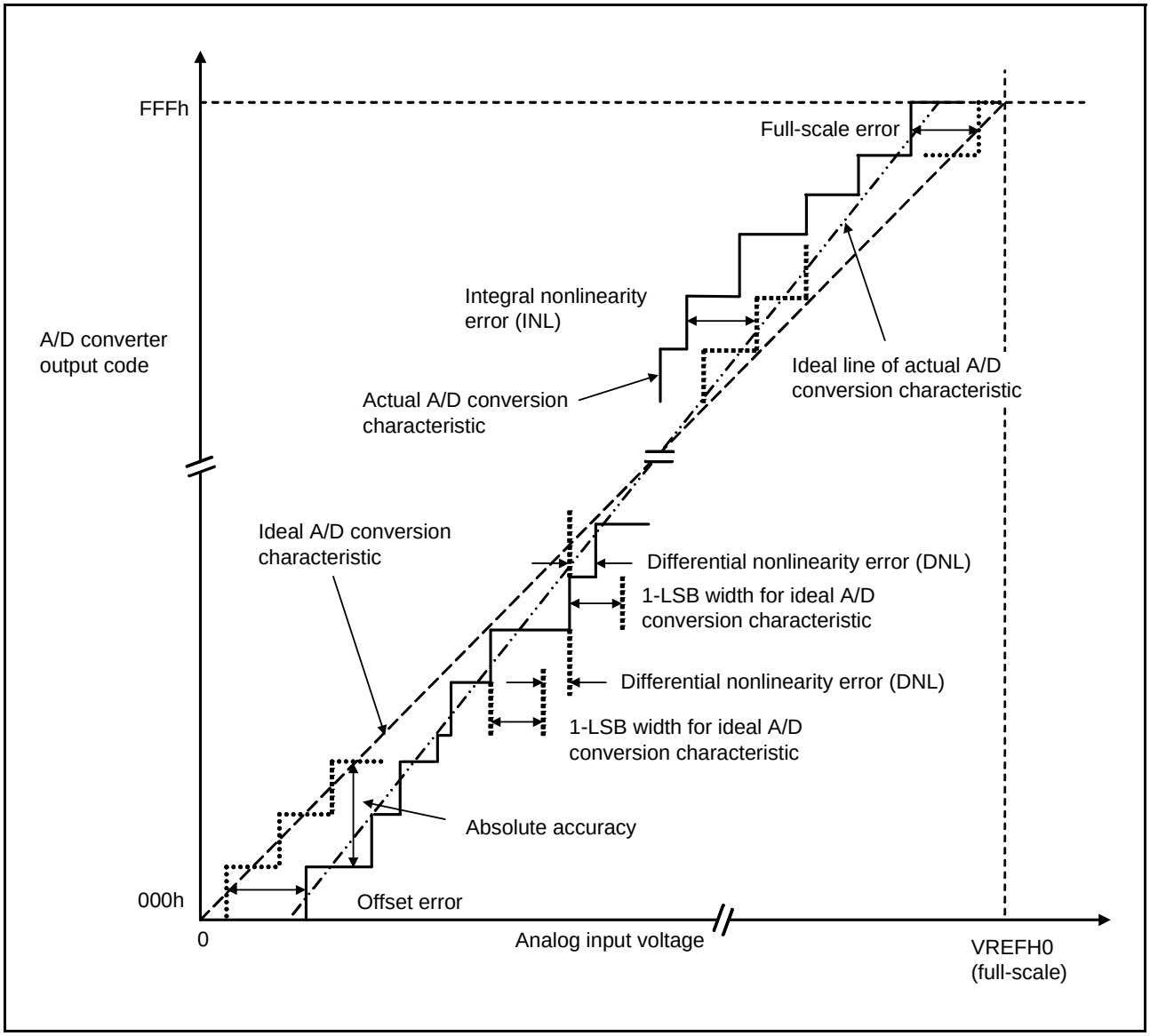



**Figure 5.101 Illustration of A/D Converter Characteristic Terms**

### Absolute accuracy

Absolute accuracy is the difference between output code based on the theoretical A/D conversion characteristics, and the actual A/D conversion result. When measuring absolute accuracy, the voltage at the midpoint of the width of analog input voltage (1-LSB width), that can meet the expectation of outputting an equal code based on the theoretical A/D conversion characteristics, is used as an analog input voltage. For example, if 12-bit resolution is used and if reference voltage (VREFH0 = 5.12 V), then 1-LSB width becomes 1.25 mV, and 0 mV, 1.25 mV, 2.5 mV, ... are used as analog input voltages.

If analog input voltage is 10 mV, absolute accuracy = ±5 LSB means that the actual A/D conversion result is in the range of 003h to 00Dh though an output code, 008h, can be expected from the theoretical A/D conversion characteristics.

### Integral nonlinearity error (INL)

Integral nonlinearity error is the maximum deviation between the ideal line when the measured offset and full-scale errors are zeroed, and the actual output code.

## 5.8 Power-on Reset Circuit and Voltage Detection Circuit Characteristics

**Table 5.71 Power-on Reset Circuit and Voltage Detection Circuit Characteristics (1)**

Conditions: VCC = AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V, $T_a$ = –40 to +105°C

| Item | | | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|---|
| Voltage detection level | Power-on reset (POR) | Low power consumption function disabled*1 | $V_{POR}$ | 1.30 | 1.40 | 1.55 | V | Figure 5.103 and Figure 5.104 |
| | | Low power consumption function enabled*2 | | 1.00 | 1.20 | 1.45 | | |
| | Voltage detection circuit (LVD0)*3 | | $V_{det0\_0}$ | 3.65 | 3.80 | 3.95 | V | Figure 5.105 |
| | | | $V_{det0\_1}$ | 2.70 | 2.80 | 2.90 | | |
| | | | $V_{det0\_2}$ | 1.80 | 1.90 | 2.00 | | |
| | | | $V_{det0\_3}$ | 1.62 | 1.72 | 1.82 | | |
| | Voltage detection circuit (LVD1)*4 | | $V_{det1\_0}$ | 4.00 | 4.15 | 4.30 | V | Figure 5.106 |
| | | | $V_{det1\_1}$ | 3.85 | 4.00 | 4.15 | | |
| | | | $V_{det1\_2}$ | 3.70 | 3.85 | 4.00 | | At falling edge VCC |
| | | | $V_{det1\_3}$ | 3.55 | 3.70 | 3.85 | | |
| | | | $V_{det1\_4}$ | 3.40 | 3.55 | 3.70 | | |
| | | | $V_{det1\_5}$ | 3.25 | 3.40 | 3.55 | | |
| | | | $V_{det1\_6}$ | 3.10 | 3.25 | 3.40 | | |
| | | | $V_{det1\_7}$ | 2.95 | 3.10 | 3.25 | | |
| | | | $V_{det1\_8}$ | 2.85 | 2.95 | 3.05 | | |
| | | | $V_{det1\_9}$ | 2.70 | 2.80 | 2.90 | | |
| | | | $V_{det1\_A}$ | 2.55 | 2.65 | 2.75 | | |
| | | | $V_{det1\_B}$ | 2.40 | 2.50 | 2.60 | | |
| | | | $V_{det1\_C}$ | 2.25 | 2.35 | 2.45 | | |
| | | | $V_{det1\_D}$ | 2.10 | 2.20 | 2.30 | | |
| | | | $V_{det1\_E}$ | 1.95 | 2.05 | 2.15 | | |
| | | | $V_{det1\_F}$ | 1.80 | 1.90 | 2.00 | | |

Note: • These characteristics apply when noise is not superimposed on the power supply.

Note 1. When the CPU is in a mode other than software standby and deep software standby modes, when the CPU transits to software standby mode with the FHSSBYCR.SOFTCUT[2] bit set to 0, or when the CPU transits to deep software standby mode with the DPSBYCR.DEEPCUT1 bit set to 0.

Note 2. When the CPU transits to software standby mode with the FHSSBYCR.SOFTCUT[2] bit set to 1 or when the CPU transits to deep software standby mode with the DPSBYCR.DEEPCUT1 bit set to 1.

Note 3. # in the symbol Vdet0_# denotes the value of the LDSEL[1:0] bits.

Note 4. # in the symbol Vdet1_# denotes the value of the LVDLVLR.LVD1LVL[3:0] bits.

[Chip version B]

**Table 5.79 ROM (Flash Memory for Code Storage) Characteristics (6) : middle-speed operating modes 1B and 2B**

Conditions: VCC = AVCC0 = 1.62 to 3.6 V, VREFH = VREFH0 = AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V
Temperature range for the programming/erasure operation: $T_a$ = –40 to +105°C

| Item | | Symbol | FCLK = 4 MHz | | | FCLK = 32 MHz*1 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | Min. | Typ. | Max. | |
| Programming time when $N_{PEC}$ ≤ 100 times | 2 bytes | $t_{P2}$ | — | 0.25 | 5.0 | — | 0.21 | 2.8 | ms |
| | 8 bytes | $t_{P8}$ | — | 0.25 | 5.3 | — | 0.21 | 3.0 | |
| | 128 bytes | $t_{P128}$ | — | 0.92 | 14.0 | — | 0.65 | 8.3 | |
| Programming time when $N_{PEC}$ > 100 times | 2 bytes | $t_{P2}$ | — | 0.31 | 6.2 | — | 0.26 | 3.5 | ms |
| | 8 bytes | $t_{P8}$ | — | 0.31 | 6.6 | — | 0.26 | 3.7 | |
| | 128 bytes | $t_{P128}$ | — | 1.09 | 17.5 | — | 0.77 | 10.0 | |
| Erasure time when $N_{PEC}$ ≤ 100 times | 2 Kbytes | $t_{E2K}$ | — | 21.0 | 113.7 | — | 18.5 | 46 | ms |
| Erasure time when $N_{PEC}$ > 100 times | 2 Kbytes | $t_{E2K}$ | — | 25.6 | 220.6 | — | 22.5 | 90 (1000 times ≥ $N_{PEC}$ > 100 times), 98 (10000 times ≥ $N_{PEC}$ > 1000 times) | ms |
| Suspend delay time during programming (in programming/erasure priority mode) | | $t_{SPD}$ | — | — | 1.7 | — | — | 1.6 | ms |
| First suspend delay time during programming (in suspend priority mode) | | $t_{SPSD1}$ | — | — | 220 | — | — | 120 | µs |
| Second suspend delay time during programming (in suspend priority mode) | | $t_{SPSD2}$ | — | — | 1.7 | — | — | 1.6 | ms |
| Suspend delay time during erasing (in programming/erasure priority mode) | | $t_{SED}$ | — | — | 1.7 | — | — | 1.6 | ms |
| First suspend delay time during erasing (in suspend priority mode) | | $t_{SESD1}$ | — | — | 220 | — | — | 120 | µs |
| Second suspend delay time during erasing (in suspend priority mode) | | $t_{SESD2}$ | — | — | 1.7 | — | — | 1.6 | ms |
| FCU reset time | | $t_{FCUR}$ | 20 µs or longer and FCLK × 6 or greater | — | — | 20 µs or longer and FCLK × 6 or greater | — | — | µs |

Note 1. The operating frequency is 20 MHz (max.) when the voltage is in the range from 1.62 V to less than 1.8 V.

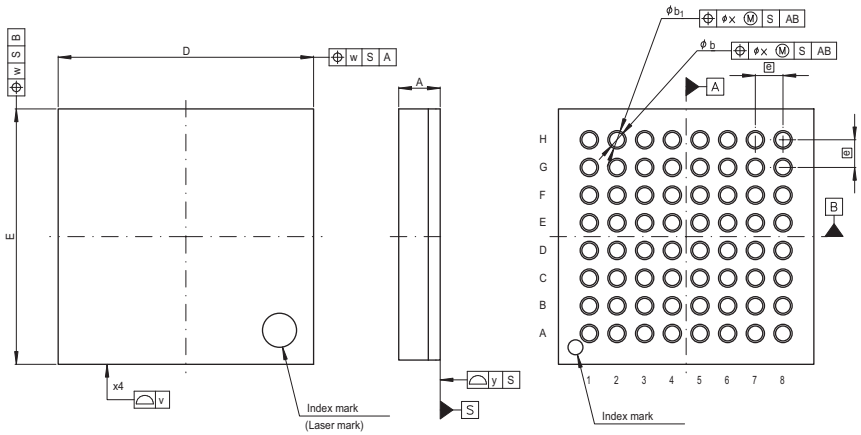
[Chip version B]

**Table 5.84 E2 DataFlash Characteristics (5)**
**: high-speed operating mode, middle-speed operating modes 1A and 2A**

Conditions: VCC = AVCC0 = 2.7 to 5.5 V, VREFH = VREFH0 = AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V
Temperature range for the programming/erasure operation: $T_a$ = –40 to +105°C

| Item | | Symbol | FCLK = 4 MHz | | | FCLK = 32 MHz | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | Min. | Typ. | Max. | |
| Programming time when $N_{DPEC}$ ≤ 100 times | 2 bytes | $t_{DP2}$ | — | 0.19 | 4.4 | — | 0.13 | 2.0 | ms |
| | 8 bytes | $t_{DP8}$ | — | 0.24 | 5.1 | — | 0.13 | 2.2 | |
| Programming time when $N_{DPEC}$ > 100 times | 2 bytes | $t_{DP2}$ | — | 0.25 | 6.4 | — | 0.17 | 3.0 | ms |
| | 8 bytes | $t_{DP8}$ | — | 0.32 | 7.5 | — | 0.18 | 3.2 | |
| Erasure time when $N_{DPEC}$ ≤ 100 times | 128 bytes | $t_{DE128}$ | — | 3.3 | 27.1 | — | 2.5 | 8 | ms |
| Erasure time when $N_{DPEC}$ > 100 times | 128 bytes | $t_{DE128}$ | — | 4.0 | 45.1 | — | 3.0 | 12 | ms |
| Blank check time | 2 bytes | $t_{DBC2}$ | — | — | 98 | — | — | 35 | µs |
| | 2 Kbytes | $t_{DBC2K}$ | — | — | 16 | — | — | 2.5 | ms |
| Suspend delay time during programming (in programming/erasure priority mode) | | $t_{DSPD}$ | — | — | 0.9 | — | — | 0.8 | ms |
| First suspend delay time during programming (in suspend priority mode) | | $t_{DSPSD1}$ | — | — | 220 | — | — | 120 | µs |
| Second suspend delay time during programming (in suspend priority mode) | | $t_{DSPSD2}$ | — | — | 0.9 | — | — | 0.8 | ms |
| Suspend delay time during erasing (in programming/erasure priority mode) | | $t_{DSED}$ | — | — | 0.9 | — | — | 0.8 | ms |
| First suspend delay time during erasing (in suspend priority mode) | | $t_{DSESD1}$ | — | — | 220 | — | — | 120 | µs |
| Second suspend delay time during erasing (in suspend priority mode) | | $t_{DSESD2}$ | — | — | 0.9 | — | — | 0.8 | ms |

| JEITA Package Code | RENESAS Code | Previous Code | MASS[Typ.] |
|---|---|---|---|
| P-TFLGA64-6x6-0.65 | PTLG0064JA-A | 64F0G | 0.07g |




| Reference Symbol | Dimension in Millimeters | | |
|---|---|---|---|
| | Min | Nom | Max |
| D | — | 6.0 | — |
| E | — | 6.0 | — |
| v | — | — | 0.15 |
| w | — | — | 0.20 |
| A | — | — | 1.05 |
| e | — | 0.65 | — |
| b | 0.31 | 0.35 | 0.39 |
| $b_1$ | 0.39 | 0.43 | 0.47 |
| x | — | — | 0.08 |
| y | — | — | 0.10 |

Figure F 64-Pin TFLGA (PTLG0064JA-A)

| Rev. | Date | Description | |
|---|---|---|---|
| | | Page | Summary |
| 1.30 | Jan 22, 2013 | 11 | Table 1.6 List of Products Chip Version C: D Version (Ta = -40 to +85°C),<br>Table 1.7 List of Products Chip Version C: G Version (Ta = -40 to +105°C), changed |
| | | 12 | Figure 1.1 How to Read the Product Part No., Memory Capacity, and Package Type, changed |
| | | 13 | Figure 1.2 Block Diagram, changed |
| | | 14 to 17 | Table 1.8 Pin Functions, changed |
| | | 18 | Figure 1.3 Pin Assignments of the 145-Pin TFLGA (Upper Perspective View), added |
| | | 19 | Figure 1.4 Pin Assignments of the 144-Pin LQFP, added |
| | | 25 to 28 | Table 1.9 List of Pins and Pin Functions (145-Pin TFLGA), changed |
| | | 29 to 32 | Table 1.10 List of Pins and Pin Functions (144-Pin LQFP), changed |
| | | 3. Address Space | |
| | | 48 | Figure 3.1 Memory Map in Each Operating Mode, changed |
| | | 4. I/O Registers | |
| | | 52 to 81 | Table 4.1 List of I/O Registers (Address Order, changed |
| | | 5. Electrical Characteristics | |
| | | 83 | Table 5.2 DC Characteristics (1),<br>Table 5.3 DC Characteristics (2), changed |
| | | 84 to 122 | Table 5.6 DC Characteristics (5) to Table 5.20 DC Characteristics (19), changed<br>Figure 5.1 Voltage Dependency in High-Speed .... for Chip Version A to<br>Figure 5.34 Temperature Dependency in .... and 100 to 145 pins, changed |
| | | 158 | Table 5.55 Timing of On-Chip Peripheral Modules (1), changed |
| | | 159 | [512 Kbytes or less of flash memory and 48 to 100 pins]<br>Table 5.56 Timing of On-Chip Peripheral Modules (2), added |
| | | 160, 161 | [768 Kbytes/1 Mbyte of flash memory or 145/145 pins]<br>Table 5.57 Timing of On-Chip Peripheral Modules (3), added |
| | | 162 | Table 5.58 Timing of On-Chip Peripheral Modules (4), changed |
| | | 165 | Figure 5.75 MTU/TPU Input/Output Timing,<br>Figure 5.76 MTU/TPU Clock Input Timing, changed |
| | | 166 | Figure 5.79 SCK Clock Input Timing,<br>Figure 5.80 SCI Input/Output Timing: Clock Synchronous Mode, changed |
| | | 167 | Figure 5.82 RSPI Clock Timing and Simple SPI Clock Timing, changed |
| | | 168 | Figure 5.83 RSPI Timing (Master, CPHA = 0) .... and Simple SPI Timing (Master, CKPH = 1),<br>Figure 5.84 RSPI Timing (Master, CPHA = 0) (Bit Rate: PCLKB Set to Divided by 2), changed |
| | | 169 | Figure 5.85 RSPI Timing (Master, CPHA = 1) .... and Simple SPI Timing (Master, CKPH = 0),<br>Figure 5.86 RSPI Timing (Master, CPHA = 1) (Bit Rate: PCLKB Set to Divided by 2), changed |
| | | 170 | Figure 5.87 RSPI Timing (Slave, CPHA = 0) and Simple SPI Timing (Slave, CKPH = 1),<br>Figure 5.88 RSPI Timing (Slave, CPHA = 1) and Simple SPI Timing (Slave, CKPH = 0), changed |
| | | 173 | Table 5.64 A/D Conversion Characteristics (2), changed |
| | | 175 | Figure 5.91 Illustration of A/D Converter Characteristic Terms,<br>Absolute accuracy, changed |
| | | 184 | Table 5.74 ROM (Flash Memory for Code Storage) Characteristics (1), changed |
| | | 189 | Table 5.80 E2 DataFlash Characteristics (1),<br>Table 5.81 E2 DataFlash Characteristics (2), changed |
| | | Appendix 1. Package Dimensions | |
| | | 195 | Figure A 145-Pin TFLGA (PTLG0145KA-A), added |
| | | 196 | Figure B 144-Pin LQFP (PLQP0144KA-A), added |
| 1.40 | Feb 19, 2013 | 1. Overview | |
| | | 2 to 6 | Table 1.1 Outline of Specifications, changed<br>Note 2, added |
| | | 9 | Table 1.4 List of Products Chip Version B: D Version (Ta = -40 to +85°C), changed |
| | | 10 | Table 1.5 List of Products Chip Version B: G Version (Ta = -40 to +105°C), changed<br>Note, added |
| | | 11 | Table 1.6 List of Products Chip Version C: D Version (Ta = -40 to +85°C): Note 1,<br>Table 1.7 List of Products Chip Version C: G Version (Ta = -40 to +105°C): Note 1 deleted,<br>Note added |
| | | 12 | Figure 1.1 How to Read the Product Part No., Memory Capacity, and Package Type, changed |
| | | 4. I/O Registers | |
| | | 58 | Table 5.1 List of I/O Registers (Address Order), changed |
| | | 5. Electrical Characteristics | |
| | | 83 | Table 5.4 DC Characteristics (3), changed |
| | | 88 | Table 5.8 DC Characteristics (7), changed |

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