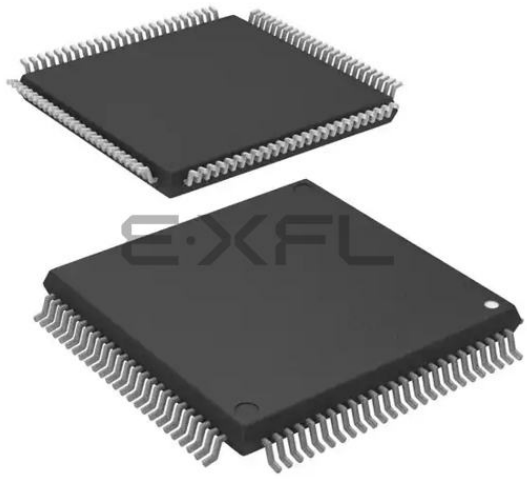
Renesas Electronics America Inc - R5F52107CDFP#30 Datasheet



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Applications of "Embedded - Microcontrollers"

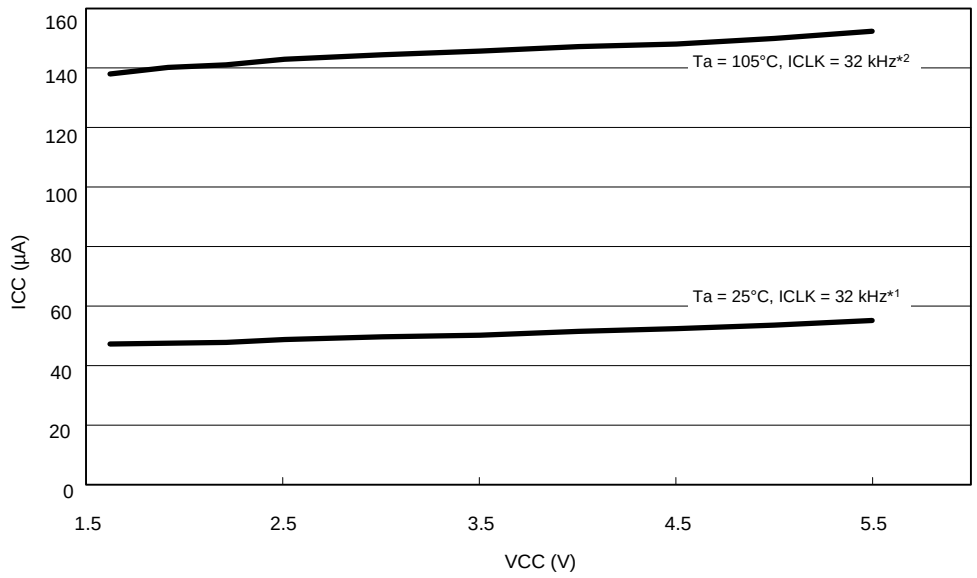
Details	
Product Status	Discontinued at Digi-Key
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	EBI/EMI, I²C, SCI, SPI
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	84
Program Memory Size	384KB (384K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	1.62V ~ 5.5V
Data Converters	A/D 16x12b; D/A 2x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LFQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f52107cdfp-30

Table 4.1 List of I/O Registers (Address Order) (10 / 29)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles: ICLK ≥ PCLK	Number of Access Cycles: ICLK < PCLK
0008 738A2	ICU	Interrupt source priority register 162	IPR162	8	8		2 ICLK
0008 73A4h	ICU	Interrupt source priority register 164	IPR164	8	8		2 ICLK
0008 73A6h	ICU	Interrupt source priority register 166	IPR166	8	8		2 ICLK
0008 73AAh	ICU	Interrupt source priority register 170	IPR170	8	8		2 ICLK
0008 73ABh	ICU	Interrupt source priority register 171	IPR171	8	8		2 ICLK
0008 73AEh	ICU	Interrupt source priority register 174	IPR174	8	8		2 ICLK
0008 73B1h	ICU	Interrupt source priority register 177	IPR177	8	8		2 ICLK
0008 73B4h	ICU	Interrupt source priority register 180	IPR180	8	8		2 ICLK
0008 73B7h	ICU	Interrupt source priority register 183	IPR183	8	8		2 ICLK
0008 73BAh	ICU	Interrupt source priority register 186	IPR186	8	8		2 ICLK
0008 73BEh	ICU	Interrupt source priority register 190	IPR190	8	8		2 ICLK
0008 73C2h	ICU	Interrupt source priority register 194	IPR194	8	8		2 ICLK
0008 73C6h	ICU	Interrupt source priority register 198	IPR198	8	8		2 ICLK
0008 73C7h	ICU	Interrupt source priority register 199	IPR199	8	8		2 ICLK
0008 73C8h	ICU	Interrupt source priority register 200	IPR200	8	8		2 ICLK
0008 73C9h	ICU	Interrupt source priority register 201	IPR201	8	8		2 ICLK
0008 73CEh	ICU	Interrupt source priority register 206	IPR206	8	8		2 ICLK
0008 73D2h	ICU	Interrupt source priority register 210	IPR210	8	8		2 ICLK
0008 73D6h	ICU	Interrupt source priority register 214	IPR214	8	8		2 ICLK
0008 73DAh	ICU	Interrupt source priority register 218	IPR218	8	8		2 ICLK
0008 73DEh	ICU	Interrupt source priority register 222	IPR222	8	8		2 ICLK
0008 73E2h	ICU	Interrupt source priority register 226	IPR226	8	8		2 ICLK
0008 73E6h	ICU	Interrupt source priority register 230	IPR230	8	8		2 ICLK
0008 73EAh	ICU	Interrupt source priority register 234	IPR234	8	8		2 ICLK
0008 73EEh	ICU	Interrupt source priority register 238	IPR238	8	8		2 ICLK
0008 73F2h	ICU	Interrupt source priority register 242	IPR242	8	8		2 ICLK
0008 73F3h	ICU	Interrupt source priority register 243	IPR243	8	8		2 ICLK
0008 73F4h	ICU	Interrupt source priority register 244	IPR244	8	8		2 ICLK
0008 73F5h	ICU	Interrupt source priority register 245	IPR245	8	8		2 ICLK
0008 73F6h	ICU	Interrupt source priority register 246	IPR246	8	8		2 ICLK
0008 73F7h	ICU	Interrupt source priority register 247	IPR247	8	8		2 ICLK
0008 73F8h	ICU	Interrupt source priority register 248	IPR248	8	8		2 ICLK
0008 73F9h	ICU	Interrupt source priority register 249	IPR249	8	8		2 ICLK
0008 73FAh	ICU	Interrupt source priority register 250	IPR250	8	8		2 ICLK
0008 7400h	ICU	DMAC activation request select register 0	DMRSR0	8	8		2 ICLK
0008 7404h	ICU	DMAC activation request select register 1	DMRSR1	8	8		2 ICLK
0008 7408h	ICU	DMAC activation request select register 2	DMRSR2	8	8		2 ICLK
0008 740Ch	ICU	DMAC activation request select register 3	DMRSR3	8	8		2 ICLK
0008 7500h	ICU	IRQ control register 0	IRQCR0	8	8		2 ICLK
0008 7501h	ICU	IRQ control register 1	IRQCR1	8	8		2 ICLK
0008 7502h	ICU	IRQ control register 2	IRQCR2	8	8		2 ICLK
0008 7503h	ICU	IRQ control register 3	IRQCR3	8	8		2 ICLK
0008 7504h	ICU	IRQ control register 4	IRQCR4	8	8		2 ICLK
0008 7505h	ICU	IRQ control register 5	IRQCR5	8	8		2 ICLK
0008 7506h	ICU	IRQ control register 6	IRQCR6	8	8		2 ICLK
0008 7507h	ICU	IRQ control register 7	IRQCR7	8	8		2 ICLK
0008 7510h	ICU	IRQ pin digital filter enable register 0	IRQFLTE0	8	8		2 ICLK
0008 7514h	ICU	IRQ pin digital filter setting register 0	IRQFLTC0	16	16		2 ICLK
0008 7580h	ICU	Non-maskable interrupt status register	NMISR	8	8		2 ICLK
0008 7581h	ICU	Non-maskable interrupt enable register	NMIER	8	8		2 ICLK
0008 7582h	ICU	Non-maskable interrupt clear register	NMICLR	8	8		2 ICLK

Table 4.1 List of I/O Registers (Address Order) (19 / 29)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles: ICLK ≥ PCLK	Number of Access Cycles: ICLK < PCLK
0008 A0CDh	SCI6	SPI mode register	SPMR	8	8	2, 3 PCLKB	2 ICLK
0008 A0E0h	SCI7	Serial mode register	SMR	8	8	2, 3 PCLKB	2 ICLK
0008 A0E1h	SCI7	Bit rate register	BRR	8	8	2, 3 PCLKB	2 ICLK
0008 A0E2h	SCI7	Serial control register	SCR	8	8	2, 3 PCLKB	2 ICLK
0008 A0E3h	SCI7	Transmit data register	TDR	8	8	2, 3 PCLKB	2 ICLK
0008 A0E4h	SCI7	Serial status register	SSR	8	8	2, 3 PCLKB	2 ICLK
0008 A0E5h	SCI7	Receive data register	RDR	8	8	2, 3 PCLKB	2 ICLK
0008 A0E6h	SCI7	Smart card mode register	SCMR	8	8	2, 3 PCLKB	2 ICLK
0008 A0E7h	SCI7	Serial extended mode register	SEMR	8	8	2, 3 PCLKB	2 ICLK
0008 A0E8h	SCI7	Noise filter setting register	SNFR	8	8	2, 3 PCLKB	2 ICLK
0008 A0E9h	SCI7	I^2C mode register 1	SIMR1	8	8	2, 3 PCLKB	2 ICLK
0008 A0EAh	SCI7	I^2C mode register 2	SIMR2	8	8	2, 3 PCLKB	2 ICLK
0008 A0EBh	SCI7	I^2C mode register 3	SIMR3	8	8	2, 3 PCLKB	2 ICLK
0008 A0ECh	SCI7	I^2C status register	SISR	8	8	2, 3 PCLKB	2 ICLK
0008 A0EDh	SCI7	SPI mode register	SPMR	8	8	2, 3 PCLKB	2 ICLK
0008 A100h	SCI8	Serial mode register	SMR	8	8	2, 3 PCLKB	2 ICLK
0008 A101h	SCI8	Bit rate register	BRR	8	8	2, 3 PCLKB	2 ICLK
0008 A102h	SCI8	Serial control register	SCR	8	8	2, 3 PCLKB	2 ICLK
0008 A103h	SCI8	Transmit data register	TDR	8	8	2, 3 PCLKB	2 ICLK
0008 A104h	SCI8	Serial status register	SSR	8	8	2, 3 PCLKB	2 ICLK
0008 A105h	SCI8	Receive data register	RDR	8	8	2, 3 PCLKB	2 ICLK
0008 A106h	SCI8	Smart card mode register	SCMR	8	8	2, 3 PCLKB	2 ICLK
0008 A107h	SCI8	Serial extended mode register	SEMR	8	8	2, 3 PCLKB	2 ICLK
0008 A108h	SCI8	Noise filter setting register	SNFR	8	8	2, 3 PCLKB	2 ICLK
0008 A109h	SCI8	I^2C mode register 1	SIMR1	8	8	2, 3 PCLKB	2 ICLK
0008 A10Ah	SCI8	I^2C mode register 2	SIMR2	8	8	2, 3 PCLKB	2 ICLK
0008 A10Bh	SCI8	I^2C mode register 3	SIMR3	8	8	2, 3 PCLKB	2 ICLK
0008 A10Ch	SCI8	I^2C status register	SISR	8	8	2, 3 PCLKB	2 ICLK
0008 A10Dh	SCI8	SPI mode register	SPMR	8	8	2, 3 PCLKB	2 ICLK
0008 A120h	SCI9	Serial mode register	SMR	8	8	2, 3 PCLKB	2 ICLK
0008 A121h	SCI9	Bit rate register	BRR	8	8	2, 3 PCLKB	2 ICLK
0008 A122h	SCI9	Serial control register	SCR	8	8	2, 3 PCLKB	2 ICLK
0008 A123h	SCI9	Transmit data register	TDR	8	8	2, 3 PCLKB	2 ICLK
0008 A124h	SCI9	Serial status register	SSR	8	8	2, 3 PCLKB	2 ICLK
0008 A125h	SCI9	Receive data register	RDR	8	8	2, 3 PCLKB	2 ICLK
0008 A126h	SCI9	Smart card mode register	SCMR	8	8	2, 3 PCLKB	2 ICLK
0008 A127h	SCI9	Serial extended mode register	SEMR	8	8	2, 3 PCLKB	2 ICLK
0008 A128h	SCI9	Noise filter setting register	SNFR	8	8	2, 3 PCLKB	2 ICLK
0008 A129h	SCI9	I^2C mode register 1	SIMR1	8	8	2, 3 PCLKB	2 ICLK
0008 A12Ah	SCI9	I^2C mode register 2	SIMR2	8	8	2, 3 PCLKB	2 ICLK
0008 A12Bh	SCI9	I^2C mode register 3	SIMR3	8	8	2, 3 PCLKB	2 ICLK
0008 A12Ch	SCI9	I^2C status register	SISR	8	8	2, 3 PCLKB	2 ICLK
0008 A12Dh	SCI9	SPI mode register	SPMR	8	8	2, 3 PCLKB	2 ICLK
0008 A140h	SCI10	Serial mode register	SMR	8	8	2, 3 PCLKB	2 ICLK
0008 A141h	SCI10	Bit rate register	BRR	8	8	2, 3 PCLKB	2 ICLK
0008 A142h	SCI10	Serial control register	SCR	8	8	2, 3 PCLKB	2 ICLK
0008 A143h	SCI10	Transmit data register	TDR	8	8	2, 3 PCLKB	2 ICLK
0008 A144h	SCI10	Serial status register	SSR	8	8	2, 3 PCLKB	2 ICLK
0008 A145h	SCI10	Receive data register	RDR	8	8	2, 3 PCLKB	2 ICLK
0008 A146h	SCI10	Smart card mode register	SCMR	8	8	2, 3 PCLKB	2 ICLK
0008 A147h	SCI10	Serial extended mode register	SEMR	8	8	2, 3 PCLKB	2 ICLK



Note 1. All peripheral operation is normal.
Average value of the tested middle samples during product evaluation.
Note 2. All peripheral operation is maximum.
Average value of the tested upper-limit samples during product evaluation.

Figure 5.21 Voltage Dependency in Low-Speed Operating Mode 2 (Reference Data) for Chip Version B with 256 Kbytes or Less of Flash Memory and 48 to 100 Pins

[Chip version B with 512 Kbytes or less of flash memory and 144 and 145 pins]

Table 5.18 DC Characteristics (17)

Conditions: VCC = AVCC0 = 2.7 to 5.5 V, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +105°C

Item					Symbol	Typ.	Max.	Unit	Test Conditions
Supply current*1	High-speed operating mode	Normal operating mode	No peripheral operation*2	ICLK = 50 MHz	I_{CC}	7.2	—	mA	
			All peripheral operation: Normal*3	ICLK = 50 MHz		25.9	—		
			All peripheral operation: Max.*3	ICLK = 50 MHz		—	45		
		Sleep mode	No peripheral operation	ICLK = 50 MHz		4.3	—		
			All peripheral operation: Normal	ICLK = 50 MHz		13	—		
		All-module clock stop mode				3.7	—		
		Increase during BGO operation*4				21	—		

Note 1. Supply current values do not include output charge/discharge current from all pins. The values apply when internal pull-up MOSs are in the off state.

Note 2. Clock supply to the peripheral functions is stopped. This does not include BGO operation. The clock source is PLL and the VCO oscillation frequency is 100 MHz. BCLK, FCLK, and PCLK are set to divided by 64.

Note 3. Clocks are supplied to the peripheral functions. This does not include BGO operation. The clock source is PLL and the VCO oscillation frequency is 100 MHz. BCLK, FCLK, and PCLK are ICLK divided by 2.

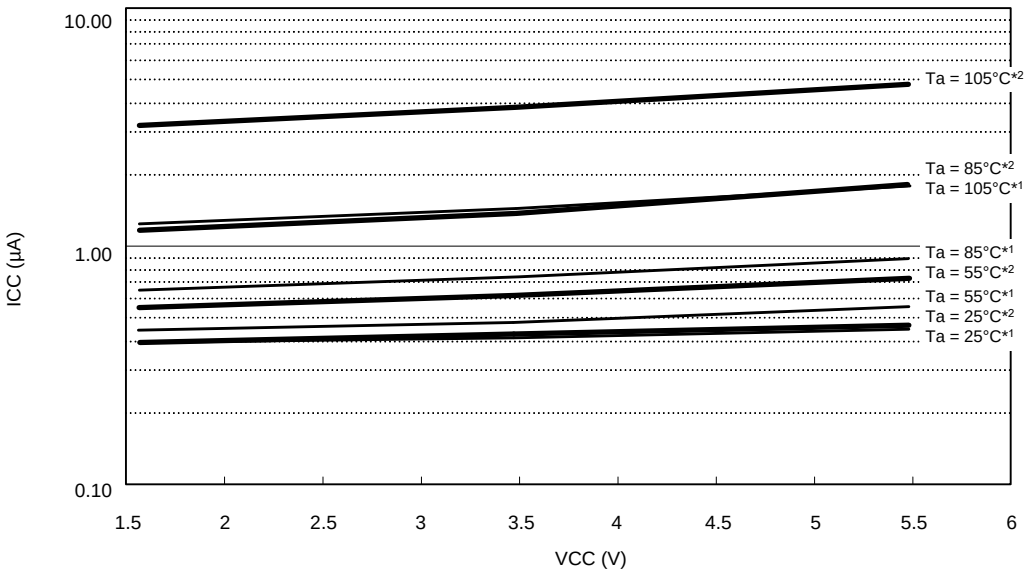
Note 4. This is the increase if data is programmed to or erasing from the ROM or E2 DataFlash during program execution.

[Chip version B with 512 Kbytes or less of flash memory and 144 and 145 pins]

Table 5.19 DC Characteristics (18)

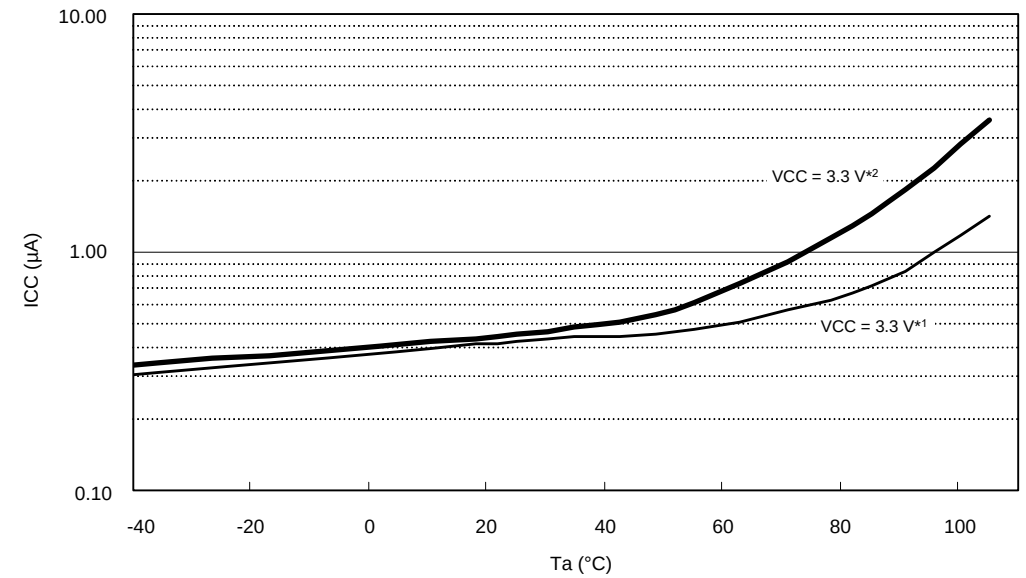
Conditions: VCC = AVCC0 = 1.62 to 5.5 V, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +105°C

Item					Symbol	Typ.	Max.	Unit	Test Conditions
Supply current*1	Middle-speed operating modes 1A and 1B	Normal operating mode	No peripheral operation	ICLK = 32 MHz*2	I_{CC}	5.3	—	mA	
				ICLK = 20 MHz*3		4.6	—		
			All peripheral operation: Normal	ICLK = 32 MHz*4		22.3	—		
				ICLK = 20 MHz*5		15.6	—		
			All peripheral operation: Max.	ICLK = 32 MHz*4		—	35		
				ICLK = 20 MHz*5		—	—		
		Sleep mode	No peripheral operation	ICLK = 32 MHz		3.4	—		
				ICLK = 20 MHz		3.3	—		
			All peripheral operation: Normal	ICLK = 32 MHz		12.8	—		
				ICLK = 20 MHz		9.8	—		
		All-module clock stop mode		ICLK = 32 MHz		3	—		
				ICLK = 20 MHz		3	—		
		Increase during BGO operation*6	Middle-speed operating mode 1A			21	—		
			Middle-speed operating mode 1B			19	—		
	Middle-speed operating modes 2A and 2B	Normal operating mode	No peripheral operation*2	ICLK = 32 MHz		4.7	—		
				ICLK = 16 MHz		3.4	—		
				ICLK = 8 MHz		2.7	—		
			All peripheral operation: Normal*4	ICLK = 32 MHz*3		21.7	—		
				ICLK = 16 MHz*3		12.3	—		
				ICLK = 8 MHz		7.6	—		
			All peripheral operation: Max.*4	ICLK = 32 MHz*3		—	34		
				ICLK = 16 MHz*3		—	—		
				ICLK = 8 MHz		—	—		
		Sleep mode	No peripheral operation	ICLK = 32 MHz		2.9	—		
				ICLK = 16 MHz		2.5	—		
				ICLK = 8 MHz		2.2	—		
			All peripheral operation: Normal	ICLK = 32 MHz		12.3	—		
				ICLK = 16 MHz		7.8	—		
				ICLK = 8 MHz		5.6	—		
		All-module clock stop mode		ICLK = 32 MHz		2.5	—		
				ICLK = 16 MHz		2.2	—		
				ICLK = 8 MHz		2.1	—		
		Increase during BGO operation*6	Middle-speed operating mode 1A			21	—		
			Middle-speed operating mode 1B			19	—		



Note 1. Average value of the tested middle samples during product evaluation.
Note 2. Average value of the tested upper-limit samples during product evaluation.

Figure 5.42 Voltage Dependency in Deep Software Standby Mode (DEEPCUT1 Bit = 1) (Reference Data) for Chip Version B with 512 Kbytes or Less of Flash Memory and 144 and 145 Pins



Note 1. Average value of the tested middle samples during product evaluation.
Note 2. Average value of the tested upper-limit samples during product evaluation.

Figure 5.43 Temperature Dependency in Deep Software Standby Mode (DEEPCUT1 Bit = 1) (Reference Data) for Chip Version B with 512 Kbytes or Less of Flash Memory and 144 and 145 Pins

Table 5.21 DC Characteristics (20)

Conditions: VCC = AVCC0 = 1.62 to 5.5 V, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +105°C

Item	Symbol	Typ.	Max.	Unit	Test Conditions
Permissible total consumption power*1	Pd	—	350	mW	Ta = –40 to 85°C
		—	150		85°C < Ta ≤ 105°C

Note: • Please contact Renesas Electronics sales office for derating of operation under Ta = +85°C to +105°C. Derating is the systematic reduction of load for the sake of improved reliability.
Note 1. Total power dissipated by the entire chip (including output currents)

Table 5.22 DC Characteristics (21)

Conditions: VCC = AVCC0 = 1.62 to 5.5 V, VREFH = 1.8 to AVCC0, VREFH0 = 1.62 to AVCC0,
VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Analog power supply current	During A/D conversion	I_{AVCC0}	—	1.0	3.2	mA	
	Temperature sensor operating, waiting for A/D conversion		—	60	200	µA	
	During D/A conversion (per channel)	I_{VREFH}*1	—	0.25	0.75	mA	
	Waiting for A/D, D/A conversion (all units)*2	—	—	0.2	5.0	µA	
Reference power supply current	During A/D conversion	I_{VREFH0}	—	0.1	0.2	mA	
	Waiting for A/D conversion		—	0.2	0.4	µA	

Note: • The values for A/D conversion apply when the sample and hold circuit is not in use.
Note 1. The reference power supply current is included in the power supply current value for D/A conversion.
Note 2. The value is the total value of I_{AVCC0} and I_{VREFH}.

Table 5.23 DC Characteristics (22)

Conditions: VCC = AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +105°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
RAM standby voltage	V_{RAM}	1.62	—	—	V	

Table 5.24 DC Characteristics (23)

Conditions: VCC = AVCC0 = 0 to 5.5 V, VREFH = VREFH0 = 0 to AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V,
T_a = –40 to +105°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
VCC rising gradient	SrVCC	0.02	—	20	ms/V	At cold start

5.3 AC Characteristics

[Chip versions A, B, and C]

Table 5.33 Operation Frequency Value (High-Speed Operating Mode)

Conditions: VCC = AVCC0 = 2.7 to 5.5 V, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +105°C

Item		Symbol	VCC	Unit
			2.7 to 5.5 V	
Maximum operating frequency	System clock (ICLK)	f_{max}	50	MHz
	FlashIF clock (FCLK)*1		32	
	Peripheral module clock (PCLKB)		32	
	Peripheral module clock (PCLKD)*2		50	
	External bus clock (BCLK)		25	
	BCLK pin output		12.5	

Note 1. The lower-limit frequency of FCLK is 4 MHz during programming or erasing of the flash memory.
Note 2. The lower-limit frequency of PCLKD is 1 MHz when the A/D converter is in use.

[Chip versions A, B, and C]

Table 5.34 Operation Frequency Value (MiddleSpeed Operating Mode 1A)

Conditions: VCC = AVCC0 = 1.62 to 5.5 V, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +105°C

Item		Symbol	VCC			Unit
			1.62 to 1.8 V	1.8 to 2.7 V	2.7 to 5.5 V	
Maximum operating frequency	System clock (ICLK)	f_{max}	20	32	32	MHz
	FlashIF clock (FCLK)*1		20	32	32	
	Peripheral module clock (PCLKB)		20	32	32	
	Peripheral module clock (PCLKD)*2		20	32	32	
	External bus clock (BCLK)		12	16	25	
	BCLK pin output		6	8	12.5	

Note 1. The VCC is 2.7 to 5.5 V and the lower-limit frequency of FCLK is 4 MHz during programming or erasing of the flash memory.
Note 2. The lower-limit frequency of PCLKD is 1 MHz when the A/D converter is in use.

[Chip versions A, B, and C]

Table 5.35 Operation Frequency Value (Middle-Speed Operating Mode 1B)

Conditions: VCC = AVCC0 = 1.62 to 5.5 V, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +105°C

Item		Symbol	VCC			Unit
			1.62 to 1.8 V	1.8 to 2.7 V	2.7 to 5.5 V	
Maximum operating frequency	System clock (ICLK)	f_{max}	20	32	32	MHz
	FlashIF clock (FCLK)*1		20	32	32	
	Peripheral module clock (PCLKB)		20	32	32	
	Peripheral module clock (PCLKD)*2		20	32	32	
	External bus clock (BCLK)		12	16	25	
	BCLK pin output		6	8	12.5	

Note 1. The VCC is 1.62 to 3.6 V and the lower-limit frequency of FCLK is 4 MHz during programming or erasing of the flash memory.
Note 2. The lower-limit frequency of PCLKD is 1 MHz when the A/D converter is in use.

5.3.1 Clock Timing

Table 5.41 BCLK Timing (1)

Conditions: VCC = AVCC0 = 2.7 to 5.5 V, VSS = AVSS0 = VREFL = VREFL0 = 0 V,
fBCLK = up to 25 MHz (BCLK pin output frequency = up to 12.5 MHz), T_a = –40 to +105°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
BCLK pin output cycle time	t_{Bcyc}	80	—	—	ns	Figure 5.59
BCLK pin output high pulse width*1	t_{CH}	20	—	—	ns	
BCLK pin output low pulse width*1	t_{CL}	20	—	—	ns	
BCLK pin output rising time	t_{Cr}	—	—	15	ns	
BCLK pin output falling time	t_{Cf}	—	—	15	ns	

Note 1. When the EXTAL external clock input is used with divided by 1 (SCKCR.BCK[3:0] bits = 0000b and BCKCR.BCLKDIV bit = 0) to output from the BCLK pin, the above should be satisfied with a duty cycle of 45 to 55%.

Table 5.42 BCLK Timing (2)

Conditions: VCC = AVCC0 = 1.8 to 2.7 V, VSS = AVSS0 = VREFL = VREFL0 = 0 V,
fBCLK = up to 16 MHz (BCLK pin output frequency= up to 8 MHz), T_a = –40 to +105°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
BCLK pin output cycle time	t_{Bcyc}	125	—	—	ns	Figure 5.59
BCLK pin output high pulse width*1	t_{CH}	30	—	—	ns	
BCLK pin output low pulse width*1	t_{CL}	30	—	—	ns	
BCLK pin output rising time	t_{Cr}	—	—	25	ns	
BCLK pin output falling time	t_{Cf}	—	—	25	ns	

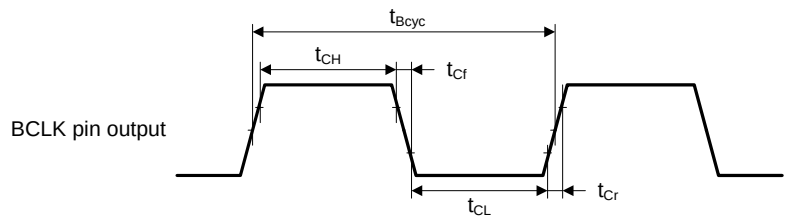
Note 1. When the EXTAL external clock input is used with divided by 1 (SCKCR.BCK[3:0] bits = 0000b and BCKCR.BCLKDIV bit = 0) to output from the BCLK pin, the above should be satisfied with a duty cycle of 45 to 55%.

Table 5.43 BCLK Timing (3)

Conditions: VCC = AVCC0 = 1.62 to 1.8 V, VSS = AVSS0 = VREFL=VREFL0 = 0 V,
fBCLK = up to 12 MHz (BCLK pin output frequency = up to 6 MHz), T_a = –40 to +105°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
BCLK pin output cycle time	t_{Bcyc}	166.6	—	—	ns	Figure 5.59
BCLK pin output high pulse width*1	t_{CH}	42	—	—	ns	
BCLK pin output low pulse width*1	t_{CL}	42	—	—	ns	
BCLK pin output rising time	t_{Cr}	—	—	35	ns	
BCLK pin output falling time	t_{Cf}	—	—	35	ns	

Note: • Set high driving ability for the output port pin to be used for the BCLK pin function.
Note 1. When the EXTAL external clock input is used with divided by 1 (SCKCR.BCK[3:0] bits = 0000b and BCKCR.BCLKDIV bit = 0) to output from the BCLK pin, the above should be satisfied with a duty cycle of 45 to 55%.



Test conditions: VOH = VCC × 0.7, VOL = VCC × 0.3, IOH = –1.0 mA, IOL = 1.0 mA, C = 30 pF

Figure 5.59 BCLK Pin Output Timing

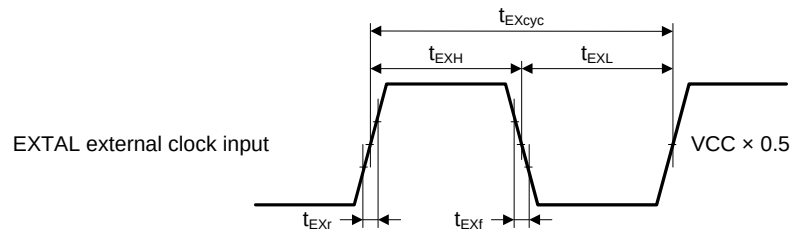


Figure 5.60 EXTAL External Clock Input Timing

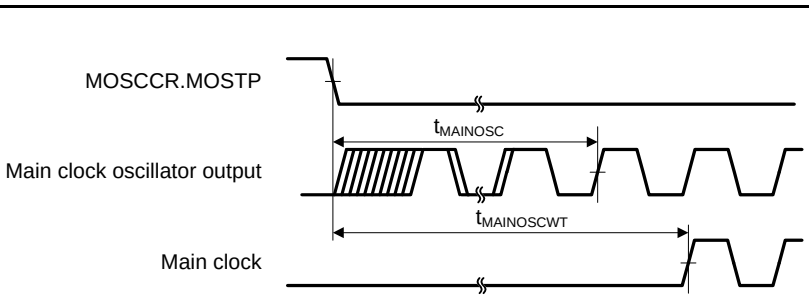


Figure 5.61 Main Clock Oscillation Start Timing

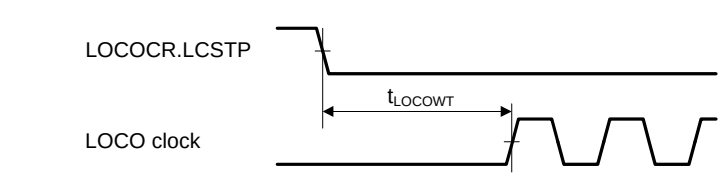


Figure 5.62 LOCO Clock Oscillation Start Timing

5.3.2 Reset Timing

Table 5.45 Reset Timing

Conditions: VCC = AVCC0 = 1.62 to 5.5 V, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
RES# pulse width	Power-on	t_{RESWP}	8	—	—	ms	Figure 5.70
	Deep software standby mode	t_{RESWD}	8	—	—	ms	Figure 5.71
	Software standby mode, low-speed operating modes 1 and 2	t_{RESWS}	1	—	—	ms	
	Programming or erasure of the ROM or E2 DataFlash memory or blank checking of the E2 DataFlash memory	t_{RESWF}	200	—	—	µs	
	Other than above	t_{RESW}	200	—	—	µs	
Wait time after RES# cancellation		t_{RESWT}	—	—	912	µs	Figure 5.70
Internal reset time (independent watchdog timer reset, watchdog timer reset, software reset)		t_{RESW2}	—	—	1.4	ms	

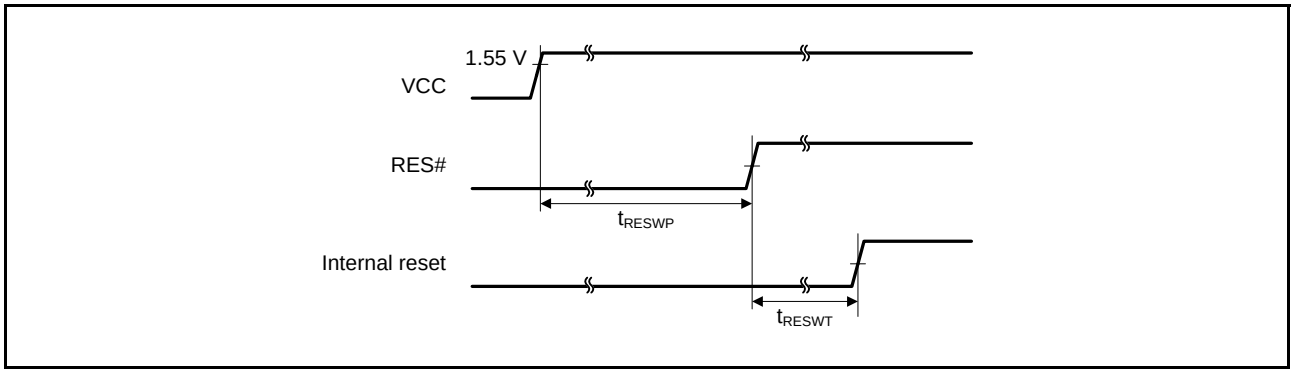


Figure 5.70 Reset Input Timing at Power-On

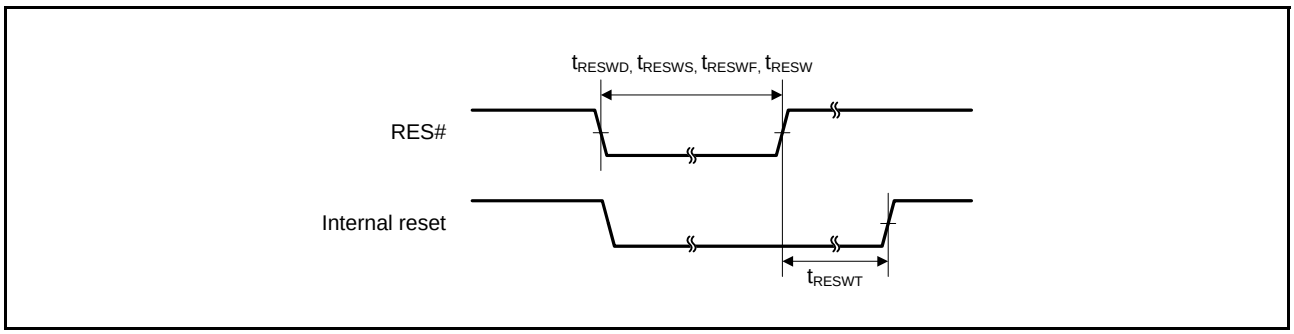


Figure 5.71 Reset Input Timing

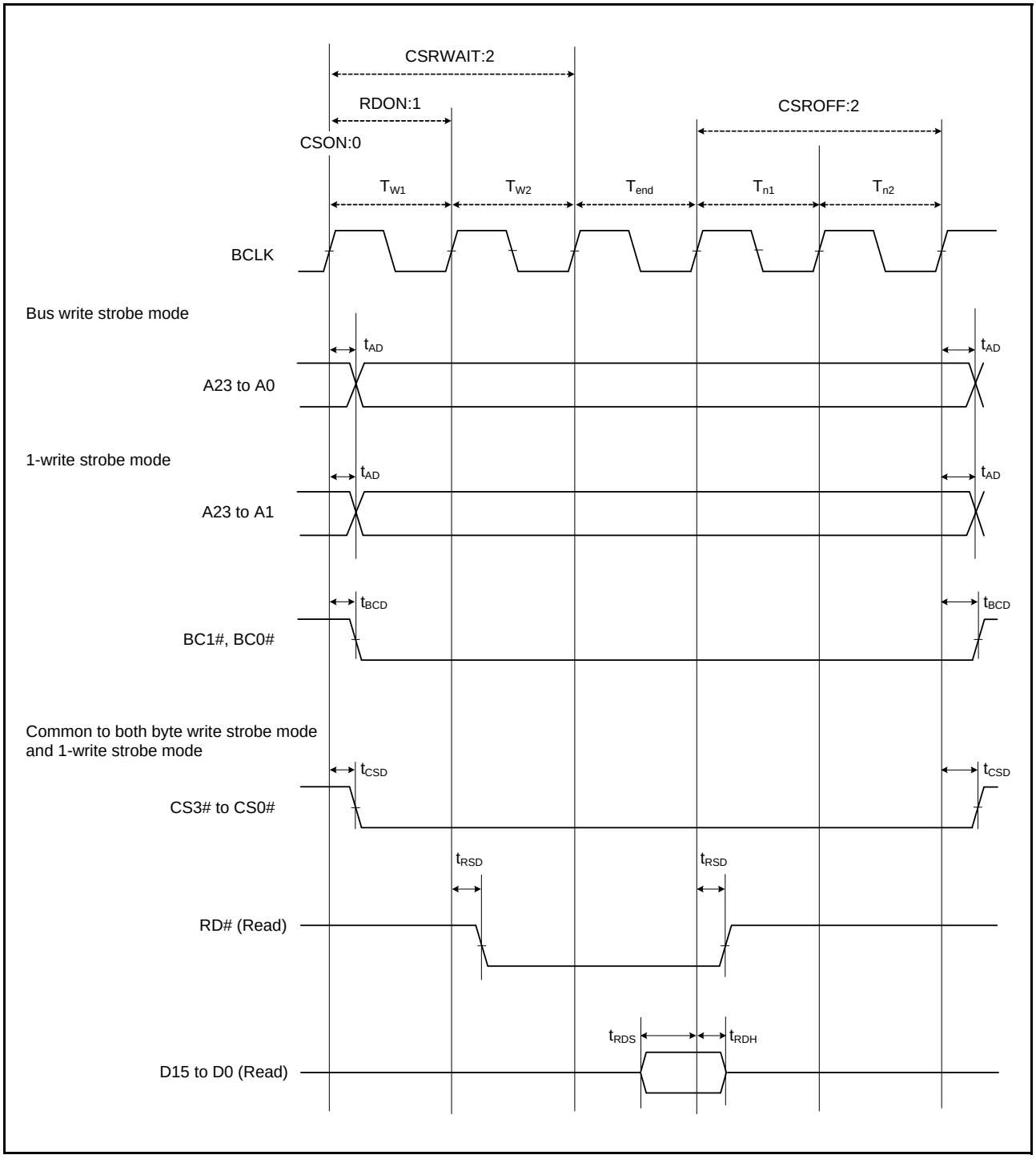
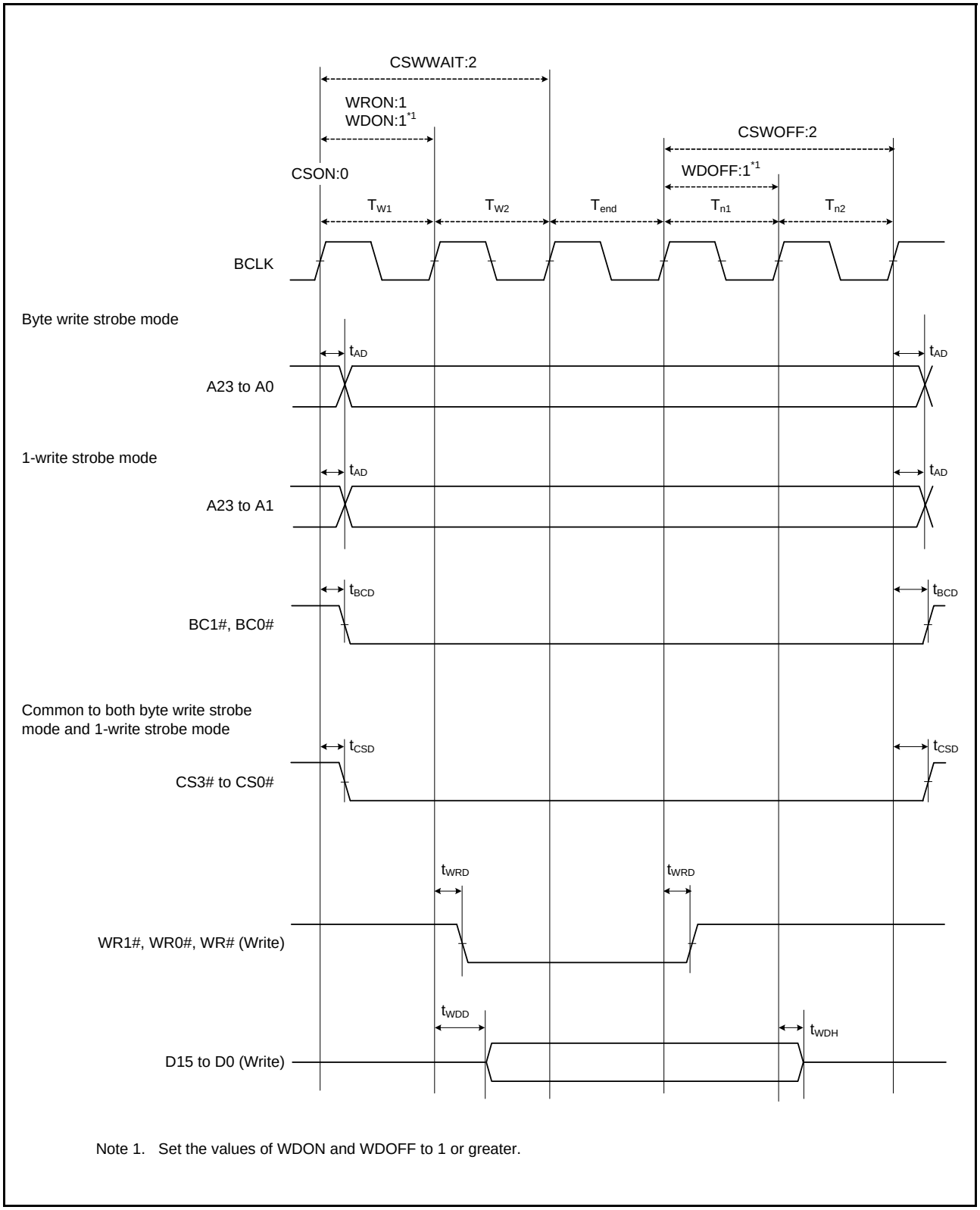


Figure 5.76 External Bus Timing/Normal Read Cycle (Bus Clock Synchronized)



Note 1. Set the values of WDON and WDOFF to 1 or greater.

Figure 5.77 External Bus Timing/Normal Write Cycle (Bus Clock Synchronized)

Item				Symbol	Min.	Max.	Unit*1	Test Conditions
RSPI	Data input setup time	Master	2.7 V ≤ VCC ≤ 5.5 V	t_{SU}	10	—	ns	C = 30pF Figure 5.92 to Figure 5.97
			1.8 V ≤ VCC < 2.7 V		25	—		
			1.62 V ≤ VCC < 1.8 V		30	—		
		Slave			25 – t_{Pcyc}	—		
	Data input hold time	Master	PCLKB set to a division ratio other than divided by 2	t_H	t_{Pcyc}	—	ns	
			PCLKB set to divided by 2*2	t_{HF}	0	—		
		Slave		t_H	20 + 2 × t_{Pcyc}	—		
	SSL setup time	Master		t_{LEAD}	1	8	t_{SPcyc}	
		Slave			4	—	t_{Pcyc}	
	SSL hold time	Master		t_{LAG}	1	8	t_{SPcyc}	
		Slave			4	—	t_{Pcyc}	
	Data output delay time	Master	2.7 V ≤ VCC ≤ 5.5 V	t_{OD}	—	14	ns	
			1.8 V ≤ VCC < 2.7 V		—	20		
			1.62 V ≤ VCC < 1.8 V		—	25		
		Slave	2.7 V ≤ VCC ≤ 5.5 V		—	3 × t_{Pcyc} + 65		
			1.8 V ≤ VCC < 2.7 V		—	3 × tPcyc +85		
			1.62 V ≤ VCC < 1.8 V		—	3 × tPcyc +95		
	Data output hold time	Master		t_{OH}	0	—	ns	
		Slave			0	—		
	Successive transmission delay time	Master		t_{TD}	t_{SPcyc} + 2 × t_{Pcyc}	8 × t_{SPcyc} + 2 × t_{Pcyc}	ns	
		Slave			4 × t_{Pcyc}	—		
	MOSI and MISO rise/fall time	Output	2.7 V ≤ VCC ≤ 5.5 V	t_{Dr}, t_{Df}	—	10	ns	
			1.8 V ≤ VCC < 2.7 V		—	15		
			1.62 V ≤ VCC < 1.8 V		—	20		
		Input			—	1	µs	
	SSL rise/fall time	Output	2.7 V ≤ VCC ≤ 5.5 V	t_{SSLr}, t_{SSLf}	—	10	ns	
			1.8 V ≤ VCC < 2.7 V		—	15		
			1.62 V ≤ VCC < 1.8 V		—	20		
		Input			—	1	µs	
	Slave access time		2.7 V ≤ VCC ≤ 5.5 V	t_{SA}	—	6	t_{Pcyc}	C = 30pF Figure 5.96 and Figure 5.97
			1.8 V ≤ VCC < 2.7 V		—	7		
			1.62 V ≤ VCC < 1.8 V		—	7		
	Slave output release time		2.7 V ≤ VCC ≤ 5.5 V	t_{REL}	—	5	t_{Pcyc}	
			1.8 V ≤ VCC < 2.7 V		—	6		
			1.62 V ≤ VCC < 1.8 V		—	6		

Note 1. t_{Pcyc}: PCLK cycle
Note 2. Divided by 2 can be set only in packages with 768 Kbytes/1 Mbyte of flash memory or 144/145 pins.

Table 5.72 Power-on Reset Circuit and Voltage Detection Circuit Characteristics (2)

Conditions: VCC = AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Voltage detection level	Voltage detection circuit (LVD2)*1	V_{det2_0}	4.00	4.15	4.30	V	Figure 5.107 At falling edge VCC
		V_{det2_1}	3.85	4.00	4.15		
		V_{det2_2}	3.70	3.85	4.00		
		V_{det2_3}	3.55	3.70	3.85		
		V_{det2_4}	3.40	3.55	3.70		
		V_{det2_5}	3.25	3.40	3.55		
		V_{det2_6}	3.10	3.25	3.40		
		V_{det2_7}	2.95	3.10	3.25		
		V_{det2_8}	2.85	2.95	3.05		
		V_{det2_9}	2.70	2.80	2.90		
		V_{det2_A}	2.55	2.65	2.75		
		V_{det2_B}	2.40	2.50	2.60		
		V_{det2_C}	2.25	2.35	2.45		
		V_{det2_D}	2.10	2.20	2.30		
		V_{det2_E}	1.95	2.05	2.15		
		V_{det2_F}	1.80	1.90	2.00		
		V_{CMPA2}	1.18	1.33	1.48		EXVCCINP2 = 1
Internal reset time	Power-on reset time	t_{POR}	—	9	—	ms	Figure 5.104
	Voltage monitoring 0 reset time	t_{LVD0}	—	9	—		Figure 5.105
	Voltage monitoring 1 reset time	t_{LVD1}	—	1.4	—		Figure 5.106
	Voltage monitoring 2 reset time	t_{LVD2}	—	1.4	—		Figure 5.107
Minimum VCC down time*2		t_{VOFF}	200	—	—	µs	Figure 5.103
Response delay time		t_{det}	—	—	200	µs	Figure 5.104
LVD operation stabilization time (after LVD is enabled)		$Td_{(E-A)}$	—	—	15	µs	Figure 5.106 and Figure 5.107
Power-on reset enable time		$t_{W(POR)}$	1	—	—	ms	Figure 5.104 VCC = 0.9 V or lower
Hysteresis width (LVD1 and LVD2)		V_{LVH}	—	100	—	mV	When selection is from among VdetX_0 to 7.
			—	50	—		When selection is from among VdetX_8 to F.

Note: • These characteristics apply when noise is not superimposed on the power supply.

Note 1. # in the symbol Vdet2_# denotes the value of the LVDLVLR.LVD2LVL[3:0] bits.

Note 2. The minimum VCC down time indicates the time when VCC is below the minimum value of voltage detection levels V_{POR}, V_{det0}, V_{det1}, and V_{det2} for the POR/LVD.

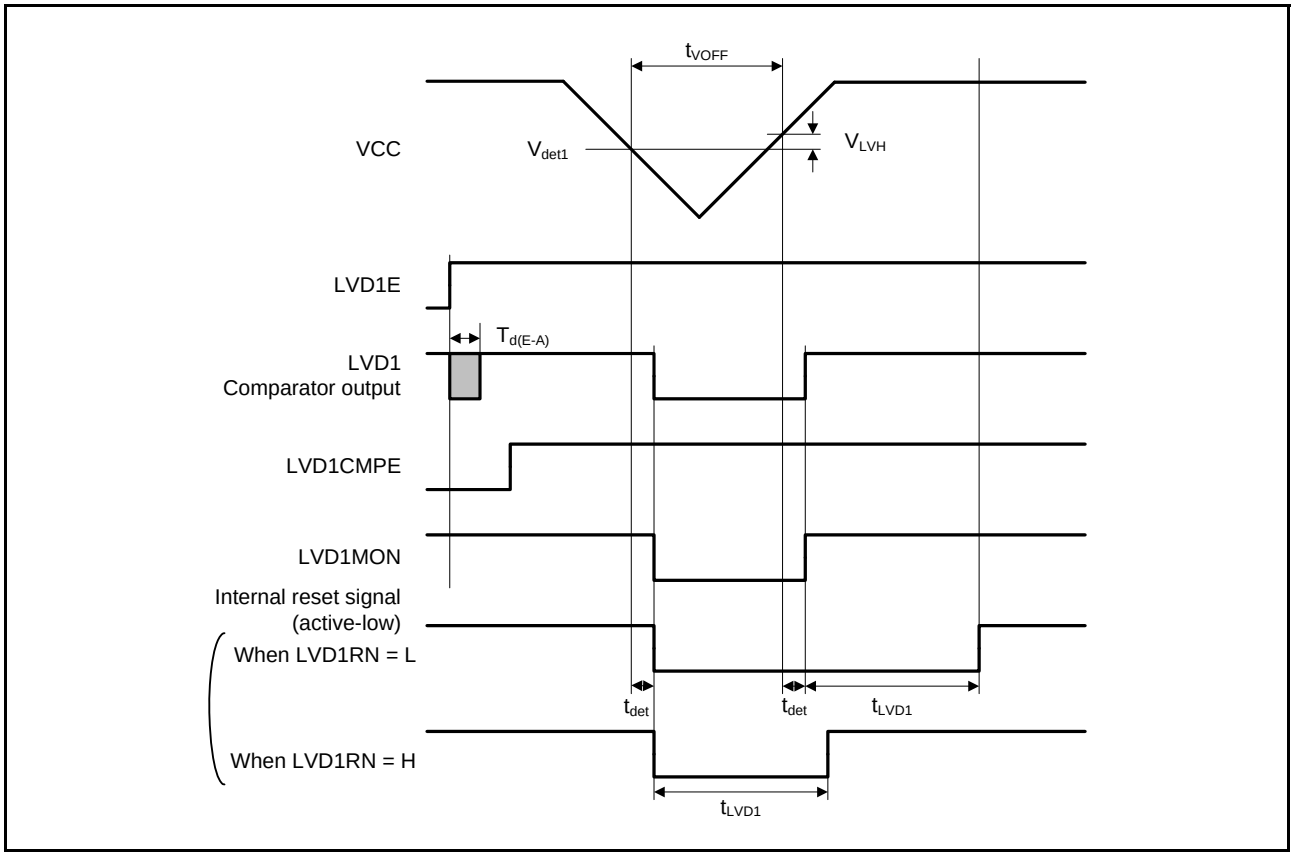


Figure 5.106 Voltage Detection Circuit Timing (V_{det1})

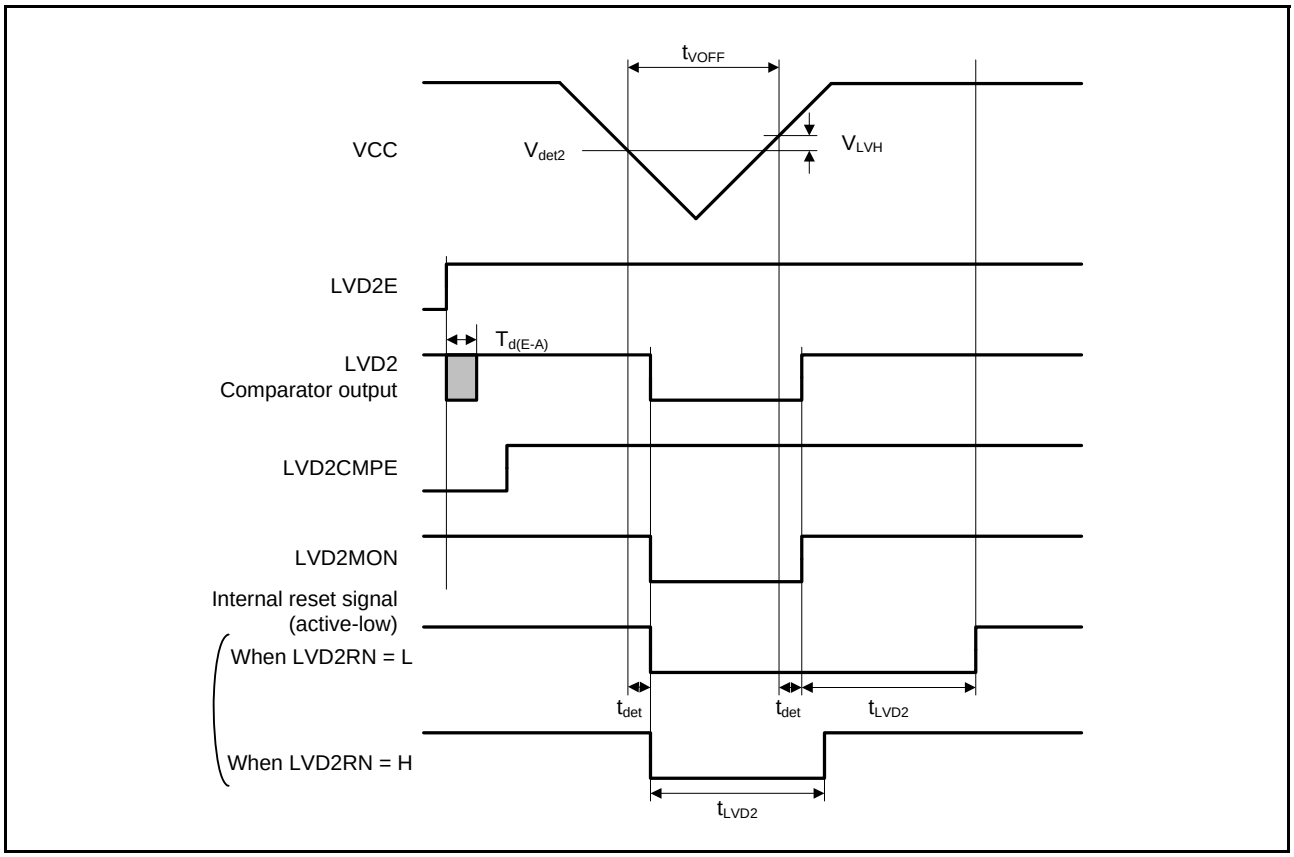


Figure 5.107 Voltage Detection Circuit Timing (V_{det2})

[Chip versions A and C]

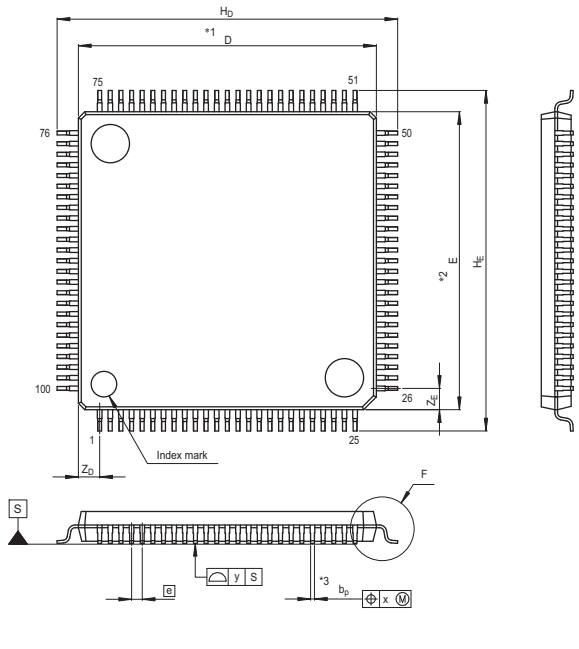
Table 5.77 ROM (Flash Memory for Code Storage) Characteristics (4) : middle-speed operating mode 1B

Conditions: VCC = AVCC0 = 1.62 to 3.6 V, VREFH = VREFH0 = AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V
Temperature range for the programming/erasure operation: T_a = –40 to +105°C

Item		Symbol	FCLK = 4 MHz			FCLK = 32 MHz*1			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Programming time when N_{PEC} ≤ 100 times	2 bytes	t_{P2}	—	0.69	6.0	—	0.30	3.5	ms
	8 bytes	t_{P8}	—	0.69	6.0	—	0.30	3.5	
	128 bytes	t_{P128}	—	1.76	14.2	—	0.85	8.3	
Programming time when N_{PEC} > 100 times	2 bytes	t_{P2}	—	0.81	7.1	—	0.35	4.2	ms
	8 bytes	t_{P8}	—	0.81	7.6	—	0.35	4.5	
	128 bytes	t_{P128}	—	1.99	17.5	—	0.96	10	
Erasure time when N_{PEC} ≤ 100 times	2 Kbytes	t_{E2K}	—	24.5	113.7	—	19.0	46	ms
Erasure time when N_{PEC} > 100 times	2 Kbytes	t_{E2K}	—	29.8	225.8	—	23.2	90 (1000 times ≥ N_{PEC} > 100 times), 98 (10000 times ≥ N_{PEC} > 1000 times)	ms
Suspend delay time during programming (in programming/erasure priority mode)		t_{SPD}	—	—	1.7	—	—	1.6	ms
First suspend delay time during programming (in suspend priority mode)		t_{SPSD1}	—	—	220	—	—	120	µs
Second suspend delay time during programming (in suspend priority mode)		t_{SPSD2}	—	—	1.7	—	—	1.6	ms
Suspend delay time during erasing (in programming/erasure priority mode)		t_{SED}	—	—	1.7	—	—	1.6	ms
First suspend delay time during erasing (in suspend priority mode)		t_{SESD1}	—	—	220	—	—	120	µs
Second suspend delay time during erasing (in suspend priority mode)		t_{SESD2}	—	—	1.7	—	—	1.6	ms
FCU reset time		t_{FCUR}	20 µs or longer and FCLK × 6 or greater	—	—	20 µs or longer and FCLK × 6 or greater	—	—	µs

Note 1. The operating frequency is 20 MHz (max.) when the voltage is in the range from 1.62 V to less than 1.8 V.

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LFQFP100-14x14-0.50	PLQP0100KB-A	100P6Q-A / FP-100U / FP-100UV	0.6g



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	13.9	14.0	14.1
E	13.9	14.0	14.1
A_2	—	1.4	—
H_D	15.8	16.0	16.2
H_E	15.8	16.0	16.2
A	—	—	1.7
A_1	0.05	0.1	0.15
b_p	0.15	0.20	0.25
b_1	—	0.18	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
Z_D	—	1.0	—
Z_E	—	1.0	—
L	0.35	0.5	0.65
L_1	—	1.0	—

Figure G 100-Pin LQFP (PLQP0100KB-A)

REVISION HISTORY	RX210 Group Datasheet

Rev.	Date	Description	
		Page	Summary
0.50	Apr.15, 2011	—	First edition, issued
0.90	Aug.10, 2011	1. Overview	
		4	Table 1.1 Outline of Specifications: Power supply voltage/ Operating frequency, changed
		17, 21, 24, 26	Table 1.5 to Table 1.8 List of Pins and Pin Functions (Pin name: LVCMP2 → CMPA2), changed
		2. CPU	
		51	Table 2.14 Instructions that are Converted into Multiple Micro-Operations (multiplier: 32 × 32 → 64 bits), (memory source operand), added
		4. I/O Registers	
		63	Table 5.1 List of I/O Registers (Address Order), SOSCWTCR, LOCOWTCR2, HOCOWTCR2, added
		114 to 116	Table 5.1 List of I/O Registers (Address Order): Interrupt source priority register, changed
		5. Electrical Characteristics	
		85 to 137	Newly added
1.20	Nov 28, 2012	All	Information on chip versions A, B, and C, corresponding descriptions and notes, added 48-pin products added, PLQP0080JA-A 14 × 14 mm, 0.65-mm pitch, package deleted
		Features	
		1	Description changed
		1. Overview	
		2	1.1 Outline of Specifications: Description, changed
		2 to 5	Table 1.1 Outline of Specifications, changed Note 1, added
		6	Table 1.2 Comparison of Functions for Different Packages, changed
		7	Table 1.3 List of Products, changed
		8 to 10	Tables 1.4 to 1.7 List of Products, added
		11	Figure 1.1 How to Read the Product Part No., Memory Capacity, and Package Type: G item added
		12	Figure 1.2 Block Diagram, changed
		13	Table 1.8 Pin Functions: Power supply and On-chip emulator, changed
		13	Table 1.8 Pin Functions: Multiplexed bus, added
		18	Figure 1.4 Pin Assignments of the 100-Pin LQFP, changed
		21	Figure 1.7 Pin Assignments of the 48-Pin LQFP, added
		23	Table 1.9 List of Pins and Pin Functions (100-Pin TFLGA): Pin No. G4, changed
		25	Table 1.10 List of Pins and Pin Functions (100-Pin LQFP): Pin No. 21, changed
		28	Table 1.11 List of Pins and Pin Functions (80-Pin LQFP): Pin No. 19, changed
		30	Table 1.12 List of Pins and Pin Functions (64-Pin LQFP): Pin No. 15, changed
		3. Address Space	
		37	Figure 3.1 Memory Map in Each Operating Mode: Note 2, changed
		4. I/O Registers	
		41 to 63	Table 4.1 List of I/O Registers (Address Order): Number of Access, changed Voltage regulator control register, Timeout internal counter L, Timeout internal counter U, and PLL power control register, added
		63	Table 4.1 List of I/O Registers (Address Order): Notes 1 and 2, added
		—	Table 4.1 List of I/O Registers (Address Order): LOCO Wait Control Register 2 (LOCOWTCR2), deleted
		5. Electrical Characteristics	
		64 to 152	Description added
1.30	Jan 22, 2013	Features	
		1	On-chip flash memory for code, no wait states, On-chip SRAM, no wait states, Real-time clock, Up to 15 communications channels, Up to 20 extended-function timers, changed
		1.Overview	
		2 to 6	Table 1.1 Outline of Specifications, changed
		7	Table 1.2 Comparison of Functions for Different Packages, changed
		9	Table 1.4 List of Products Chip Version B: D Version (Ta = -40 to +85°C), changed
		10	Table 1.5 List of Products Chip Version B: G Version (Ta = -40 to +105°C), changed

Rev.	Date	Description	
		Page	Summary
1.40	Feb 19, 2013	96	Table 5.11 DC Characteristics (10), changed
		105	Table 5.14 DC Characteristics (13), changed
		114	Table 5.17 DC Characteristics (16), changed
		115	Figure 5.31 Voltage Dependency in Software Standby Mode (SOFTCUT[2:0] Bits = 110b) (Reference Data) for Chip Version B with 768 Kbytes/1 Mbyte of Flash Memory and 100 to 145 Pins, changed
		116	Figure 5.32 Temperature Dependency in Software Standby Mode (SOFTCUT[2:0] Bits = 110b) (Reference Data) for Chip Version B with 768 Kbytes/1 Mbyte of Flash Memory and 100 to 145 Pins, changed
		118	Table 5.18 DC Characteristics (17), changed
		119, 120	Table 5.19 DC Characteristics (18), changed
		121 to 123	Figure 5.35 Voltage Dependency in High-Speed Operating Mode (Reference Data) for Chip Version B with 512 Kbytes or Less of Flash Memory and 144 and 145 Pins to Figure 5.39 Voltage Dependency in Low-Speed Operating Mode 2 (Reference Data) for Chip Version B with 512 Kbytes or Less of Flash Memory and 144 and 145 Pins, added
		124	Table 5.20 DC Characteristics (19), changed
		125 to 127	Figure 5.40 Voltage Dependency in Software Standby Mode (SOFTCUT[2:0] Bits = 110b) (Reference Data) for Chip Version B with 512 Kbytes or Less of Flash Memory and 144 and 145 Pins to Figure 5.43 Temperature Dependency in Deep Software Standby Mode (DEEPCUT1 Bit = 1) (Reference Data) for Chip Version B with 512 Kbytes or Less of Flash Memory and 144 and 145 Pins, added
		128	Table 5.22 DC Characteristics (21), changed, Note 2 added
		144	Table 5.44 Clock Timing: Note 5, changed
		154	Table 5.49 Bus Timing (1), Table 5.50 Bus Timing (2), changed
		155	Table 5.51 Bus Timing (3), changed
		160	Table 5.52 Bus Timing (Multiplexed Bus) (1), Table 5.53 Bus Timing (Multiplexed Bus) (2), changed
		161	Table 5.54 Bus Timing (Multiplexed Bus) (3), changed
		164	Table 5.56 Timing of On-Chip Peripheral Modules (2), changed
		166	Table 5.57 Timing of On-Chip Peripheral Modules (3), changed
		177	Table 5.61 A/D Conversion Characteristics (1), Note 3, deleted Figure 5.99 AVCC to AVREFH Voltage Range, added
		179	Table 5.64 A/D Conversion Characteristics (2), Note 3, Table 5.65 A/D Conversion Characteristics (3), Note 3, deleted
		186	Table 5.72 Power-on Reset Circuit and Voltage Detection Circuit Characteristics (2), changed
1.50	Oct 18, 2013	All	69-Pin WLBGA package products, added
		Features	
		1	SWBG0069LA-A 3.91 × 4.26mm, 0.40-mm pitch, ■ Applications, added
		1. Overview	
		2	1.1 Outline of Specifications, changed
		2 to 6	Table 1.1 Outline of Specifications, Note 2, changed
		7	Table 1.2 Comparison of Functions for Different Packages, changed
		8	Table 1.3 List of Products Chip Version A: D Version (Ta = -40 to +85°C), changed, Note, added
		9	Table 1.4 List of Products Chip Version B: D Version (Ta = -40 to +85°C), Note 1, changed, Note added
		10	Table 1.5 List of Products Chip Version B: G Version (Ta = -40 to +105°C), Note, changed, Note 1, deleted
		11	Table 1.6 List of Products Chip Version C: D Version (Ta = -40 to +85°C), Table 1.7 List of Products Chip Version C: G Version (Ta = -40 to +105°C), Note, changed
		12	Figure 1.1 How to Read the Product Part No., Memory Capacity, and Package Type, changed
		23	Figure 1.8 Pin Assignments of the 69-Pin WLBGA, added
		43, 44	Table 1.14 List of Pins and Pin Functions (69-Pin WLBGA), added
		5. Electrical Characteristics	
		134	Table 5.21 DC Characteristics (20) Note, added
		149, 150	Table 5.44 Clock Timing Note 6, Note 7, added
		183	Table 5.61 A/D Conversion Characteristics (1) Note, changed, Note 4, deleted
		184	Table 5.62 Channel Classification for A/D Converter, changed
		185	Table 5.64 A/D Conversion Characteristics (2) Note, changed
		Appendix 1. Package Dimensions	
		211	Figure E 69-Pin WLBGA (SWBG0069LA-A), added