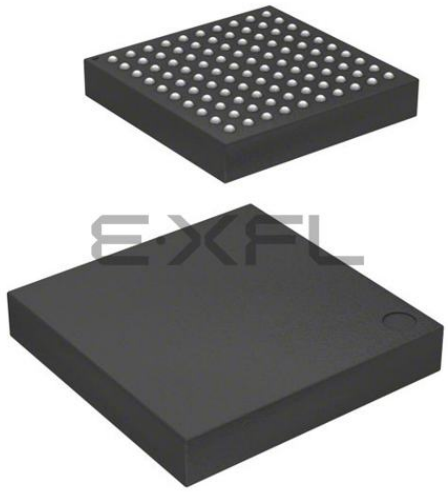

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Details	
Product Status	Not For New Designs
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	EBI/EMI, I²C, SCI, SPI
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	84
Program Memory Size	384KB (384K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	1.62V ~ 5.5V
Data Converters	A/D 16x12b; D/A 2x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TFLGA
Supplier Device Package	100-TFLGA (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f52107cdlj-u0

Table 1.1 Outline of Specifications (4 / 5)

Classification	Module/Function	Description
Communication functions	Serial communications interfaces (SCIc, SCId)	• 13 channels (channel 0 to 11: SCIc, channel 12: SCId) • Serial communications modes: Asynchronous, clock synchronous, and smart-card interface • On-chip baud rate generator allows selection of the desired bit rate • Choice of LSB-first or MSB-first transfer • Average transfer rate clock can be input from TMR timers (SCI5, SCI6, and SCI12) • Simple IIC • Simple SPI • Master/slave mode supported (SCId only) • Start frame and information frame are included (SCId only)
	I^2C bus interface (RIIC)	• 1 channel • Communications formats: I^2C bus format/SMBus format • Master/slave selectable • Supports the fast mode
	Serial peripheral interface (RSPI)	• 1 channel • Transfer facility Using the MOSI (master out, slave in), MISO (master in, slave out), SSL (slave select), and RSPI clock (RSPCK) signals enables serial transfer through SPI operation (four lines) or clock-synchronous operation (three lines) • Capable of handling serial transfer as a master or slave • Data formats • Choice of LSB-first or MSB-first transfer The number of bits in each transfer can be changed to any number of bits from 8 to 16, 20, 24, or 32 bits. 128-bit buffers for transmission and reception Up to four frames can be transmitted or received in a single transfer operation (with each frame having up to 32 bits) • Double buffers for both transmission and reception
12-bit A/D converter (S12ADb)		• 12 bits (16 channels × 1 unit) • 12-bit resolution • Minimum conversion time: 1.0 μs per channel (in operation with ADCLK at 50 MHz) • Operating modes Scan mode (single scan mode, continuous scan mode, and group scan mode) • Sample-and-hold function • Self-diagnosis for the A/D converter • Assistance in detecting disconnected analog inputs • Double-trigger mode (duplication of A/D conversion data) • A/D conversion start conditions A software trigger, a trigger from a timer (MTU), an external trigger signal, or ELC
Temperature sensor (TEMPSa)		• Outputs the voltage that changes depending on the temperature • PGA gain switchable: Four levels according to the voltage range
D/A converter (DA)		• 2 channels • 10-bit resolution • Output voltage: 0 V to VREFH
CRC calculator (CRC)		• CRC code generation for arbitrary amounts of data in 8-bit units • Select any of three generating polynomials: $X^8 + X^2 + X + 1$, $X^{16} + X^{15} + X^2 + 1$, or $X^{16} + X^{12} + X^5 + 1$ • Generation of CRC codes for use with LSB-first or MSB-first communications is selectable.
Comparator A (CMPA)		• 2 channels • Comparison of reference voltage and analog input voltage
Comparator B (CMPB)		• 2 channels • Comparison of reference voltage and analog input voltage
Data Operation Circuit (DOC)		Comparison, addition, and subtraction of 16-bit data
Power supply voltage/Operating frequency		VCC = 1.62 to 1.8 V: 20 MHz, VCC = 1.8 to 2.7 V: 32 MHz, VCC = 2.7 to 5.5 V: 50 MHz
Operating temperature		D version: −40 to +85°C, G version: −40 to +105°C*2

Table 1.5 List of Products Chip Version B: G Version (Ta = –40 to +105°C)

Group	Part No.	Orderable Part No.	Package	ROM Capacity	RAM Capacity	E2 DataFlash	Operating Frequency (Max.)	Operating Temperature
RX210	R5F5210BBGFB	R5F5210BBGFB#30	PLQP0144KA-A	1 Mbytes	96 Kbytes	8 Kbytes	50 MHz	–40 to +105°C
	R5F5210BBGFP	R5F5210BBGFP#30	PLQP0100KB-A					
	R5F5210ABGFB	R5F5210ABGFB#30	PLQP0144KA-A	768 Kbytes				
	R5F5210ABGFP	R5F5210ABGFP#30	PLQP0100KB-A					
	R5F52108BGFB	R5F52108BGFB#30	PLQP0144KA-A	512 Kbytes	64 Kbytes			
	R5F52107BGFB	R5F52107BGFB#30	PLQP0144KA-A	384 Kbytes				
	R5F52106BGFB	R5F52106BGFB#30	PLQP0144KA-A	256 Kbytes	32 Kbytes			
	R5F52106BGFP	R5F52106BGFP#30	PLQP0100KB-A					
	R5F52106BGFN	R5F52106BGFN#30	PLQP0080KB-A					
	R5F52106BGFM	R5F52106BGFM#30	PLQP0064KB-A					
	R5F52106BGFL	R5F52106BGFL#30	PLQP0048KB-A					
	R5F52106BGFF	R5F52106BGFF#V0	PTLG0100JA-A					
	R5F52106BGFK	R5F52106BGFK#30	PLQP0064GA-A					
	R5F52105BGFB	R5F52105BGFB#30	PLQP0144KA-A	128 Kbytes	20 Kbytes			
	R5F52105BGFP	R5F52105BGFP#30	PLQP0100KB-A					
	R5F52105BGFN	R5F52105BGFN#30	PLQP0080KB-A					
	R5F52105BGFM	R5F52105BGFM#30	PLQP0064KB-A					
	R5F52105BGFL	R5F52105BGFL#30	PLQP0048KB-A					
	R5F52105BGFF	R5F52105BGFF#V0	PLQP0080JA-A					
	R5F52105BGFK	R5F52105BGFK#30	PLQP0064GA-A					
	R5F52104BGFM	R5F52104BGFM#30	PLQP0064KB-A	96 Kbytes	16 Kbytes			
	R5F52104BGFL	R5F52104BGFL#30	PLQP0048KB-A					
	R5F52104BGFF	R5F52104BGFF#V0	PLQP0080JA-A					
	R5F52103BGFM	R5F52103BGFM#30	PLQP0064KB-A	64 Kbytes	12 Kbytes			
	R5F52103BGFL	R5F52103BGFL#30	PLQP0048KB-A					
	R5F52103BGFF	R5F52103BGFF#V0	PLQP0080JA-A					

Note: • Please contact Renesas Electronics sales office for derating of operation under Ta = +85°C to +105°C. Derating is the systematic reduction of load for the sake of improved reliability.

Note: • Orderable part numbers are current as of when this manual was published. Please make sure to refer to the relevant product page on the Renesas website for the latest part numbers.

Table 1.10 List of Pins and Pin Functions (144-Pin LQFP) (2 / 4)

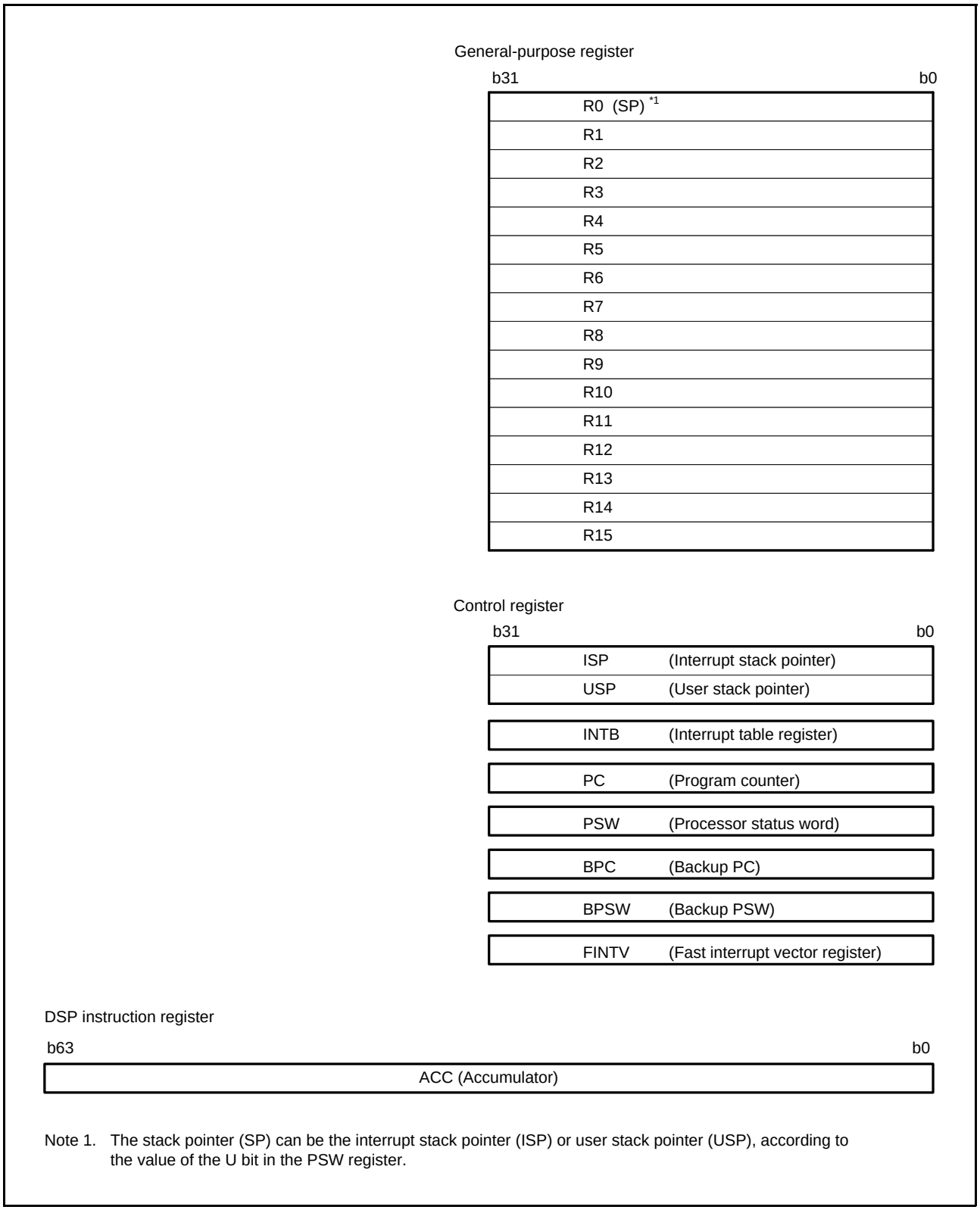
Pin No.	Power Supply, Clock, System Control	I/O Port	External Bus	Timers (MTU, TMR, POE)	Communications (SCIc, SCId, RSPI, RIIC)	Others
40		P16		MTIOC3C/MTIOC3D/ TMO2/TIOCB1/TCLKC	TXD1/SMOSI1/SSDA1/ MOSIA/SCL-DS/RXD3/ SMISO3/SSCL3	IRQ6/RTCOUT/ ADTRG0#
41		P86		TIOCA0		
42		P15		MTIOC0B/MTCLKB/ TMCI2/TIOCB2/TCLKB	RXD1/SMISO1/SSCL1/ SCK3	IRQ5
43		P14		MTIOC3A/MTCLKA/ TMRI2/TIOCB5/TCLKA	CTS1#/RTS1#/SS1#	IRQ4
44		P13		MTIOC0B/TMO3/ TIOCA5	SDA/TXD2/SMOSI2/ SSDA2	IRQ3
45		P12		TMCI1	SCL/RXD2/SMISO2/ SSCL2	IRQ2
46		PH3		TMCI0		
47		PH2		TMRI0		IRQ1
48		PH1		TMO0		IRQ0
49		PH0				CACREF
50		P56		MTIOC3C/TIOCA1		
51		P55	WAIT#	MTIOC4D/TMO3		
52		P54	ALE	MTIOC4B/TMCI1	CTS2#/RTS2#/SS2#	
53	BCLK	P53				
54		P52	RD#		RXD2/SMISO2/SSCL2	
55		P51	WR1#/BC1#/WAIT#		SCK2	
56		P50	WR0#/WR#		TXD2/SMOSI2/SSDA2	
57	VSS					
58		P83		MTIOC4C	CTS10#/RTS10#	
59	VCC					
60		PC7	A23/CS0#	MTIOC3A/TMO2/ MTCLKB	TXD8/SMOSI8/SSDA8/ MISOA	CACREF
61		PC6	A22/CS1#	MTIOC3C/MTCLKA/ TMCI2	RXD8/SMISO8/SSCL8/ MOSIA	
62		PC5	A21/CS2#/WAIT#	MTIOC3B/MTCLKD/ TMRI2	SCK8/RSPCKA	
63		P82		MTIOC4A	TXD10/SMOSI10/SSDA10	
64		P81		MTIOC3D	RXD10/SMISO10/SSCL10	
65		P80		MTIOC3B	SCK10	
66		PC4	A20/CS3#	MTIOC3D/MTCLKC/ TMCI1/POE0#	SCK5/CTS8#/RTS8#/ SS8#/SSLA0	
67		PC3	A19	MTIOC4D/TCLKB	TXD5/SMOSI5/SSDA5	
68		P77			TXD11/SMOSI11/SSDA11	
69		P76			RXD11/SMISO11/SSCL11	
70		PC2	A18	MTIOC4B/TCLKA	RXD5/SMISO5/SSCL5/ ISSLA3	
71		P75			SCK11	
72		P74			CTS11#/RTS11#/SS11#	
73		PC1	A17	MTIOC3A/TCLKD	SCK5/SSLA2	
74		PL1				
75		PC0	A16	MTIOC3C/TCLKC	CTS5#/RTS5#/SS5#/ SSLA1	
76		PL0				
77		P73				
78		PB7	A15	MTIOC3B/TIOCB5	TXD9/SMOSI9/SSDA9	
79		PB6	A14	MTIOC3D/TIOCA5	RXD9/SMISO9/SSCL9	
80		PB5	A13	MTIOC2A/MTIOC1B/ TMRI1/POE1#/TIOCB4	SCK9	

Table 1.12 List of Pins and Pin Functions (100-Pin LQFP) (1 / 3)

Pin No.	Power Supply, Clock, System Control	I/O Port	External Bus	Timers (MTU, TMR, POE)	Communications (SCIc, SCId, RSPI, RIIC)	Others
1	VREFH					
2		P03				DA0
3	VREFL					
4		PJ3		MTIOC3C	CTS6#/RTS6#/SS6#	
5	VCL					
6		PJ1		MTIOC3A		
7	MD					FINED
8	XCIN					
9	XCOUT					
10	RES#					
11	XTAL	P37				
12	VSS					
13	EXTAL	P36				
14	VCC					
15		P35				NMI
16		P34		MTIOC0A/TMCI3/ POE2#	SCK6	IRQ4
17		P33		MTIOC0D/TMRI3/ POE3#	RXD6/SMISO6/SSCL6	IRQ3-DS
18		P32		MTIOC0C/TMO3	TXD6/SMOSI6/SSDA6	IRQ2-DS/RTCOUT/ RTCIC2
19		P31		MTIOC4D/TMCI2	CTS1#/RTS1#/SS1#	IRQ1-DS/RTCIC1
20		P30		MTIOC4B/TMRI3/ POE8#	RXD1/SMISO1/SSCL1	IRQ0-DS/RTCIC0
21		P27	CS3#	MTIOC2B/TMCI3	SCK1	
22		P26	CS2#	MTIOC2A/TMO1	TXD1/SMOSI1/SSDA1	
23		P25	CS1#	MTIOC4C/MTCLKB		ADTRG0#
24		P24	CS0#	MTIOC4A/MTCLKA/ TMRI1		
25		P23		MTIOC3D/MTCLKD	CTS0#/RTS0#/SS0#	
26		P22		MTIOC3B/MTCLKC/ TMO0	SCK0	
27		P21		MTIOC1B/TMCI0	RXD0/SMISO0/SSCL0	
28		P20		MTIOC1A/TMRI0	TXD0/SMOSI0/SSDA0	
29		P17		MTIOC3A/MTIOC3B/ TMO1/POE8#	SCK1/MISOA/ SDA-DS	IRQ7
30		P16		MTIOC3C/MTIOC3D/ TMO2	TXD1/SMOSI1/SSDA1/ MOSIA/SCL-DS	IRQ6/RTCOUT/ ADTRG0#
31		P15		MTIOC0B/MTCLKB/ TMCI2	RXD1/SMISO1/SSCL1	IRQ5
32		P14		MTIOC3A/MTCLKA/ TMRI2	CTS1#/RTS1#/SS1#	IRQ4
33		P13		MTIOC0B/TMO3	SDA	IRQ3
34		P12		TMCI1	SCL	IRQ2
35		PH3		TMCI0		
36		PH2		TMRI0		IRQ1
37		PH1		TMO0		IRQ0
38		PH0				CACREF
39		P55	WAIT#	MTIOC4D/TMO3		
40		P54	ALE	MTIOC4B/TMCI1		
41	BCLK	P53				

2. CPU

Figure 2.1 shows the register set of the CPU.



Note 1. The stack pointer (SP) can be the interrupt stack pointer (ISP) or user stack pointer (USP), according to the value of the U bit in the PSW register.

Figure 2.1 Register Set of the CPU

Table 4.1 List of I/O Registers (Address Order) (17 / 29)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles: ICLK ≥ PCLK	Number of Access Cycles: ICLK < PCLK
0008 9076h	S12AD	A/D sampling state register 4	ADSSTR4	8	8	2, 3 PCLKB	2 ICLK
0008 9077h	S12AD	A/D sampling state register 5	ADSSTR5	8	8	2, 3 PCLKB	2 ICLK
0008 9078h	S12AD	A/D sampling state register 6	ADSSTR6	8	8	2, 3 PCLKB	2 ICLK
0008 9079h	S12AD	A/D sampling state register 7	ADSSTR7	8	8	2, 3 PCLKB	2 ICLK
0008 907Ah	S12AD	A/D disconnecting detection control register	ADDISCR	8	8	2, 3 PCLKB	2 ICLK
0008 A000h	SCI0	Serial mode register	SMR	8	8	2, 3 PCLKB	2 ICLK
0008 A001h	SCI0	Bit rate register	BRR	8	8	2, 3 PCLKB	2 ICLK
0008 A002h	SCI0	Serial control register	SCR	8	8	2, 3 PCLKB	2 ICLK
0008 A003h	SCI0	Transmit data register	TDR	8	8	2, 3 PCLKB	2 ICLK
0008 A004h	SCI0	Serial status register	SSR	8	8	2, 3 PCLKB	2 ICLK
0008 A005h	SCI0	Receive data register	RDR	8	8	2, 3 PCLKB	2 ICLK
0008 A006h	SCI0	Smart card mode register	SCMR	8	8	2, 3 PCLKB	2 ICLK
0008 A007h	SCI0	Serial extended mode register	SEMR	8	8	2, 3 PCLKB	2 ICLK
0008 A008h	SCI0	Noise filter setting register	SNFR	8	8	2, 3 PCLKB	2 ICLK
0008 A009h	SCI0	I^2C mode register 1	SIMR1	8	8	2, 3 PCLKB	2 ICLK
0008 A00Ah	SCI0	I^2C mode register 2	SIMR2	8	8	2, 3 PCLKB	2 ICLK
0008 A00Bh	SCI0	I^2C mode register 3	SIMR3	8	8	2, 3 PCLKB	2 ICLK
0008 A00Ch	SCI0	I^2C status register	SISR	8	8	2, 3 PCLKB	2 ICLK
0008 A00Dh	SCI0	SPI mode register	SPMR	8	8	2, 3 PCLKB	2 ICLK
0008 A020h	SCI1	Serial mode register	SMR	8	8	2, 3 PCLKB	2 ICLK
0008 A021h	SCI1	Bit rate register	BRR	8	8	2, 3 PCLKB	2 ICLK
0008 A022h	SCI1	Serial control register	SCR	8	8	2, 3 PCLKB	2 ICLK
0008 A023h	SCI1	Transmit data register	TDR	8	8	2, 3 PCLKB	2 ICLK
0008 A024h	SCI1	Serial status register	SSR	8	8	2, 3 PCLKB	2 ICLK
0008 A025h	SCI1	Receive data register	RDR	8	8	2, 3 PCLKB	2 ICLK
0008 A026h	SCI1	Smart card mode register	SCMR	8	8	2, 3 PCLKB	2 ICLK
0008 A027h	SCI1	Serial extended mode register	SEMR	8	8	2, 3 PCLKB	2 ICLK
0008 A028h	SCI1	Noise filter setting register	SNFR	8	8	2, 3 PCLKB	2 ICLK
0008 A029h	SCI1	I^2C mode register 1	SIMR1	8	8	2, 3 PCLKB	2 ICLK
0008 A02Ah	SCI1	I^2C mode register 2	SIMR2	8	8	2, 3 PCLKB	2 ICLK
0008 A02Bh	SCI1	I^2C mode register 3	SIMR3	8	8	2, 3 PCLKB	2 ICLK
0008 A02Ch	SCI1	I^2C status register	SISR	8	8	2, 3 PCLKB	2 ICLK
0008 A02Dh	SCI1	SPI mode register	SPMR	8	8	2, 3 PCLKB	2 ICLK
0008 A040h	SCI2	Serial mode register	SMR	8	8	2, 3 PCLKB	2 ICLK
0008 A041h	SCI2	Bit rate register	BRR	8	8	2, 3 PCLKB	2 ICLK
0008 A042h	SCI2	Serial control register	SCR	8	8	2, 3 PCLKB	2 ICLK
0008 A043h	SCI2	Transmit data register	TDR	8	8	2, 3 PCLKB	2 ICLK
0008 A044h	SCI2	Serial status register	SSR	8	8	2, 3 PCLKB	2 ICLK
0008 A045h	SCI2	Receive data register	RDR	8	8	2, 3 PCLKB	2 ICLK
0008 A046h	SCI2	Smart card mode register	SCMR	8	8	2, 3 PCLKB	2 ICLK
0008 A047h	SCI2	Serial extended mode register	SEMR	8	8	2, 3 PCLKB	2 ICLK
0008 A048h	SCI2	Noise filter setting register	SNFR	8	8	2, 3 PCLKB	2 ICLK
0008 A049h	SCI2	I^2C mode register 1	SIMR1	8	8	2, 3 PCLKB	2 ICLK
0008 A04Ah	SCI2	I^2C mode register 2	SIMR2	8	8	2, 3 PCLKB	2 ICLK
0008 A04Bh	SCI2	I^2C mode register 3	SIMR3	8	8	2, 3 PCLKB	2 ICLK
0008 A04Ch	SCI2	I^2C status register	SISR	8	8	2, 3 PCLKB	2 ICLK
0008 A04Dh	SCI2	SPI mode register	SPMR	8	8	2, 3 PCLKB	2 ICLK
0008 A060h	SCI3	Serial mode register	SMR	8	8	2, 3 PCLKB	2 ICLK
0008 A061h	SCI3	Bit rate register	BRR	8	8	2, 3 PCLKB	2 ICLK
0008 A062h	SCI3	Serial control register	SCR	8	8	2, 3 PCLKB	2 ICLK
0008 A063h	SCI3	Transmit data register	TDR	8	8	2, 3 PCLKB	2 ICLK

[Chip version A]

Table 5.7 DC Characteristics (6)

Conditions: VCC = AVCC0 = 1.62 to 5.5 V, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +105°C

Item					Symbol	Typ.	Max.	Unit	Test Conditions
Supply current*1	Middle-speed operating modes 1A and 1B	Normal operating mode	No peripheral operation	ICLK = 32 MHz*2	I_{CC}	7.0	—	mA	
				ICLK = 20 MHz*3		6.0	—		
			All peripheral operation: Normal	ICLK = 32 MHz*4		26	—		
				ICLK = 20 MHz*5		18.5	—		
			All peripheral operation: Max.	ICLK = 32 MHz*4		—	40		
				ICLK = 20 MHz*5		—	30		
		Sleep mode	No peripheral operation	ICLK = 32 MHz		5.0	—		
				ICLK = 20 MHz		4.6	—		
			All peripheral operation: Normal	ICLK = 32 MHz		15.5	—		
				ICLK = 20 MHz		12	—		
		All-module clock stop mode		ICLK = 32 MHz		4.5	—		
				ICLK = 20 MHz		4.3	—		
		Increase during BGO operation*6	Middle-speed operating mode 1A			25	—		
			Middle-speed operating mode 1B			20	—		
	Low-speed operating mode 1	Normal operating mode	No peripheral operation*7	ICLK = 1 MHz		0.68	—		
			All peripheral operation: Normal*8	ICLK = 1 MHz		2.4	—		
			All peripheral operation: Max.*8	ICLK = 1 MHz		—	7		
		Sleep mode	No peripheral operation	ICLK = 1 MHz		0.6	—		
			All peripheral operation: Normal	ICLK = 1 MHz		2	—		
		All-module clock stop mode				0.58	—		
	Low-speed operating mode 2	Normal operating mode	No peripheral operation*9	ICLK = 32 kHz		0.024	—		
			All peripheral operation: Normal*10	ICLK = 32 kHz		0.05	—		
			All peripheral operation: Max.*10	ICLK = 32 kHz		—	3*11		
		Sleep mode	No peripheral operation	ICLK = 32 kHz		0.02	—		
			All peripheral operation: Normal	ICLK = 32 kHz		0.04	—		
		All-module clock stop mode				0.018	—		

Note 1. Supply current values do not include output charge/discharge current from all pins. The values apply when internal pull-up MOSs are in the off state.

Note 2. Clock supply to the peripheral functions is stopped. This does not include BGO operation. The clock source is PLL and the VCO oscillation frequency is 64 MHz. BCLK, FCLK, and PCLK are set to divided by 64.

Note 3. Clock supply to the peripheral functions is stopped. This does not include BGO operation. The clock source is HOCO and the oscillation frequency is 40 MHz. BCLK, FCLK, and PCLK are set to divided by 64.

Note 4. Clocks are supplied to the peripheral functions. This does not include BGO operation. The clock source is PLL and the VCO oscillation frequency is 64 MHz. BCLK, FCLK, and PCLK are ICLK divided by 1.

[Chip version B with 256 Kbytes or less of flash memory and 48 to 100 pins]

Table 5.13 DC Characteristics (12)

Conditions: VCC = AVCC0 = 1.62 to 5.5 V, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +105°C

Item					Symbol	Typ.	Max.	Unit	Test Conditions
Supply current*1	Middle-speed operating modes 1A and 1B	Normal operating mode	No peripheral operation	ICLK = 32 MHz*2	I_{CC}	5.3	—	mA	
				ICLK = 20 MHz*3		4.6	—		
			All peripheral operation: Normal	ICLK = 32 MHz*4		20.1	—		
				ICLK = 20 MHz*5		14.3	—		
			All peripheral operation: Max.	ICLK = 32 MHz*4		—	35		
				ICLK = 20 MHz*5		—	—		
		Sleep mode	No peripheral operation	ICLK = 32 MHz		3.4	—		
				ICLK = 20 MHz		3.3	—		
			All peripheral operation: Normal	ICLK = 32 MHz		11.5	—		
				ICLK = 20 MHz		9	—		
		All-module clock stop mode		ICLK = 32 MHz		3	—		
				ICLK = 20 MHz		3	—		
		Increase during BGO operation*6	Middle-speed operating mode 1A			17	—		
			Middle-speed operating mode 1B			17	—		
	Middle-speed operating modes 2A and 2B	Normal operating mode	No peripheral operation*2	ICLK = 32 MHz		4.7	—		
				ICLK = 16 MHz		3.4	—		
				ICLK = 8 MHz		2.7	—		
			All peripheral operation: Normal*4	ICLK = 32 MHz		19.6	—		
				ICLK =16 MHz		11.3	—		
				ICLK = 8 MHz		7.2	—		
			All peripheral operation: Max.*4	ICLK = 32 MHz		—	34		
				ICLK = 16 MHz		—	—		
				ICLK = 8 MHz		—	—		
		Sleep mode	No peripheral operation	ICLK = 32 MHz		2.8	—		
				ICLK = 16 MHz		2.5	—		
				ICLK = 8 MHz		2.2	—		
			All peripheral operation: Normal	ICLK = 32 MHz		11	—		
				ICLK = 16 MHz		7.2	—		
				ICLK = 8 MHz		5.3	—		
		All-module clock stop mode		ICLK = 32 MHz		2.4	—		
				ICLK = 16 MHz		2.2	—		
				ICLK = 8 MHz		2.1	—		
		Increase during BGO operation*6	Middle-speed operating mode 1A			17	—		
			Middle-speed operating mode 1B			17	—		

[Chip version B with 512 Kbytes or less of flash memory and 144 and 145 pins]

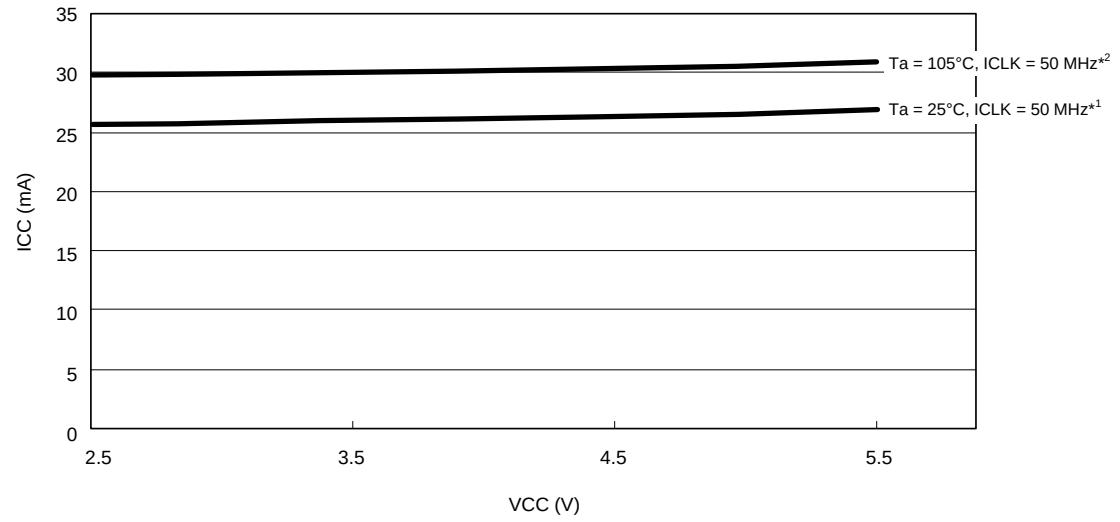
Table 5.19 DC Characteristics (18)

Conditions: VCC = AVCC0 = 1.62 to 5.5 V, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +105°C

Item					Symbol	Typ.	Max.	Unit	Test Conditions
Supply current*1	Middle-speed operating modes 1A and 1B	Normal operating mode	No peripheral operation	ICLK = 32 MHz*2	I_{CC}	5.3	—	mA	
				ICLK = 20 MHz*3		4.6	—		
			All peripheral operation: Normal	ICLK = 32 MHz*4		22.3	—		
				ICLK = 20 MHz*5		15.6	—		
			All peripheral operation: Max.	ICLK = 32 MHz*4		—	35		
				ICLK = 20 MHz*5		—	—		
		Sleep mode	No peripheral operation	ICLK = 32 MHz		3.4	—		
				ICLK = 20 MHz		3.3	—		
			All peripheral operation: Normal	ICLK = 32 MHz		12.8	—		
				ICLK = 20 MHz		9.8	—		
		All-module clock stop mode		ICLK = 32 MHz		3	—		
				ICLK = 20 MHz		3	—		
		Increase during BGO operation*6	Middle-speed operating mode 1A			21	—		
			Middle-speed operating mode 1B			19	—		
	Middle-speed operating modes 2A and 2B	Normal operating mode	No peripheral operation*2	ICLK = 32 MHz		4.7	—		
				ICLK = 16 MHz		3.4	—		
				ICLK = 8 MHz		2.7	—		
			All peripheral operation: Normal*4	ICLK = 32 MHz*3		21.7	—		
				ICLK = 16 MHz*3		12.3	—		
				ICLK = 8 MHz		7.6	—		
			All peripheral operation: Max.*4	ICLK = 32 MHz*3		—	34		
				ICLK = 16 MHz*3		—	—		
				ICLK = 8 MHz		—	—		
		Sleep mode	No peripheral operation	ICLK = 32 MHz		2.9	—		
				ICLK = 16 MHz		2.5	—		
				ICLK = 8 MHz		2.2	—		
			All peripheral operation: Normal	ICLK = 32 MHz		12.3	—		
				ICLK = 16 MHz		7.8	—		
				ICLK = 8 MHz		5.6	—		
		All-module clock stop mode		ICLK = 32 MHz		2.5	—		
				ICLK = 16 MHz		2.2	—		
				ICLK = 8 MHz		2.1	—		
		Increase during BGO operation*6	Middle-speed operating mode 1A			21	—		
			Middle-speed operating mode 1B			19	—		

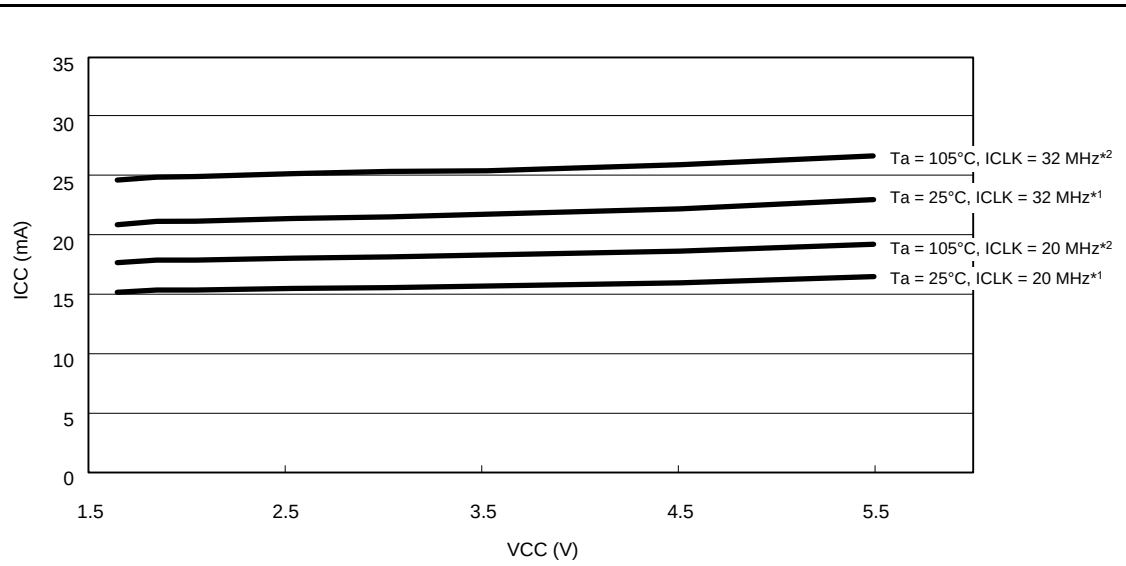
Item					Symbol	Typ.	Max.	Unit	Test Conditions
Supply current*1	Low-speed operating mode 1	Normal operating mode	No peripheral operation*7	ICLK = 8 MHz	I_{CC}	2.0	—	mA	
				ICLK = 4 MHz		1.6	—		
				ICLK = 2 MHz		1.5	—		
			All peripheral operation: Normal*8	ICLK = 8 MHz		6.4	—		
				ICLK = 4 MHz		4.0	—		
				ICLK = 2 MHz		2.8	—		
			All peripheral operation: Max.*8	ICLK = 8 MHz		—	12		
				ICLK = 4 MHz		—	—		
				ICLK = 2 MHz		—	—		
		Sleep mode	No peripheral operation	ICLK = 8 MHz		1.5	—		
				ICLK = 4 MHz		1.4	—		
				ICLK = 2 MHz		1.3	—		
			All peripheral operation: Normal	ICLK = 8 MHz		3.9	—		
				ICLK = 4 MHz		2.8	—		
				ICLK = 2 MHz		2.2	—		
		All-module clock stop mode		ICLK = 8 MHz		1.4	—		
				ICLK = 4 MHz		1.3	—		
				ICLK = 2 MHz		1.2	—		
	Low-speed operating mode 2	Normal operating mode	No peripheral operation*9	ICLK = 32 kHz		0.021	—		
			All peripheral operation: Normal*10	ICLK = 32 kHz		0.06	—		
			All peripheral operation: Max.*10	ICLK = 32 kHz		—	3*11		
		Sleep mode	No peripheral operation	ICLK = 32 kHz		0.017	—		
			All peripheral operation: Normal	ICLK = 32 kHz		0.035	—		
		All-module clock stop mode				0.016	—		

Note 1. Supply current values do not include output charge/discharge current from all pins. The values apply when internal pull-up MOSs are in the off state.
Note 2. Clock supply to the peripheral functions is stopped. This does not include BGO operation. The clock source is PLL and the VCO oscillation frequency is 64 MHz. BCLK, FCLK, and PCLK are set to divided by 64.
Note 3. Clock supply to the peripheral functions is stopped. This does not include BGO operation. The clock source is HOCO and the oscillation frequency is 40 MHz. BCLK, FCLK, and PCLK are set to divided by 64.
Note 4. Clocks are supplied to the peripheral functions. This does not include BGO operation. The clock source is PLL and the VCO oscillation frequency is 64 MHz. BCLK, FCLK, and PCLK are ICLK divided by 1.
Note 5. Clocks are supplied to the peripheral functions. This does not include BGO operation. The clock source is HOCO and the oscillation frequency is 40 MHz. BCLK, FCLK, and PCLK are ICLK divided by 1.
Note 6. This is the increase if data is programmed to or erasing from the ROM or E2 DataFlash during program execution.
Note 7. Clock supply to the peripheral functions is stopped. This does not include BGO operation. The clock source is HOCO and the oscillation frequency is 32 MHz. BCLK, FCLK, and PCLK are set to divided by 64.
Note 8. Clocks are supplied to the peripheral functions. This does not include BGO operation. The clock source is HOCO and the oscillation frequency is 32 MHz. BCLK, FCLK, and PCLK are ICLK divided by 1.
Note 9. Clock supply to the peripheral functions is stopped. This does not include BGO operation. The clock source is the sub oscillation circuit. BCLK, FCLK, and PCLK are set to divided by 64.
Note 10. Clocks are supplied to the peripheral functions. This does not include BGO operation. The clock source is the sub oscillation circuit. BCLK, FCLK, and PCLK are ICLK divided by 1.
Note 11. Value when the main clock continues oscillating at 12.5 MHz.



Note 1. All peripheral operation is normal. This does not include BGO operation.
Average value of the tested middle samples during product evaluation
Note 2. All peripheral operation is maximum. This does not include BGO operation.
Average value of the tested upper-limit samples during product evaluation.

Figure 5.35 Voltage Dependency in High-Speed Operating Mode (Reference Data) for Chip Version B with 512 Kbytes or Less of Flash Memory and 144 and 145 Pins



Note 1. All peripheral operation is normal. This does not include BGO operation.
Average value of the tested middle samples during product evaluation
Note 2. All peripheral operation is maximum. This does not include BGO operation.
Average value of the tested upper-limit samples during product evaluation.

Figure 5.36 Voltage Dependency in Middle-Speed Operating Modes 1A and 1B (Reference Data) for Chip Version B with 512 Kbytes or Less of Flash Memory and 144 and 145 Pins

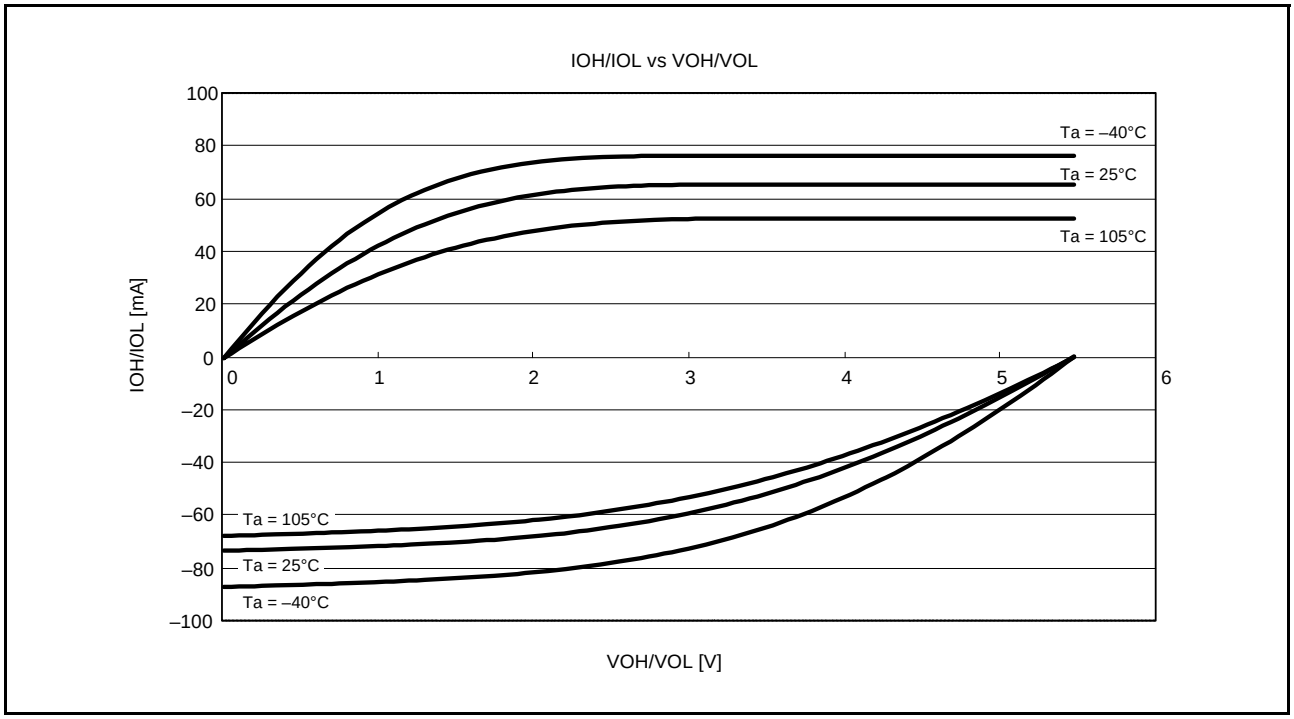


Figure 5.54 VOH/VOL and IOH/IOL Temperature Characteristics at VCC = 5.5 V when High-Drive Output is Selected (Reference Data)

Note 2. When specifying the main clock oscillator stabilization time, load the MOSCWTCR register with a stabilization time value that is greater than the resonator-vendor-recommended value. When determining the main lock oscillation stabilization wait time, allow an adequate margin (2 times is recommended) for the main clock oscillation stabilization time.
Start using the main clock in the main clock oscillation stabilization wait time (tMAINOSCWT) after setting up the main clock oscillator for operation with the MOSCCR.MOSTP bit.
The indicated value is a reference value that is measured for an 8 MHz resonator.
Note 3. Sum of the main clock oscillation stabilization time and the PLL oscillation stabilization time.
Note 4. The indicated value is a reference value that is measured for an 8 MHz resonator.
Note 5. When specifying the sub-clock oscillation stabilization time, load the SOSCWTCR register with the resonator-vendor-recommended stabilization time value minus 2 seconds. When determining the sub-clock oscillation stabilization wait time, allow an adequate margin (2 times is recommended) for the sub-clock oscillation stabilization time. Start using the sub-clock in the sub-clock oscillation stabilization wait time (tSUBOSCWT) after setting up the sub-clock oscillator for operation with the SOSCCR.SOSTP or RCR3.RTCEN bit.
Note 6. There is no minimum or maximum value for 69-pin WLBGA.
Note 7. Characteristic value before mounting on the board for 69-pin WLBGA.

5.3.5 Bus Timing

Table 5.49 Bus Timing (1)

Conditions: VCC = AVCC0 = 2.7 to 5.5 V, VSS = AVSS0 = VREFL = VREFL0 = 0 V,
fBCLK ≤ 25 MHz (BCLK pin output frequency ≤ 12.5 MHz), T_a = –40 to +105°C, V_{OH} = VCC × 0.5,
V_{OL} = VCC × 0.5, I_{OH} = –1.0 mA, I_{OL} = 1.0 mA, C_L = 30 pF
When normal output is selected by the drive capacity register

Item	Symbol	Min.	Max.	Unit	Test Conditions
Address delay time	t_{AD}	—	60	ns	Figure 5.76 to Figure 5.79
Byte control delay time	t_{BCD}	—	60	ns	
CS# delay time	t_{CSD}	—	60	ns	
RD# delay time	t_{RSD}	—	60	ns	
Read data setup time	t_{RDS}	40	—	ns	
Read data hold time	t_{RDH}	0	—	ns	
WR# delay time	t_{WRD}	—	60	ns	
Write data delay time	t_{WDD}	—	60	ns	
Write data hold time	t_{WDH}	0	—	ns	
WAIT# setup time	t_{WTS}	40	—	ns	Figure 5.80
WAIT# hold time	t_{WTH}	0	—	ns	

Table 5.50 Bus Timing (2)

Conditions: VCC = AVCC0 = 1.8 to 2.7 V, VSS = AVSS0 = VREFL = VREFL0 = 0 V,
fBCLK ≤ 16 MHz (BCLK pin output frequency ≤ 8 MHz), T_a = –40 to +105°C, V_{OH} = VCC × 0.5,
V_{OL} = VCC × 0.5, I_{OH} = –1.0 mA, I_{OL} = 1.0 mA, C_L = 30 pF
When normal output is selected by the drive capacity register

Item	Symbol	Min.	Max.	Unit	Test Conditions
Address delay time	t_{AD}	—	90	ns	Figure 5.76 to Figure 5.79
Byte control delay time	t_{BCD}	—	90	ns	
CS# delay time	t_{CSD}	—	90	ns	
RD# delay time	t_{RSD}	—	90	ns	
Read data setup time	t_{RDS}	60	—	ns	
Read data hold time	t_{RDH}	0	—	ns	
WR# delay time	t_{WRD}	—	90	ns	
Write data delay time	t_{WDD}	—	90	ns	
Write data hold time	t_{WDH}	0	—	ns	
WAIT# setup time	t_{WTS}	60	—	ns	Figure 5.80
WAIT# hold time	t_{WTH}	0	—	ns	

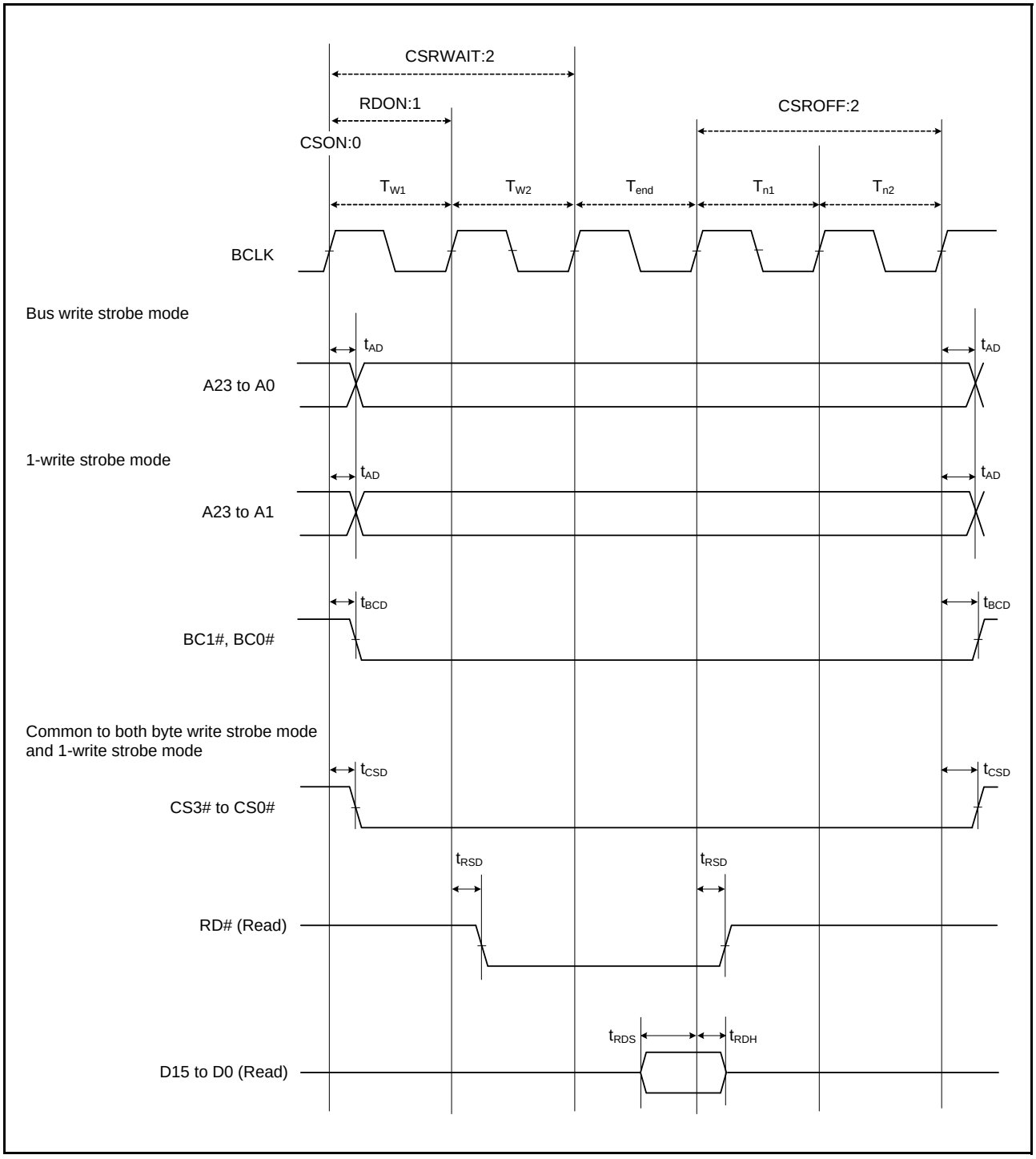


Figure 5.76 External Bus Timing/Normal Read Cycle (Bus Clock Synchronized)

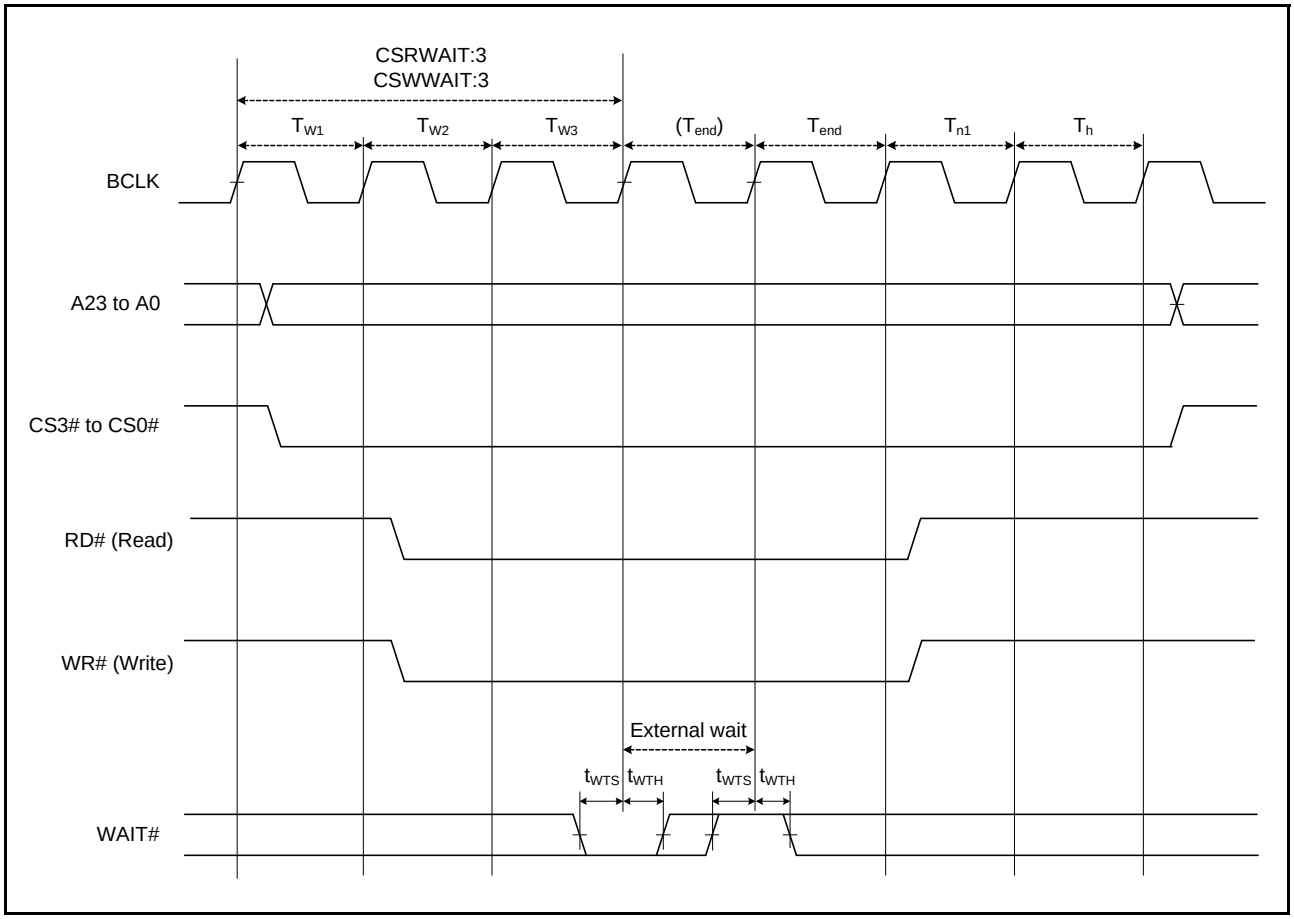


Figure 5.80 External Bus Timing/External Wait Control

Item				Symbol	Min.	Max.	Unit*1	Test Conditions
RSPI	MOSI and MISO rise/fall time	Output		t_{Dr}, t_{Df}	—	20	ns	C = 30 pF Figure 5.92 to Figure 5.97
		Input			—	1	μs	
	SSL rise/fall time	Output		t_{SSLr}, t_{SSLf}	—	20	ns	
		Input			—	1	μs	
	Slave access time		2.7 V ≤ VCC ≤ 5.5 V	t_{SA}	—	6	t_{Pcyc}	C = 30 pF Figure 5.96 and Figure 5.97
			1.8 V ≤ VCC < 2.7 V		—	7		
			1.62 V ≤ VCC < 1.8 V		—	7		
	Slave output release time		2.7 V ≤ VCC ≤ 5.5 V	t_{REL}	—	5	t_{Pcyc}	
			1.8 V ≤ VCC < 2.7 V		—	6		
			1.62 V ≤ VCC < 1.8 V		—	6		

Note 1. t_{Pcyc}: PCLK cycle

[768 Kbytes/1 Mbyte of flash memory or 144/145 pins]

Table 5.57 Timing of On-Chip Peripheral Modules (3)

Conditions: VCC = AVCC0 = 1.62 to 5.5 V, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +105°C
When high-drive output is selected by the drive capacity register

Item				Symbol	Min.	Max.	Unit*1	Test Conditions
RSPI	RSPCK clock cycle	Master		t_{SPcyc}	2	4096	t_{Pcyc}	C = 30pF Figure 5.91
		Slave			8	4096		
	RSPCK clock high pulse width	Master	2.7 V ≤ VCC ≤ 5.5 V	t_{SPCKWH}	$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2 - 3$	—	ns	
			1.8 V ≤ VCC < 2.7 V		$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2 - 3$	—		
			1.62 V ≤ VCC < 1.8 V		$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2 - 10$	—		
		Slave			$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2$	—		
	RSPCK clock low pulse width	Master	2.7 V ≤ VCC ≤ 5.5 V	t_{SPCKWL}	$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2 - 3$	—	ns	
			1.8 V ≤ VCC < 2.7 V		$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2 - 3$	—		
			1.62 V ≤ VCC < 1.8 V		$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2 - 10$	—		
		Slave			$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2$	—		
	RSPCK clock rise/fall time	Output	2.7 V ≤ VCC ≤ 5.5 V	t_{SPCKr}, t_{SPCKf}	—	10	ns	
			1.8 V ≤ VCC < 2.7 V		—	15		
			1.62 V ≤ VCC < 1.8 V		—	20		
		Input			—	1	μs	

Table 5.60 Timing of On-Chip Peripheral Modules (6)

Conditions: VCC = AVCC0 = 2.7 to 5.5 V, VSS = AVSS0 = VREFL = VREFL0 = 0 V, fPCLKB = up to 32 MHz,
T_a = –40 to +105°C
When high-drive output is selected by the drive capacity register

Item		Symbol	Min.*1	Max.	Unit	Test Conditions
Simple IIC (Standard mode)	SDA input rise time	t_{Sr}	—	1000	ns	Figure 5.98
	SDA input fall time	t_{Sf}	—	300	ns	
	SDA input spike pulse removal time	t_{SP}	0	$4 \times t_{pcyc}$*2	ns	
	Data input setup time	t_{SDAS}	250	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	
Simple IIC (Fast mode)	SCL, SDA input rise time	t_{Sr}	$20 + 0.1C_b$	300	ns	Figure 5.98
	SCL, SDA input fall time	t_{Sf}	$20 + 0.1C_b$	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	$4 \times t_{pcyc}$*2	ns	
	Data input setup time	t_{SDAS}	100	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	

Note: • t_{Pcyc}: PCLK cycle
Note 1. C_b indicates the total capacity of the bus line.
Note 2. This applies when the SMR.CKS[1:0] bits = 00b and the SNFR.NFCS[2:0] bits = 010b while the SNFR.NFE bit = 1 and the digital filter is enabled.

Table 5.62 Channel Classification for A/D Converter

Classification	Channel	Channel-Dedicated Sample-and-Hold Circuit	Conditions	
High-precision channel	AN000 to AN002	Used	AVCC0 = 2.7 to 5.5 V AVCC0 - 0.9 V ≤ VREFH0 ≤ AVCC0 VREFH0 ≥ 2.7 V AVSS0 = VREFL0 = 0 V 0.25 V ≤ V_{AN} ≤ AVCC0 - 0.25 V V_{AN} ≤ VREFH0	It is disallowed to use pins AN000 to AN007 as digital outputs when the A/D converter is used.
		Not used	AVCC0 = 1.62 to 5.5 V When AVCC0 ≥ 1.8 V, AVCC0 - 0.9 V ≤ VREFH0 ≤ AVCC0 VREFH0 ≥ 1.8 V When AVCC0 < 1.8 V, VREFH0 = AVCC0 AVSS0 = VREFL0 = 0 V 0 V ≤ V_{AN} ≤ VREFH0	
	AN003 to AN007	—		
Normal-precision channel	AN008 to AN015	—		

Table 5.63 A/D Internal Reference Voltage Characteristics

Conditions: VCC = AVCC0 = 1.62 to 5.5 V, VSS = AVSS0 = VREFL = VREFL0 = 0 V, Ta = −40 to +105°C

Item	Min.	Typ.	Max.	Unit	Test Conditions
A/D internal reference voltage	1.35	1.50	1.65	V	

[Chip versions A and C]

**Table 5.83 E2 DataFlash Characteristics (4)
: middle-speed operating mode 1B**

Conditions: VCC = AVCC0 = 1.62 to 3.6 V, VREFH = VREFH0 = AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V
Temperature range for the programming/erasure operation: T_a = –40 to +105°C

Item		Symbol	FCLK = 4 MHz			FCLK = 32 MHz*1			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Programming time when N_{DPEC} ≤ 100 times	2 bytes	t_{DP2}	—	0.52	5.1	—	0.24	2.8	ms
	8 bytes	t_{DP8}	—	0.57	6.0	—	0.26	3.2	
Programming time when N_{DPEC} > 100 times	2 bytes	t_{DP2}	—	0.77	7.6	—	0.36	4.2	ms
	8 bytes	t_{DP8}	—	0.84	8.8	—	0.38	4.5	
Erasure time when N_{DPEC} ≤ 100 times	128 bytes	t_{DE128}	—	6.8	32.5	—	4.4	12	ms
Erasure time when N_{DPEC} > 100 times	128 bytes	t_{DE128}	—	8.2	51.4	—	5.3	17	ms
Blank check time	2 bytes	t_{DBC2}	—	—	110	—	—	40	µs
	2 Kbytes	t_{DBC2K}	—	—	16.3	—	—	2.6	ms
Suspend delay time during programming (in programming/erasure priority mode)		t_{DSPD}	—	—	1.7	—	—	1.6	ms
First suspend delay time during programming (in suspend priority mode)		t_{DSPSD1}	—	—	220	—	—	120	µs
Second suspend delay time during programming (in suspend priority mode)		t_{DSPSD2}	—	—	1.7	—	—	1.6	ms
Suspend delay time during erasing (in programming/erasure priority mode)		t_{DSED}	—	—	1.7	—	—	1.6	ms
First suspend delay time during erasing (in suspend priority mode)		t_{DSESD1}	—	—	220	—	—	120	µs
Second suspend delay time during erasing (in suspend priority mode)		t_{DSESD2}	—	—	1.7	—	—	1.6	ms

Note 1. The operating frequency is 20 MHz (max.) when the voltage is in the range from 1.62 V to less than 1.8 V.